High Efficiency Single Synchronous Buck PWM Controller

General Description

The RT8129A is a high efficiency single phase synchronous buck controller with 5V/12V supply voltage. The RT8129A integrates a Constant-On-Time (COT) PWM controller and a MOSFET drivers with internal bootstrap diodes, which is specifically designed to improve converter efficiency at light load condition. At light load condition, it automatically operates in the diode emulation mode to reduce switching frequency and improve conversion efficiency.

Other features include power good indication, enable/disable control and internal soft-start function. The RT8129A also provide protection functions including Over Voltage Protection (OVP), Under Voltage Protection (UVP), current limit and thermal shutdown.

This device uses lossless low-side MOSFET $R_{DS(ON)}$ current sense technique for current limit with adjustable threshold set by connecting a resistor between the LGATE/OCSET and GND.

With above functions, the RT8129A provides customers a cost-effective solution for high efficiency power conversion. The RT8129A is available in the WDFN-10L 3x3 package.

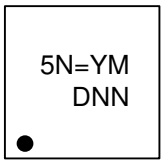
Features

- **Wide Input Voltage Range : 2.5V to 25V**
- **High Light Load Efficiency**
- **Integrated High Driving Capability N-MOSFET Gate**
- **Drivers and Embedded Switching Boot Diode**
- **Single IC Supply Voltage : 4.5V to 13.2V**
- **Power-Good Indicator**
- **Enable/Disable Control**
- **Internal Soft-Start**
- **Programmable Current Limit Threshold**
- **Under Voltage Protection**
- **Over Voltage Protection**
- **Thermal Shutdown**

Applications

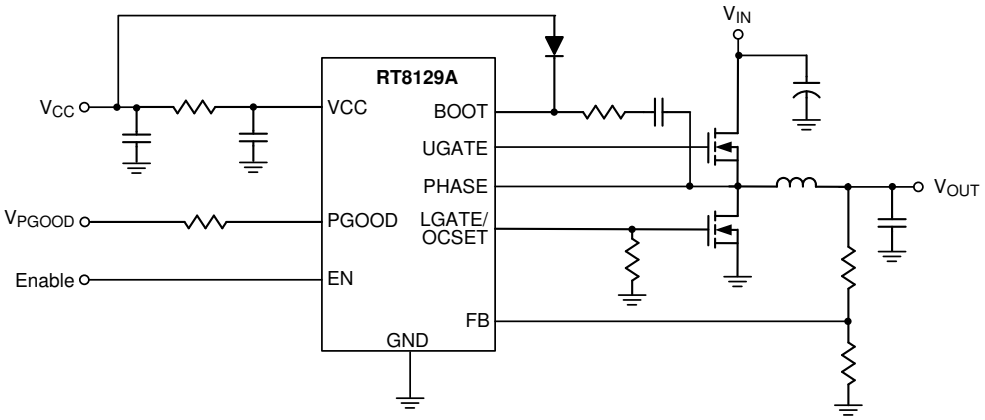
- Motherboard, Memory/Chip-set Power
- Graphic Card, GPU/Memory Core Power
- Low Voltage, High Current DC/DC Regulator

Marking Information



5N= : Product Code
YMDNN : Date Code

Simplified Application Circuit



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Ordering Information

RT8129A□□

Package Type
QW : WDFN-10L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

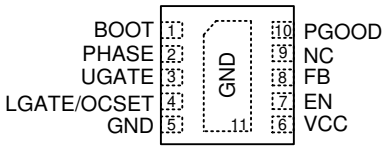
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap Supply for High Side Gate Driver. Connect this pin to a power source VCC through a bootstrap diode, and connect a 0.1μF or greater ceramic capacitor from this pin to the PHASE pin to supply the power for high side gate driver.
2	PHASE	Switch Node. Connect this pin to the switching node of Buck converter. Connect this pin to the Source of high-side MOSFET together with the Drain of low-side MOSFET and the inductor. The PHASE voltage is sensed for zero current detection and over current protection when low side MOSFET is on.
3	UGATE	High Side MOSFET Gate Driver Output. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the Gate of high-side MOSFET.
4	LGATE/OCSET	Low Side MOSFET Gate Driver Output. Connect this pin to the Gate of low side MOSFET. This pin is also used for current limit threshold setting. Connect a resistor (ROCSET) from this pin to the GND pin to set the current limit threshold.
5, 11 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	VCC	Supply Voltage Input. It is recommended to connect a 4.7μF ceramic capacitor from this pin to the GND pin. VCC also powers the low side gate driver.
7	EN	Enable Control Input. Drive EN higher than 2V to turn on the controller, lower than 0.8V to turn it off. If the EN pin is open, it will be pulled to high by internal circuit.
8	FB	This pin is used for output voltage feedback input and it is also monitored for power good indication, over voltage and under voltage protections. Connect this pin to the converter output through voltage divider resistors for output voltage regulation.
9	NC	No Internal Connection.
10	PGOOD	Power Good Indication Output. This pin provides an open drain output. Connect this pin to a voltage source through a pull up resistor. The PGOOD voltage goes high to indicate the output voltage is in regulation. This pin can be left open if the power good indication function is not used.

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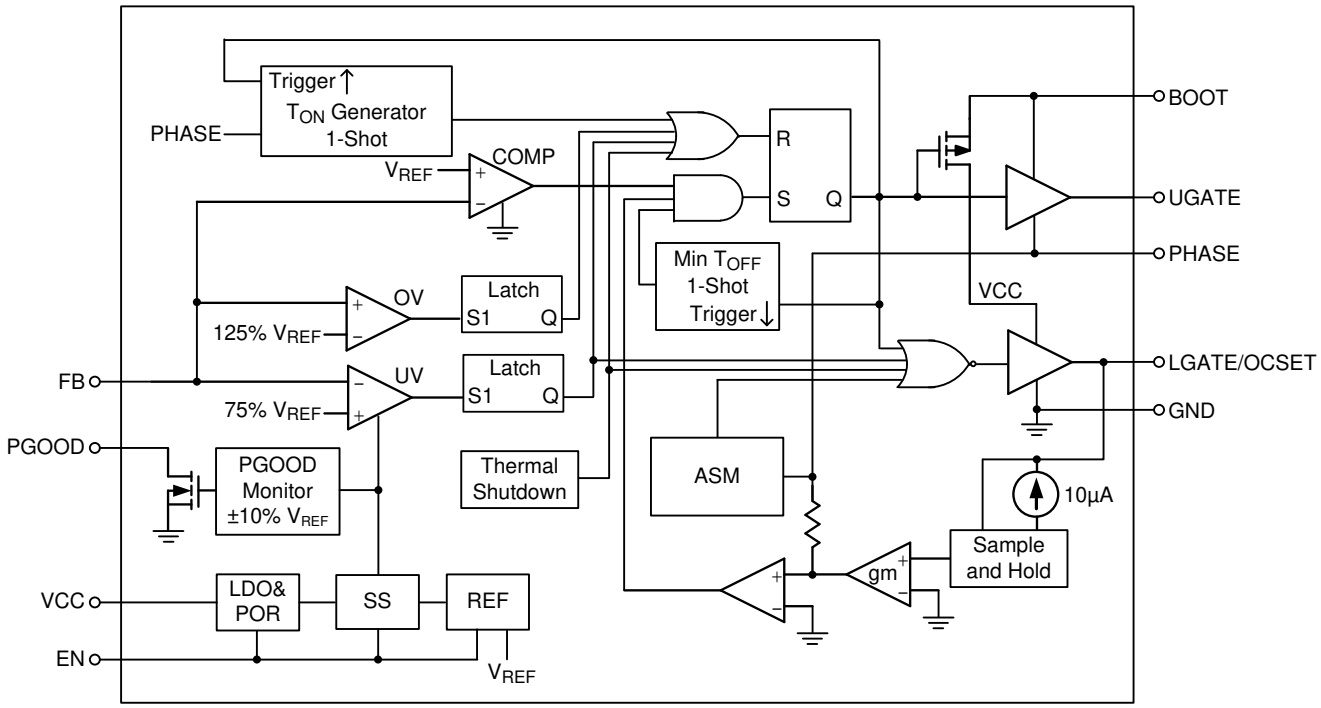
Function Block Diagram



Operation

The RT8129A integrates a Constant-On-Time (COT) PWM controller and MOSFET driver so that the external circuit is easily designed and the components are reduced.

The controller provides the PWM signal which relies on the FB voltage comparing with internal reference voltage. The synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the controller's input voltage and the output voltage to keep the frequency fairly constant over the input voltage and output voltage range. Another one-shot sets a minimum off-time.

Enable

The RT8129A remains in shutdown if the EN pin voltage is lower than 0.8V. When the EN pin voltage rises above the2V, the RT8129A will begin a new initialization and soft-start cycle.

PGOOD

The power good output is an open-drain architecture, and it requires a pull-up resistor. During soft-start process, PGOOD is actively held low and is allowed to be pulled high after soft start process is completed and no protection occur. In addition, if the FB pin voltage is higher than 110% of VREF or lower than 90% of VREF during operation, PGOOD will be pulled low immediately.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage.

The output voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

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Over Voltage Protection (OVP)

The FB voltage can be continuously monitored for over voltage protection. When the FB voltage exceeds 125% of the reference voltage, UGATE goes low and LGATE is forced high. The controller is latched until VCC is re-supplied and exceeds the POR rising threshold voltage.

There is a 5μs delay built into the under voltage protection circuit to prevent false transitions.

Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the FB voltage is less than 75% of the reference voltage, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until VCC or EN pin voltage is re-supplied and exceeds the POR rising threshold voltage.

There is a 3μs delay built into the under voltage protection circuit to prevent false transitions.

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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 15V
- Other Pins ---------- –0.3V to 6.5V
- BOOT to PHASE
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –0.3V to 20V
- PHASE to GND
  - DC ---------- –5V to 25V
  - <100ns ---------- –10V to 30V
- BOOT to GND
  - DC ---------- –0.3V to 40V
  - <100ns ---------- –0.3V to 45V
- UGATE to GND
  - DC ---------- –0.3V to 40V
  - <100ns ---------- –10V to 45V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - <40ns ---------- –5V to 20V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –5V to 20V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Power Input Voltage, VIN ---------- 2.5V to 25V
- Control Voltage, VCC ---------- 4.5V to 13.2V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

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Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller							
VCC POR Threshold			VCC rising	--	--	4.4	V
			VCC falling	3.9	--	--	
Reference Voltage		V_{REF}		--	0.8	--	V
FB Error Comparator Threshold			Reference and Error Amplifier Excluding External Resistive Divider Tolerance	–1	--	1	%
Output Voltage Range				0.8	--	3.3	V
PWM Frequency		F_{SW}	(Note 5)	270	300	330	kHz
Minimum On-Time		$T_{ON(MIN)}$		--	70	--	ns
Minimum Off-Time		$T_{OFF(MIN)}$		--	300	--	ns
EN Threshold							
EN Internal Pull Migh Current			V_{EN} = 0V	--	10	40	µA
EN Input Voltage	Logic-High	V_{ENH}		2	--	--	V
	Logic-Low	V_{ENL}		--	--	0.8	
PGOOD							
Over-Voltage Until PGOOD Goes Low			Measured at FB, with respect to reference, no load	--	880	902	mV
Under-Voltage Until PGOOD Goes Low			Measured at FB, with respect to reference, no load	--	720	--	mV
Fault Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	1	--	µs
Output Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		I_{LEAK}	High state, forced to 5V	--	--	1	µA
Driver							
UGATE Gate Driver Source		$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V, I_{SOURCE} = 100mA	--	1.5	3	Ω
UGATE Gate Driver Sink		$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 12V, I_{SINK} = 10mA	--	2.25	4	Ω
LGATE Gate Driver Source		$R_{LGATEsr}$	V_{CC} = 12V, I_{SOURCE} = 100mA	--	1.5	3	Ω
LGATE Gate Driver Sink		$R_{LGATEsk}$	V_{CC} = 12V, I_{SOURCE} = 10mA	--	1	2	Ω
Dead Time			From UG falling to LG rising, PHASE = 1.5V	5	20	--	ns
			From LG falling to UG rising	5	20	--	
Internal Boot Charging Switch on Resistance			VCC to BOOT, 10mA	--	--	80	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection						
Current Limit Setting Current	I_{OCSET}		9.5	10	10.5	μA
Current Limit Threshold Offset			-20	--	20	mV
Over Voltage Protection Threshold	V_{OVP}		0.95	1	1.03	V
OVP latch delay			--	5	--	μs
Under Voltage Protection Threshold	V_{UVP}		0.57	0.6	0.63	V
Voltage Ramp Soft-Start Time		From FB 0% to FB 100%	1.2	2	2.8	ms
Thermal Shutdown Threshold	T_{SD}		145	--	165	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

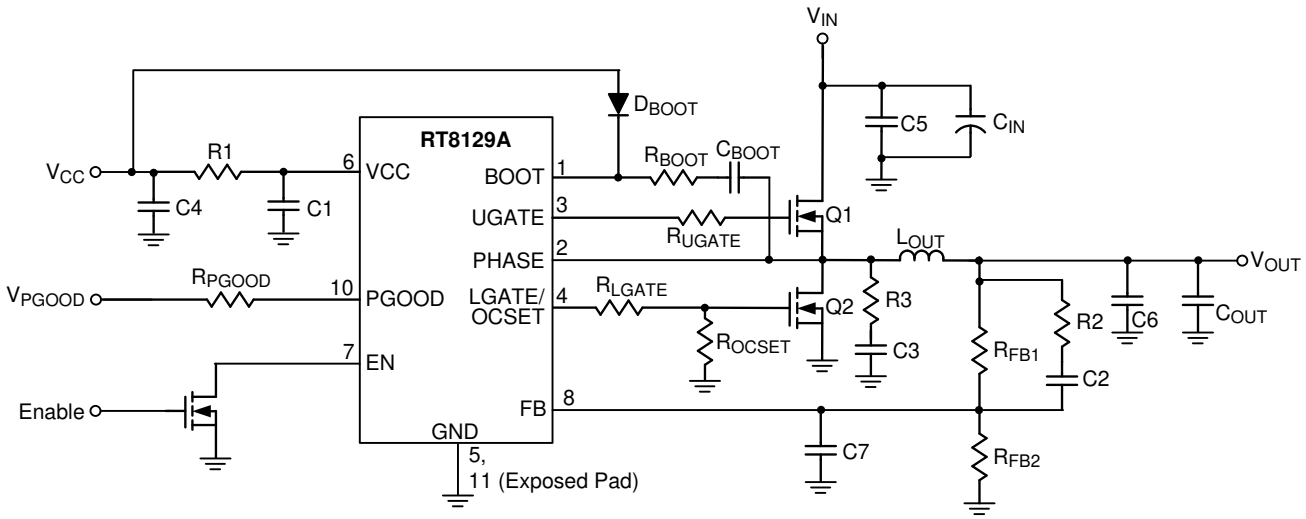
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. No production tested. Test condition V_{IN} = 7V, V_{OUT} = 1.25V, I_{OUT} = 10A using application circuit.

Typical Application Circuit



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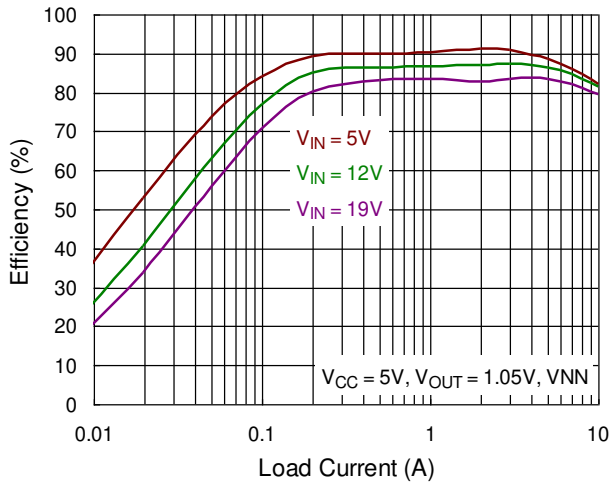
Typical Operating Characteristics

Efficiency vs. Load Current



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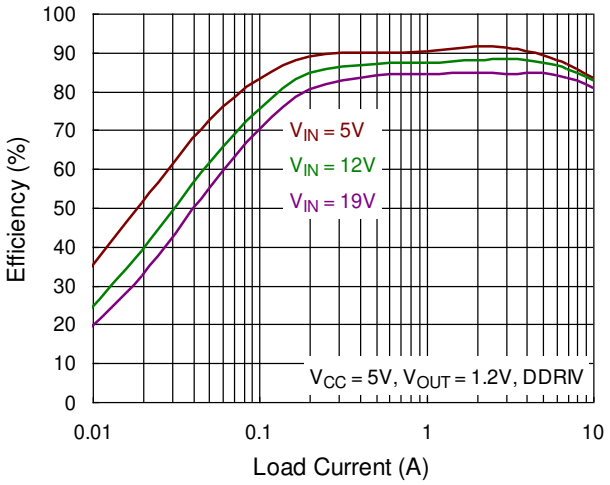

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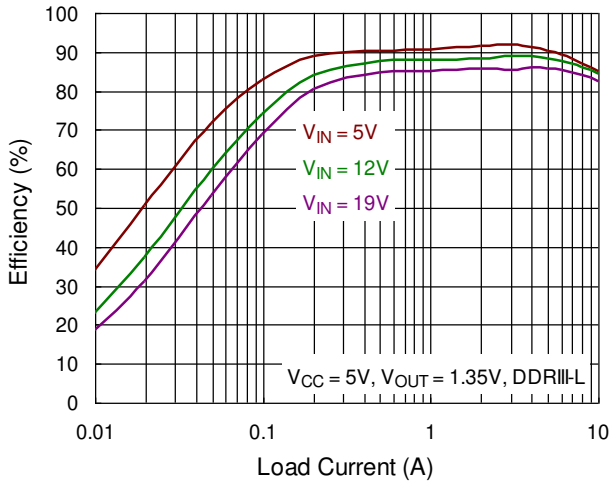
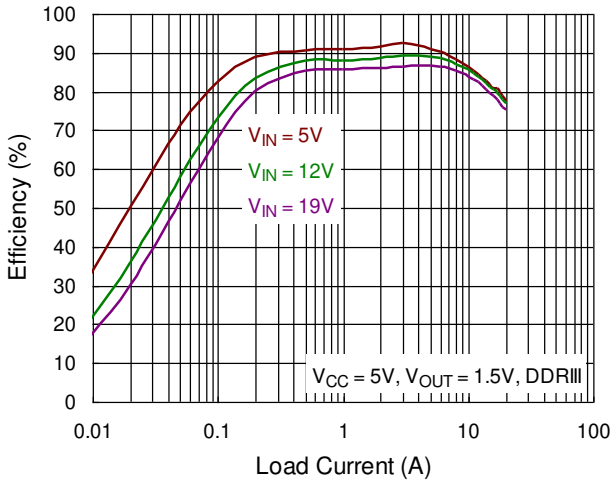
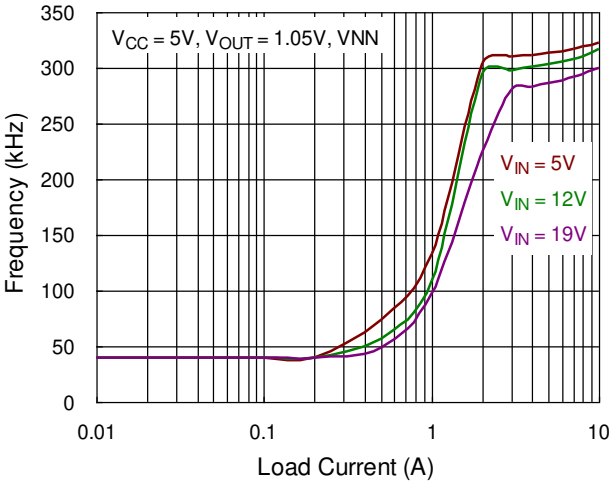


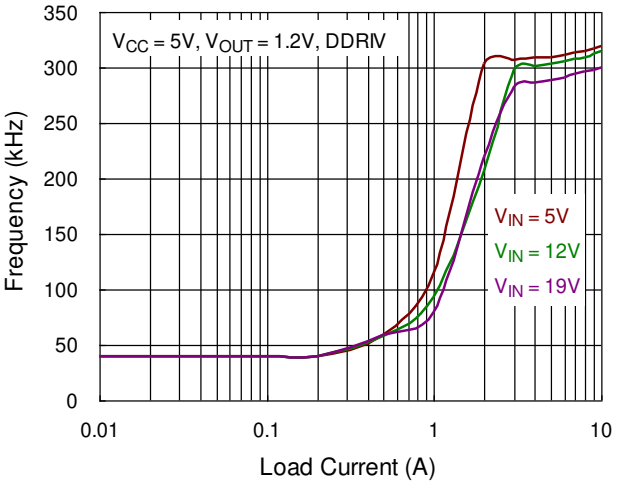
Efficiency vs. Load Current



Frequency vs. Load Current



Frequency vs. Load Current



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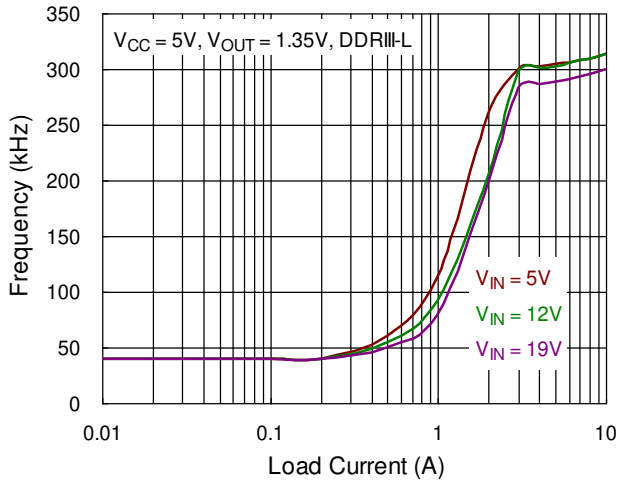
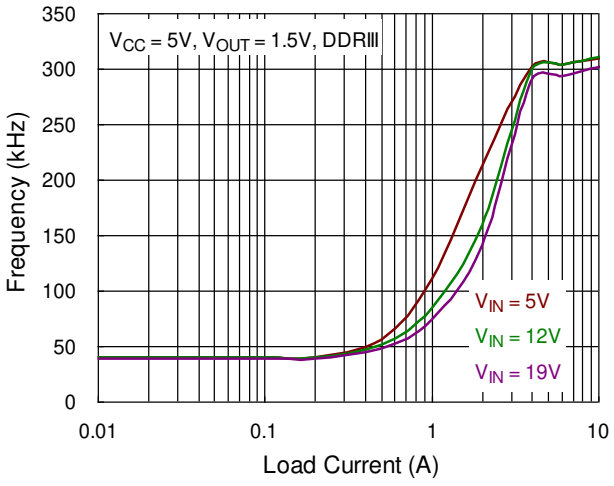
Frequency vs. Load Current



Frequency vs. Load Current



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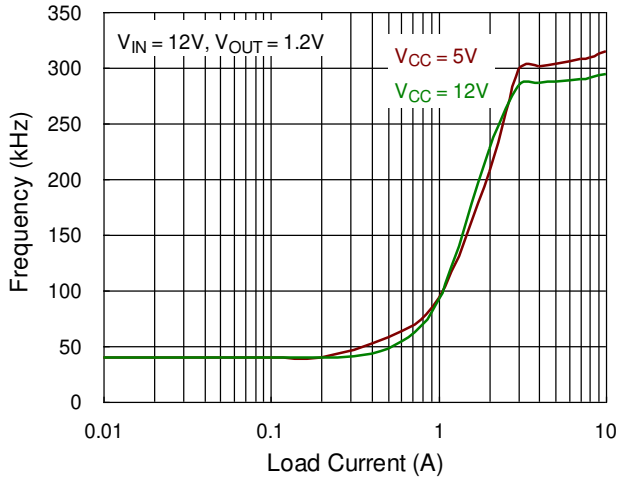
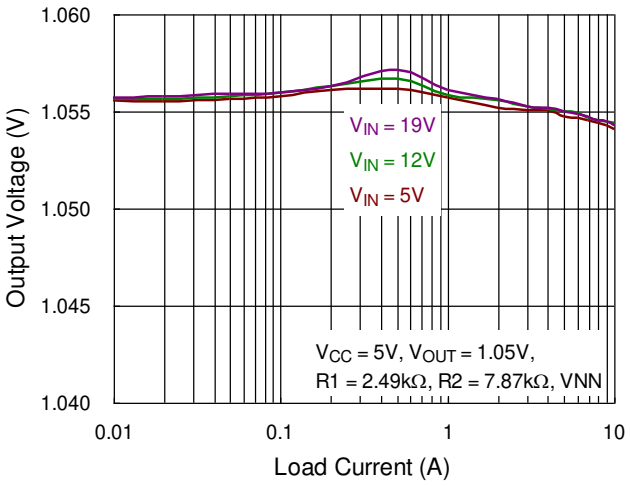


Output Voltage vs. Load Current



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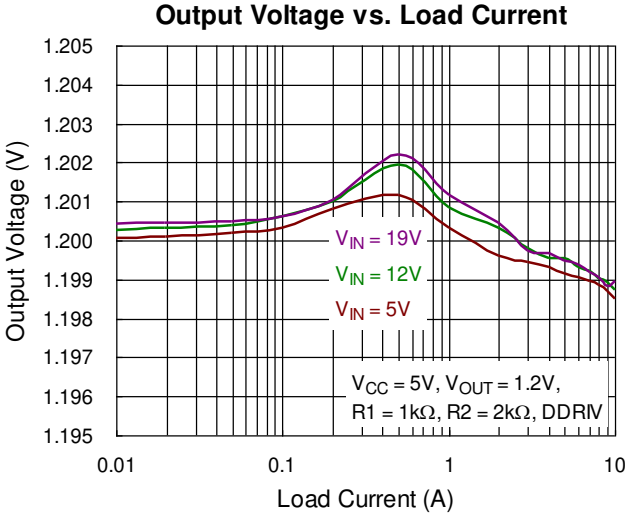
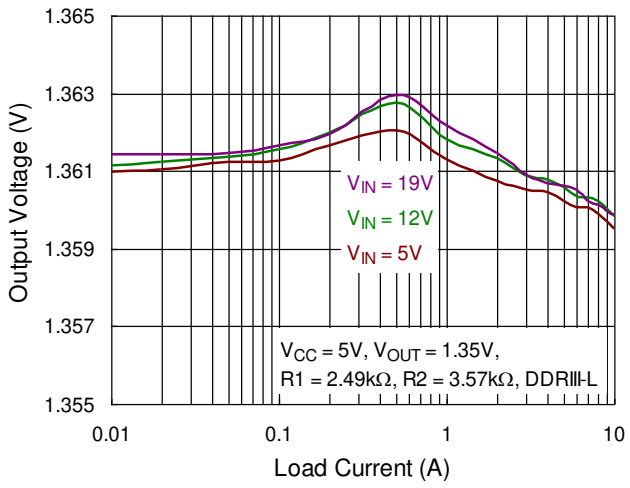


Output Voltage vs. Load Current



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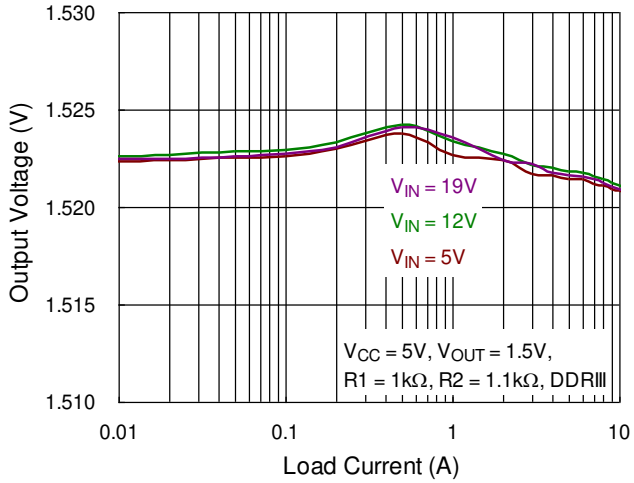
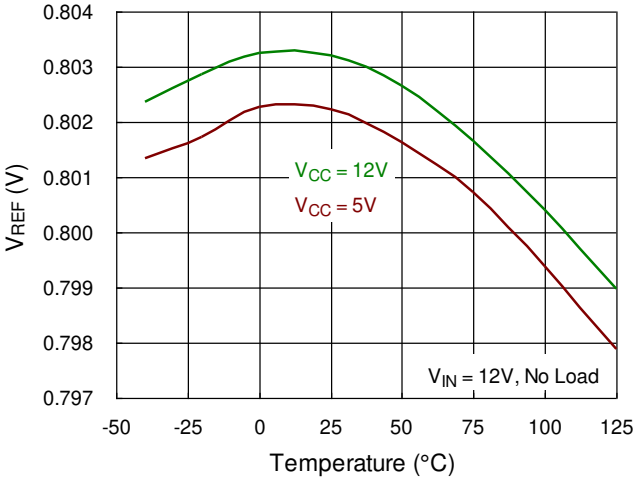
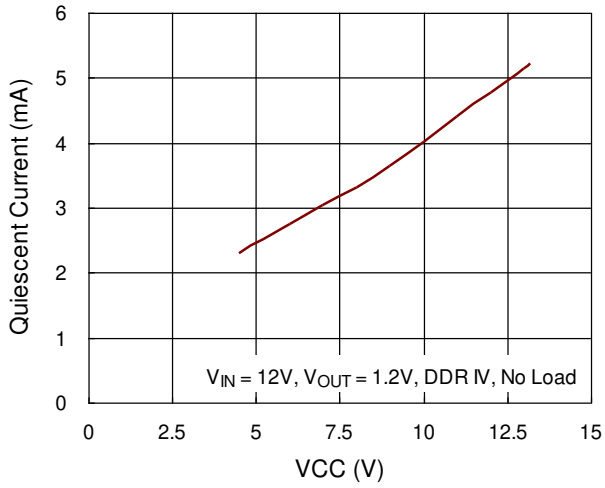
Output Voltage vs. Load Current



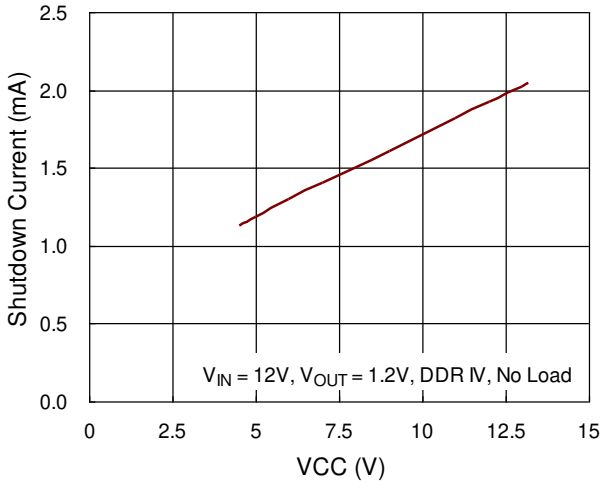
V_{REF} vs. Temperature



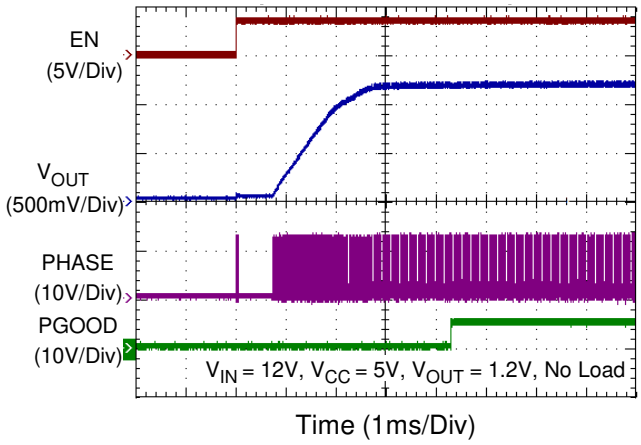
Quiescent Current vs. VCC



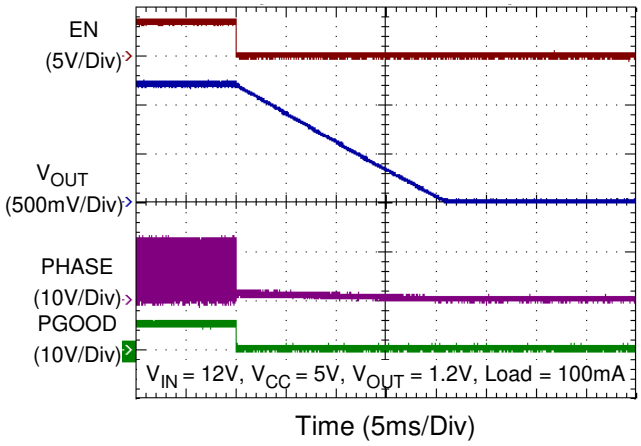
Shutdown Current vs. VCC



Power On from EN



Power Off from EN



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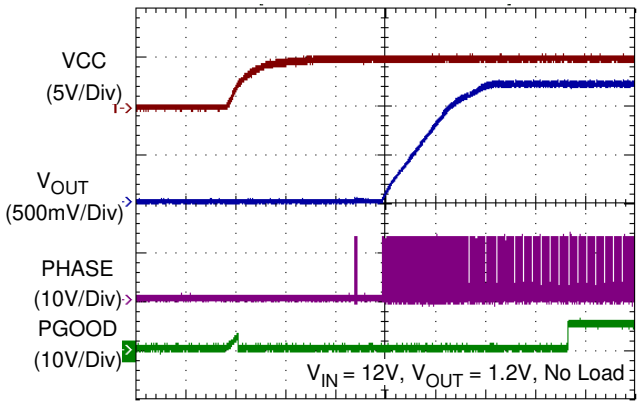
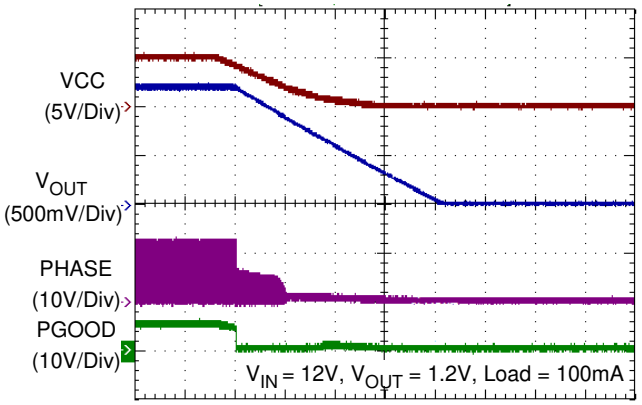
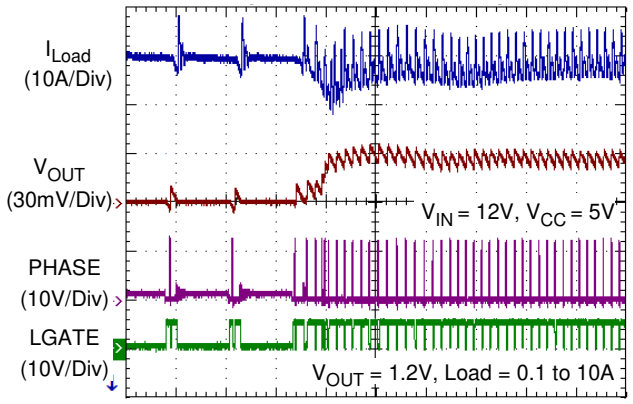
Power On from VCC



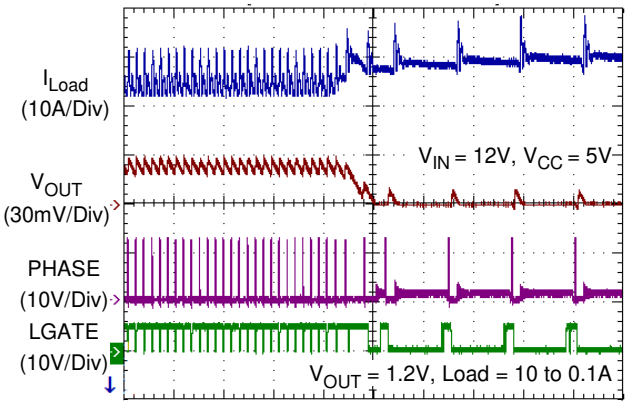
Power Off from VCC



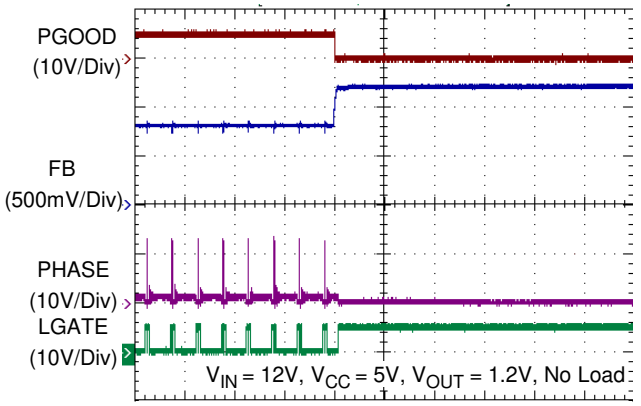
Load Transient Response



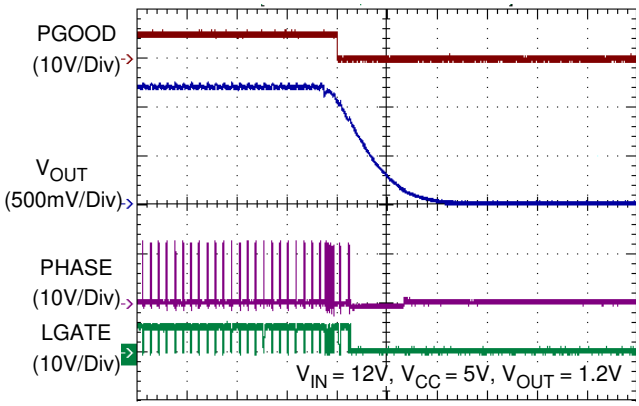
Load Transient Response



OVP



UVP



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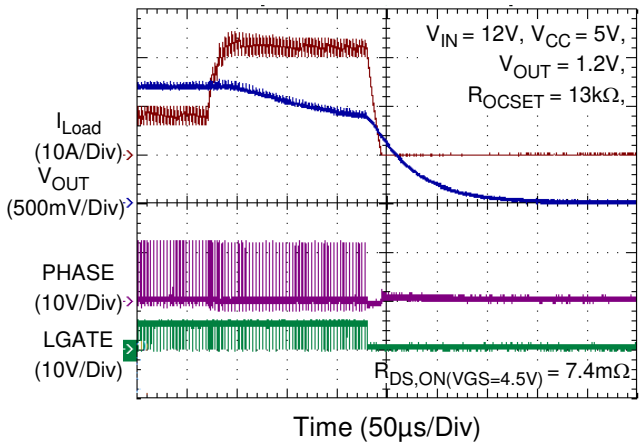
OCP



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Application Information

The RT8129A is a single-phase synchronous buck PWM controller with integrated drivers which is optimized for high performance graphic microprocessor and computer applications. A COT (Constant-On-Time) PWM controller and two MOSFET drivers with internal bootstrap diodes are integrated so that the external circuit is easily designed and the component count is reduced.

The topology solves the poor load transient timing problems of fixed-frequency current-mode PWM and avoids the problems caused by widely varying switching frequencies in conventional constant-on-time and constant off-time PWM schemes.

RT8129A also features complete fault protection functions including OVP, UVP and Current Limit.

PWM Operation

The RT8129A integrates a Constant-On-Time PWM controller, and the controller provides the PWM signal which relies on the FB voltage comparing with internal reference voltage as shown in Figure 1. Referring to the function block diagram of TON generator, the synchronous UGATE driver will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time.

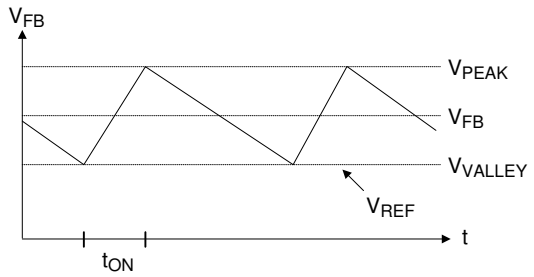

Figure 1. Constant On-Time PWM Control

Diode-Emulation Mode

In diode-emulation mode, the RT8129A automatically reduces switching frequency at light-load conditions to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative level. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next “ON” cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition.

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrade load-transient response (especially at low input-voltage levels).

Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8129A remains in shutdown if the EN pin is lower than 800mV. When EN pin rises above the 2V, the RT8129A will begin a new initialization and soft-start cycle.

Power-On Reset (POR), UVLO

Power-on reset (POR) occurs when VCC rises above to approximately 4.4V (typical), the RT8129A will reset the fault latch and preparing the PWM for operation. Below 4V (typical), the VCC under voltage-lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

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VIN Detection

When VCC exceeds its POR rising threshold, LGATE will be forced low UGATE and UGATE will output continuous pulses (~25kHz, 100ns), for input voltage VIN detection. If the PHASE pin voltage exceeds 1V for 3 consecutive cycles when the UGATE is turned on, VIN is recognized as ready. The controller will initiate soft-start operation.

Soft-Start

The RT8129A provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins after the chip is enabled.

When soft-start process starts, an internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. The PWM pulse width increases gradually to limit the input current. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, both the duty cycle of the UGATE and the input current are limited during the soft-start interval. If the protection is not triggered during soft-start process, the soft-start process is finished until the signal Internal SSOK goes high, Figure 2 shows the internal soft-start sequence.

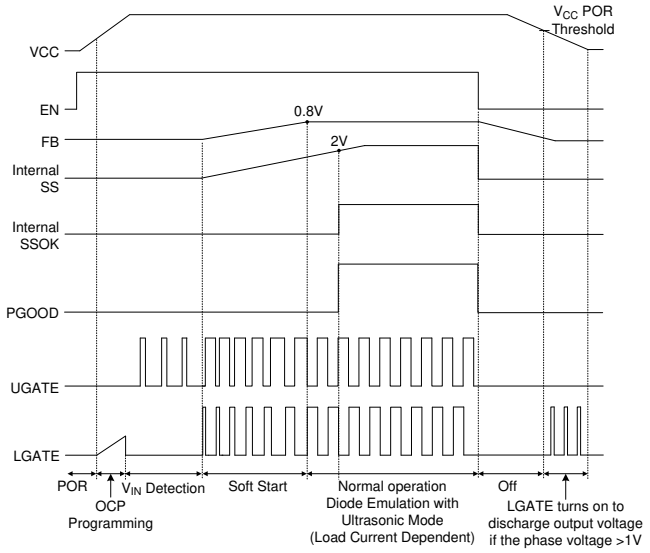

Figure 2. Soft-Start Sequence

Power-Good Output (PGOOD)

The power good output is an open drain architecture, and it requires a pull-up resistor. During soft-start, PGOOD is actively held low and is allowed to transition high after soft start is completed. In addition, if the FB pin voltage is higher than 110% of V_{REF} or lower than 90% of V_{REF}, PGOOD will go low immediately.

Current Limit

The RT8129A provides cycle-by-cycle current limit control by detecting the PHASE voltage drop across the low-side MOSFET when it is turned on. The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle.

In an over-current condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Current Limit Threshold Setting

Current limit threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the over current protection threshold VOCSET. After that, the current source is switched off.

R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{\left(I_{VALLEY} \times R_{LGDS(ON)}\right)}{I_{OCSET}}$$

Where I_{VALLEY} represents the desired inductor limit current (valley inductor current) and I_{OCSET} is current limit setting current.

If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 640mV. The recommended range for R_{OCSET} is 5kΩ to 60kΩ which means the threshold voltage range is 50mV to 600mV.

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Output Over-Voltage Protection (OVP)

The voltage on the FB pin is monitored for over-voltage protection. When the FB voltage exceeds than 1V (typically 125% x V_{REF}), over voltage protection is triggered and low-side MOSFET is forced on. This activates low-side MOSFET to discharge the output capacitor. The RT8129A is latched once OVP is triggered and can only be released by VCC power-on reset. A 5μs delay is used in OVP detection circuit to prevent false trigger.

Output Under-Voltage Protection (UVP)

The voltage on the FB pin is monitored for under voltage protection. When the FB voltage is less than 0.6V (typically 75% x V_{REF}) during normal operation, under voltage protection is triggered and then UGATE and LGATE gate drivers are forced low. The RT8129A is latched once UVP is triggered and can only be released by VCC or EN power-on reset. There is a 3μs delay built into the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

Output Voltage Setting

The output voltage waveform is shown as Figure 3, which can be adjusted from 0.8V to 3.3V by setting the feedback resistors, R_{FB1} and R_{FB2} (see Figure 4). Choose R_{FB2} to be approximately 10kΩ and solve for R_{FB1} using the equation below :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where the V_{REF} is 0.8V (typical).

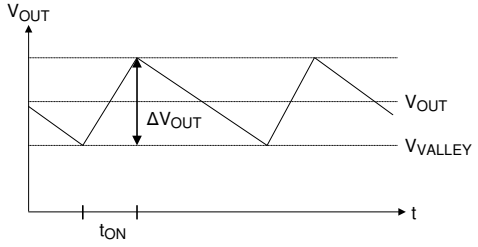

Figure 3. Output Voltage Waveform

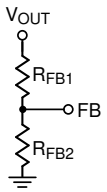

Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

MOSFET Gate Driver

The RT8129A integrates high current gate drivers for the MOSFET to obtain high efficiency power conversion in synchronous buck topology. A dead time is used to prevent the crossover conduction for high side and low side MOSFET. Because both the two gate signals are off during the dead time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to the power loss. The RT8129A employs adaptive dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent short through conduction. For high output current applications, two or more power MOSFET are usually paralleled to reduce $R_{DS(ON)}$.

The gate driver needs to provide more current to switch on/off these paralleled MOSFET. The gate driver with lower source/sink current capability result in longer rising/ falling time in gate signals, and therefore higher switching loss. The RT8129A embeds high current gate drivers to obtain high efficiency power conversion.

Inductor Selection

Inductor plays an importance role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the dc resistance (DCR) of inductor should be as small as possible to minimize the copper loss. In addition, because inductor cost most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with

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inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed such that the ripple current ranges between 20% ~ 40% of full load current. The inductance can be calculated using the following equation.

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times k \times I_{OUT_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. Generally, input capacitor has a voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select proper capacitor for RMS current rating. Use more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the drain of the high-side MOSFET is helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without triggering the OVP circuit. Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFET. For low-voltage high-current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFET with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (30.5°C/W) = 3.27W for WDFN-10L 3x3 package

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The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

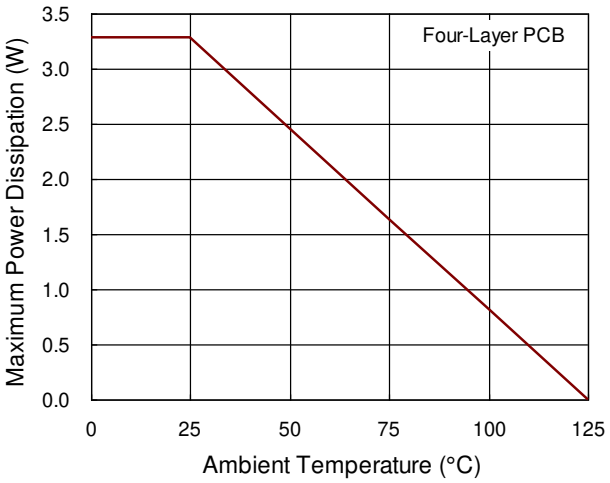

Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for RT8129A.

- Connect RC low pass filter as close as possible VCC pin.
- Keep current protection setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as FB, EN, PGOOD, and VCC should be placed away from high-voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

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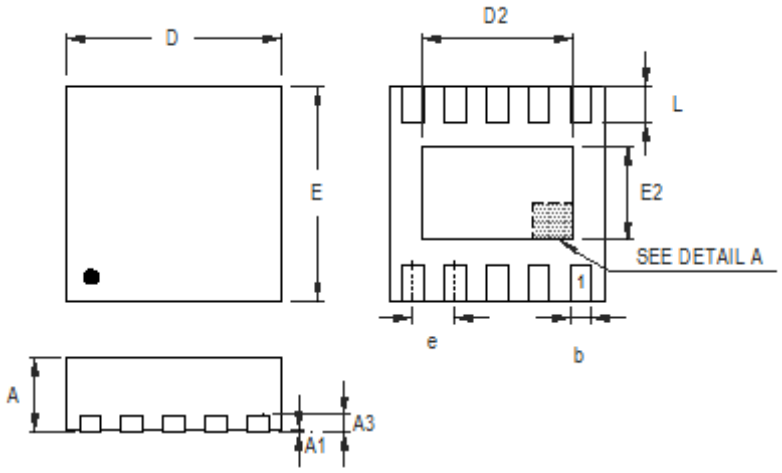
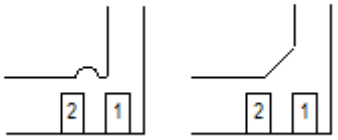
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

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