

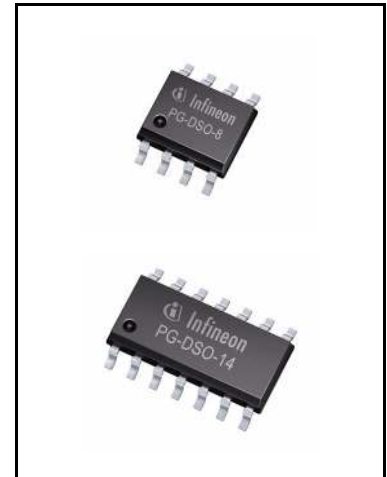
# OPTIREG™ Linear TLE4279

## 5V low drop fixed voltage regulator



### Features

- Output voltage tolerance  $\leq \pm 2\%$
- 150 mA current capability
- Very low current consumption
- Early warning
- Reset output low down to  $V_Q = 1\text{ V}$
- Overtemperature protection
- Reverse polarity proof
- Adjustable reset threshold
- Very low-drop voltage
- Wide temperature range
- Green Product (RoHS compliant)



### Potential applications

General automotive applications.

### Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

### Description

The OPTIREG™ Linear TLE4279 is an automotive voltage regulator with a 5 V fixed output, in a PG-DSO-8 or PG-DSO-14 package. The maximum operating voltage is 45 V. The output is able to drive 150 mA load. The device features short-circuit protection. The thermal shutdown feature switches the output off when the junction temperature exceeds 150°C to ensure the device is not damaged by overheating. A reset signal is generated when the output voltage drops below  $V_Q < 4.65\text{ V}$ . The reset threshold voltage can be decreased by an external connection of a voltage divider. The reset delay time can be set by an external capacitor. If the application requires pull-up resistors at the logic outputs (Reset, Sense Out) the TLE4269 with integrated resistors can be used. It is also possible to supervise the input voltage by using an integrated comparator to give a low voltage warning.

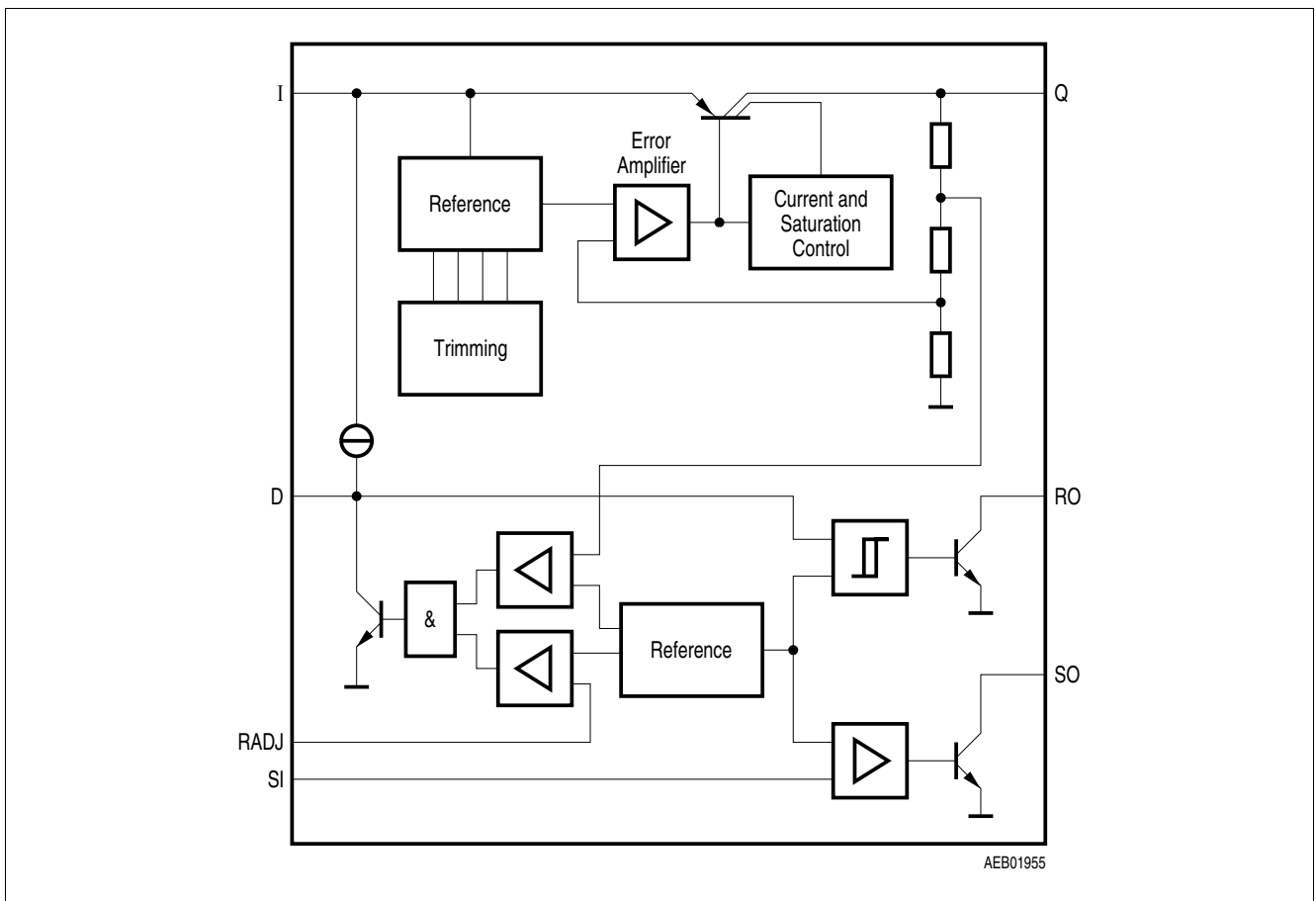
Type	Package	Marking
TLE4279G	PG-DSO-8	TLE4279
TLE4279GM	PG-DSO-14	TLE 4279

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**Block diagram**

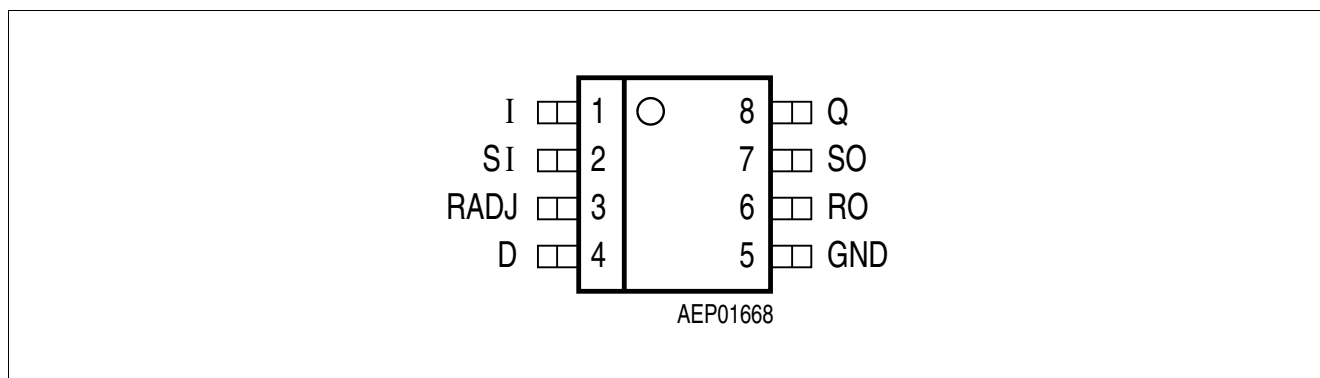
**1 Block diagram**



**Figure 1 Block diagram**

**Pin configuration**

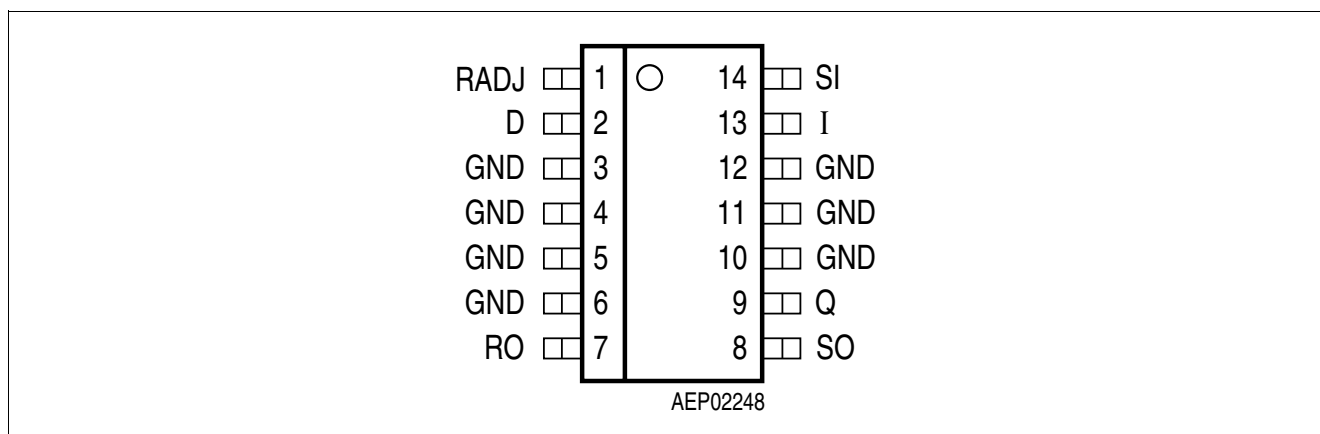
**2 Pin configuration**



**Figure 2 Pin configuration PG-DSO-8 (top view)**

**Table 1 Pin definitions and functions (TLE4279G)**

Pin No.	Symbol	Function
1	I	<b>Input;</b> block to GND directly at the IC with a ceramic capacitor
2	SI	<b>Sense input;</b> if not needed connect to Q
3	RADJ	<b>Reset threshold adjust;</b> if not needed connect to ground
4	D	<b>Reset delay;</b> to select the delay time, connect to GND via external capacitor
5	GND	<b>Ground</b>
6	RO	<b>Reset output;</b> open-collector output. Keep open, if not needed
7	SO	<b>Sense output;</b> open-collector output. Keep open, if not needed
8	Q	<b>5-V output;</b> connect to GND with a 10 µF capacitor, ESR < 10 Ω



**Figure 3 Pin configuration PG-DSO-14 (top view)**

**Table 2 Pin definitions and functions (TLE4279GM)**

Pin No.	Symbol	Function
1	RADJ	<b>Reset threshold adjust;</b> if not needed connect to GND
2	D	<b>Reset delay;</b> connect to GND via external delay capacitor for setting delay time
3, 4, 5, 6	GND	<b>Ground</b>

**Pin configuration**

**Table 2 Pin definitions and functions (TLE4279GM) (cont'd)**

<b>Pin No.</b>	<b>Symbol</b>	<b>Function</b>
7	RO	<b>Reset output;</b> open-collector output. Keep open, if not needed
8	SO	<b>Sense output;</b> open-collector output. Keep open, if not needed
9	Q	<b>5-V output;</b> connect to GND via 10 $\mu$ F capacitor, ESR < 10 $\Omega$
10, 11, 12	GND	<b>Ground</b>
13	I	<b>Input;</b> block to GND directly at the IC by a ceramic capacitor
14	SI	<b>Sense input;</b> if not needed connect to Q

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 3 Absolute maximum ratings**

$T_j = -40$  to  $150$  °C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Input</b>						
Input voltage	$V_I$	-40	-	45	V	-
Input current	$I_I$	-	-	-	-	internal limited
<b>Sense input</b>						
Input voltage	$V_{SI}$	-40	-	45	V	-
Input current	$I_{SI}$	1	-	1	mA	-
<b>Reset threshold</b>						
Voltage	$V_{RADJ}$	-40	-	7	V	-
Current	$I_{RADJ}$	-10	-	10	mA	-
<b>Reset delay</b>						
Voltage	$V_D$	-0.3	-	7	V	-
Current	$I_D$	-	-	-	-	internal limited
<b>Ground</b>						
Current	$I_{GND}$	50	-	-	mA	-
<b>Reset output</b>						
Voltage	$V_R$	-0.3	-	7	V	-
Current	$I_R$	-	-	-	-	internal limited
<b>Sense output</b>						
Voltage	$V_{SO}$	-0.3	-	7	V	-
Current	$I_{SO}$	-	-	-	-	internal limited
<b>5-V Output</b>						
Output voltage	$V_Q$	-0.5	-	7	V	-
Output current	$I_Q$	-10	-	-	mA	-
<b>Temperature</b>						
Junction temperature	$T_j$	-	-	150	°C	-
Storage temperature	$T_{Stg}$	-50	-	150	°C	-

**General product characteristics**

**Table 3 Absolute maximum ratings (cont'd)**

$T_j = -40$  to  $150$  °C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Operating range</b>						
Input voltage	$V_I$	–	–	45	V	–
Junction temperature	$T_j$	-40	–	150	°C	–
<b>Thermal data</b>						
Junction-ambient	$R_{thja}$	–	–	200	K/W	PG-DSO-8
		–	–	70	K/W	PG-DSO-14
Junction-pin	$R_{thjp}$	–	–	30	K/W	PG-DSO-14 <sup>1)</sup>

1) measured to Pin 4

**General product characteristics**

**3.2 Electrical characteristics**

**Table 4 Electrical characteristics**

$V_I = 13.5\text{ V}; -40\text{ °C} \leq T_j \leq 125\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage	$V_Q$	4.90	5.00	5.10	V	$1\text{ mA} \leq I_Q \leq 100\text{ mA}$ $6\text{ V} \leq V_I \leq 16\text{ V}$
Current limit	$I_Q$	150	200	500	mA	–
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	150	300	$\mu\text{A}$	$I_Q \leq 1\text{ mA}, T_j < 85\text{ °C}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	250	700	$\mu\text{A}$	$I_Q = 10\text{ mA}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	2	8	mA	$I_Q = 50\text{ mA}$
Drop voltage	$V_{dr}$	–	0.25	0.5	V	$I_Q = 100\text{ mA}^{1)}$
Load regulation	$\Delta V_Q$	–	10	30	mV	$I_Q = 5\text{ mA to } 100\text{ mA}$
Line regulation	$\Delta V_Q$	–	10	40	mV	$V_I = 6\text{ V to } 26\text{ V}$ $I_Q = 1\text{ mA}$

**Reset generator**

Switching threshold	$V_{RT}$	4.50	4.65	4.80	V	–
Reset adjust switching voltage	$V_{RADJ,TH}$	1.26	1.35	1.44	V	$V_Q > 3.5\text{ V}$
Reset low voltage	$V_{RO,SAT}$	–	0.1	0.4	V	$R_{\text{extern}} = 20\text{ k}\Omega$
Upper delay switching threshold	$V_{UD}$	1.4	1.8	2.2	V	–
Lower delay switching threshold	$V_{LD}$	0.3	0.45	0.60	V	–
Reset delay low voltage	$V_{D,SAT}$	–	–	0.1	V	$V_Q < V_{RT}$
Charge current	$I_D$	3.0	6.5	9.5	$\mu\text{A}$	$V_D = 1\text{ V}$
Delay time L → H	$t_d$	17	28	–	ms	$C_D = 100\text{ nF}$
Delay time H → L	$t_t$	–	1	–	$\mu\text{s}$	$C_D = 100\text{ nF}$

**Input voltage sense**

Sense threshold high	$V_{SI,high}$	1.24	1.31	1.38	V	–
Sense threshold low	$V_{SI,low}$	1.16	1.20	1.28	V	–
Sense output low voltage	$V_{SO,low}$	–	0.1	0.4	V	$V_{SI} < 1.20\text{ V};$ $V_Q > 3\text{ V};$ $R_{\text{extern}} = 20\text{ k}\Omega$
Sense input current	$I_{SI}$	-1	0.1	1	$\mu\text{A}$	–

1) Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.)



## Functional description

### 4 Functional description

The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor  $C_D$  is greater or equal  $V_{UD}$ . The delay capacitor  $C_D$  is charged with the current  $I_D$  for output voltages greater than the reset threshold  $V_{RT}$ . If the output voltage gets lower than  $V_{RT}$  ('reset condition') a fast discharge of the delay capacitor  $C_D$  sets in and as soon as  $V_D$  gets lower than  $V_{LD}$  the reset output RO is set to low-level.

The time gap for the delay capacitor discharge is the reset reaction time  $t_{RR}$ .

The reset threshold  $V_{RT}$  can be decreased via an external voltage divider connected to the pin RADJ. In this case the reset condition is reached if  $V_Q < V_{RT}$  and  $V_{RADJ} < V_{RAQDJ,TH}$ . Dimensioning the voltage divider (see [Figure 4](#)) according to:

(4.1)

$$V_{THRES} = \frac{V_{RAD(J, TH)} \times (R_{ADJ1} + R_{ADJ2})}{R_{ADJ2}}$$

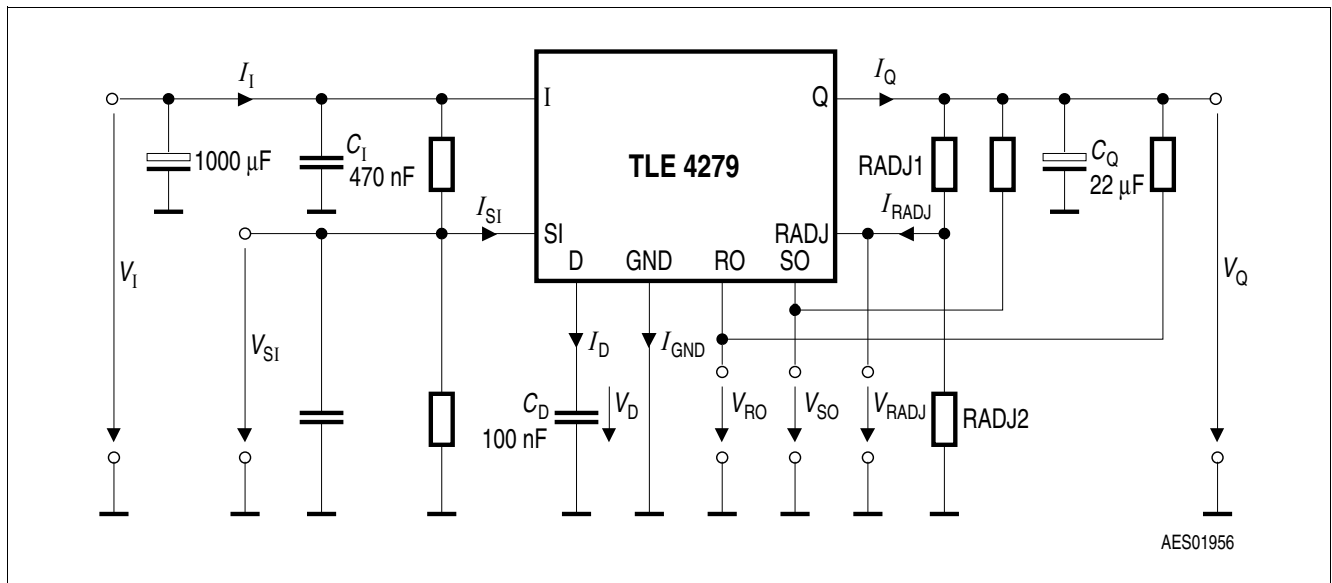
the reset threshold can be decreased down to 3.5 V. If the reset-adjust-option is not needed the RADJ-pin should be connected to GND causing the reset threshold to go to its default value (typ. 4.65 V).

A built in comparator compares the signal of the pin SI, normally fed by a voltage divider from the input voltage, with the reference and gives an early warning on the pin SO. It is also possible to superwise another voltage e.g. of a second regulator, or to build a watchdog circuit with few external components.

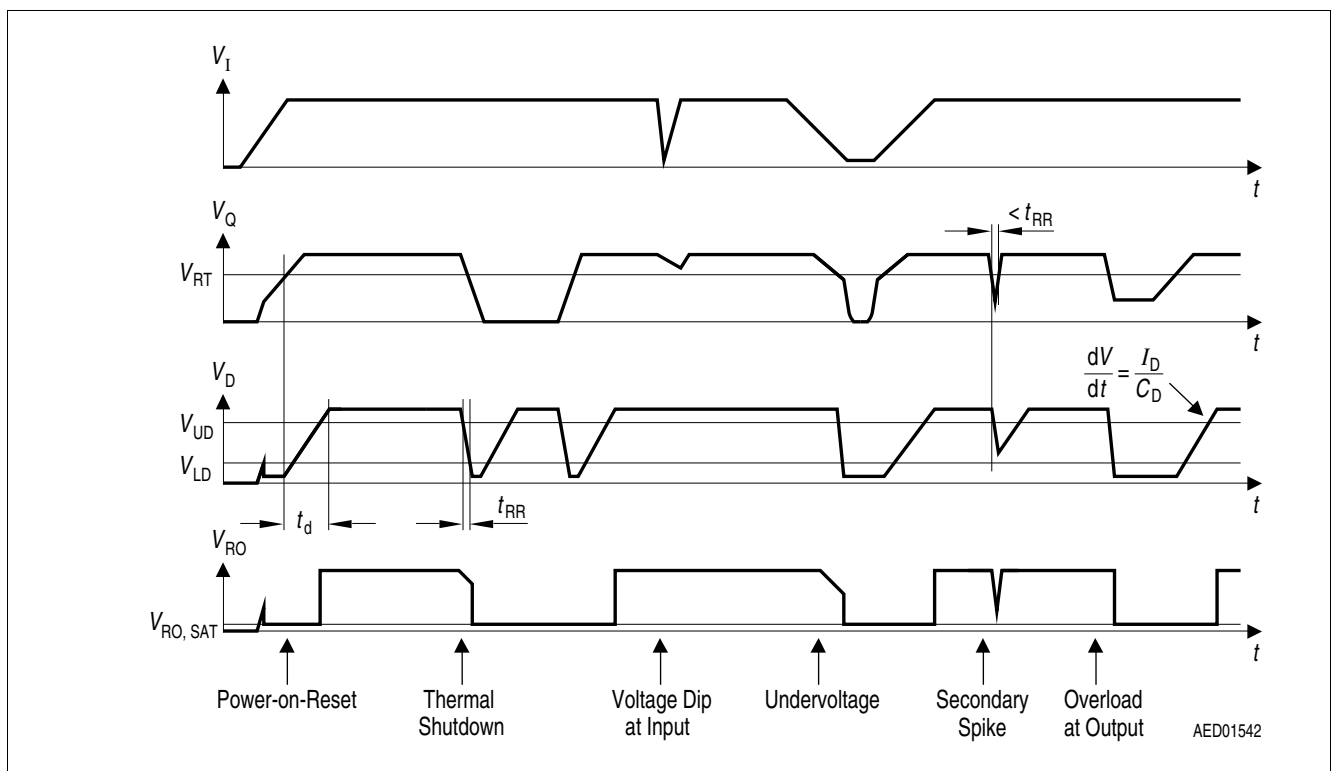
**Application information**

**5 Application information**

The input capacitor  $C_1$  is necessary for compensating line influences. Using a resistor of approx.  $1\ \Omega$  in series with  $C_1$ , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor  $C_Q$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values  $\geq 10\ \mu\text{F}$  and an  $\text{ESR} \leq 10\ \Omega$  within the operating temperature range. Both reset output and sense output are open collector outputs and have to be connected to 5 V output via external pull-up resistors  $\geq 10\ \text{k}\Omega$ . For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

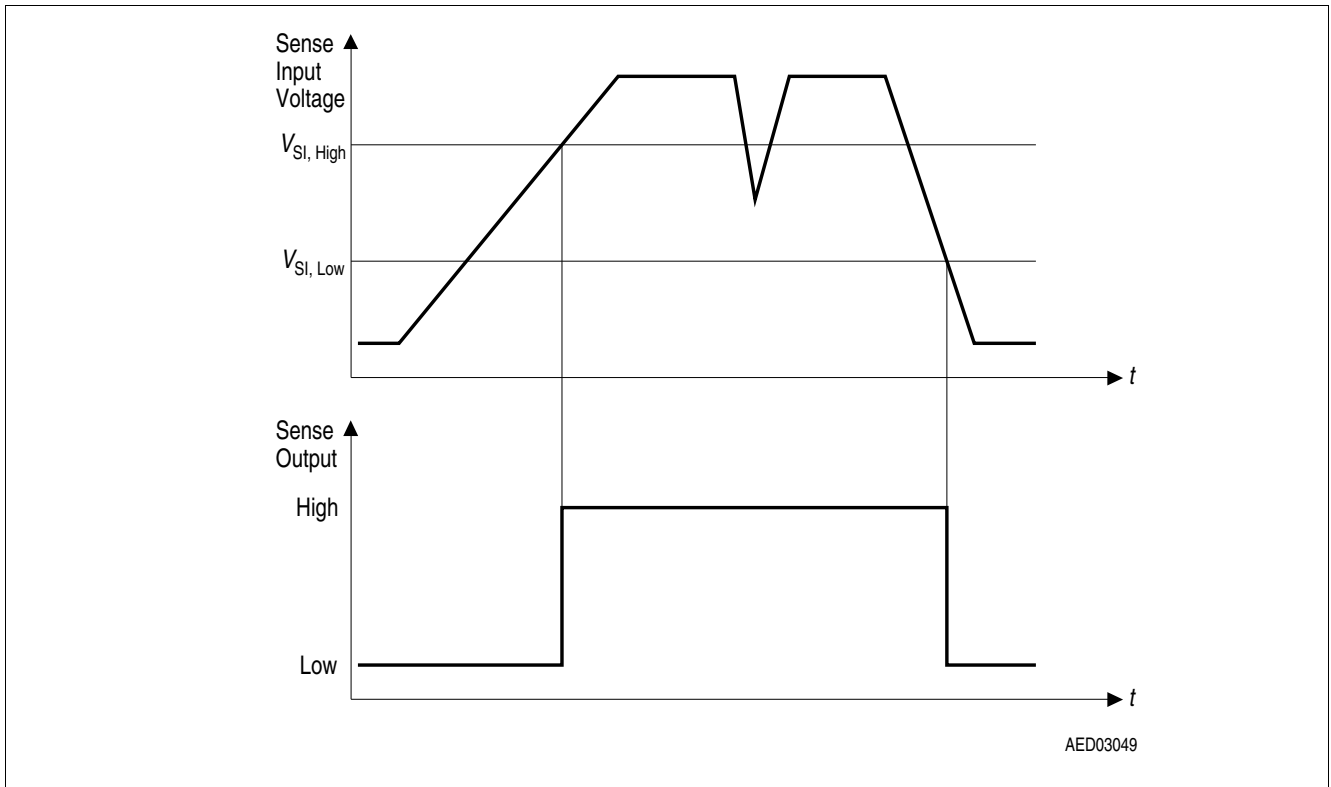


**Figure 4 Measuring circuit**



**Figure 5 Reset timing diagram**

**Application information**

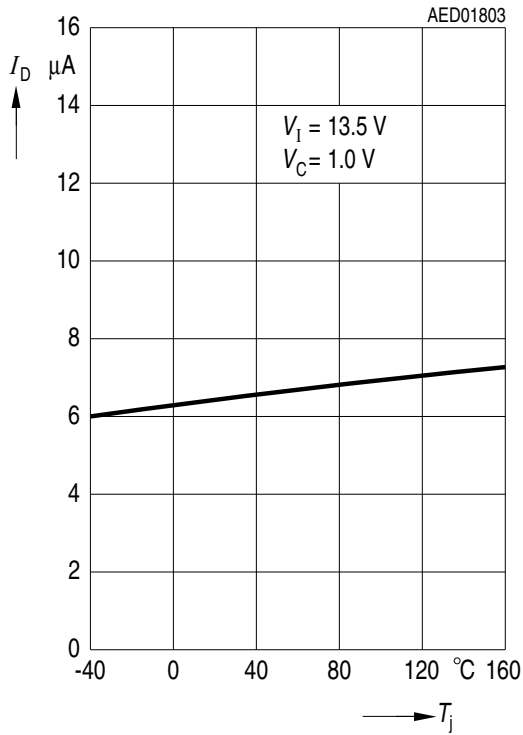


**Figure 6 Sense input timing diagram**

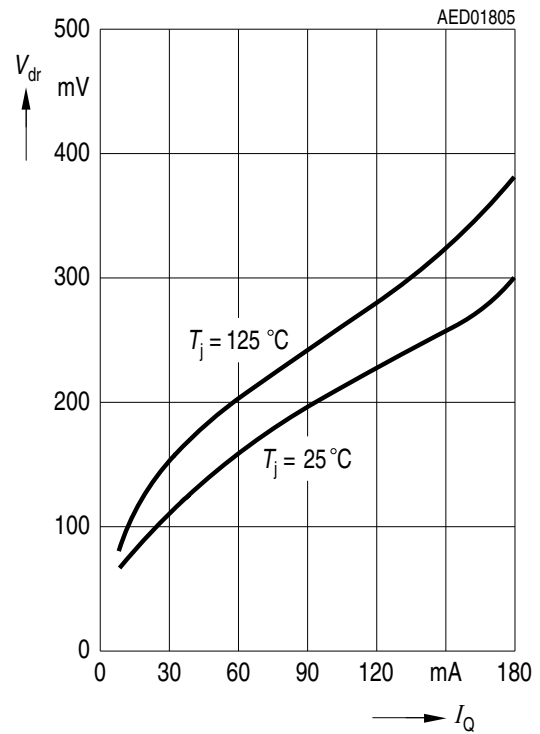
**Application information**

**5.1 Typical performance characteristics**

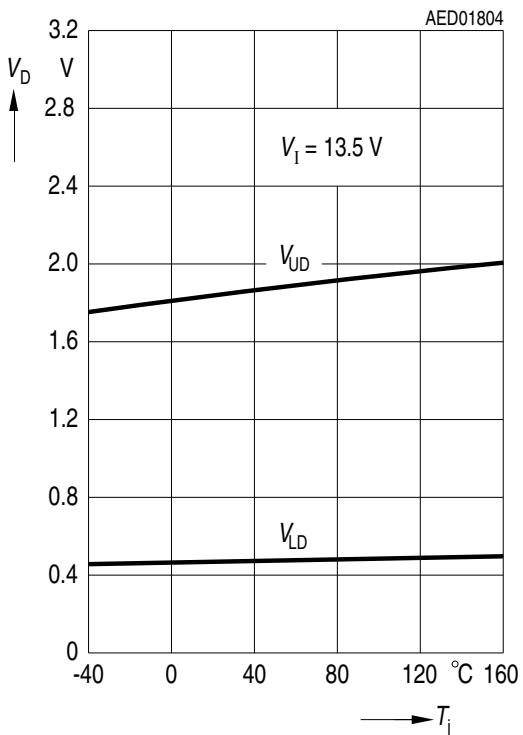
**Charge current  $I_D$  versus temperature  $T_j$**



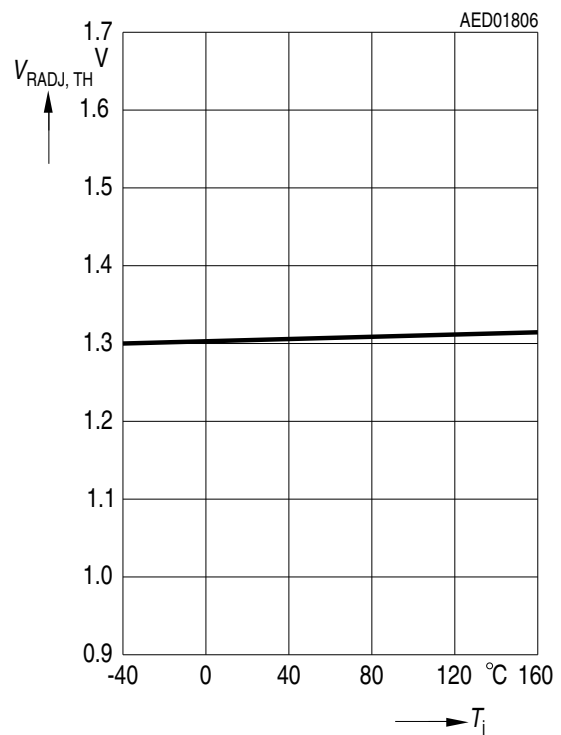
**Drop voltage  $V_{dr}$  versus output current  $I_Q$**



**Switching voltage  $V_{UD}$  and  $V_{LD}$  versus temperature  $T_j$**

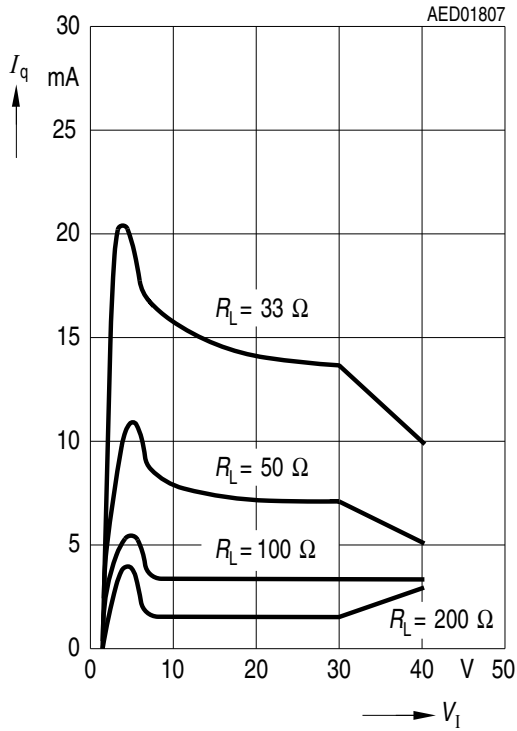


**Reset adjust switching threshold  $V_{RADJ,TH}$  versus temperature  $T_j$**

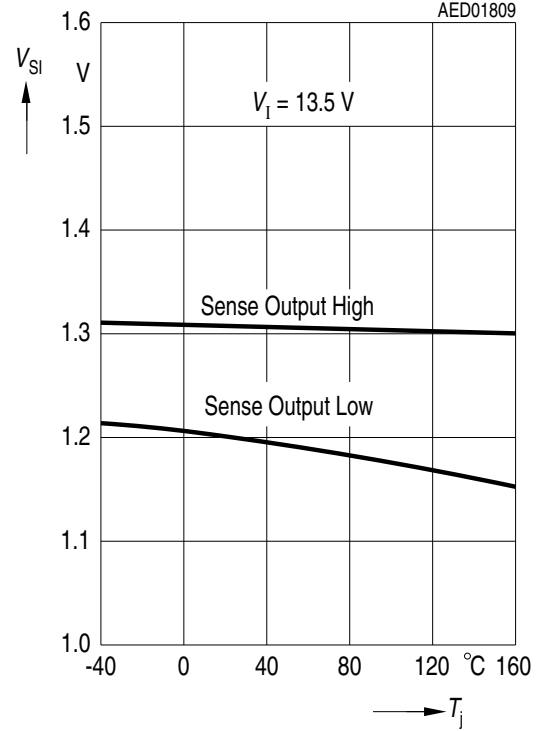


**Application information**

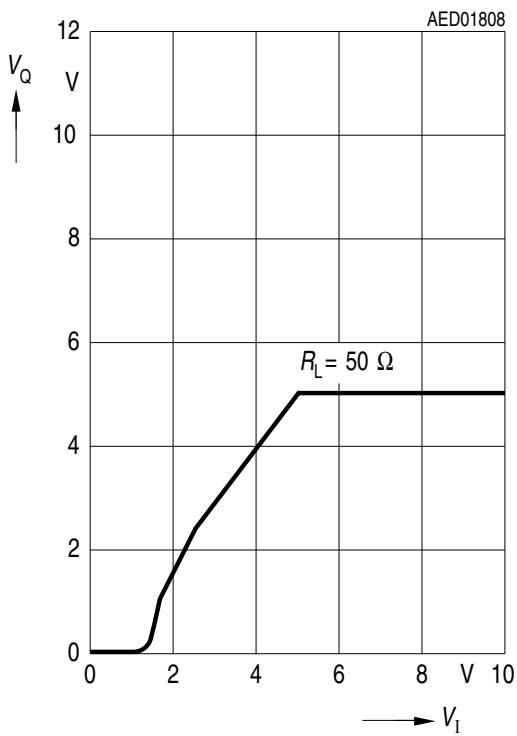
**Current consumption  $I_Q$  versus input voltage  $V_I$**



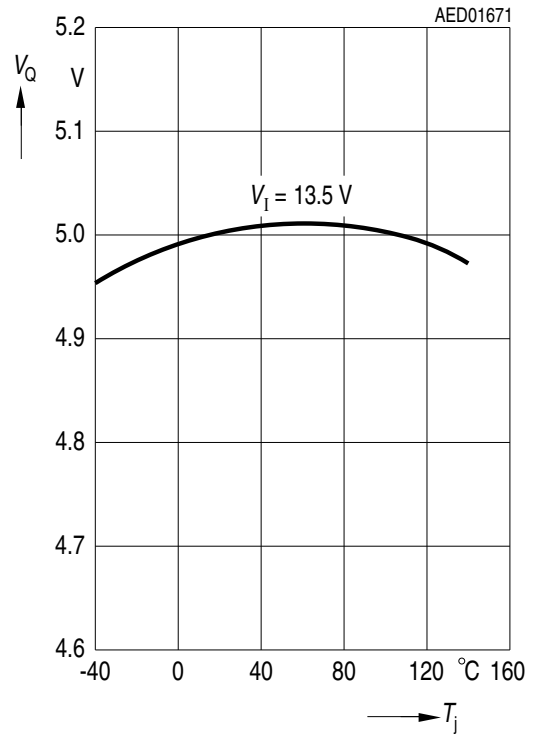
**Sense threshold  $V_{SI}$  versus temperature  $T_j$**



**Output voltage  $V_Q$  versus input voltage  $V_I$**

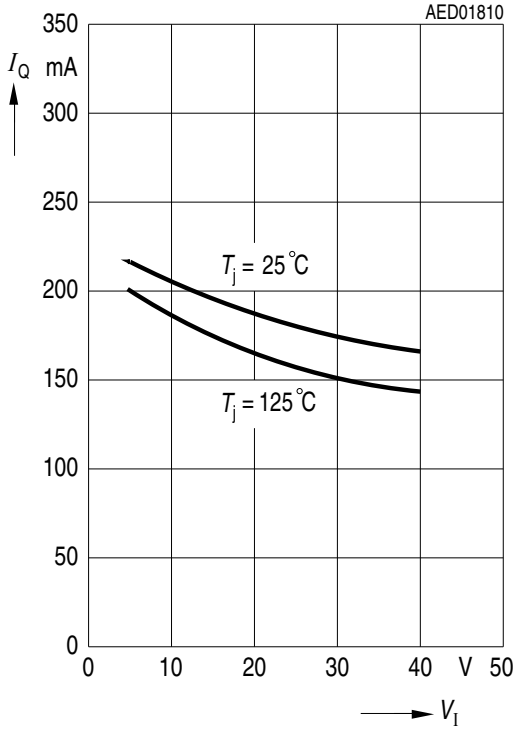


**Output voltage  $V_Q$  versus temperature  $T_j$**

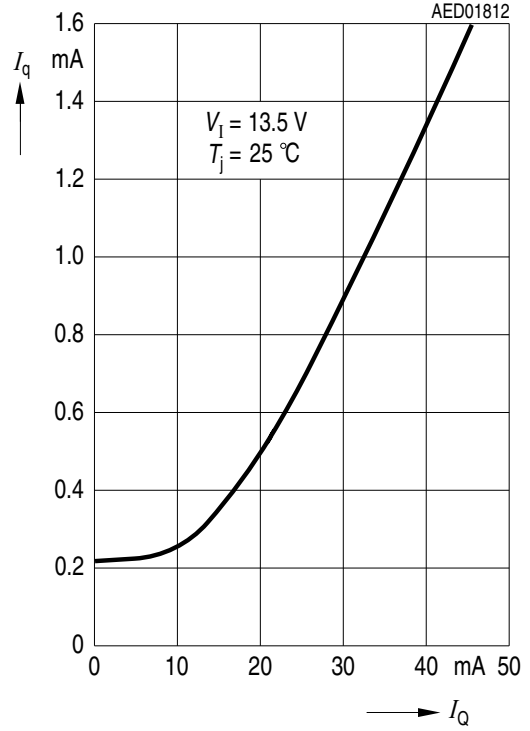


**Application information**

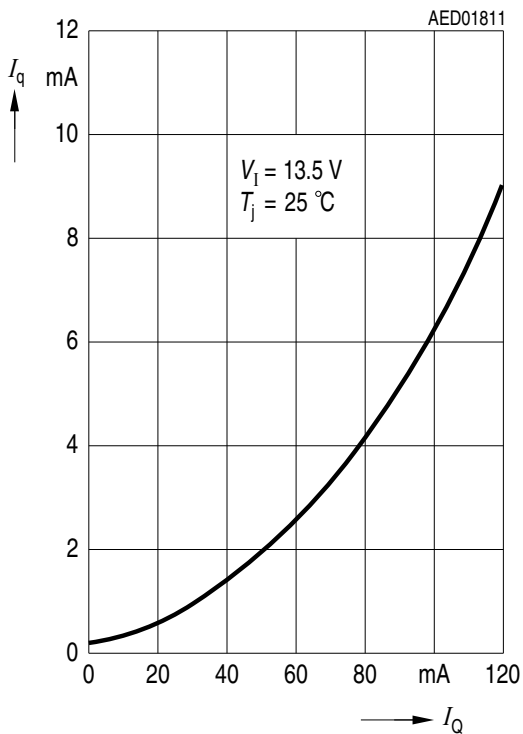
**Output current  $I_Q$  versus input voltage  $V_I$**



**Current consumption  $I_q$  versus output current  $I_Q$**

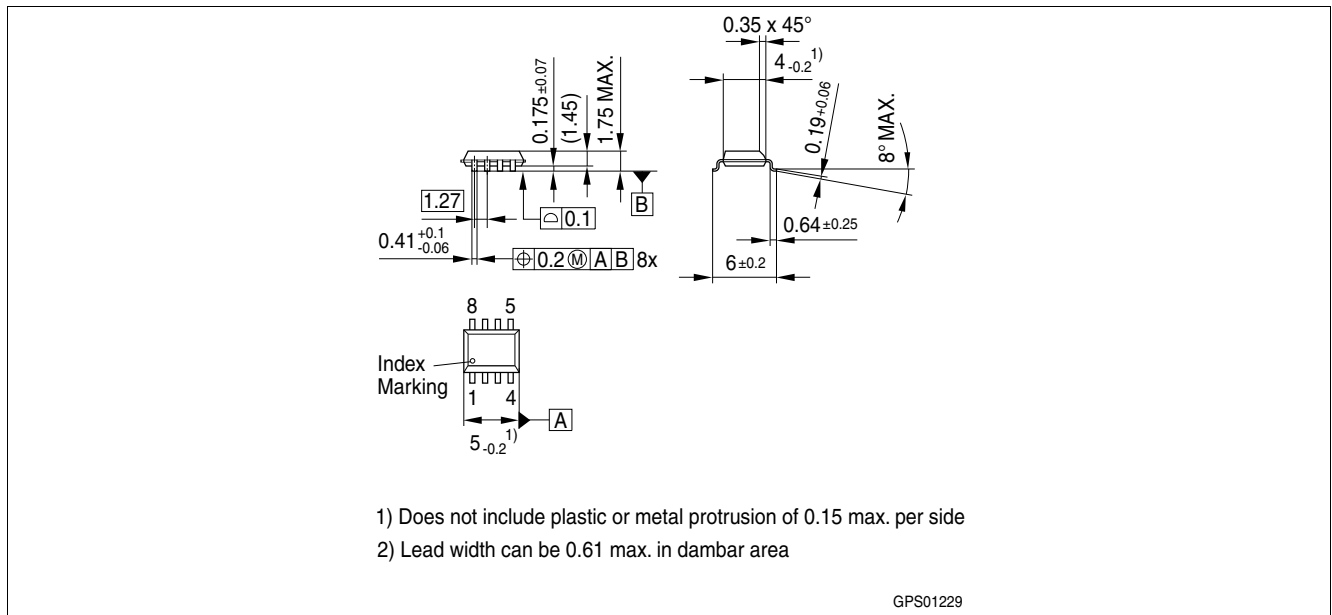


**Current consumption  $I_q$  versus output current  $I_Q$**

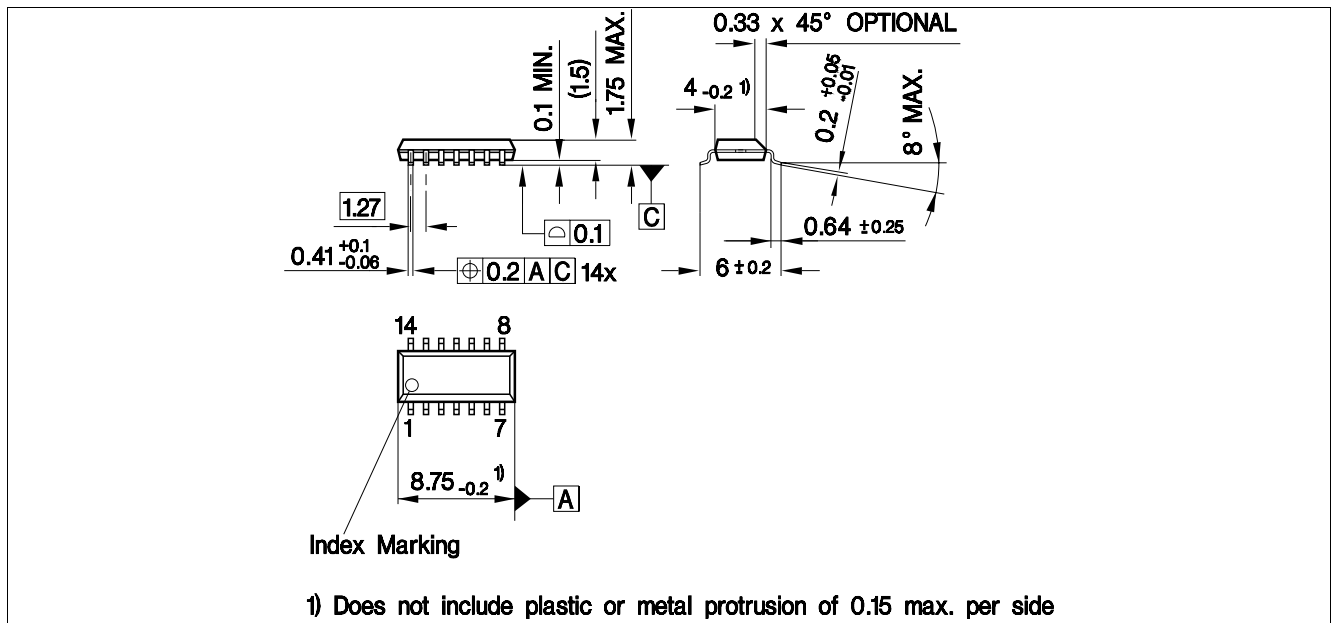


**Package information**

**6 Package information**



**Figure 7 PG-DSO-8 (Plastic Dual Small Outline)<sup>1)</sup>**



**Figure 8 PG-DSO-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages**

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
2.5	2018-11-19	Updated package drawing “PG-DSO-14” Editorial changes
2.4	2007-03-20	Initial version of RoHS-compliant derivate of TLE4279 Page 1: AEC certified statement added Page1 and 15: RoHS compliance statement and Green product feature added Package changed to RoHS compliant version Legal disclaimer updated



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**Document reference**

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