BROADCOM®

Data Sheet

AFBR-58x3xxZ

125-Mbaud Fast Ethernet Transceiver

Description

The Broadcom® AFBR-58x3xxZ transceivers provide the system designer with products to implement a range of 125-Mbaud Fast Ethernet and FDDI as well as 100-Mb/s Asynchronous Transfer Mode (ATM) designs.

As an enhancement, the AFBR-5823xxZ transceivers are compatible with SFF-8472 (digital diagnostic interface for optical transceivers). Using the 2-wire serial interface defined in the SFF-8472 MSA, the AFBR-5823xxZ transceivers provide real-time information on temperature, bias current, LED average output power, and receiver average input power. The interface also adds the ability to monitor the Receiver Loss of Signal (Rx_LOS). The transceivers are all supplied in the industry standard 1 × 9 and 2 × 9 package style with either a duplex SC or a duplex ST[1] connector interface.

Product Overview

The following table shows the complete list of available part numbers, as well as the form factor and the fiber connector type of each of the part numbers.

Part Number	Form Factor	Fiber Connector
AFBR-5813TQZ	1 × 9 transceiver	ST connector
AFBR-5813QZ	1 × 9 transceiver	SC connector
AFBR-5823TQZ	2 × 9 transceiver	ST connector
AFBR-5823QZ	2 × 9 transceiver	SC connector

Features

- Full compatibility with 100BASE-FX version IEEE802.3u
- Full compatibility with FDDI
- Multisource 1 × 9 package style with choice of duplex SC or duplex ST receptacle
- DMI interface with 2 × 9 devices
- Single 3.3V power supply operation
- ACPECL differential data input with integrated termination
- DCPECL differential data output
- DCPECL signal detect output
- Industrial temperature range –40°C to 85°C
- Wave solder and aqueous wash process compatible
- RoHS compliant

Applications

- Multimode 50-µm or 62.5-µm core fiber backbone links up to 2 km
- Multimode fiber wiring closet to desktop links
- Very low cost multimode fiber links from wiring closet to desktop
- Multimode fiber media converters

1. ST is a registered trademark of AT&T Lightguide Cable Connectors.

Transmitter Sections

The transmitter sections of the AFBR-58x3xxZ series use 1300-nm surface-emitting InGaP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a silicon IC, which converts differential PECL logic signals, ECL referenced (shifted) to a 3.3V supply, into an analog LED drive current.

The input of the transmitter sections is internally AC-coupled and terminated. If a DC signal is received, there is no light output.

Receiver Sections

The receiver sections of the AFBR-58x3xxZ series use InGaAs PIN photodiodes coupled to a silicon IC, which are packaged in the optical subassembly portion of the receiver.

The IC combines the functionality of a transimpedance amplifier and a quantizer providing final pulse shaping for the logical output and the signal detect function. The data output is differential and the signal detect is single ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3V power supply.

The receiver has no AC detection implemented. However, if the input power gets too low, squelch mode of the receiver is activated and the data output switches to high resistance.

Package

The overall package concept for the Broadcom transceivers consists of the following basic elements: two optical subassemblies, an electric subassembly, and the housing as illustrated in Figure 1, Figure 2, Figure 3, and Figure 4.

The package outline drawings and pinout are shown in Figure 5, Figure 6, Figure 7, and Figure 8. The details of this package outline and pinout are compliant with the multisource definition of the 1 × 9 SIP. The low profile of the Broadcom transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

The optical subassemblies use a high-volume assembly process together with low-cost lens elements, which result in a cost-effective building block.

The electrical subassembly consists of a high-volume, multilayer printed circuit board on which the IC chips and various surface-mounted passive circuit elements are attached.

The outer housing including the duplex SC connector receptacle or the duplex ST ports is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Broadcom design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts that exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with duplex of simplex SC or ST connectored fiber cables.

Figure 1: Block Diagram 1 × 9 ST Transceiver

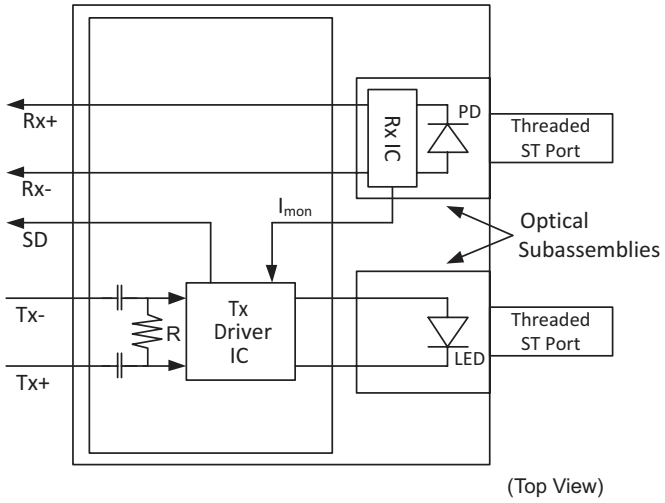


Figure 2: Block Diagram 1 × 9 SC Transceiver

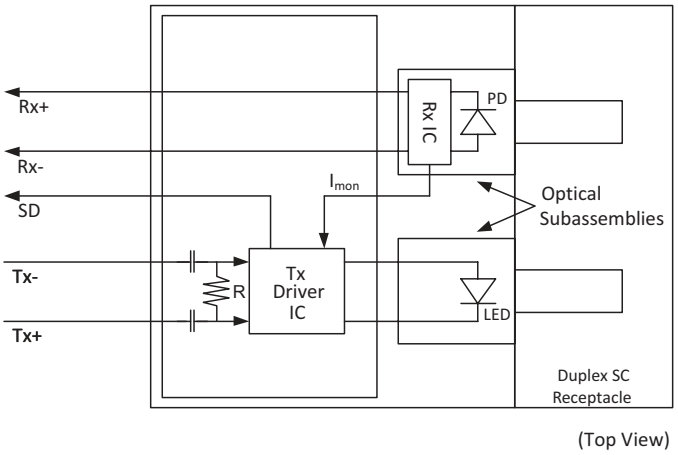


Figure 3: Block Diagram 2 × 9 ST Transceiver

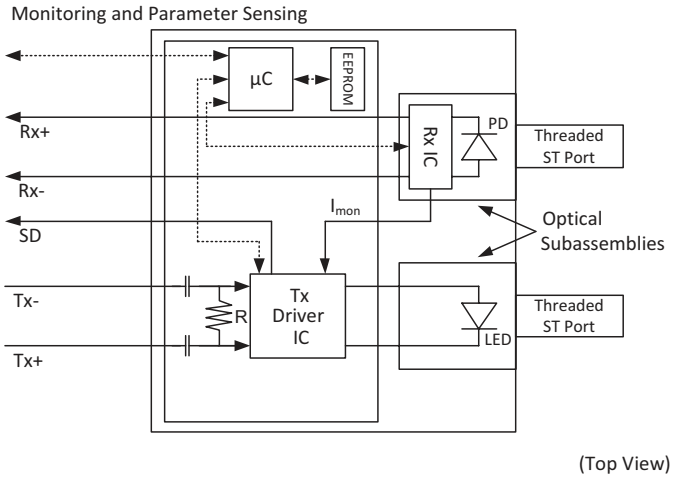


Figure 4: Block Diagram 2 × 9 SC Transceiver

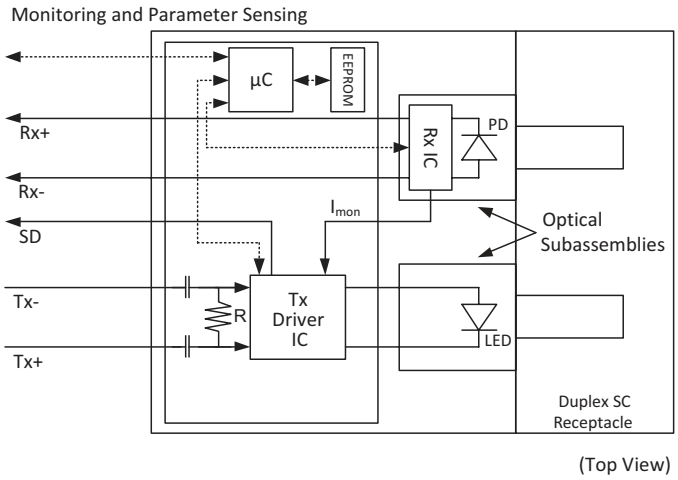


Figure 5: 1 × 9 ST Package Outline Drawings (Dimensions in mm)

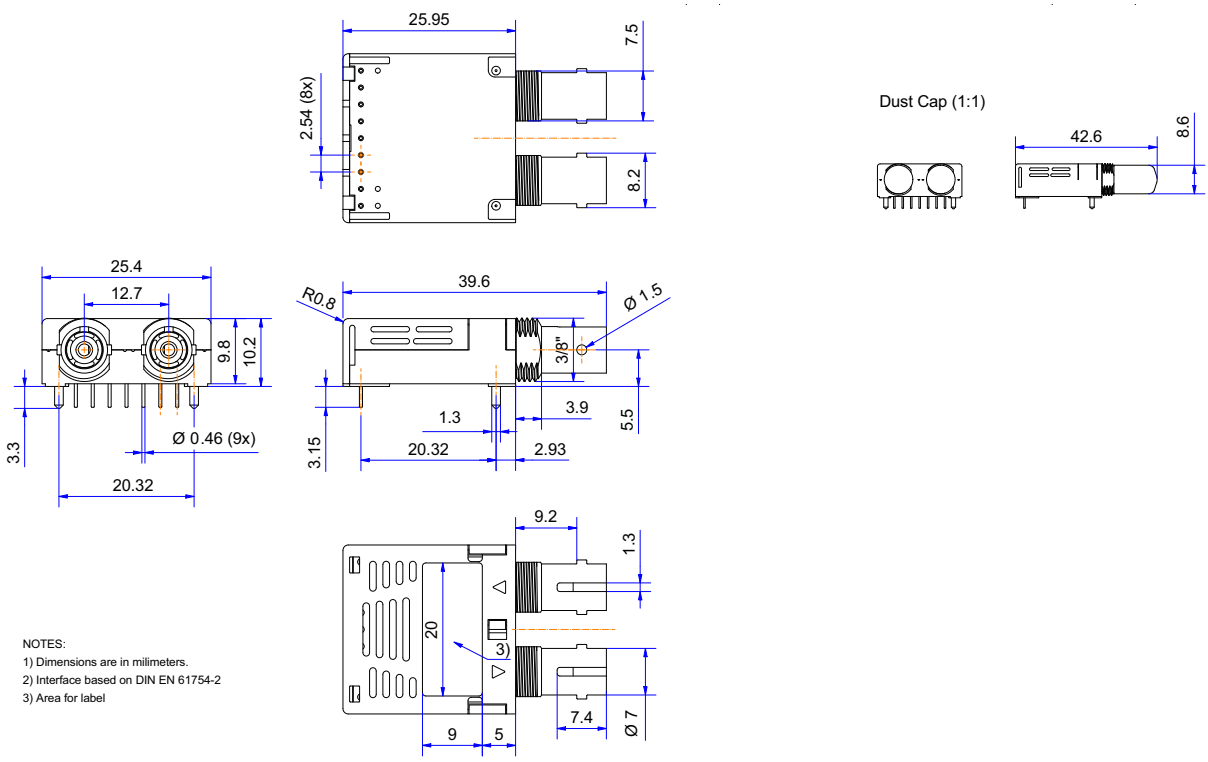


Figure 6: 2 × 9 ST Package Outline Drawings (Dimensions in mm)

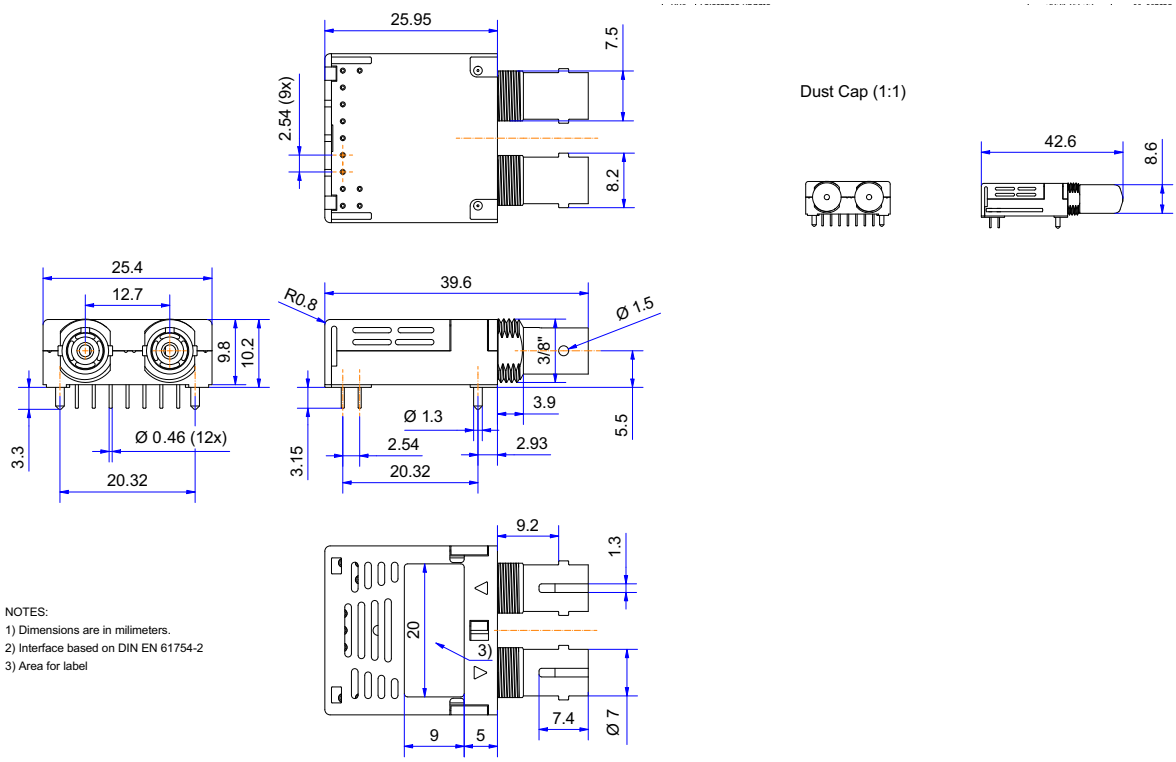


Figure 7: 1 × 9 SC Package Outline Drawings (Dimensions in mm)

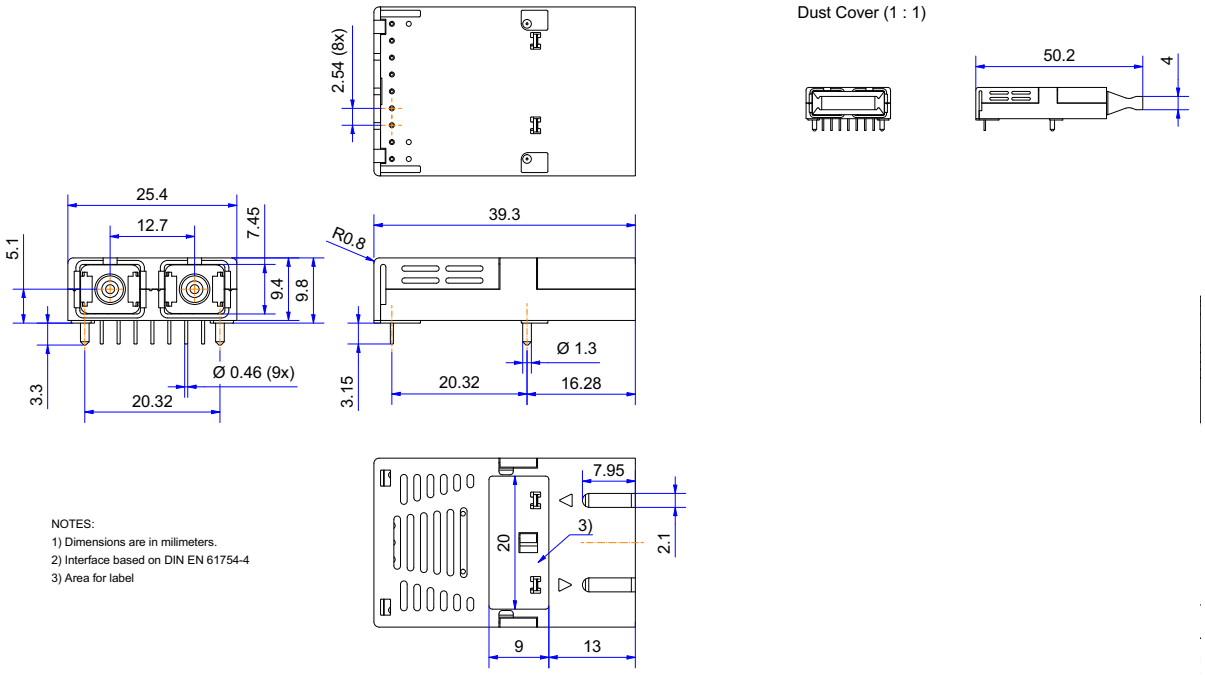


Figure 8: 2 × 9 SC Package Outline Drawings (Dimensions in mm)

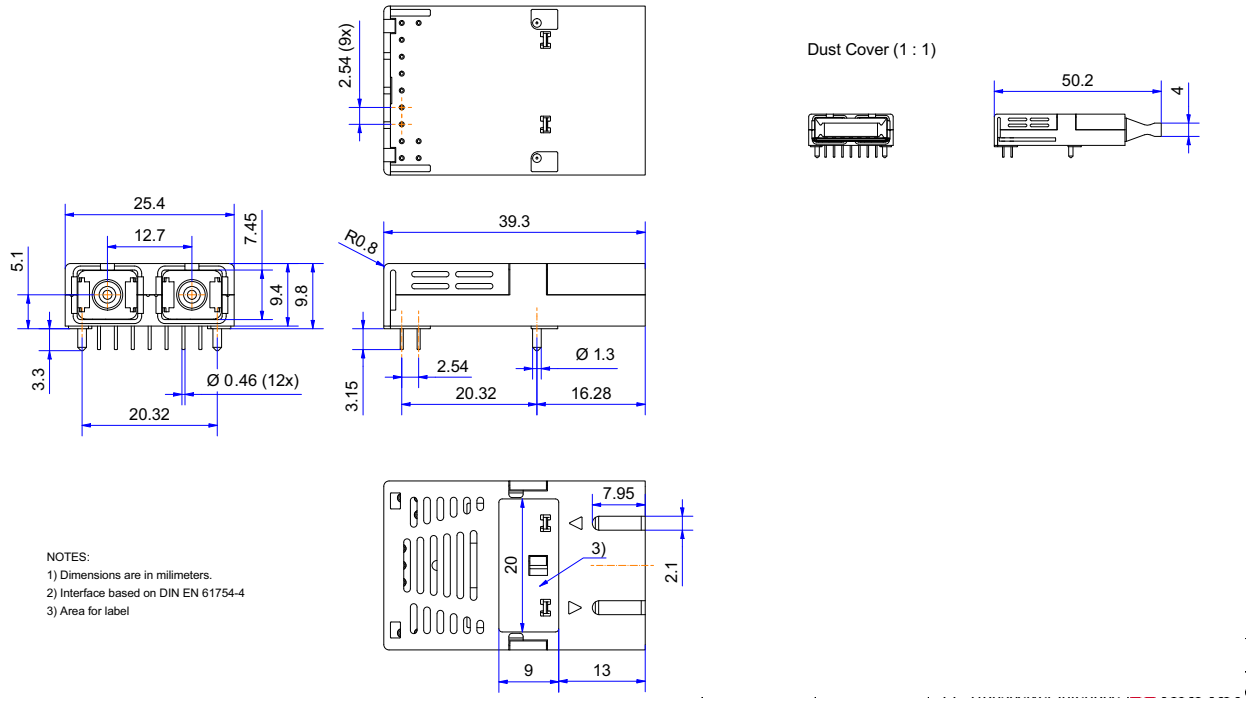
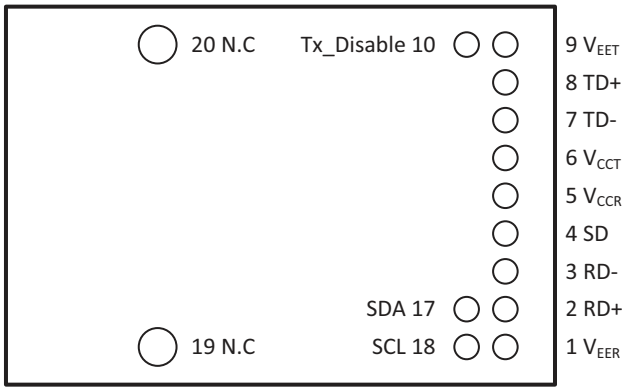


Figure 9: Pin Out Diagram of the Transceiver (Top View)



Pin	Description
1	V_{EER}
2	RD+
3	RD-
4	SD
5	V_{CCR}
6	V_{CCT}
7	TD-
8	TD+
9	V_{EET}
10	TX_Disable
17	SDA
18	SCL
19	N.C.
20	N.C.

Pin Descriptions

Pin 1 V_{EER}: Receiver ground pin. Directly connect these pin to the ground plane of the host board.

Pin 2 RD+: Receiver data out. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated.

Pin 3 RD-: Receiver data out bar. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated.

Pin 4 SD: Signal detect pin. If an optical signal is present at the optical input, SD output is a logic "1". Absence of an optical input signal results in a logic "0" output. This pin can be used to drive a DCPECL input of an upstream circuit.

Pin 5 V_{CCR}: Receiver power supply pin. Provide +3.3 V DC via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the Rx Vcc pin.

Pin 6 V_{CCT}: Transmitter power supply pin. Provide +3.3 V DC via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the Tx Vcc pin.

Pin 7 TD-: Transmitter data in bar. This input is a 3.3V LVPECL/LVDS compatible differential line.

Pin 8 TD+: Transmitter data in. This input is a 3.3V LVPECL/LVDS compatible differential line.

Pin 9 V_{EET}: Transmitter ground pin. Directly connect these pins to the ground plane of the host board.

Pin 10 TX_Disable: Disables the Transmitter output driver when set to high (only available for 2 x 9 devices).

Pin 17 SDA: System Data. Data stream input for the DMI interface (only available for 2 x 9 devices).

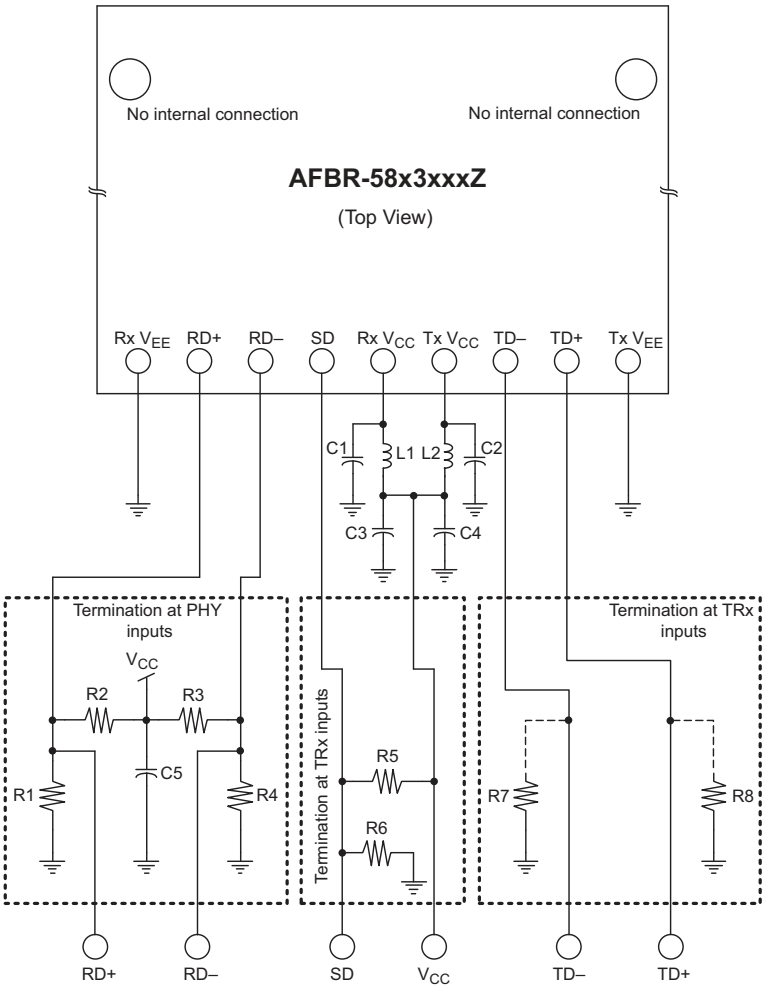
Pin 18 SCL: System Clock. Clock input for the DMI interface (only available for 2 x 9 devices).

Pin 19 N.C.: For mechanical stabilization only. No electrical function.

Pin 20 N.C.: For mechanical stabilization only. No electrical function.

Recommended Application Circuit

Figure 10: Recommended Decoupling and Termination Circuits



NOTE: The split-load termination for ECL signals needs to be located at the input of devices receiving those ECL signals. For the application board, it is recommended to use a four-layer printed circuit board with 50Ω microstrip signal paths. The value of the elements shown in the schematic in Figure 10 are as follows:

R1 = R4 = R6 = 82Ω
R2 = R3 = R5 = 130Ω
R7 = R8 = 150Ω
C1 = C2 = C3 = C5 =0.1 µF
C4 = 10 µF
L1 = L2 = 1 µH Coil or Ferrite Inductor

The output of the SD is regulated DCPECL, and therefore, to minimize the current consumption, output R9 can be removed and R10 can be selected up to 680Ω (in total, up to 30 mA can be saved by implementing this termination).

* Optional bias resistor to ground (depending on the SerDes used) is typically 150Ω if needed. Otherwise, no external termination at the Tx-Side is required.

Recommended Handling Precautions

Take normal static precautions in the handling and assembly of these transceivers to prevent damage that may be induced by electrostatic discharge (ESD). The AFBR-58x3xxZ series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Take care to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the duplex SC or duplex ST connector receptacle. This process plugs protect the optical subassemblies during wave soldering and aqueous wash processing and acts as a dust cover during the processes.

The transceivers are compatible with either industry-standard wave or hand soldering processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout

Take care when laying out your circuit boards to achieve optimum performance from these transceivers. Figure 10 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. Use a contiguous ground plane in the circuit board directly under the transceiver to provide a low inductance ground for signal return current; this is in keeping with good frequency board layout practices.

Board Layout – Hole Pattern

The Broadcom transceiver complies with the circuit board Common Transceiver Footprint hole pattern defined in the original multisource announcement that defined the 1 × 9 package style.

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See Regulatory Compliance for details. Additional information is available from your Broadcom sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD-sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD-controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs using these high-speed transceivers from Broadcom will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

Immunity

Equipment utilizing transceivers will be subject to radio-frequency electromagnetic fields in some environments. The AFBR-58x3xxZ transceivers have a high immunity to such fields.

Transceiver Reliability and Performance Qualification Data

The AFBR-58x3xxZ transceivers have passed Broadcom reliability and performance qualification testing and are undergoing ongoing quality monitoring. In particular this includes a monitoring test of the TOSA/ROSA wire bond quality after 300°C/1 hour baking. Further details are available from your Broadcom sales representative. TOSA/ROSA are hermetically sealed and monitored with a gross and fine leakage test.

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD)	JEDEC JS-001-2011	HBM 2 kV.
Immunity	EN 55024 EN 61000-4-3	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 2 GHz and 3V/m field swept from 2 GHz to 6 GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye Safety	EN 60825-1:Edition 3.0	Laser class 1 product (LED radiation only). TÜV certificate: R 50377267. Use of controls or adjustments of performance or procedures other than those specified herein may result in hazardous radiation exposure.
Component Recognition	Underwriter Laboratories	UL File E173874, Vol 1.
Housing Material	Underwriter Laboratories	Flammability class 94V-0.
EMI	FCC Class B CENELEC EN55022 Class B	Transceivers typically provide a 6-dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card. However, note that the final margin depends on the customer's board and chassis design.
RoHS I and II Compliance	—	Reference to RoHS Directive 2011/65EU Annex II and RoHS RL (EU) 2015-863.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	–40	+100	°C	—
Supply Voltage	V_{CC}	–0.3	4	V	—
Data Input Voltage	V_i	–0.5	V_{CC}	V	—
Lead Soldering Temperature	T_{sold}	—	260	°C	MSL1
Lead Soldering Time	t_{sold}	—	10	s	—
Differential Input Voltage (Peak-to-Peak)	V_D	0.1	2	V	Voltage between Din+ and Din-
Output Current	I_O	—	40	mA	—

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Ambient Operating Temperature	T_C	–40	—	+85	°C	a
Supply Voltage	V_{CC}	3.13	3.3	3.47	V	—
Data Output Load	R_L	—	100	—	Ω	—
Signaling Rate (Fast Ethernet)	B_{FE}	—	125	—	Mbaud	b
Data Input Differential Amplitude	V_{DIFF}	0.5	1.0	1.8	V	—

a. Electrical and optical specifications of the product are guaranteed across the recommended ambient operating temperature range only.

b. 4B/5B+NRZI. Ethernet autonegotiation pulses are not supported.

Transmitter Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	Tx_Icc	—	—	100	mA	Current over Tx IC
Power Dissipation	PDISS	—	—	300	mW	—
Data Input Differential Termination	Rin	—	100	—	Ω	—

Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Average Launched Power 62.5/125-µm NA = 0.275 Fiber	Po	–20	–17	–13	dBm	EOL (–19 dBm minimum BOL)
Average Launched Power 50/125-µm NA = 0.2 Fiber	Po	–23.5	–20	–13	dBm	EOL (–22.5 dBm minimum BOL)
Extinction Ratio	EXT	10	—	—	dB	—
Central Wavelength	λ_c	1270	1308	1380	nm	—
Spectral Width – FWHM	$\Delta\lambda$	—	147	—	nm	—
Optical Rise Time (10% to 90%)	t_r	0.6	—	3.0	ns	—
Optical Fall Time (90% to 10%)	t_f	0.6	—	3.0	ns	—
Duty Cycle Distortion Contributed by the Transmitter	DCD	—	0.2	0.6	ns	a, b
Data Dependent Jitter Contributed by the Transmitter	DDJ	—	—	0.6	ns	b
Random Jitter Contributed by the Transmitter (Peak-to-Peak)	RJ	—	0.1	0.69	ns	b

a. DCD contributed by the transmitter is measured at the 50% threshold of the optical output signal.

b. Characterized with PRBS7.

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	Rx_Icc	—	—	50	mA	a
Power Dissipation	Pdiss	—	—	175	mW	—
Data Output Voltage – Low	V_{OL}–V_{CC}	–2	—	–1.55	V	—
Data Output Voltage – High	V_{OH}–V_{CC}	–1.3	—	–0.88	V	—
Receiver Differential Output Voltage	D_Ampl	1	—	1.8	V	—
Data Output Rise Time (10% to 90%)	t_r	0.35	—	2.2	ns	—
Data Output Fall Time (90% to 10%)	t_f	0.35	—	2.2	ns	—
Duty Cycle Distortion	DCD	—	—	0.4	ns	b, c
Data Dependent Jitter (Rise/Fall)	DDJ	—	—	1.0	ns	c
Random Jitter (Peak-to-Peak)	RJ	—	—	2.14	ns	c
Signal Detect Output Voltage – Low	V_{OL}-V_{CC}	–2	—	–1.55	V	—
Signal Detect Output Voltage – High	V_{OH}-V_{CC}	–1	—	–0.7	V	—
Signal Detect Rise Time (10% to 90%)	t_{SD_R}	—	—	10	ns	—
Signal Detect Fall Time (90% to 10%)	t_{SD_F}	—	—	10	ns	—

a. Current over Rx IC only. Values for 2 × 9 configurations. Due to different SD configuration change values by +15 mA for 1 × 9 Rx_Icc and –15 mA for 1 × 9 Tx_ICC. With SD terminated to 680Ω only, subtract 15 mA for 2 × 9 Tx_Icc and 15 mA for 1 × 9 Rx_Icc.

b. DCD contributed by the receiver is measured at the 50% threshold of the electrical output signal.

c. Characterized with PRBS7.

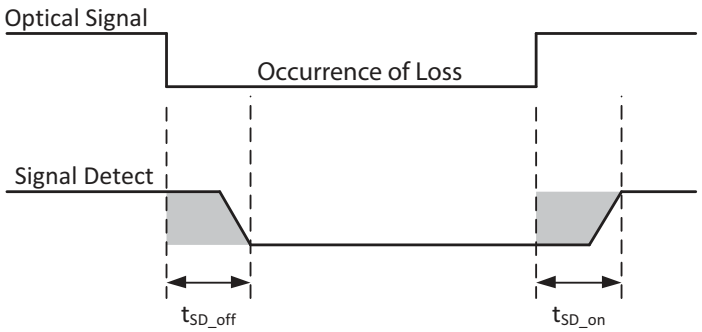
Transceiver Timing Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Hardware SD Assert Time	t_sd_on	—	100	µs	a
Hardware SD Deassert Time	t_sd_off	—	350	µs	b

a. Time from valid optical signal to SD assertion.

b. Time from loss of optical signal to SD deassertion.

Figure 11: Signal Detect Timing Diagram



Receiver Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Optical Input Power	P_{in}	–31	—	–12	dBm	a
Operating Wavelength	λ_c	1270	—	1380	nm	—
Signal Detect Asserted	P_A	—	—	–33	dBm	Average power
Signal Detect Deasserted	P_D	–45	—	—	dBm	Average power
Signal Detect Hysteresis	$P_A - P_D$	1.5	—	—	dB	—

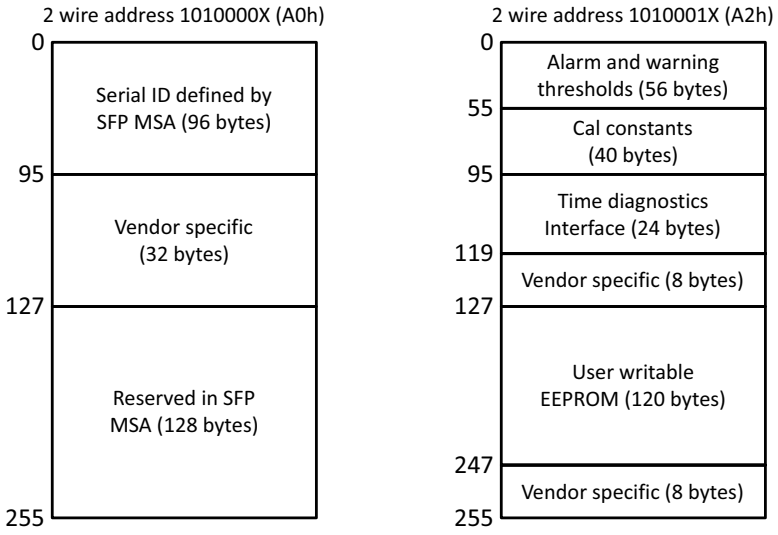
a. Average power, measured with a PRBS7 sequence, BER < 1×10^{-10}, and with a 62.5/125-µm NA = 0.275 fiber.

Digital Diagnostics Monitoring Interface

The transceivers AFBR-5823xxZ feature an enhanced digital diagnostic interface, compliant to the “Digital Diagnostic Monitoring Interface for Optical Transceivers” SFF-8472 Multi-source Agreement (MSA). Refer to the MSA document to access information on the range of options, both hardware and software, available to the host system for utilizing the available digital diagnostic features.

The enhanced digital interface allows real-time access to device operating parameters, and includes optional digital features, such as soft control and monitoring of I/O signals. In addition, it fully incorporates the functionality needed to implement digital alarms and warnings, as defined by the SFF-8472 MSA. With the digital diagnostic monitoring interface, the user has capability of performing component monitoring, fault isolation and failure prediction in their transceiver-based applications. The diagnostic monitoring interface (DMI) has two 256-byte memory maps in EEPROM that are accessible over a two-wire interface: the serial ID memory map at address 1010000X (0xA0) and the digital diagnostic memory map at address 1010001X (0xA2).

Figure 12: EEPROM Memory Maps



The serial ID memory map contains a serial identification and vendor-specific information. This information is read-only.

The digital diagnostic memory map contains device operating parameters as well as alarm and warning flags. The operating parameters are to be retrieved through a sequential read command ensuring that the MSB and LSB of each parameter are "coherent". Furthermore, it contains 120 bytes that can be written by the user as well as a writable soft control byte.

For applications which require continuous update of alarm and warning limits, use the available real-time monitor in combination with software algorithms. Continuous writing to alarm/warning registers should be avoided. See Absolute Maximum Ratings.

Transceiver Diagnostics Timing Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Time to Initialize	t_init	—	300	ms	a
Hardware TxDIS Assert Time	t_on	—	10	µs	b
Hardware TxDIS Deassert Time	t_off	—	30	µs	c
Software Tx_Disable Assert Time	t_off_soft	—	100	ms	d
Software Tx_Disable Deassert Time	t_on_soft	—	100	ms	e
Software Rx_LOS Assert Time	t_loss_on_soft	—	100	ms	f
Software Rx_LOS Deassert Time	t_loss_off_soft	—	100	ms	g
Analog Parameter Data Ready	t_data	—	1000	ms	h
Serial Hardware Ready	t_serial	—	300	ms	i
Write Cycle Time	t_write	—	10	ms	j
Serial ID Clock Rate	f_serial_clock	—	400	kHz	k

a. Time from power on to transmitter and receiver is ready to send/receive data. Refer to Figure 13.

b. Time from the rising edge of TxDIS to when the modulated optical output falls below 10% of nominal. Refer to Figure 14.

c. Time from the falling edge of TxDIS to when the modulated optical output rises above 90% of nominal. Refer to Figure 14.

d. Time from two-wired interface assertion of Tx_Disable (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.

e. Time from two-wired interface deassertion of Tx_Disable (A2h, byte 110, bit 6) to when the optical output rises above 90% of nominal.

f. Time from two-wired interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.

g. Time from two-wired interface deassertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.

h. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.

i. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).

j. Time from stop bit to completion of a 1-8 byte write command.

k. It is not recommended to continuously read the A2 digital diagnostic interface for more than 20 ms without a minimum time pause interval of 20 ms.
A2 can be accessed with up to 100 kHz without any special clock timing required.
Consideration of following timing is required when accessing A2 above 100 kHz. A2 can be accessed up to 400 kHz with following timing requirements:
Between every byte read/write transaction (that is, 8 clocks for data + 1 for ACK), there should be a time pause for minimum 5 µs (or better 10 µs), meaning that after a byte read/write next clock on the I²C bus from master should appear minimum after 5 µs (better 10 µs).

Figure 13: t_{init} for TxDIS Negated (Also Applicable for All 1 × 9 AFBR-58x3xxZ)

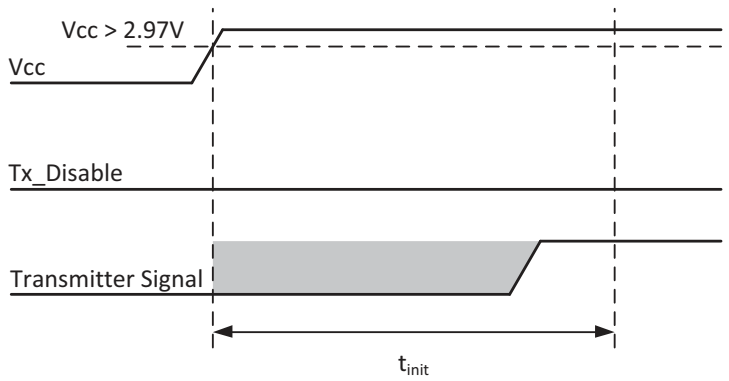
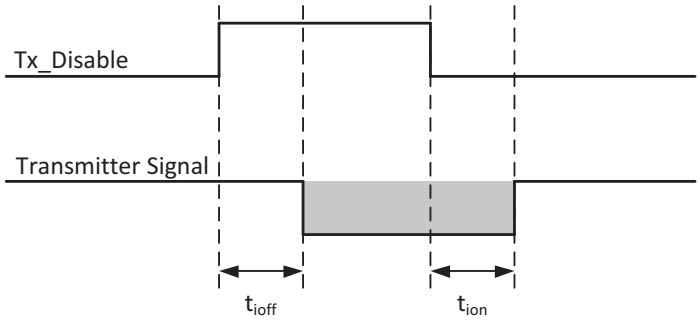


Figure 14: t_{off} and t_{on} for TxDIS Asserted and Then Negated



Transceiver Digital Diagnostic Monitor (Real-Time Parameter Accuracy) Characteristics

Parameter	Symbol	Max.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±5.0	°C	Registers indicate case temperature, which is derived from the internally measured temperature. Valid from –40°C to +85°C case temperature with Tx Enabled.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	±0.2	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP VCC pin. Valid over 3.3V ± 10%.
Transmitter LED DC Bias Current Accuracy	I_{BIAS}	±10	%	I_{BIAS} is better than ± 10% nominal value by design, the value is not monitored.
Transmitter Average Optical Power Accuracy	P_T	±3.0	dB	Transmitter power is PRBS7 modulated signal LED power value by design. P_T is actively not monitored.
Received Average Optical Input Power Accuracy	P_R	±3.0	dB	Coupled in a 62.5/125-µm fiber. Averaging time constant is about 100 kHz.

EEPROM and Serial ID

Table 1: EEPROM Serial ID Memory Contents – Address A0h

Byte Number Decimal	Hex	ASCII	Description	Byte # Decimal	Hex	ASCII	Description
0	00	—	0	37	00	—	—
1	00	—	—	38	17	—	—
2	01	—	SC connector; Hex 00 for ST connector	39	6A	—	—
3	00	—	—	40	41	A	—
4	00	—	—	41	46	F	—
5	00	—	—	42	42	B	—
6	20	—	—	43	52	R	—
7	00	—	—	44	2D	—	—
8	00	—	—	45	35	5	—
9	08	—	—	46	38	8	—
10	00	—	—	47	32	2	—
11	02	—	—	48	33	3	—
12	01	—	—	49	51	Q	Hex 54 ("T") for ST connector
13	00	—	—	50	5A	Z	Hex 51 ("Q") for ST connector
14	00	—	—	51	20	—	Hex 5A ("Z") for ST connector
15	00	—	—	52	20	—	—
16	C8	—	—	53	20	—	—
17	C8	—	—	54	20	—	—
18	00	—	—	55	20	—	—
19	00	—	—	56	30	—	—
20	42	B	—	57	30	—	—
21	52	R	—	58	30	—	—
22	4F	O	—	59	30	—	—
23	41	A	—	60	05	—	[a]
24	44	D	—	61	1E	—	[a]
25	23	C	—	62	00	—	—
26	4F	O	—	63	5B	—	Hex 8E for ST connector; [b]
27	4D	M	—	64	00	—	—
28	20	—	—	65	12	—	—
29	20	—	—	66	00	—	—
30	20	—	—	67	00	—	—
31	20	—	—	68 to 83	—	—	[c]
32	20	—	—	84 to 91	—	—	[d]
33	20	—	—	92	68	—	Internally calibrated. Average RX Power.
34	20	—	—	93	D0	—	Alarms, Warnings implemented.

Table 1: EEPROM Serial ID Memory Contents – Address A0h (Continued)

Byte Number Decimal	Hex	ASCII	Description	Byte # Decimal	Hex	ASCII	Description
35	20	—	—	94	06	—	Includes functionality described in Rev 12.2 of SFF-8472
36	00	—	—	95	xx	—	[b]
—	—	—	—	96 to 127	00	—	[e]

a. LED wavelength is represented in 16 unsigned bits. The hexadecimal representation of 1310 (nm) is 0x051E.

b. Address 63 is the checksum for bytes 0 to 62 and address 95 is the checksum for bytes 64 to 94. They are calculated (per SFF-8472) and stored prior to product shipment.

c. Addresses 68 to 83 specify a unique module serial number.

d. Addresses 84 to 91 specify the date code.

e. Addresses 96 to 127 are vendor specific.

Table 2: EEPROM Serial ID Memory Contents — Enhanced Features (Address A2h)

Address	Hex	Dec	Notes	Address	Hex	Dec	Notes	Address	Notes
0	55	85	Temp H Alarm MSB[a]	26	0	0	Tx Power L Alarm MSB[g]	104	Real Time Rx Power MSB[b]
1	0	0	Temp H Alarm LSB[a]	27	32	50	Tx Power L Alarm LSB[g]	105	Real Time Rx Power LSB[b]
2	D8	216	Temp L Alarm MSB[a]	28	2	2	Tx Power H Warning MSB[g]	106	Reserved
3	0	0	Temp L Alarm LSB[a]	29	76	118	Tx Power H Warning LSB[g]	107	Reserved
4	50	80	Temp H Warning MSB[a]	30	0	0	Tx Power L Warning MSB[g]	108	Reserved
5	0	0	Temp H Warning LSB[a]	31	3F	63	Tx Power L Warning LSB[g]	109	Reserved
6	DD	221	Temp L Warning MSB[a]	32	3	3	Rx Power H Alarm MSB[b]	110	Status/Control
7	0	0	Temp L Warning LSB[a]	33	E8	232	Rx Power H Alarm LSB[b]	111	Reserved
8	8C	140	Vcc H Alarm MSB[c]	34	0	0	Rx Power L Alarm MSB[b]	112	Flag Bits
9	9F	159	Vcc H Alarm LSB[c]	35	5	5	Rx Power L Alarm LSB[b]	113	Flag Bits
10	75	117	Vcc L Alarm MSB[c]	36	2	2	Rx Power H Warning MSB[b]	114	Reserved
11	30	48	Vcc L Alarm LSB[c]	37	76	118	Rx Power H Warning LSB[b]	115	Reserved
12	88	136	Vcc H Warning MSB[c]	38	0	0	Rx Power L Warning MSB[b]	116	Flag Bits
13	B8	184	Vcc H Warning LSB[c]	39	6	6	Rx Power L Warning LSB[b]	117	Flag Bits
14	79	121	Vcc L Warning MSB[c]	40–55	—	—	Reserved	118–127	Reserved
15	17	23	Vcc L Warning LSB[c]	56–94	—	—	External Calibration Constants[d]	128–247	Customer Writable
16	EA	234	Tx Bias H Alarm MSB[e]	95	—	—	Checksum for Bytes 0–94[f]	248–255	Vendor Specific
17	60	96	Tx Bias H Alarm LSB[e]	96	—	—	Real Time Temperature MSB[a]	—	—
18	13	19	Tx Bias L Alarm MSB[e]	97	—	—	Real Time Temperature LSB[a]	—	—
19	88	136	Tx Bias L Alarm LSB[e]	98	—	—	Real Time Vcc MSB[c]	—	—

Table 2: EEPROM Serial ID Memory Contents — Enhanced Features (Address A2h) (Continued)

Address	Hex	Dec	Notes	Address	Hex	Dec	Notes	Address	Notes
20	D6	214	Tx Bias H Warning MSB[e]	99	—	—	Real Time Vcc LSB[c]	—	—
21	D8	216	Tx Bias H Warning LSB[e]	100	—	—	Real Time Tx Bias MSB[e]	—	—
22	1D	29	Tx Bias L Warning MSB[e]	101	—	—	Real Time Tx Bias LSB[e]	—	—
23	4C	76	Tx Bias L Warning LSB[e]	102	—	—	Real Time Tx Power MSB[g]	—	—
24	3	3	Tx Power H Alarm MSB[g]	103	—	—	Real Time Tx Power LSB[g]	—	—
25	1A	26	Tx Power H Alarm LSB[g]	—	—	—	—	—	—

a. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256°C.

b. Received average optical power (Rx Pwr) is decoded as a 16-bit unsigned integer in increments of 0.1 µW.

c. Supply Voltage (Vcc) is decoded as a 16-bit unsigned integer in increments of 100 µV.

d. Bytes 56–94 are not intended for use with AFBR-58x3xxZ, but have been set to default values per SFF-8472.

e. Tx bias current (Tx Bias) is decoded as a 16-bit unsigned integer in increments of 2 µA.

f. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

g. Transmitted average optical power (Tx Pwr) is decoded as a 16-bit unsigned integer in increments of 0.1 µW.

Table 3: EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit Number	Status/Control Name	Description	Notes
7	Tx_DISABLE State	Digital state of TX_DISABLE input pin (logic 1 = TX_DISABLE asserted).	a
6	Soft TX_DISABLE	Read/write bit for changing digital state of TX_DISABLE function.	a, b
5	Reserved	—	c
4	Not supported	—	d
3	Not supported	—	e
2	Not supported	—	f
1	Rx_SD State	Digital state of the Rx_SD output pin (logic 1 = RX_SD asserted).	a
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = ready).	g

a. The response time for soft commands of the AFBR-58x3xxZ is 100 ms as specified by SFF-8472.

b. Bit 6 is logic ORed with the TX_DISABLE input pin. Either asserted will disable the transmitter.

c. Reserved bits return 0 when read. A write to a reserved bit will be acknowledged but not stored.

d. A read from bit 4 returns 1. A write will be acknowledged but not stored.

e. A read/write from bit 3 will be acknowledged and stored but will be ignored by the transceiver.

f. A read from bit 2 returns 0. A write will be acknowledged but not stored.

g. Meets the MSA-SFF-8472 data ready timing of 1000 ms.

Table 4: EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold.
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold.
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold.
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold.
	3	Tx Bias High Alarm	Set when transceiver LED bias exceeds high alarm threshold.
	2	Tx Bias Low Alarm	Set when transceiver LED bias exceeds low alarm threshold.
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold.
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold.
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold.
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold.
	0 to 5	Reserved	—
116	7	Temp High Warning	Set when transceiver case temperature exceeds high warning threshold.
	6	Temp Low Warning	Set when transceiver case temperature exceeds low warning threshold.
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold.
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold.
	3	Tx Bias High Warning	Set when transceiver LED bias exceeds high warning threshold.
	2	Tx Bias Low Warning	Set when transceiver LED bias exceeds low warning threshold.
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold.
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold.
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold.
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold.
	0 to 5	Reserved	—

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