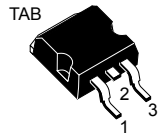
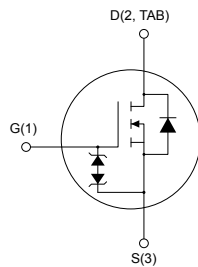


## Automotive-grade N-channel 400 V, 0.063 $\Omega$ typ., 38 A, MDmesh™ DM2 Power MOSFET in a D<sup>2</sup>PAK package


 D<sup>2</sup>PAK


AM01475V1


**Product status**


STB45N40DM2AG

**Product summary**

|                   |                    |
|-------------------|--------------------|
| <b>Order code</b> | STB45N40DM2AG      |
| <b>Marking</b>    | 45N40DM2           |
| <b>Package</b>    | D <sup>2</sup> PAK |
| <b>Packing</b>    | Tape and reel      |

### Features

| Order code    | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> | P <sub>TOT</sub> |
|---------------|-----------------|--------------------------|----------------|------------------|
| STB45N40DM2AG | 400 V           | 0.072 $\Omega$           | 38 A           | 250 W            |

- AEC-Q101 qualified 
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q<sub>rr</sub>) and time (t<sub>rr</sub>) combined with low R<sub>DS(on)</sub>, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter  | Value      | Unit |
|----------------|--|------------|------|
| $V_{GS}$       | Gate-source voltage                                      | ±25        | V    |
| $I_D$          | Drain current (continuous) at $T_{case} = 25\text{ °C}$  | 38         | A    |
|                | Drain current (continuous) at $T_{case} = 100\text{ °C}$ | 24         |      |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                   | 110        | A    |
| $P_{TOT}$      | Total power dissipation at $T_{case} = 25\text{ °C}$     | 250        | W    |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                        | 50         | V/ns |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                | 50         |      |
| $T_{stg}$      | Storage temperature range                                | -55 to 150 | °C   |
| $T_j$          | Operating junction temperature range                     |            |      |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 38\text{ A}$ ,  $di/dt = 800\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$
3.  $V_{DS} \leq 320\text{ V}$

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit |
|---------------------|----------------------------------|-------|------|
| $R_{thj-case}$      | Thermal resistance junction-case | 0.5   | °C/W |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 30    |      |

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

| Symbol         | Parameter                                       | Value | Unit |
|----------------|---|-------|------|
| $I_{AR}^{(1)}$ | Avalanche current, repetitive or not repetitive | 7     | A    |
| $E_{AS}^{(2)}$ | Single pulse avalanche energy                   | 1100  | mJ   |

1. Pulse width is limited by  $T_{jmax}$ .
2. starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. Static**

| Symbol                      | Parameter                         | Test conditions  | Min. | Typ.  | Max.    | Unit          |
|-----------------------------|-----------------------------------|--|------|-------|---------|---------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage    | $V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$  | 400  |       |         | V             |
| $I_{\text{DSS}}$            | Zero gate voltage drain current   | $V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 400\text{ V}$  |      |       | 10      | $\mu\text{A}$ |
|                             |                                   | $V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 400\text{ V}$ ,<br>$T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |       | 100     |               |
| $I_{\text{GSS}}$            | Gate-body leakage current         | $V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$   |      |       | $\pm 5$ | $\mu\text{A}$ |
| $V_{\text{GS}(\text{th})}$  | Gate threshold voltage            | $V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$  | 3    | 4     | 5       | V             |
| $R_{\text{DS}(\text{on})}$  | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 19\text{ A}$   |      | 0.063 | 0.072   | $\Omega$      |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|----------------------------|-------------------------------|--|------|------|------|---------------|
| $C_{\text{iSS}}$           | Input capacitance             | $V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{\text{GS}} = 0\text{ V}$  | -    | 2600 | -    | $\mu\text{F}$ |
| $C_{\text{OSS}}$           | Output capacitance            |  | -    | 180  | -    |               |
| $C_{\text{rSS}}$           | Reverse transfer capacitance  |  | -    | 3.5  | -    |               |
| $C_{\text{OSS eq.}}^{(1)}$ | Equivalent output capacitance | $V_{\text{DS}} = 0\text{ to }320\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$  | -    | 300  | -    | $\mu\text{F}$ |
| $R_{\text{G}}$             | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$   | -    | 4    | -    | $\Omega$      |
| $Q_{\text{g}}$             | Total gate charge             | $V_{\text{DD}} = 320\text{ V}$ , $I_{\text{D}} = 38\text{ A}$ ,<br>$V_{\text{GS}} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 56   | -    | nC            |
| $Q_{\text{GS}}$            | Gate-source charge            |  | -    | 13   | -    |               |
| $Q_{\text{GD}}$            | Gate-drain charge             |  | -    | 28   | -    |               |

1.  $C_{\text{OSS eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 6. Switching times**

| Symbol                     | Parameter           | Test conditions  | Min. | Typ. | Max. | Unit |
|----------------------------|---------------------|--|------|------|------|------|
| $t_{\text{d}(\text{on})}$  | Turn-on delay time  | $V_{\text{DD}} = 200\text{ V}$ , $I_{\text{D}} = 19\text{ A}$ ,<br>$R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$<br>(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 20   | -    | ns   |
| $t_{\text{r}}$             | Rise time           |  | -    | 6.7  | -    |      |
| $t_{\text{d}(\text{off})}$ | Turn-off delay time |  | -    | 68   | -    |      |
| $t_{\text{f}}$             | Fall time           |  | -    | 9.8  | -    |      |

**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 38   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 110  | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 38\text{ A}$   | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 38\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                     | -    | 95   |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 0.4  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 8.5  |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 38\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 185  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 1.62 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 17.5 |      | A             |

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

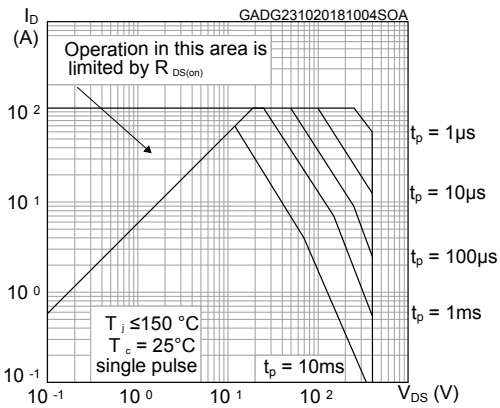
**Table 8. Gate-source Zener diode**

| Symbol        | Parameter                     | Test conditions  | Min.     | Typ. | Max. | Unit |
|---------------|-------------------------------|--|----------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 250\text{ }\mu\text{A}$ , $I_D = 0\text{ A}$ | $\pm 30$ | -    | -    | V    |

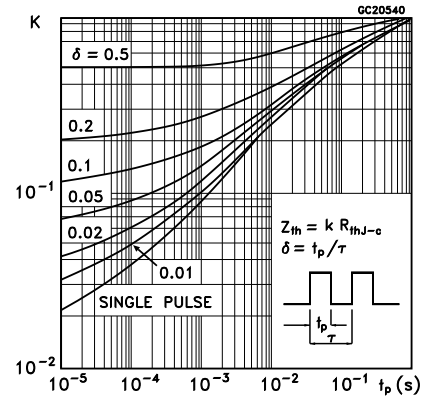
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

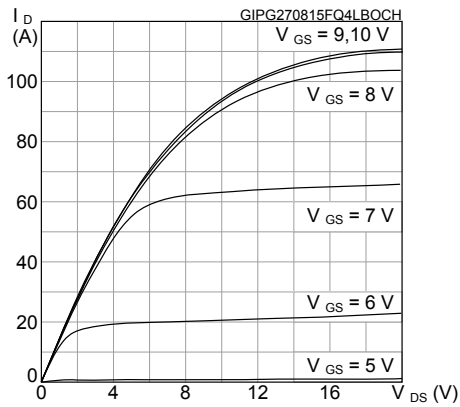
**Figure 1. Safe operating area**



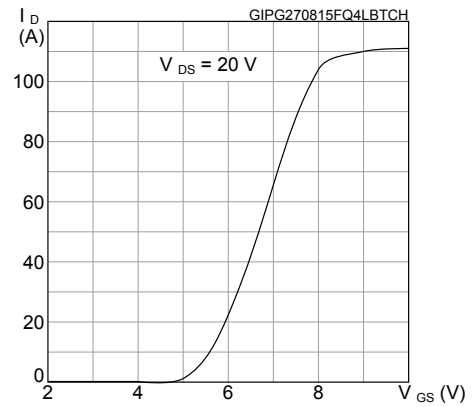
**Figure 2. Thermal impedance**



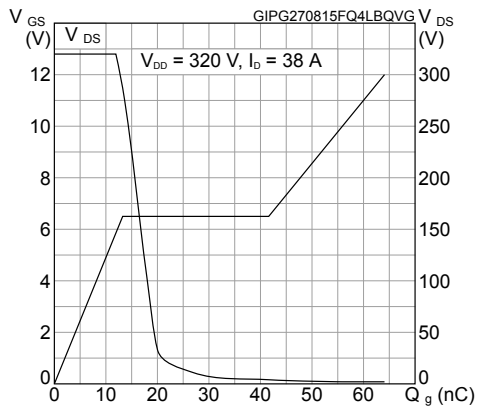
**Figure 3. Output characteristics**



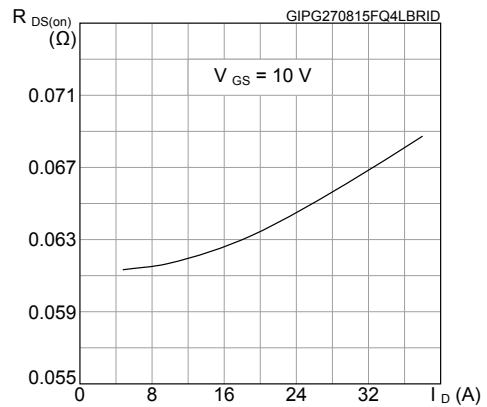
**Figure 4. Transfer characteristics**



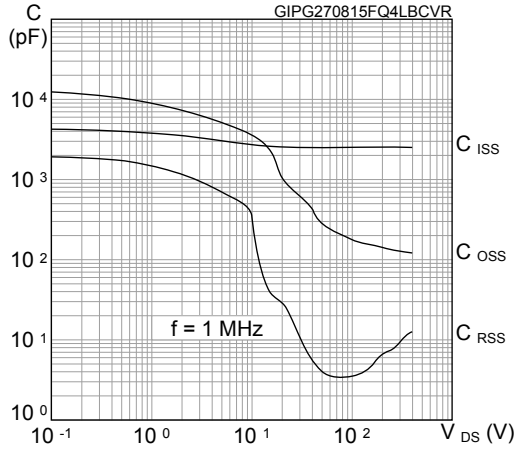
**Figure 5. Gate charge vs gate-source voltage**



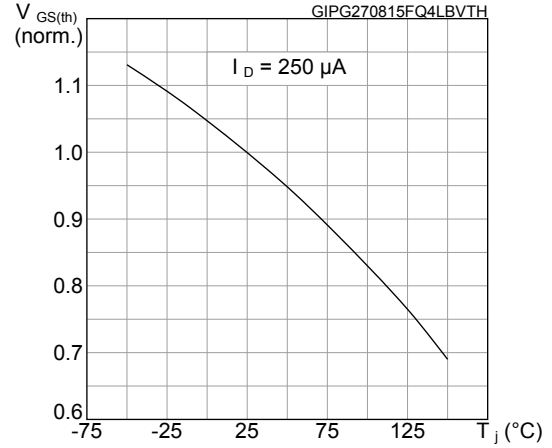
**Figure 6. Static drain-source on-resistance**



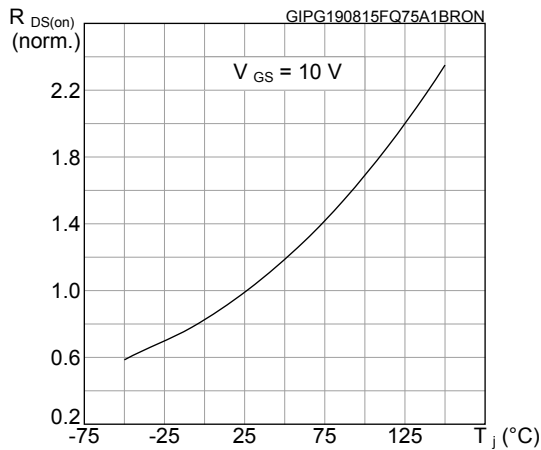
**Figure 7. Capacitance variations**



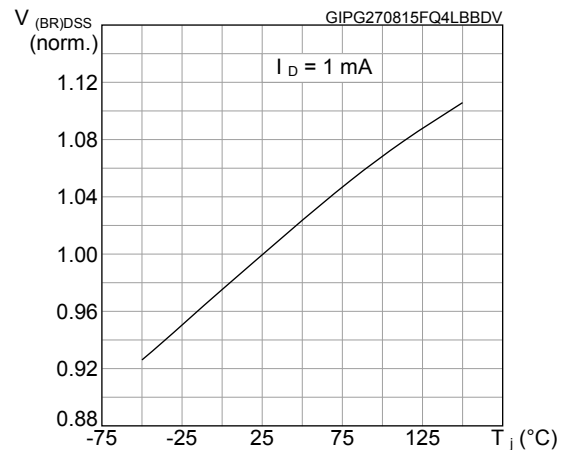
**Figure 8. Normalized gate threshold voltage vs temperature**



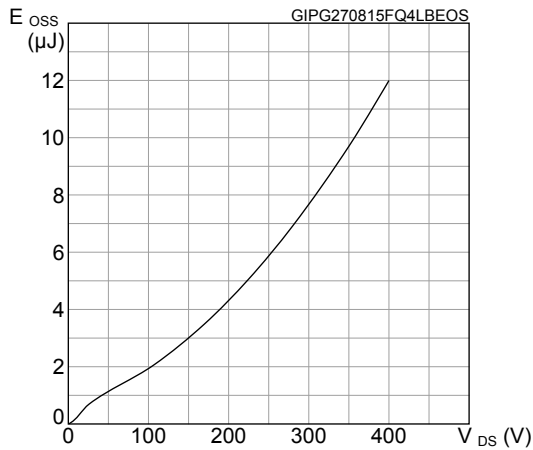
**Figure 9. Normalized on-resistance vs temperature**



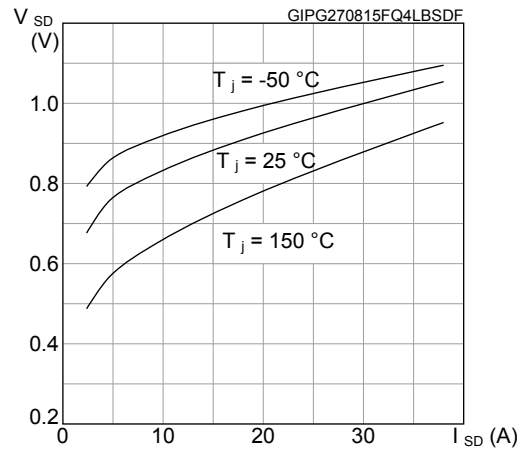
**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**



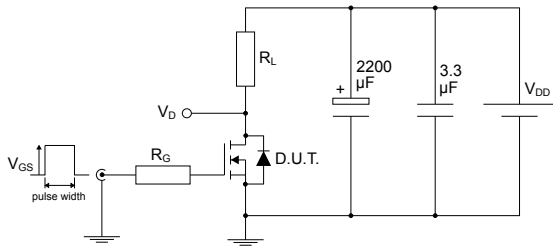
**Figure 11. Output capacitance stored energy**



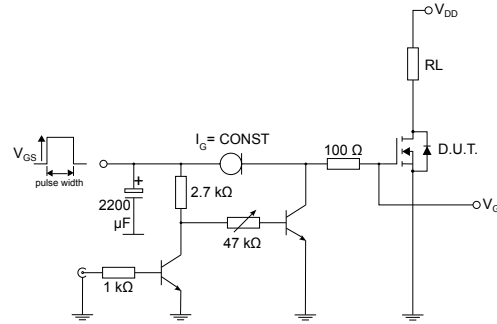
**Figure 12. Source-drain diode forward characteristics**



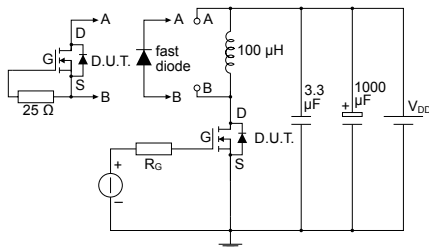
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


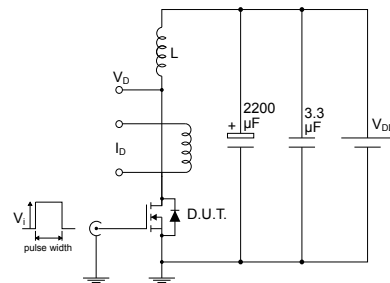
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


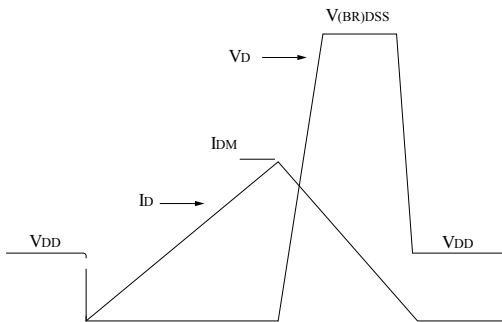
AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


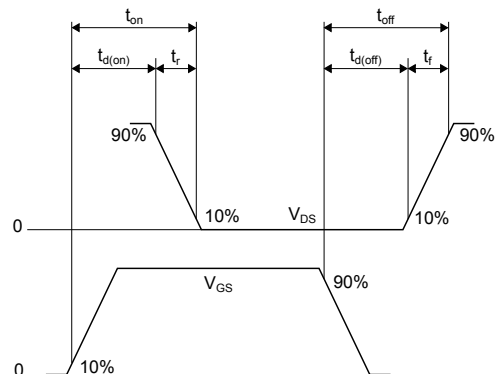
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

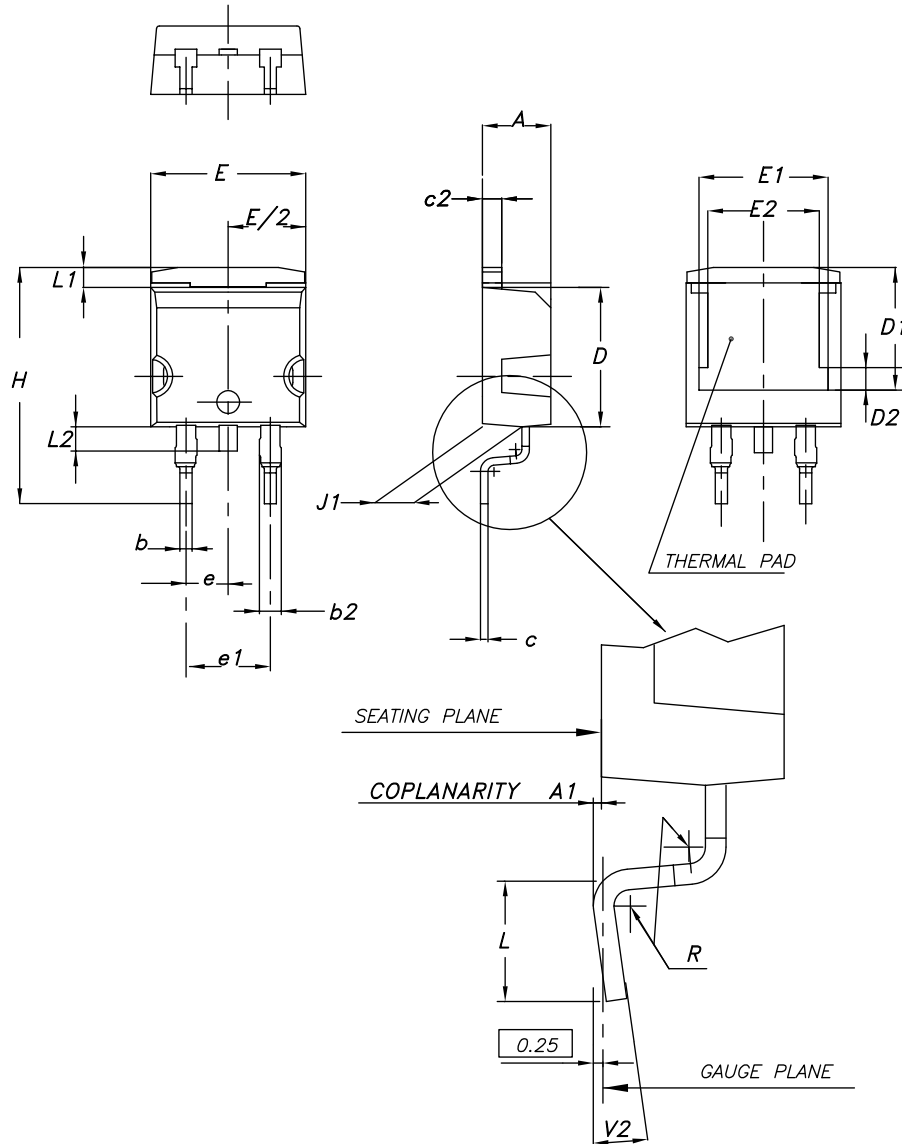
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK<sup>®</sup>** packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



### 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

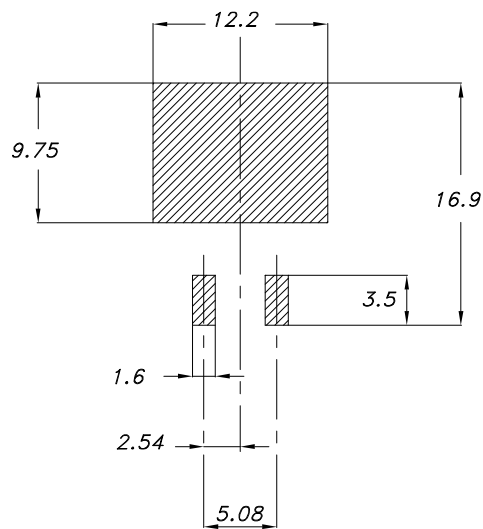
Figure 19. D<sup>2</sup>PAK (TO-263) type A2 package outline



0079457\_A2\_25

**Table 9. D<sup>2</sup>PAK (TO-263) type A2 package mechanical data**

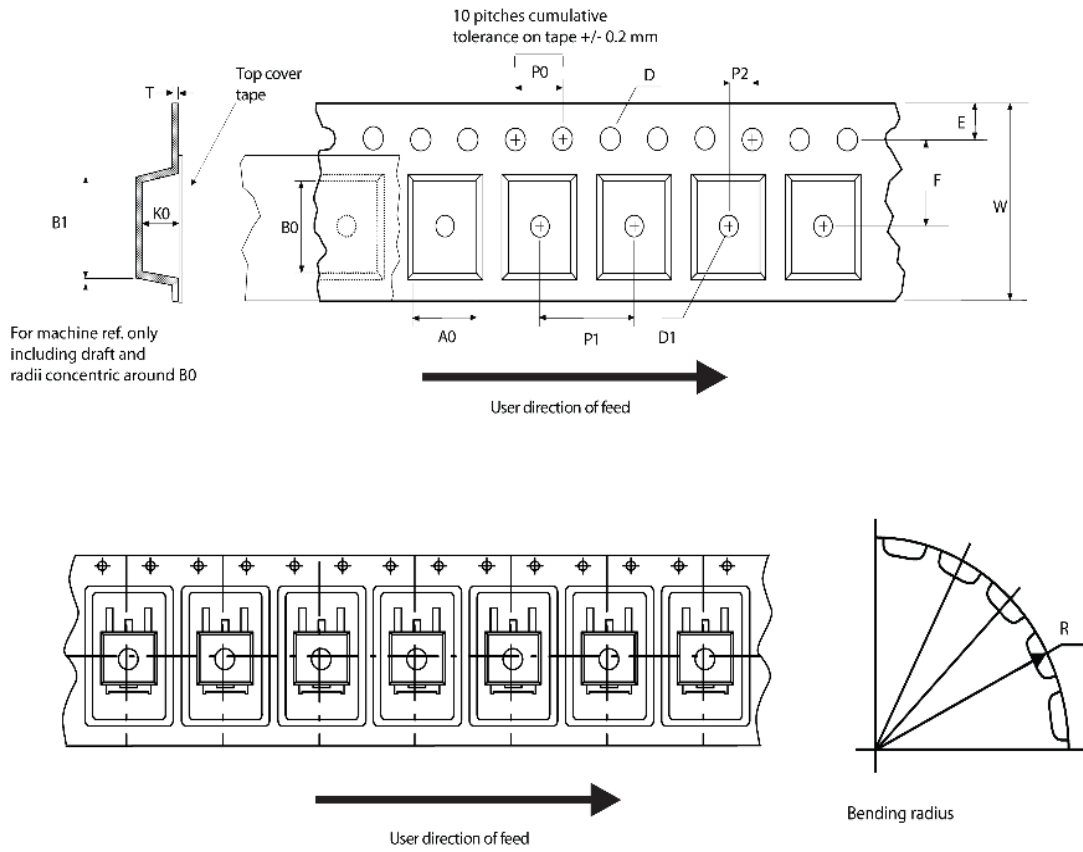
| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.40  |      | 4.60  |
| A1   | 0.03  |      | 0.23  |
| b    | 0.70  |      | 0.93  |
| b2   | 1.14  |      | 1.70  |
| c    | 0.45  |      | 0.60  |
| c2   | 1.23  |      | 1.36  |
| D    | 8.95  |      | 9.35  |
| D1   | 7.50  | 7.75 | 8.00  |
| D2   | 1.10  | 1.30 | 1.50  |
| E    | 10.00 |      | 10.40 |
| E1   | 8.70  | 8.90 | 9.10  |
| E2   | 7.30  | 7.50 | 7.70  |
| e    |       | 2.54 |       |
| e1   | 4.88  |      | 5.28  |
| H    | 15.00 |      | 15.85 |
| J1   | 2.49  |      | 2.69  |
| L    | 2.29  |      | 2.79  |
| L1   | 1.27  |      | 1.40  |
| L2   | 1.30  |      | 1.75  |
| R    |       | 0.40 |       |
| V2   | 0°    |      | 8°    |

**Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**


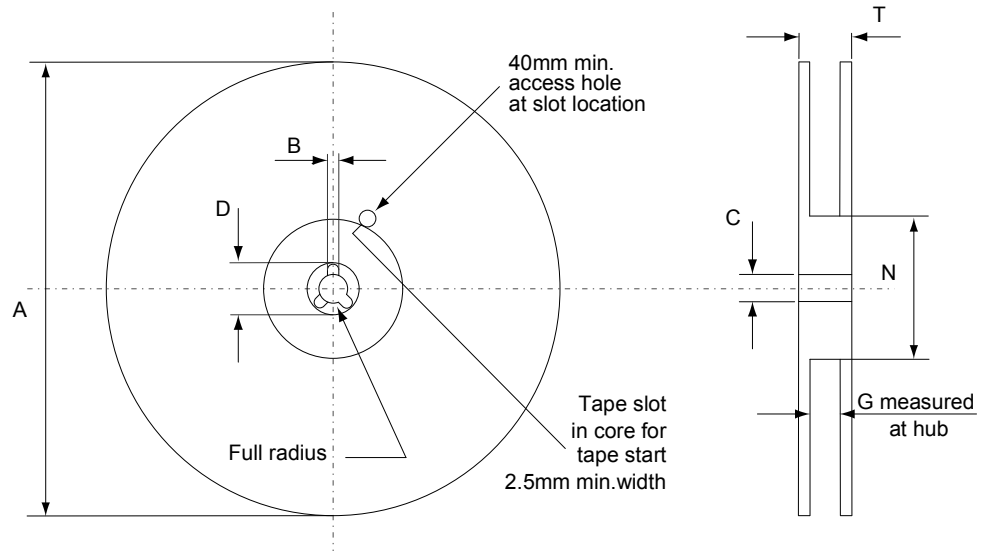
Footprint

## 4.2 D<sup>2</sup>PAK packing information

Figure 21. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 10. D<sup>2</sup>PAK tape and reel mechanical data**

| Tape |      |      | Reel                           |      |      |      |
|------|------|------|--------------------------------|------|------|------|
| Dim. | mm   |      | Dim.                           | mm   |      |      |
|      | Min. | Max. |                                | Min. | Max. |      |
| A0   | 10.5 | 10.7 | A                              |      | 330  |      |
| B0   | 15.7 | 15.9 | B                              | 1.5  |      |      |
| D    | 1.5  | 1.6  | C                              | 12.8 | 13.2 |      |
| D1   | 1.59 | 1.61 | D                              | 20.2 |      |      |
| E    | 1.65 | 1.85 | G                              | 24.4 | 26.4 |      |
| F    | 11.4 | 11.6 | N                              | 100  |      |      |
| K0   | 4.8  | 5.0  | T                              |      | 30.4 |      |
| P0   | 3.9  | 4.1  | Base quantity<br>Bulk quantity |      |      |      |
| P1   | 11.9 | 12.1 |                                |      |      | 1000 |
| P2   | 1.9  | 2.1  |                                |      |      | 1000 |
| R    | 50   |      |                                |      |      |      |
| T    | 0.25 | 0.35 |                                |      |      |      |
| W    | 23.7 | 24.3 |                                |      |      |      |

## Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 27-Aug-2015 | 1        | Initial version  |
| 04-Aug-2016 | 2        | Updated <i>Figure 2: "Safe operating area"</i> .<br>Minor text changes.  |
| 14-Feb-2018 | 3        | Removed maturity status indication from cover page.<br>Updated <i>Section 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information</i> .<br>Minor text changes  |
| 23-Oct-2018 | 4        | Updated <a href="#">Table 1. Absolute maximum ratings</a> and <a href="#">Table 7. Source-drain diode</a> .<br>Updated <a href="#">Figure 1. Safe operating area</a> and <a href="#">Figure 14. Test circuit for gate charge behavior</a> .<br>Minor text changes. |

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