

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 66 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2300 to 2400 MHz.

2300 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQA} = 750$ mA, $V_{GSB} = 0.7$ Vdc, $P_{out} = 66$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

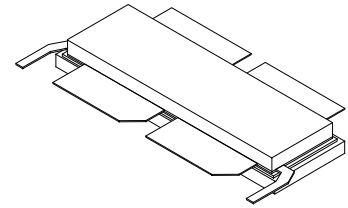
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	14.9	46.7	7.8	-34.0
2350 MHz	15.1	46.5	7.8	-35.6
2400 MHz	15.1	46.4	7.5	-34.6

Features

- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T23H300-24SR6

2300-2400 MHz, 66 W AVG., 28 V
 AIRFAST RF POWER LDMOS
 TRANSISTOR



NI-1230S-4L2L

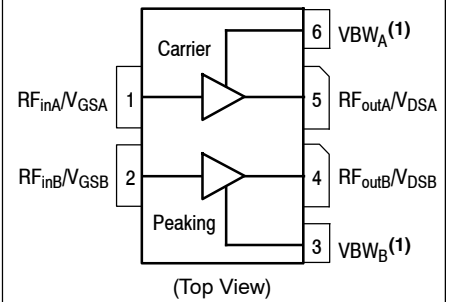


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	248 1.2	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 66 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 750$ mA, $V_{GSB} = 0.7$ Vdc, 2350 MHz	$R_{\theta JC}$	0.25	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics - Side A (Carrier)

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 160$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_{DA} = 750$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.6$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

On Characteristics - Side B (Peaking)

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 240$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 2.4$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to [AN1955](#), *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 750\text{ mA}$, $V_{GSB} = 0.7\text{ Vdc}$, $P_{out} = 66\text{ W Avg.}$, $f = 2300\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	14.0	14.9	17.0	dB
Drain Efficiency	η_D	43.0	46.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.0	-31.0	dBc

Load Mismatch ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $I_{DQA} = 750\text{ mA}$, $V_{GSB} = 0.7\text{ Vdc}$, $f = 2350\text{ MHz}$, 100 μsec (on), 10% Duty Cycle

VSWR 5:1 at 32 Vdc, 417 W Pulsed CW Output Power (3 dB Input Overdrive from 324 W Pulsed CW Rated Power)	No Device Degradation
---	-----------------------

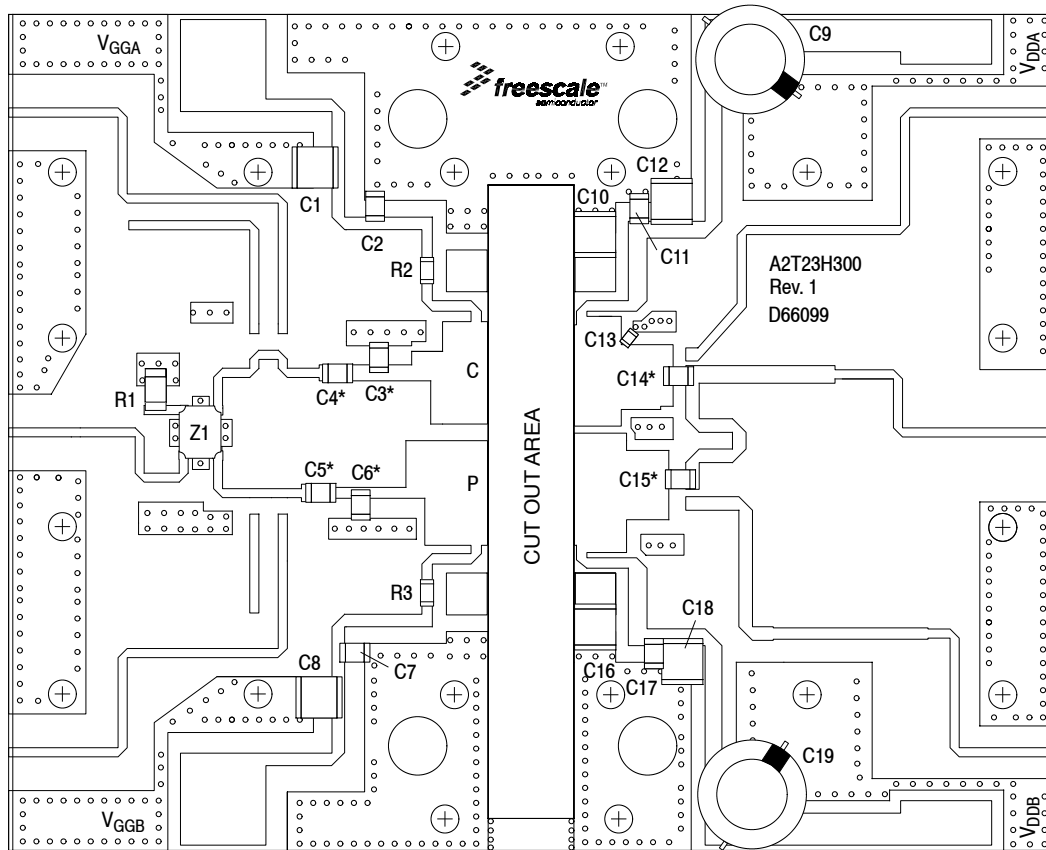
Typical Performance ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 750\text{ mA}$, $V_{GSB} = 0.7\text{ Vdc}$, 2300–2400 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	275	—	W
P_{out} @ 3 dB Compression Point ⁽³⁾	P3dB	—	410	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2400 MHz frequency range)	Φ	—	-12.3	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	90	—	MHz
Gain Flatness in 100 MHz Bandwidth @ $P_{out} = 66\text{ W Avg.}$	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.0075	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.0075	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T23H300-24SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C3, C4, C5, C6, C14 and C15 are mounted vertically.

Figure 2. A2T23H300-24SR6 Test Circuit Component Layout

Table 6. A2T23H300-24SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C8, C10, C12, C16, C18	10 μ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C4, C5, C7, C11, C17	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C3	0.7 pF Chip Capacitor	ATC100B0R7CT500XT	ATC
C6	0.8 pF Chip Capacitor	ATC100B0R8CT500XT	ATC
C9, C19	470 μ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26	Multicomp
C13	0.6 pF Chip Capacitor	ATC00F0R6BT250XT	ATC
C14	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C15	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
R1	50 Ω , 10 W Termination	CW12010T0050GBK	ATC
R2, R3	3.0 Ω , 1/4 W Chip Resistors	CRCW12063R0FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D66099	MTL

TYPICAL CHARACTERISTICS — 2300–2400 MHz

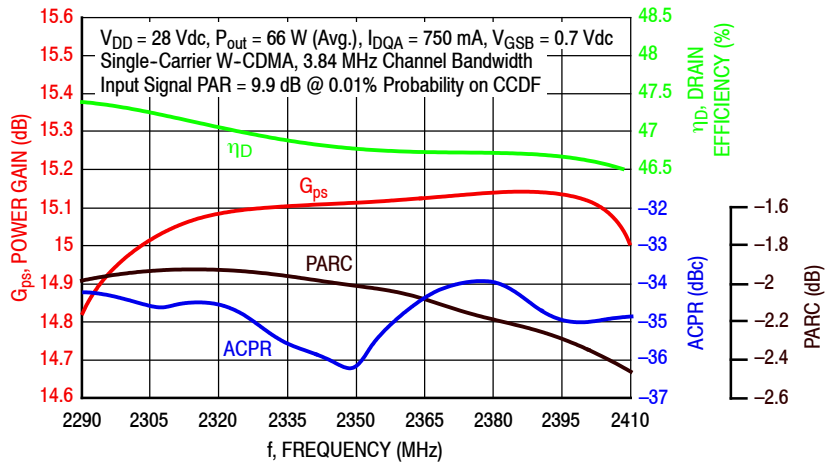


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 66$ Watts Avg.

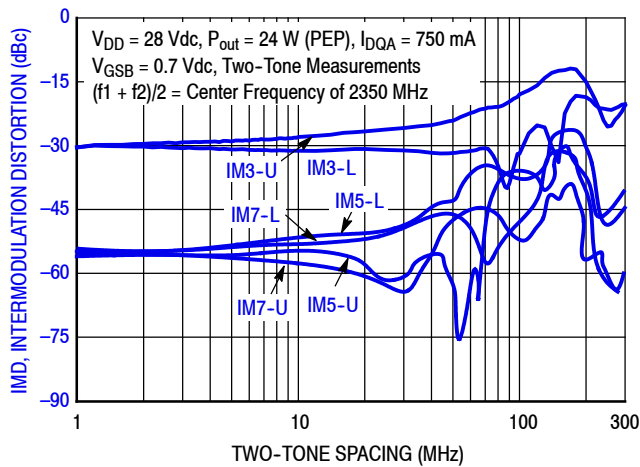


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

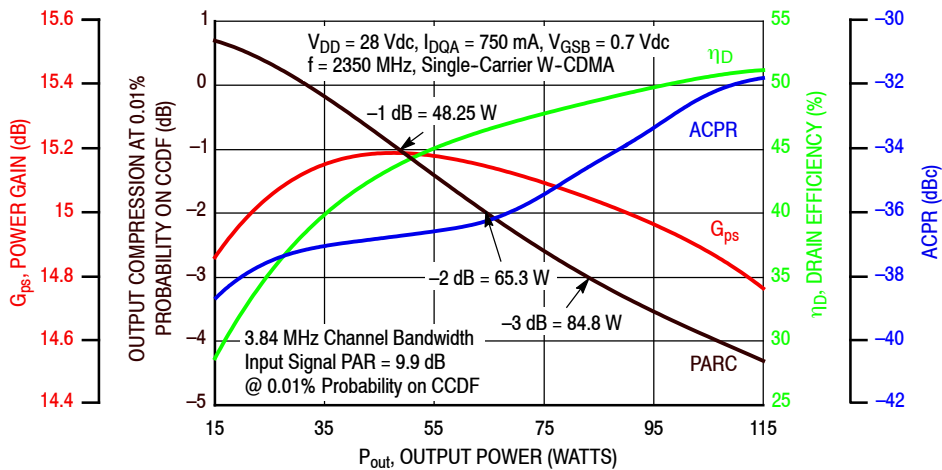


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2300–2400 MHz

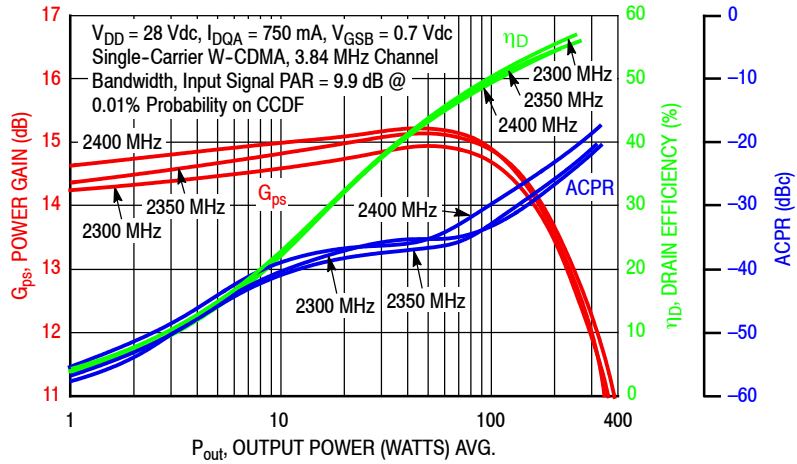


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

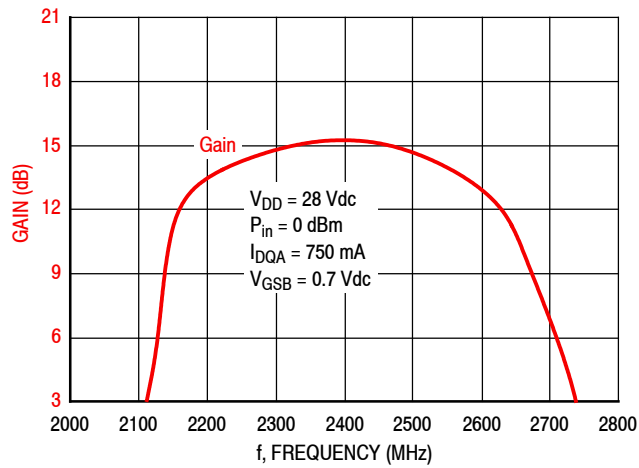


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 792 \text{ mA}$, Pulsed CW, 10 μsec (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.89 – j11.2	5.24 + j10.5	1.78 – j4.54	17.8	52.5	179	56.8	–14
2350	8.32 – j12.4	7.67 + j11.4	1.75 – j4.50	17.9	52.5	179	56.8	–14
2400	12.6 – j12.7	11.7 + j11.9	1.68 – j4.54	18.0	52.4	175	55.9	–14

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.89 – j11.2	5.24 + j11.4	1.72 – j4.83	15.6	53.3	213	57.0	–19
2350	8.32 – j12.4	8.12 + j12.7	1.68 – j4.82	15.6	53.2	211	56.3	–19
2400	12.6 – j12.7	13.2 + j13.5	1.65 – j4.81	15.8	53.2	208	55.8	–20

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 792 \text{ mA}$, Pulsed CW, 10 μsec (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.89 – j11.2	4.97 + j11.1	4.10 – j2.52	20.6	50.1	103	67.1	–22
2350	8.32 – j12.4	7.36 + j12.4	3.57 – j2.19	20.7	50.0	99	66.9	–24
2400	12.6 – j12.7	11.6 + j13.0	3.31 – j2.28	20.9	49.9	97	66.2	–22

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.89 – j11.2	4.88 + j11.6	3.40 – j3.40	17.9	51.7	149	66.7	–28
2350	8.32 – j12.4	7.51 + j13.2	3.07 – j3.11	18.1	51.6	145	66.3	–29
2400	12.6 – j12.7	12.6 + j14.5	2.64 – j3.24	18.1	51.8	152	65.7	–28

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

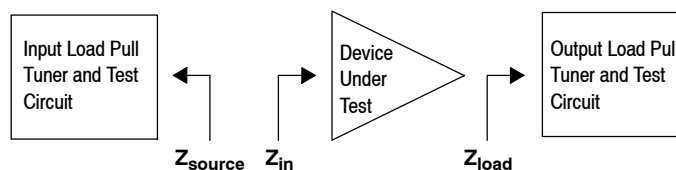
 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28$ Vdc, $V_{GSB} = 1.7$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2300	5.90 – j10.4	5.66 + j9.30	1.81 – j5.44	17.1	54.7	293	53.9	–19
2350	10.2 – j11.1	8.59 + j9.73	1.90 – j5.61	17.3	54.6	287	53.0	–20
2400	14.7 – j8.30	12.6 + j7.98	1.98 – j5.78	17.4	54.4	277	51.8	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2300	5.90 – j10.4	5.71 + j9.97	1.70 – j5.69	14.8	55.3	342	54.6	–24
2350	10.2 – j11.1	9.18 + j10.6	1.84 – j5.84	15.0	55.3	335	53.7	–25
2400	14.7 – j8.30	14.2 + j8.34	1.98 – j6.02	15.3	55.1	326	52.8	–25

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28$ Vdc, $V_{GSB} = 1.7$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2300	5.90 – j10.4	5.97 + j9.73	4.06 – j5.24	19.2	53.2	209	63.8	–25
2350	10.2 – j11.1	9.06 + j10.3	4.47 – j4.20	19.7	52.6	181	62.8	–27
2400	14.7 – j8.30	13.0 + j8.08	3.78 – j4.57	19.4	53.1	202	61.4	–24

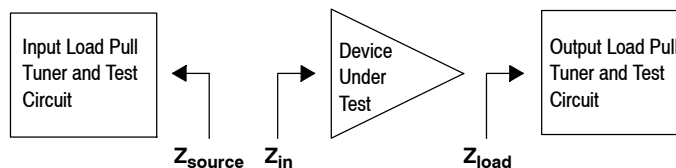
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2300	5.90 – j10.4	5.91 + j10.3	3.98 – j5.24	17.1	53.9	246	64.5	–32
2350	10.2 – j11.1	9.64 + j10.8	4.23 – j4.68	17.4	53.7	233	64.0	–34
2400	14.7 – j8.30	14.7 + j8.19	3.93 – j4.31	17.6	53.7	233	63.4	–34

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2350 MHz

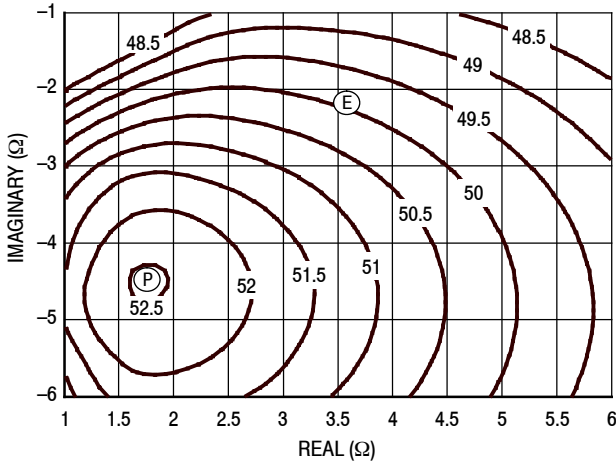


Figure 8. P1dB Load Pull Output Power Contours (dB)

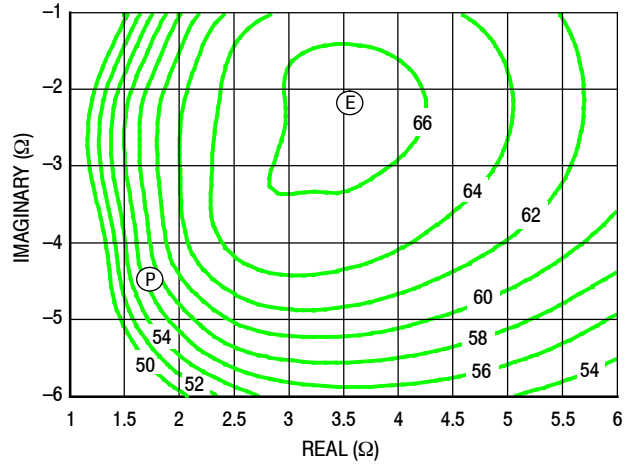


Figure 9. P1dB Load Pull Efficiency Contours (%)

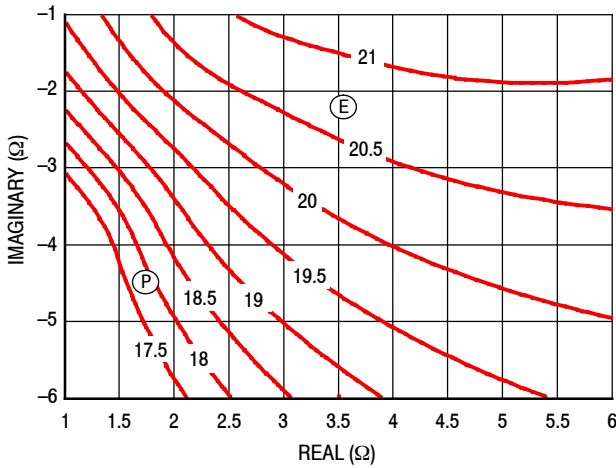


Figure 10. P1dB Load Pull Gain Contours (dB)

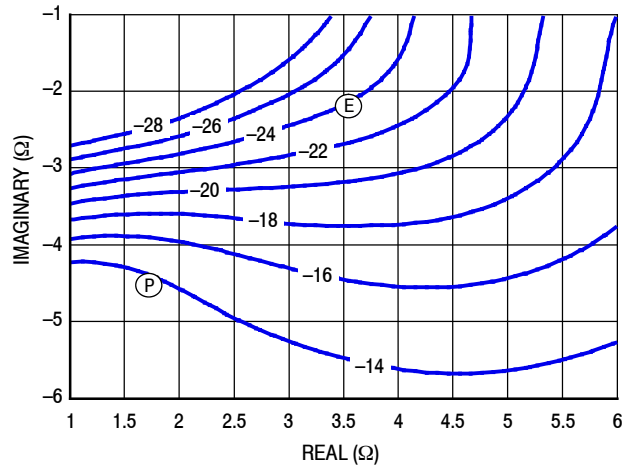


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2350 MHz

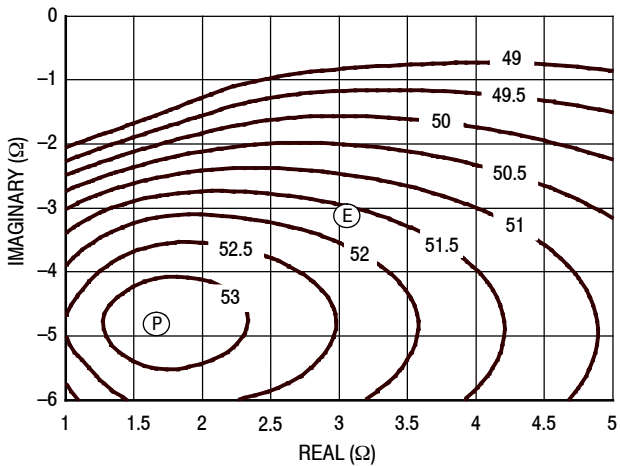


Figure 12. P3dB Load Pull Output Power Contours (dBm)

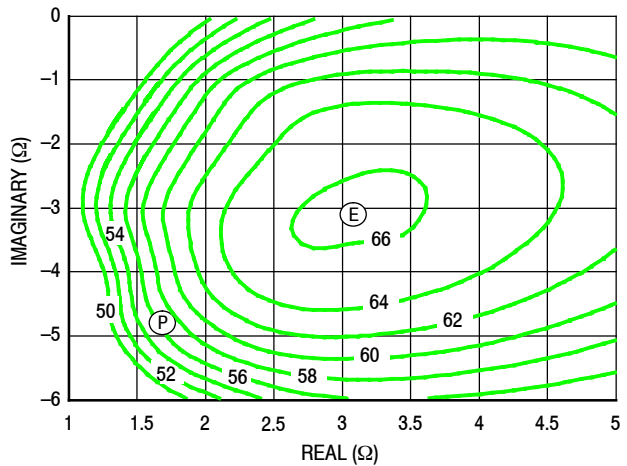


Figure 13. P3dB Load Pull Efficiency Contours (%)

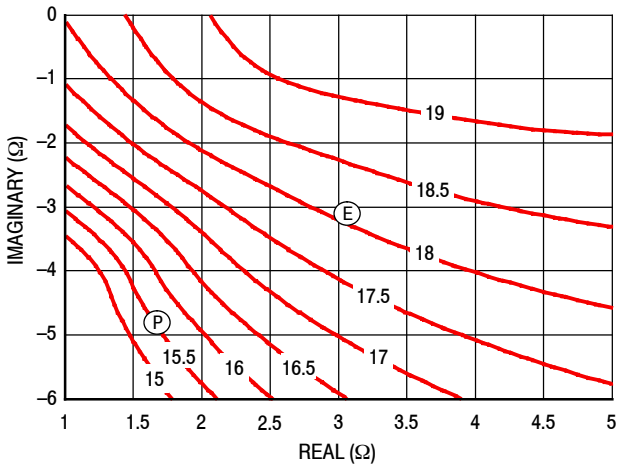


Figure 14. P3dB Load Pull Gain Contours (dB)

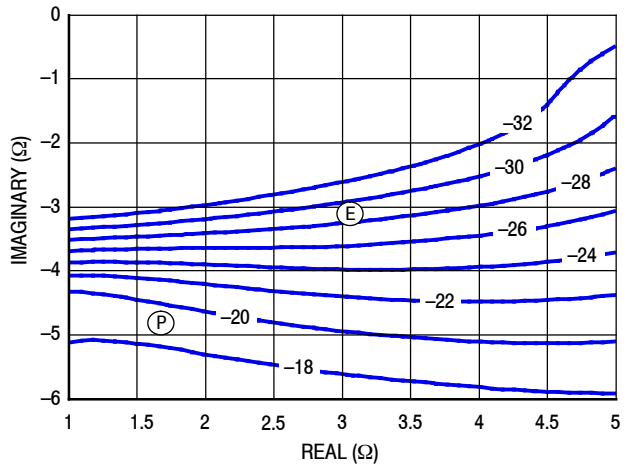


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2350 MHz

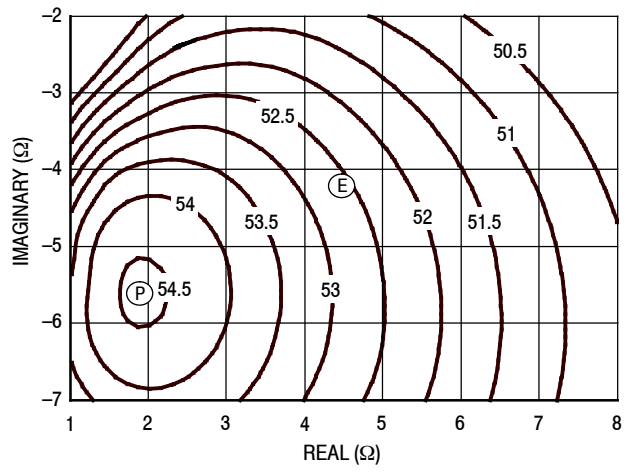


Figure 16. P1dB Load Pull Output Power Contours (dBm)

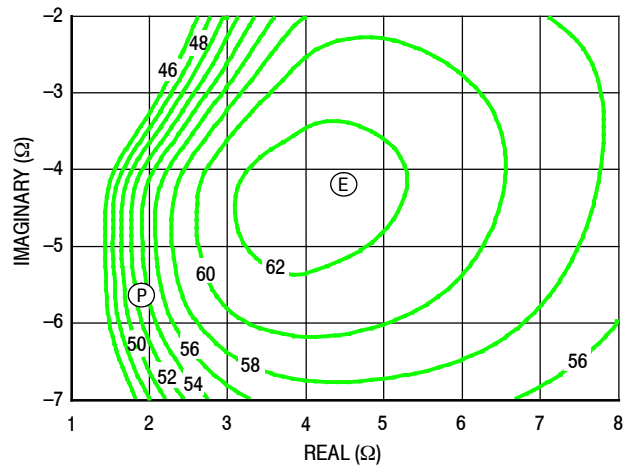


Figure 17. P1dB Load Pull Efficiency Contours (%)

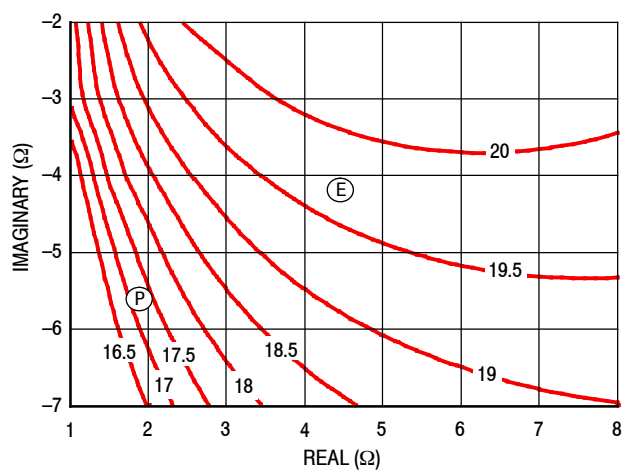


Figure 18. P1dB Load Pull Gain Contours (dB)

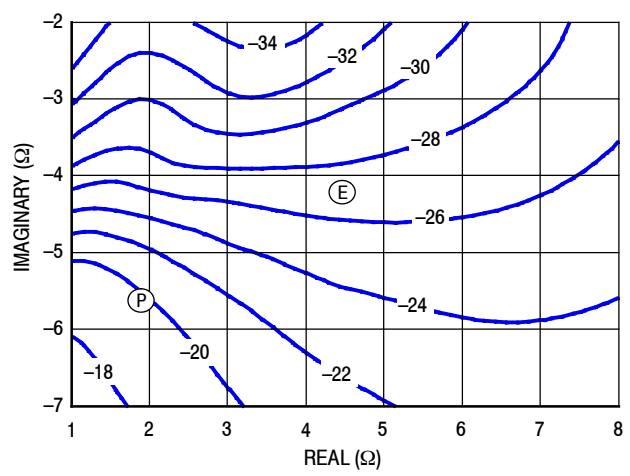


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2350 MHz

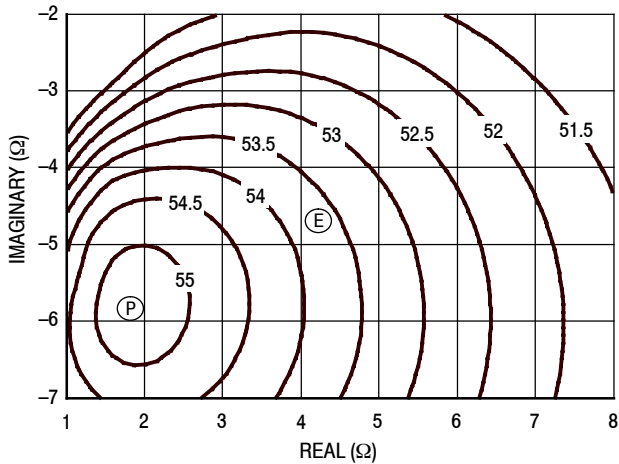


Figure 20. P3dB Load Pull Output Power Contours (dBm)

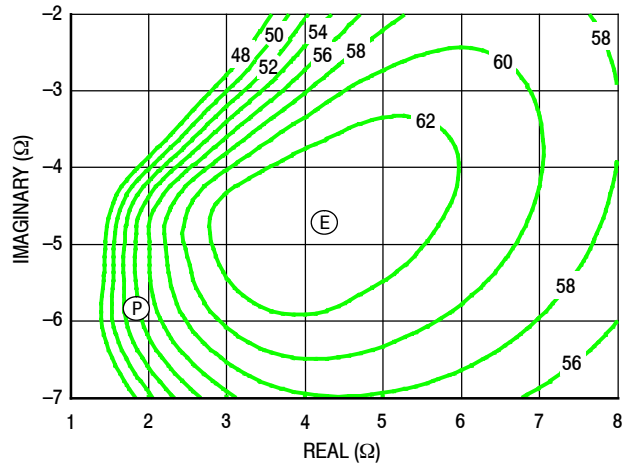


Figure 21. P3dB Load Pull Efficiency Contours (%)

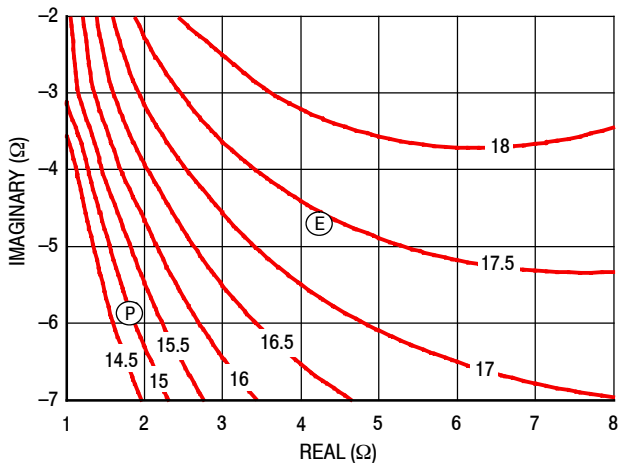


Figure 22. P3dB Load Pull Gain Contours (dB)

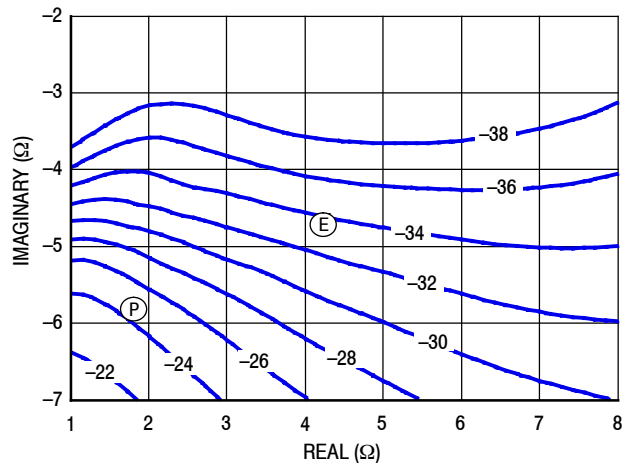
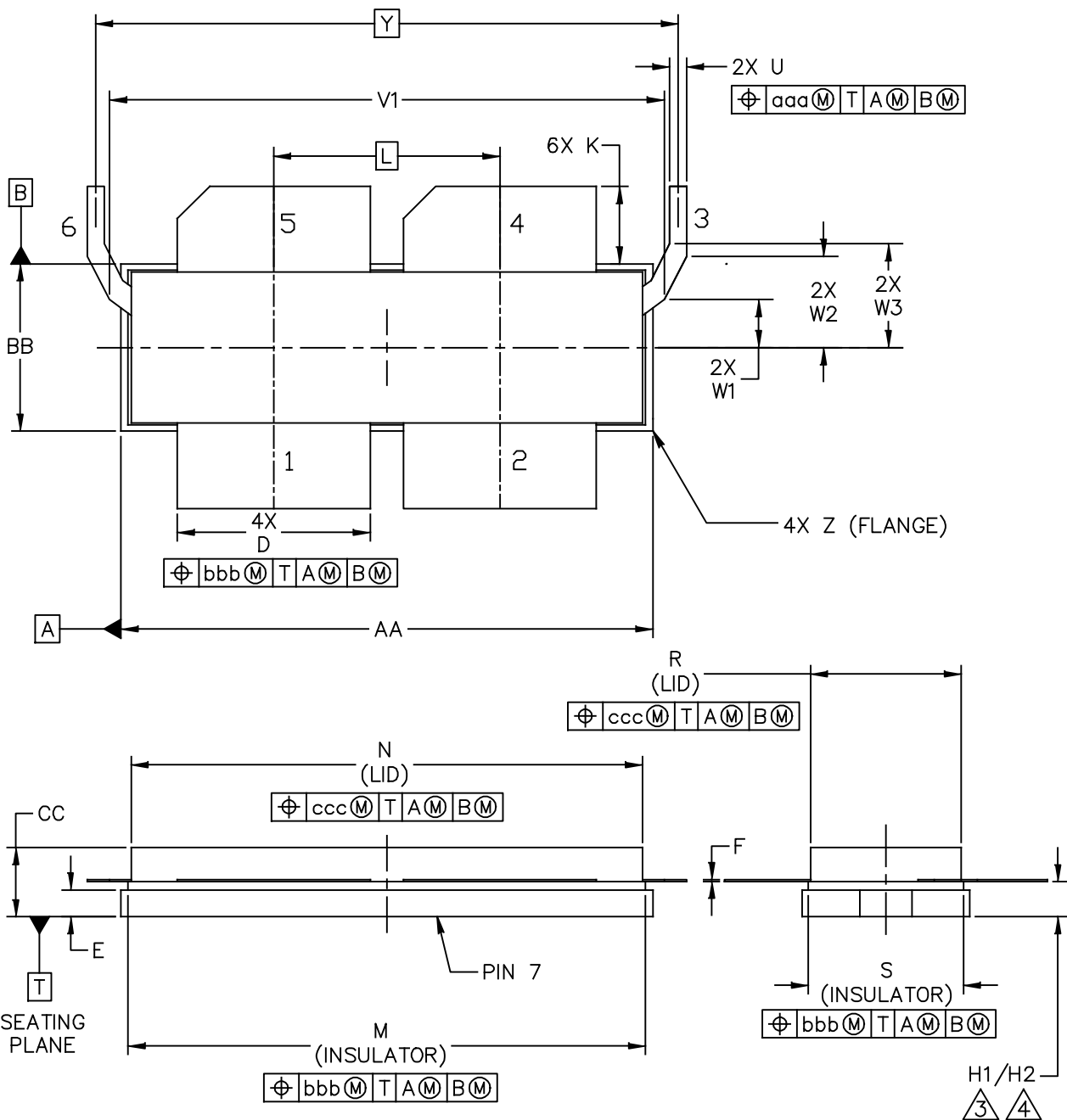


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-1230-4LS2L	DOCUMENT NO: 98ASA00513D STANDARD: NON-JEDEC	REV: A 08 MAR 2013

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-1230-4LS2L		DOCUMENT NO: 98ASA00513D	REV: A
		STANDARD: NON-JEDEC	
		08 MAR 2013	

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2015	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2015 Freescale Semiconductor, Inc.