ispGDX®160V/VA Device Datasheet

June 2010

Select Devices Discontinued!

Product Change Notification (PCN) #09-10 has been issued to discontinue select devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispGDX160V	ispGDX160V-5B272	**Discontinued**	PCN#09-10
	ispGDX160V-7B272		
	ispGDX160V-5B208	Active / Orderable	
	ispGDX160V-7B208		
	ispGDX160V-5Q208		
	ispGDX160V-7Q208		
	ispGDX160V-7Q208I		
ispGDX160VA	ispGDX160VA-3B272	**Discontinued**	PCN#09-10
	ispGDX160VA-5B272		
	ispGDX160VA-7B272		
	ispGDX160VA-5B272I		
	ispGDX160VA-7B272I		
	ispGDX160VA-9B272I		
	ispGDX160VA-3Q208	Active / Orderable	
	ispGDX160VA-5Q208		
	ispGDX160VA-7Q208		
	ispGDX160VA-5Q208I		
	ispGDX160VA-7Q208I		
	ispGDX160VA-9Q208I		
	ispGDX160VA-3B208		
	ispGDX160VA-3BN208		
	ispGDX160VA-5B208		
	ispGDX160VA-5BN208		
	ispGDX160VA-7B208		
	ispGDX160VA-7BN208		
	ispGDX160VA-5B208I		
	ispGDX160VA-5BN208I		
	ispGDX160VA-7B208I		
	ispGDX160VA-7BN208I		
	ispGDX160VA-9B208I		
	ispGDX160VA-9BN208I		

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Lattice Semiconductor Corporation

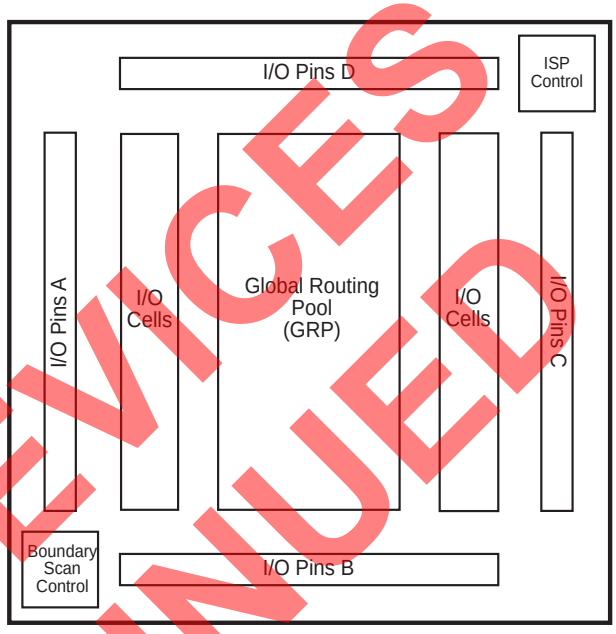
Lead-Free Package Options Available!

ispGDX®160V/VA

In-System Programmable 3.3V Generic Digital Crosspoint

- **IN-SYSTEM PROGRAMMABLE GENERIC DIGITAL CROSSPOINT FAMILY**
  - — Advanced Architecture Addresses Programmable PCB Interconnect, Bus Interface Integration and Jumper/Switch Replacement
  - — "Any Input to Any Output" Routing
  - — Fixed HIGH or LOW Output Option for Jumper/DIP Switch Emulation
  - — Space-Saving PQFP and BGA Packaging
  - — Dedicated IEEE 1149.1-Compliant Boundary Scan Test
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - — 3.3V Core Power Supply
  - — 3.5ns Input-to-Output/3.5ns Clock-to-Output Delay*
  - — 250MHz Maximum Clock Frequency*
  - — TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels (Individually Programmable)*
  - — Low-Power: 16.5mA Quiescent Icc*
  - — 24mA I_{OL} Drive with Programmable Slew Rate Control Option
  - — PCI Compatible Drive Capability*
  - — Schmitt Trigger Inputs for Noise Immunity
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile E^2CMOS Technology
- **ispGDXV OFFERS THE FOLLOWING ADVANTAGES**
  - — 3.3V In-System Programmable Using Boundary Scan Test Access Port (TAP)
  - — Change Interconnects in Seconds
- **FLEXIBLE ARCHITECTURE**
  - — Combinatorial/Latched/Registered Inputs or Outputs
  - — Individual I/O Tri-state Control with Polarity Control
  - — Dedicated Clock/Clock Enable Input Pins (four) or Programmable Clocks/Clock Enables from I/O Pins (40)
  - — Single Level 4:1 Dynamic Path Selection (Tpd = 3.5ns)
  - — Programmable Wide-MUX Cascade Feature Supports up to 16:1 MUX
  - — Programmable Pull-ups, Bus Hold Latch and Open Drain on I/O Pins
  - — Outputs Tri-state During Power-up ("Live Insertion" Friendly)
- **LEAD-FREE PACKAGE OPTIONS**

*** "VA" Version Only**



The ispGDXV/VA architecture provides a family of fast, flexible programmable devices to address a variety of system-level digital signal routing and interface requirements including:

- Multi-Port Multiprocessor Interfaces
- Wide Data and Address Bus Multiplexing (e.g. 16:1 High-Speed Bus MUX)
- Programmable Control Signal Routing (e.g. Interrupts, DMAREQs, etc.)
- Board-Level PCB Signal Routing for Prototyping or Programmable Bus Interfaces

The devices feature fast operation, with input-to-output signal delays (Tpd) of 3.5ns and clock-to-output delays of 3.5ns.

The architecture of the devices consists of a series of programmable I/O cells interconnected by a Global Routing Pool (GRP). All I/O pin inputs enter the GRP directly or are registered or latched so they can be routed to the required I/O outputs. I/O pin inputs are defined as four sets (A,B,C,D) which have access to the four MUX inputs

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found in each I/O cell. Each output has individual, programmable I/O tri-state control (OE), output latch clock (CLK), clock enable (CLKEN), and two multiplexer control (MUX0 and MUX1) inputs. Polarity for these signals is programmable for each I/O cell. The MUX0 and MUX1 inputs control a fast 4:1 MUX, allowing dynamic selection of up to four signal sources for a given output. A wider 16:1 MUX can be implemented with the MUX expander feature of each I/O and a propagation delay increase of 2.0ns. OE, CLK, CLKEN, and MUX0 and MUX1 inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock input pins give minimum clock-to-output delays. CLK and CLKEN share the same set of I/O pins. CLKEN disables the register clock when CLKEN = 0.

Through in-system programming, connections between I/O pins and architectural features (latched or registered inputs or outputs, output enable control, etc.) can be defined. In keeping with its data path application focus, the ispGDXV devices contain no programmable logic arrays. All input pins include Schmitt trigger buffers for noise immunity. These connections are programmed into the device using non-volatile E^2CMOS technology. Non-volatile technology means the device configuration is saved even when the power is removed from the device.

In addition, there are no pin-to-pin routing constraints for 1:1 or 1:n signal routing. That is, *any* I/O pin configured as an input can drive one or more I/O pins configured as outputs.

The device pins also have the ability to set outputs to fixed HIGH or LOW logic levels (Jumper or DIP Switch mode). Device outputs are specified for 24mA sink and 12mA source current (at JEDEC LVTTL levels) and can be tied together in parallel for greater drive. On the ispGDXVA, each I/O pin is individually programmable for 3.3V or 2.5V output levels as described later. Programmable output slew rate control can be defined independently for each I/O pin to reduce overall ground bounce and switching noise.

All I/O pins are equipped with IEEE1149.1-compliant Boundary Scan Test circuitry for enhanced testability. In addition, in-system programming is supported through the Test Access Port via a special set of private commands.

The ispGDXV I/Os are designed to withstand "live insertion" system environments. The I/O buffers are disabled during power-up and power-down cycles. When designing for "live insertion," absolute maximum rating conditions for the Vcc and I/O pins must still be met.

Table 1. ispGDXV Family Members

	ispGDXVA Device		
	ispGDX80VA	ispGDX160VA	ispGDX240VA
I/O Pins	80	160	240
I/O-OE Inputs*	20	40	60
I/O-CLK / CLKEN Inputs*	20	40	60
I/O-MUXsel1 Inputs*	20	40	60
I/O-MUXsel2 Inputs*	20	40	60
Dedicated Clock Pins**	2	4	4
EPEN	1	1	1
TOE	1	1	1
BSCAN Interface	4	4	4
$\overline{\text{RESET}}$	1	1	1
Pin Count/Package	100-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Ball fpBGA

* The CLK/CLK_EN, OE, MUX0 and MUX1 terminals on each I/O cell can each be assigned to 25% of the I/Os.

** Global clock pins Y0, Y1, Y2 and Y3 are multiplexed with CLKEN0, CLKEN1, CLKEN2 and CLKEN3 respectively in all devices.

The ispGDXV/VA architecture is different from traditional PLD architectures, in keeping with its unique application focus. The block diagram is shown below. The programmable interconnect consists of a single Global Routing Pool (GRP). Unlike ispLSI® devices, there are no programmable logic arrays on the device. Control signals for OEs, Clocks/Clock Enables and MUX Controls must come from designated sets of I/O pins. The polarity of these signals can be independently programmed in each I/O cell.

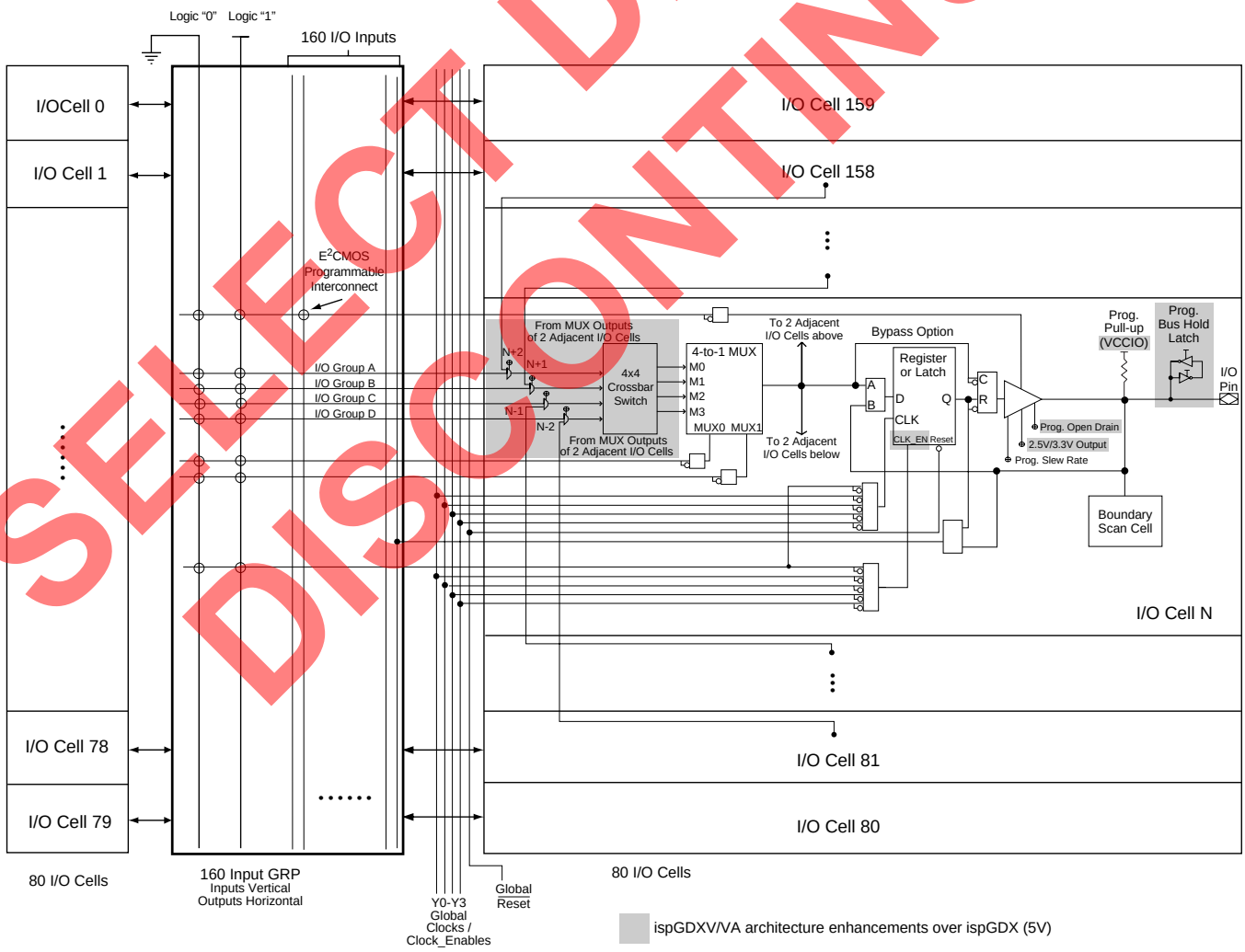
Each I/O cell drives a unique pin. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O pins (I/O-OE set). The I/O-OE set consists of 25% of the total I/O pins. Boundary Scan test is supported by dedicated registers at each I/O pin. In-system programming is accomplished through the standard Boundary Scan protocol.

The various I/O pin sets are also shown in the block diagram below. The A, B, C, and D I/O pins are grouped together with one group per side.

I/O Architecture

Each I/O cell contains a 4:1 dynamic MUX controlled by two select lines as well as a 4x4 crossbar switch controlled by software for increased routing flexiability (Figure 1). The four data inputs to the MUX (called M0, M1, M2, and M3) come from I/O signals in the GRP and/or adjacent I/O cells. Each MUX data input can access one quarter of the total I/Os. For example, in a 160 I/O ispGDXV, each data input can connect to one of 40 I/O pins. MUX0 and MUX1 can be driven by designated I/O pins called MUXsel1 and MUXsel2. Each MUXsel input covers 25% of the total I/O pins (e.g. 40 out of 160). MUX0 and MUX1 can be driven from either MUXsel1 or MUXsel2.

Figure 1. ispGDXV/VA I/O Cell and GRP Detail (160 I/O Device)



I/O MUX Operation

MUX1	MUX0	Data Input Selected
0	0	M0
0	1	M1
1	1	M2
1	0	M3

Flexible mapping of $MUXsel_X$ to MUX_X allows the user to change the MUX select assignment after the ispGDXV/VA device has been soldered to the board. Figure 1 shows that the I/O cell can accept (by programming the appropriate fuses) inputs from the MUX outputs of four adjacent I/O cells, two above and two below. This enables cascading of the MUXes to enable wider (up to 16:1) MUX implementations.

The I/O cell also includes a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. As shown in Figure 1, when the input control MUX of the register/latch selects the "A" path, the register/latch gets its inputs from the 4:1 MUX and drives the I/O output. When selecting the "B" path, the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O-CLK/CLKEN set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Y_X). The programmable polarity Clock Enable input to the register can be programmed to connect to any of the I/O-CLK/CLKEN input pin set or to the global clock enable inputs ($CLKEN_X$). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass MUX. I/O cell output polarity can be programmed as active high or active low.

The ispGDXV/VA allows adjacent I/O cell MUXes to be cascaded to form wider input MUXes (up to 16 x 1) without incurring an additional full Tpd penalty. However, there are certain dependencies on the locality of the adjacent MUXes when used along with direct MUX inputs.

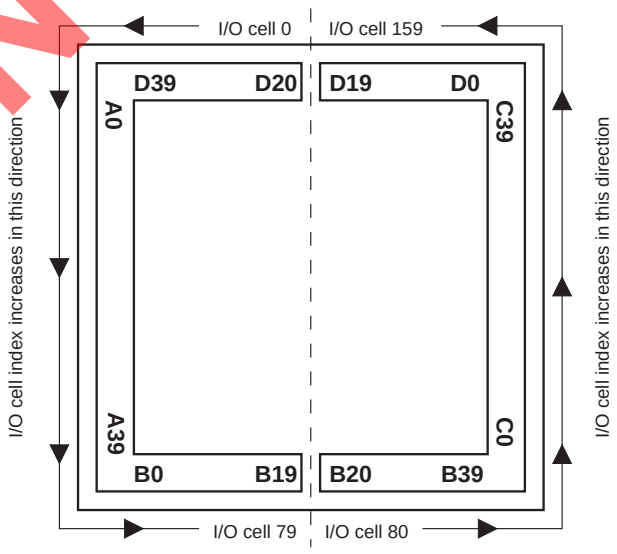
Adjacent I/O Cells

Expansion inputs MUXOUT[n-2], MUXOUT[n-1], MUXOUT[n+1], and MUXOUT[n+2] are fuse-selectable for each I/O cell MUX. These expansion inputs share the same path as the standard A, B, C and D MUX inputs, and allow adjacent I/O cell outputs to be directly connected without passing through the global routing pool. The relationship between the [N+i] adjacent cells and A, B, C and D inputs will vary depending on where the I/O cell is located on the physical die. The I/O cells can be grouped into "normal" and "reflected" I/O cells or I/O "hemispheres." These are defined as:

Device	Normal I/O Cells	Reflected I/O Cells
ispGDX80VA	TBA	TBA
ispGDX160V/VA	B19-B0, A39-A20, A19-A0, D39-D20	B20-B39, C0-C19, C20-C39, D0-D19
ispGDX240VA	TBA	TBA

Table 2 shows the relationship between adjacent I/O cells as well as their relationship to direct MUX inputs. Note that the MUX expansion is circular and that I/O cell B20, for example, draws on I/Os B19 and B18, as well as B21 and B22, even though they are in different hemispheres of the physical die. Table 2 shows some typical cases and all boundary cases. All other cells can be extrapolated from the pattern shown in the table.

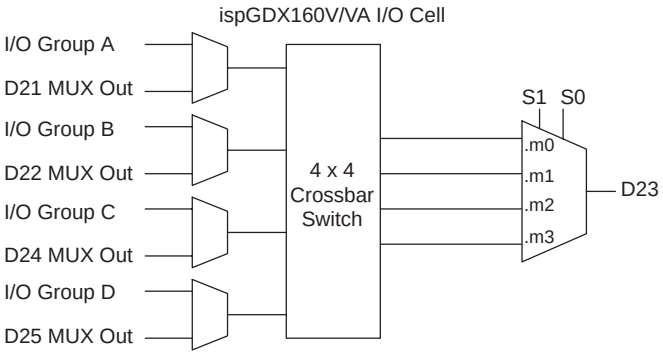
Figure 2. I/O Hemisphere Configuration of ispGDX160V/VA



Direct and Expander Input Routing

Table 2 also illustrates the routing of MUX direct inputs that are accessible when using adjacent I/O cells as inputs. Take I/O cell D23 as an example, which is also shown in Figure 3.

Figure 3. Adjacent I/O Cells vs. Direct Input Path for ispGDX160V/VA, I/O D23



It can be seen from Figure 3 that if the D21 adjacent I/O cell is used, the I/O group "A" input is no longer available as a direct MUX input.

The ispGDXV/VA can implement MUXes up to 16 bits wide in a single level of logic, but care must be taken when combining adjacent I/O cell outputs with direct MUX inputs. Any particular combination of adjacent I/O cells as MUX inputs will dictate what I/O groups (A, B, C or D) can be routed to the remaining inputs. By properly choosing the adjacent I/O cells, all of the MUX inputs can be utilized.

Table 2. Adjacent I/O Cells (Mapping of ispGDX160V/VA)

		Data A/ MUXOUT	Data B/ MUXOUT	Data C/ MUXOUT	Data D/ MUXOUT
Reflected I/O Cells	B20	B22	B21	B19	B18
	B21	B23	B22	B20	B19
	B22	B24	B23	B21	B20
	B23	B25	B24	B22	B21
	D16	D18	D17	D15	D14
	D17	D19	D18	D16	D15
	D18	D20	D19	D17	D16
	D19	D21	D20	D18	D17
Normal I/O Cells	D20	D18	D19	D21	D22
	D21	D19	D20	D22	D23
	D22	D20	D21	D23	D24
	D23	D21	D22	D24	D25
	B16	B14	B15	B17	B18
	B17	B15	B16	B18	B19
	B18	B16	B17	B19	B20
	B19	B17	B18	B20	B21

Slew Rate Control

All output buffers contain a programmable slew rate control that provides software-selectable slew rate options.

Open Drain Control

All output buffers provide a programmable Open-Drain option which allows the user to drive system level reset, interrupt and enable/disable lines directly without the need for an off-chip Open-Drain or Open-Collector buffer. Wire-OR logic functions can be performed at the printed circuit board level.

Pull-up Resistor

All pins have a programmable active pull-up. A typical resistor value for the pull-up ranges from 50kΩ to 80kΩ.

Output Latch (Bus Hold)

All pins have a programmable circuit that weakly holds the previously driven state when all drivers connected to the pin (including the pin's output driver as well as any other devices connected to the pin by external bus) are tristated.

Unique to the ispGDX160VA are user-programmable I/Os supporting either 3.3V or 2.5V output voltage level options. The ispGDX160VA uses a VCCIO pin to provide the 2.5V reference voltage when used. The ispGDX160VA VCCIO pin occupies the same location as VCC on the ispGDX160V, allowing drop-in replacement. The ispGDX160VA offers improved performance by reducing fanout delays and has PCI compatible drive capability.

Only the ispGDX160VA is available in the fastest (3.5ns) Commercial speed grade and in -5,-7, and -9ns Industrial grades in all packages.

The ispGDX160VA has a device ID different from the ispGDX160V requiring that the latest Lattice download software be used for programming and verification. Although the ispGDX160VA and ispGDX160V are functionally equivalent, they are not 100% JEDEC compatible. All design files must be recompiled targeting the ispGDX160VA.

The ispGDXV/VA Family architecture has been developed to deliver an in-system programmable signal routing solution with high speed and high flexibility. The devices are targeted for three similar but distinct classes of end-system applications:

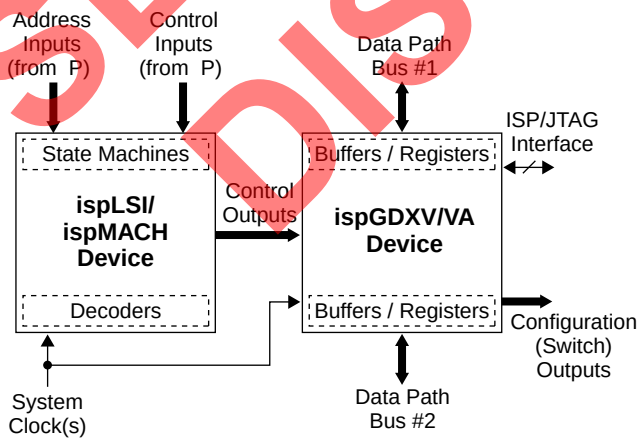
Programmable, Random Signal Interconnect (PRSI)

This class includes PCB-level programmable signal routing and may be used to provide arbitrary signal swapping between chips. It opens up the possibilities of programmable system hardware. It is characterized by the need to provide a large number of 1:1 pin connections which are statically configured, i.e., the pin-to-pin paths do not need to change dynamically in response to control inputs.

Programmable Data Path (PDP)

This application area includes system data path transceiver, MUX and latch functions. With today's 32- and 64-bit microprocessor buses, but standard data path glue components still relegated primarily to eight bits, PCBs are frequently crammed with a dozen or more data path glue chips that use valuable real estate. Many of these applications consist of "on-board" bus and memory interfaces that do not require the very high drive of standard glue functions but can benefit from higher integration. Therefore, there is a need for a flexible means to integrate these on-board data path functions in an analogous way to programmable logic's solution to control logic integration. Lattice's CPLDs make an ideal control logic complement to the ispGDXV/VA in-system programmable data path devices as shown below.

Figure 4. ispGDXV/VA Complements Lattice CPLDs



Programmable Switch Replacement (PSR)

Includes solid-state replacement and integration of mechanical DIP Switch and jumper functions. Through in-system programming, pins of the ispGDXV/VA devices can be driven to HIGH or LOW logic levels to emulate the traditional device outputs. PSR functions do not require any input pin connections.

These applications actually require somewhat different silicon features. PRSI functions require that the device support arbitrary signal routing on-chip between any two pins with no routing restrictions. The routing connections are static (determined at programming time) and each input-to-output path operates independently. As a result, there is little need for dynamic signal controls (OE, clocks, etc.). Because the ispGDXV/VA device will interface with control logic outputs from other components (such as ispLSI or ispMACH™) on the board (which frequently change late in the design process as control logic is finalized), there must be no restrictions on pin-to-pin signal routing for this type of application.

PDP functions, on the other hand, require the ability to dynamically switch signal routing (MUXing) as well as latch and tri-state output signals. As a result, the programmable interconnect is used to define *possible* signal routes that are then selected dynamically by control signals from an external MPU or control logic. These functions are usually formulated early in the conceptual design of a product. The data path requirements are driven by the microprocessor, bus and memory architecture defined for the system. This part of the design is the earliest portion of the system design frozen, and will not usually change late in the design because the result would be total system and PCB redesign. As a result, the ability to accommodate *arbitrary* any pin-to-any pin re-routing is not a strong requirement as long as the designer has the ability to define his functions with a reasonable degree of freedom initially.

As a result, the ispGDXV/VA architecture has been defined to support PSR and PRSI applications (including bidirectional paths) with no restrictions, while PDP applications (using dynamic MUXing) are supported with a minimal number of restrictions as described below. In this way, speed and cost can be optimized and the devices can still support the system designer's needs.

The following diagrams illustrate several ispGDXV/VA applications.

Figure 5. Address Demultiplex/Data Buffering

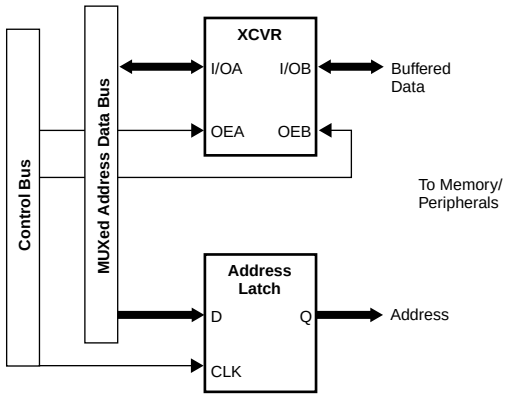


Figure 6. Data Bus Byte Swapper

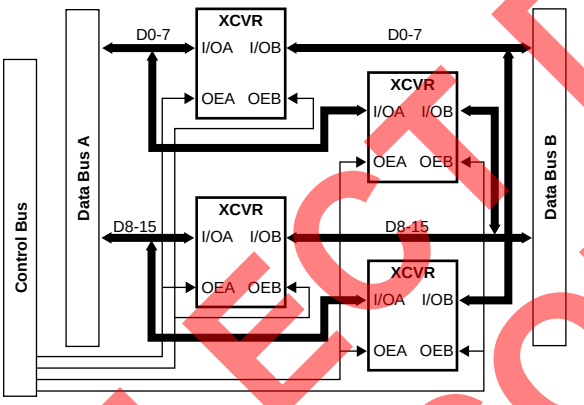
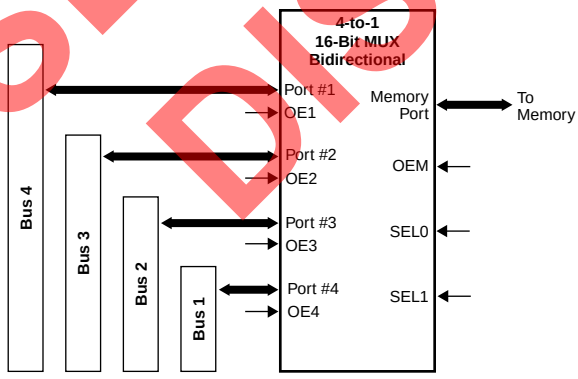


Figure 7. Four-Port Memory Interface



Note: All OE and SEL lines driven by external arbiter logic (not shown).

Designing with the ispGDXV/VA

As mentioned earlier, this architecture satisfies the PRSI class of applications without restrictions: any I/O pin as a single input or bidirectional can drive any other I/O pin as output.

For the case of PDP applications, the designer does have to take into consideration the limitations on pins that can be used as control (MUX0, MUX1, OE, CLK) or data (MUXA-D) inputs. The restrictions on control inputs are not likely to cause any major design issues because the input possibilities span 25% of the total pins.

The MUXA-D input partitioning requires that designers consciously assign pinouts so that MUX inputs are in the appropriate, disjoint groups. For example, since the MUXA group includes I/O0-39 (160 I/O device), it is not possible to use I/O0 and I/O9 in the same MUX function. As previously discussed, data path functions will be assigned early in the design process and these restrictions are reasonable in order to optimize speed and cost.

User Electronic Signature

The ispGDXV/VA Family includes dedicated User Electronic Signature (UES) E^2CMOS storage to allow users to code design-specific information into the devices to identify particular manufacturing dates, code revisions, or the like. The UES information is accessible through the boundary scan programming port via a specific command. This information can be read even when the security cell is programmed.

Security

The ispGDXV/VA Family includes a security feature that prevents reading the device program once set. Even when set, it does not inhibit reading the UES or device ID code. It can be erased only via a device bulk erase.

Supply Voltage V_{cc} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	3.00	3.60	V
		Industrial	T_A = -40°C to +85°C	3.00	3.60	V
V_{CCIO}	I/O Reference Voltage			2.3	3.60	V

Table 2-0005/gdx160va

SYMBOL	PARAMETER	PACKAGE TYPE	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	PQFP	7	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
		BGA, fpBGA	10	pf	
C_2	Dedicated Clock Capacitance	PQFP	8	pf	V_{CC} = 3.3V, V_Y = 2.0V
		BGA, fpBGA	10	pf	

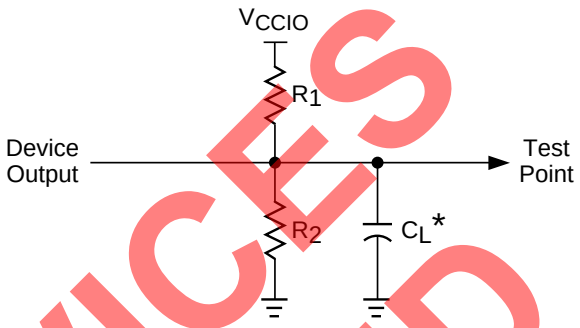
Table 2-0006/gdx160va

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Input Pulse Levels	GND to $V_{CCIO(MIN)}$
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Load	See Figure 8

3-state levels are measured 0.5V from steady-state active level.

Figure 8. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load Conditions (See Figure 8)

TEST CONDITION		3.3V R1	3.3V R2	2.5V R1	2.5V R2	CL
A		153Ω	134Ω	156Ω	144Ω	35pF
B	Active High	∞	134Ω	∞	144Ω	35pF
	Active Low	153Ω	∞	156Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	134Ω	∞	144Ω	5pF
	Active Low to Z at V_{OL}+0.5V	153Ω	∞	156Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/gdx160va

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–		3.0	–	3.6	V
V_{IL}	Input Low Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL\ (MAX)}$		-0.3	–	0.8	V
V_{IH}	Input High Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$		2.0	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC\ (MIN)}$	I_{OL} = +100µA	–	–	0.2	V
			I_{OL} = +24mA	–	–	0.55	V
V_{OH}	Output High Voltage	$V_{CC} = V_{CC\ (MIN)}$	I_{OH} = -100µA	2.8	–	–	V
			I_{OH} = -12mA	2.4	–	–	V

1. I/O voltage configuration must be set to VCC.

Table 2-0007/gdx160va

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–	2.3	–	2.7	V
V_{IL}	Input Low Voltage	$V_{OH(MIN)} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$	-0.3	–	0.7	V
V_{IH}	Input High Voltage	$V_{OH(MIN)} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$	1.7	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO=MIN}$, I_{OL} = 100µA	–	–	0.2	V
		$V_{CCIO=MIN}$, I_{OL} = 8mA	–	–	0.6	V
V_{OH}	Output High Voltage	$V_{CCIO=MIN}$, I_{OH} = -100µA	2.1	–	–	V
		$V_{CCIO=MIN}$, I_{OH} = -8mA	1.8	–	–	V

1. I/O voltage configuration must be set to VCCIO.

2.5V/gdx160va

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL\ (MAX)}$	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2) \le V_{IN} \le V_{CCIO}$	–	–	10	µA
		$V_{CCIO} \le V_{IN} \le 5.25V$	–	–	50	µA
I_{PU}	I/O Active Pullup Current	$0V \le V_{IN} \le V_{IL\ (MAX)}$	–	–	-200	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL\ (MAX)}$	40	–	–	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH\ (MIN)}$	-40	–	–	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	550	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	-550	µA
I_{BHT}	Bus Hold Trip Points		V_{IL}	–	V_{IH}	V
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V, T_A = 25°C	–	–	-250	mA
I_{CCQ}[4]	Quiescent Power Supply Current	V_{IL} = 0.5V, V_{IH} = V_{CC}	–	16.5	–	mA
I_{CC}	Dynamic Power Supply Current per Input Switching	One input toggling at 50% duty cycle, outputs open.	–	See Note 3	–	mA/ MHz
I_{CONT}[5]	Maximum Continuous I/O Pin Sink Current Through Any GND Pin	–	–	–	160	mA

1. One output at a time for a maximum of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized, but not 100% tested.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. I_{CC} / MHz = (0.003 x I/O cell fanout) + 0.029.
   e.g. An input driving four I/O cells at 40MHz results in a dynamic I_{CC} of approximately ((0.003 x 4) + 0.029) x 40 = 1.64mA.
4. For a typical application with 50% of I/O pins used as inputs, 50% used as outputs or bi-directionals.
5. This parameter limits the total current sinking of I/O pins surrounding the nearest GND pin.

DC Char_gdx160va

Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-3		-5		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd}[2]	A	1	Data Prop. Delay from Any I/O pin to Any I/O Pin (4:1 MUX)	–	3.5	–	5.0	ns
t_{sel}[2]	A	2	Data Prop. Delay from MUXsel Inputs to Any Output (4:1 MUX)	–	3.5	–	5.0	ns
f_{max} (Tog.)	–	3	Clock Frequency, Max. Toggle	250	–	143	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $(\frac{1}{tsu3+tgco1})$	166.7	–	111	–	MHz
t_{su1}	–	5	Input Latch or Register Setup Time Before Y_x	3.0	–	4.0	–	ns
t_{su2}	–	6	Input Latch or Register Setup Time Before I/O Clock	2.5	–	3.0	–	ns
t_{su3}	–	7	Output Latch or Register Setup Time Before Y_x	2.5	–	4.0	–	ns
t_{su4}	–	8	Output Latch or Register Setup Time Before I/O Clock	2.0	–	3.0	–	ns
t_{suce1}	–	9	Global Clock Enable Setup Time Before Y_x	2.5	–	2.5	–	ns
t_{suce2}	–	10	Global Clock Enable Setup Time Before I/O Clock	1.5	–	1.5	–	ns
t_{suce3}	–	11	I/O Clock Enable Setup Time Before Y_x	3.0	–	4.5	–	ns
t_{h1}	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h2}	–	13	Input Latch or Reg. Hold Time (I/O Clock)	0.5	–	1.5	–	ns
t_{h3}	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h4}	–	15	Output Latch or Reg. Hold Time (I/O Clock)	1.0	–	1.5	–	ns
t_{hce1}	–	16	Global Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{hce2}	–	17	Global Clock Enable Hold Time (I/O Clock)	1.0	–	1.5	–	ns
t_{hce3}	–	18	I/O Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{gco1}[2]	A	19	Output Latch or Reg. Clock (from Y_x) to Output Delay	–	3.5	–	5.0	ns
t_{gco2}[2]	A	20	Input Latch or Register Clock (from Y_x) to Output Delay	–	6.0	–	8.5	ns
t_{co1}[2]	A	21	Output Latch or Register Clock (from I/O pin) to Output Delay	–	4.0	–	6.0	ns
t_{co2}[2]	A	22	Input Latch or Register Clock (from I/O pin) to Output Delay	–	7.0	–	9.5	ns
t_{en}[2]	B	23	Input to Output Enable	–	5.0	–	6.0	ns
t_{dis}[2]	C	24	Input to Output Disable	–	5.0	–	6.0	ns
t_{toeen}[2]	B	25	Test OE Output Enable	–	6.0	–	6.0	ns
t_{toedis}[2]	C	26	Test OE Output Disable	–	6.0	–	6.0	ns
t_{wh}	–	27	Clock Pulse Duration, High	2.0	–	3.5	–	ns
t_{wl}	–	28	Clock Pulse Duration, Low	2.0	–	3.5	–	ns
t_{rst}	–	29	Register Reset Delay from RESET Low	–	8.0	–	14.0	ns
t_{rw}	–	30	Reset Pulse Width	5.0	–	10.0	–	ns
t_{sl}	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	3.5	–	5.0	ns
t_{sk}	A	32	Output Skew (tgco1 Across Chip)	–	0.5	–	0.5	ns

1. All timings measured with one output switching, fast output slew rate setting, except t_{sl}.
2. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

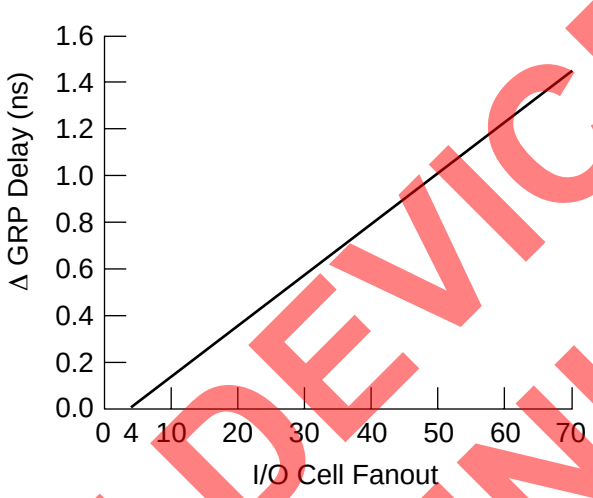
Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-7		-9		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd}[2]	A	1	Data Prop. Delay from Any I/O pin to Any I/O Pin (4:1 MUX)	–	7.0	–	9.0	ns
t_{sel}[2]	A	2	Data Prop. Delay from MUXsel Inputs to Any Output (4:1 MUX)	–	7.0	–	9.0	ns
f_{max} (Tog.)	–	3	Clock Frequency, Max. Toggle	100	–	83	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $(\frac{1}{tsu3+tgco1})$	80	–	62.5	–	MHz
t_{su1}	–	5	Input Latch or Register Setup Time Before Y_x	5.5	–	7.0	–	ns
t_{su2}	–	6	Input Latch or Register Setup Time Before I/O Clock	4.5	–	6.0	–	ns
t_{su3}	–	7	Output Latch or Register Setup Time Before Y_x	5.5	–	7.0	–	ns
t_{su4}	–	8	Output Latch or Register Setup Time Before I/O Clock	4.5	–	6.0	–	ns
t_{suce1}	–	9	Global Clock Enable Setup Time Before Y_x	3.5	–	4.0	–	ns
t_{suce2}	–	10	Global Clock Enable Setup Time Before I/O Clock	2.5	–	3.0	–	ns
t_{suce3}	–	11	I/O Clock Enable Setup Time Before Y_x	6.5	–	8.5	–	ns
t_{h1}	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h2}	–	13	Input Latch or Reg. Hold Time (I/O Clock)	2.5	–	3.0	–	ns
t_{h3}	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h4}	–	15	Output Latch or Reg. Hold Time (I/O Clock)	2.5	–	3.0	–	ns
t_{hce1}	–	16	Global Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{hce2}	–	17	Global Clock Enable Hold Time (I/O Clock)	2.5	–	3.0	–	ns
t_{hce3}	–	18	I/O Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{gco1}[2]	A	19	Output Latch or Reg. Clock (from Y_x) to Output Delay	–	7.0	–	9.0	ns
t_{gco2}[2]	A	20	Input Latch or Register Clock (from Y_x) to Output Delay	–	11.0	–	13.5	ns
t_{co1}[2]	A	21	Output Latch or Register Clock (from I/O pin) to Output Delay	–	9.0	–	11.5	ns
t_{co2}[2]	A	22	Input Latch or Register Clock (from I/O pin) to Output Delay	–	13.0	–	15.7	ns
t_{en}[2]	B	23	Input to Output Enable	–	8.5	–	10.5	ns
t_{dis}[2]	C	24	Input to Output Disable	–	8.5	–	10.5	ns
t_{toeen}[2]	B	25	Test OE Output Enable	–	8.5	–	10.5	ns
t_{toedis}[2]	C	26	Test OE Output Disable	–	8.5	–	10.5	ns
t_{wh}	–	27	Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	28	Clock Pulse Duration, Low	5.0	–	6.0	–	ns
t_{rst}	–	29	Register Reset Delay from RESET Low	–	18.0	–	22.0	ns
t_{rw}	–	30	Reset Pulse Width	14.0	–	18.0	–	ns
t_{sl}	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	7.0	–	9.0	ns
t_{sk}	A	32	Output Skew (tgco1 Across Chip)	–	0.5	–	1.0	ns

1. All timings measured with one output switching, fast output slew rate setting, except t_{sl}.
2. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

ispGDX160VA timings are specified with a GRP load (fanout) of four I/O cells. The figure below shows the Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK/CLKEN, MUXsel0-1). Global Clock signals which do not use the GRP have no fanout delay adder.

ispGDX160VA Maximum Δ GRP Delay vs. I/O Cell Fanout



Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-3		-5		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	32	Input Buffer Delay	—	0.4	—	0.9	ns
GRP							
t_{grp}	33	GRP Delay	—	1.1	—	1.1	ns
MUX							
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	1.0	—	1.5	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	1.5	—	2.0	ns
t_{muxs}	36	I/O Cell Data Select	—	1.0	—	1.5	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	1.5	—	3.0	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	1.5	—	2.0	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	1.5	—	2.0	ns
Register							
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	0.8	—	2.0	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	1.7	—	1.5	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	1.2	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.0	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.3	—	2.0	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	0.2	—	0.5	ns
Data Path							
t_{fdbk}	47	I/O Register Feedback Delay	—	0.6	—	0.9	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.0	—	0.0	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.0	—	0.0	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	1.5	—	2.0	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	1.5	—	3.0	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	3.5	—	4.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	3.5	—	5.0	ns
Outputs							
t_{ob}	54	Output Buffer Delay	—	1.0	—	1.5	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	4.5	—	6.5	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	3.5	—	4.0	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	3.5	—	4.0	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	2.5	—	2.0	ns
Clocks							
t_{ioclk}	60	I/O Clock Delay	—	0.3	—	2.0	ns
t_{gclk}	61	Global Clock Delay	—	1.3	—	2.0	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clock)	—	1.5	—	2.5	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clock)	—	1.0	—	3.5	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clock)	—	0.5	—	2.5	ns
Global Reset							
t_{gr}	65	Global Reset to I/O Register Latch	—	6.0	—	11.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-7		-9		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	32	Input Buffer Delay	—	1.4	—	1.9	ns
GRP							
t_{grp}	33	GRP Delay	—	1.1	—	1.1	ns
MUX							
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	2.0	—	2.5	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	2.5	—	3.0	ns
t_{muxs}	36	I/O Cell Data Select	—	2.0	—	2.5	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	4.5	—	6.0	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	2.5	—	3.0	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	2.5	—	3.0	ns
Register							
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	3.2	—	4.4	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	2.3	—	2.6	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	0.5	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.5	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.5	—	2.0	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	1.0	—	2.0	ns
Data Path							
t_{fdbk}	47	I/O Register Feedback Delay	—	1.2	—	1.3	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.3	—	0.6	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.6	—	0.7	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	2.5	—	3.0	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	4.5	—	6.0	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	5.0	—	6.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	7.0	—	9.0	ns
Outputs							
t_{ob}	54	Output Buffer Delay	—	2.2	—	2.9	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	9.2	—	11.9	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	6.0	—	7.5	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	6.0	—	7.5	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	2.5	—	3.0	ns
Clocks							
t_{ioclk}	60	I/O Clock Delay	—	3.2	—	4.4	ns
t_{gclk}	61	Global Clock Delay	—	2.7	—	3.4	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clock)	—	3.7	—	5.4	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clock)	—	5.7	—	8.4	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clock)	—	4.2	—	6.4	ns
Global Reset							
t_{gr}	65	Global Reset to I/O Register Latch	—	13.7	—	16.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.

Supply Voltage V_{cc} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to +70°C	3.0	3.6	V
		Industrial T_A = -40°C to +85°C	3.0	3.6	V
V_{IL}[1]	Input Low Voltage		-0.3	0.8	V
V_{IH}[1]	Input High Voltage		2.0	5.25	V

1. Typical 100mV of input hysteresis.

Table 2-0005/gdxv

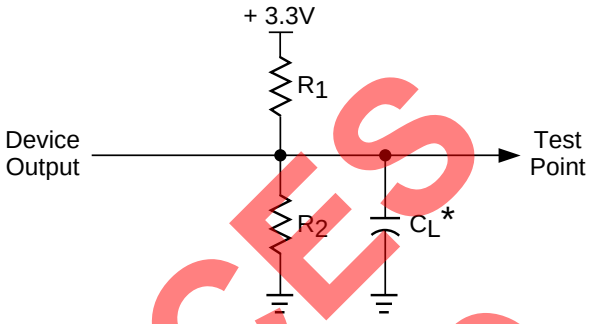
SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	8	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_2	Dedicated Clock Capacitance	10	pf	V_{CC} = 3.3V, V_Y = 2.0V

Table 2 - 0006

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure at right

3-state levels are measured 0.5V from steady-state active level.



*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions

TEST CONDITION		R1	R2	CL
A		153Ω	134Ω	35pF
B	Active High	∞	134Ω	35pF
	Active Low	153Ω	∞	35pF
C	Active High to Z at V_{OH} -0.5V	∞	134Ω	5pF
	Active Low to Z at V_{OL} +0.5V	153Ω	∞	5pF
D	Slow Slew	∞	∞	35pF

Table 2-0004A

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =24 mA	–	–	0.55	V
V_{OH}	Output High Voltage	I_{OH} =-12 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{CC} ≤ V_{IN} ≤ 5.25V	–	–	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (Max.)	50	–	–	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = V_{IH} (Min.)	-50	–	–	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0V ≤ V_{IN} ≤ V_{CC}	–	–	550	µA
I_{BHHO}	Bus Hold High Overdrive Current	0V ≤ V_{IN} ≤ V_{CC}	–	–	-550	µA
I_{BHT}	Bus Hold Trip Points		V_{IL}	–	V_{IH}	V
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V, T_A = 25˚C	–	–	-250	mA
I_{CCQ}[4]	Quiescent Power Supply Current	V_{IL} = 0.5V, V_{IH} = V_{CC}	–	70	–	mA
I_{CC}	Dynamic Power Supply Current per Input Switching	One input toggling @ 50% duty cycle, outputs open.	–	See Note 3	–	mA/MHz
I_{CONT}[5]	Maximum Continuous I/O Pin Sink Current Through Any GND Pin		–	–	96	mA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. I_{CC} / MHz = (0.01 x I/O cell fanout) + 0.04
   e.g. An input driving four I/O cells at 40 MHz results in a dynamic I_{CC} of approximately ((0.01 x 4) + 0.04) x 40 = 3.2 mA.
4. For a typical application with 50% of I/O pins used as inputs, 50% used as outputs or bidirectionals.
5. This parameter limits the total current sinking of I/O pins surrounding the nearest GND pin.

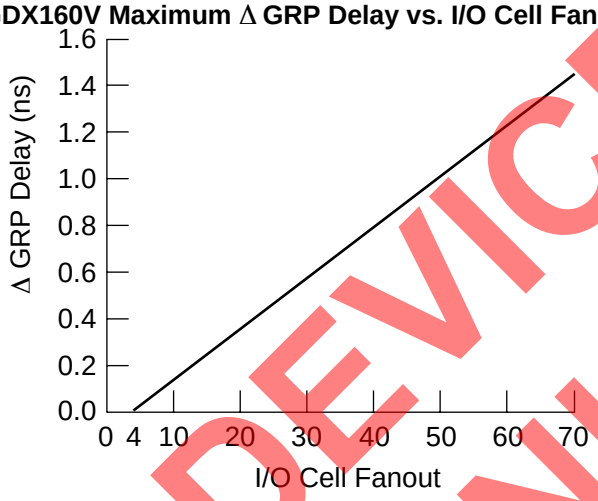
Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-5		-7		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd	A	1	Data Prop. Delay from Any I/O pin to Any I/O pin (4:1 MUX)	–	5.0	–	7.0	ns
tsel	A	2	Data Prop. Delay from MUXsel Inputs to Any Output (4:1 MUX)	–	6.5	–	9.0	ns
fmax (Tog.)	–	3	Clock Frequency, Max. Toggle	143	–	100	–	MHz
fmax (Ext.)	–	4	Clock Frequency with External Feedback ($\frac{1}{tsu3+tgco1}$)	110	–	80.0	–	MHz
tsu1	–	5	Input Latch or Register Setup Time Before Y_x	4.0	–	5.5	–	ns
tsu2	–	6	Input Latch or Register Setup Time Before I/O Clock	3.0	–	4.5	–	ns
tsu3	–	7	Output Latch or Register Setup Time Before Y_x	4.0	–	5.5	–	ns
tsu4	–	8	Output Latch or Register Setup Time Before I/O Clock	3.0	–	4.5	–	ns
tsuce1	–	9	Global Clock Enable Setup Time Before Y_x	2.5	–	3.5	–	ns
tsuce2	–	10	Global Clock Enable Setup Time Before I/O Clock	1.5	–	2.5	–	ns
tsuce3	–	11	I/O Clock Enable Setup Time Before Y_x	4.5	–	6.5	–	ns
th1	–	12	Input Latch or Register Hold Time (Y_x)	0.0	–	0.0	–	ns
th2	–	13	Input Latch or Register Hold Time (I/O Clock)	1.5	–	2.5	–	ns
th3	–	14	Output Latch or Register Hold Time (Y_x)	0.0	–	0.0	–	ns
th4	–	15	Output Latch or Register Hold Time (I/O Clock)	1.5	–	2.5	–	ns
thce1	–	16	Global Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
thce2	–	17	Global Clock Enable Hold Time (I/O Clock)	1.5	–	2.5	–	ns
thce3	–	18	I/O Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
tgco1	A	19	Output Latch or Register Clock (from Y_x) to Output Delay	–	5.0	–	7.0	ns
tgco2	A	20	Input Latch or Register Clock (from Y_x) to Output Delay	–	8.5	–	11.0	ns
tco1	A	21	Output Latch or Register Clock (from I/O pin) to Output Delay	–	6.0	–	9.0	ns
tco2	A	22	Input Latch or Register Clock (from I/O pin) to Output Delay	–	9.5	–	13.0	ns
ten	B	23	Input to Output Enable	–	6.0	–	8.5	ns
tdis	C	24	Input to Output Disable	–	6.0	–	8.5	ns
ttoeen	B	25	Test OE Output Enable	–	9.0	–	12.0	ns
ttoedis	C	26	Test OE Output Disable	–	9.0	–	12.0	ns
twh	–	27	Clock Pulse Duration, High	3.5	–	5.0	–	ns
twl	–	28	Clock Pulse Duration, Low	3.5	–	5.0	–	ns
trst	–	29	Register Reset Delay from RESET Low	–	14.0	–	18.0	ns
trw	–	30	Reset Pulse Width	10.0	–	14.0	–	ns
tsl	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	8.0	–	12.0	ns
tsk	A	32	Output Skew (tgco1 Across Chip)	–	0.5	–	0.5	ns

1. All timings measured with one output switching, fast output slew rate setting, except tsl.

ispGDX160V timings are specified with a GRP load (fanout) of four I/O cells. The figure below shows the Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK/CLKEN, MUXsel0-1). Global Clock signals which do not use the GRP have no fanout delay adder.

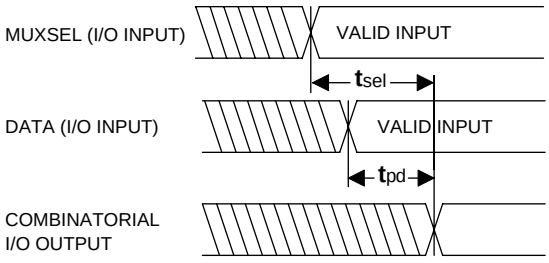
ispGDX160V Maximum Δ GRP Delay vs. I/O Cell Fanout



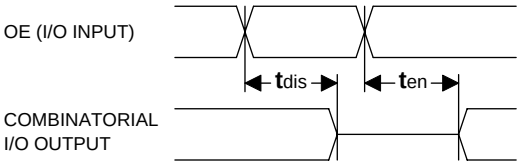
Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-5		-7		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	32	Input Buffer Delay	—	0.9	—	1.4	ns
GRP							
t_{grp}	33	GRP Delay	—	1.1	—	1.1	ns
MUX							
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	1.5	—	2.0	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	2.0	—	2.5	ns
t_{muxs}	36	I/O Cell Data Select	—	3.0	—	4.0	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clk)	—	4.5	—	6.5	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clk)	—	3.5	—	4.5	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	3.5	—	4.5	ns
Register							
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	2.0	—	3.2	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	1.5	—	2.3	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	0.5	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.5	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.0	—	2.5	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	0.5	—	1.0	ns
Data Path							
t_{fdbk}	47	I/O Register Feedback Delay	—	0.9	—	1.2	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.0	—	0.3	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.0	—	0.6	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clk)	—	2.0	—	2.5	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clk)	—	3.0	—	4.5	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clk)	—	4.0	—	5.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clk)	—	5.0	—	7.0	ns
Outputs							
t_{ob}	54	Output Buffer Delay	—	1.5	—	2.2	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	9.5	—	14.2	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	4.0	—	6.0	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	4.0	—	6.0	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	5.0	—	6.0	ns
Clocks							
t_{ioclk}	60	I/O Clock Delay	—	2.0	—	3.2	ns
t_{gclk}	61	Global Clock Delay	—	2.0	—	2.7	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clk)	—	2.5	—	3.7	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clk)	—	3.5	—	5.7	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clk)	—	2.5	—	4.2	ns
Global Reset							
t_{gr}	65	Global Reset to I/O Register Latch	—	11.0	—	13.7	ns

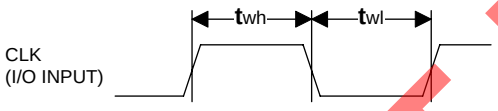
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.



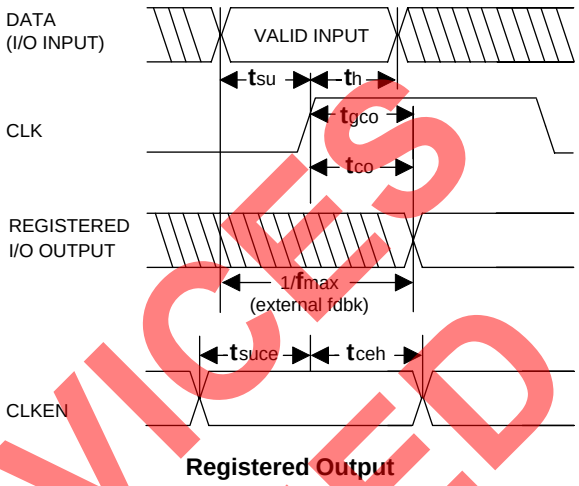
Combinatorial Output



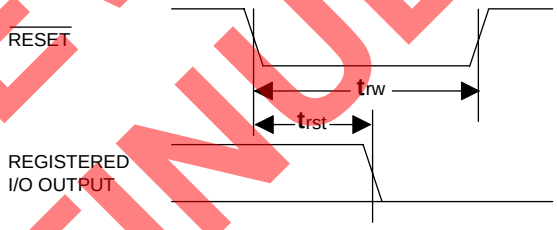
I/O Output Enable/Disable



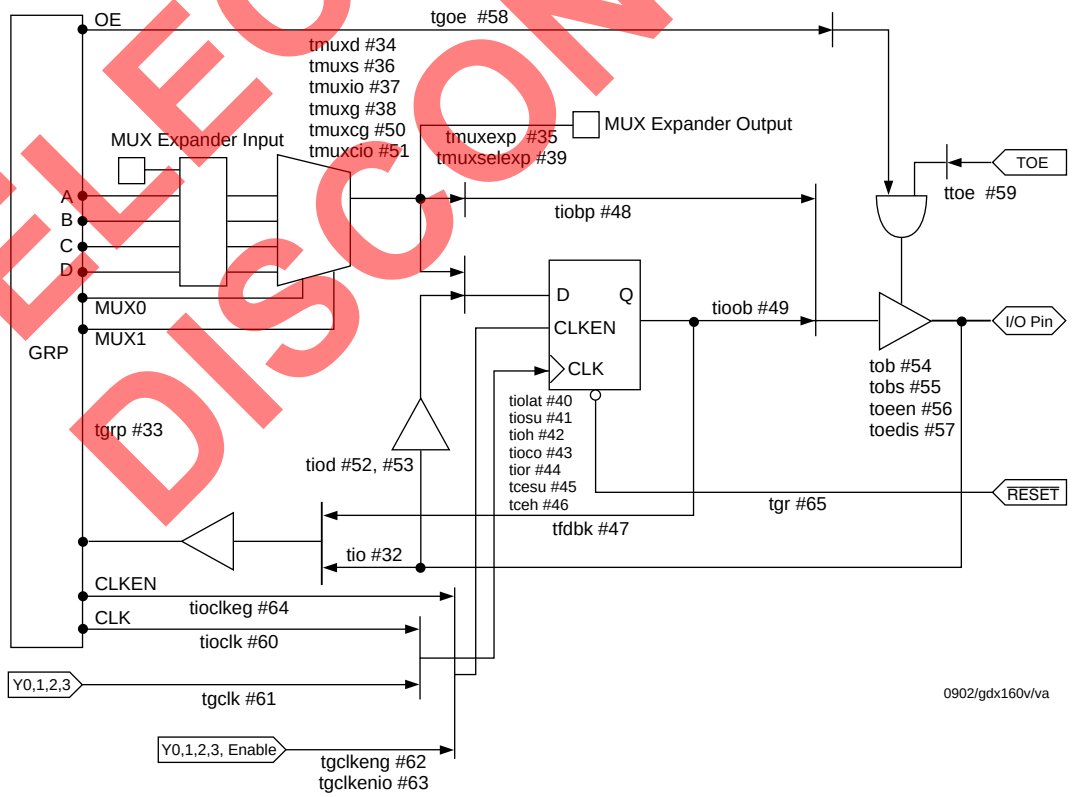
Clock Width



Registered Output



Reset



The ispLEVER Development System supports ispGDX design using a VHDL or Verilog language syntax. From creation to in-system programming, the ispLEVER system is an easy-to-use, self-contained design tool.

Features

- VHDL and Verilog Synthesis Support Available
- ispGDX Design Compiler
  - Design Rule Checker
  - I/O Connectivity Checker
  - Automatic Compiler Function
- Industry Standard JEDEC File for Programming
- Min/Max Timing Report
- Interfaces To Popular Timing Simulators
- User Electronic Signature (UES) Support
- Detailed Log and Report Files For Easy Design Debug
- On-line Help
- Windows® XP, Windows 2000, Windows 98 and Windows NT® Compatible
- Solaris® and HP-UX Versions Available

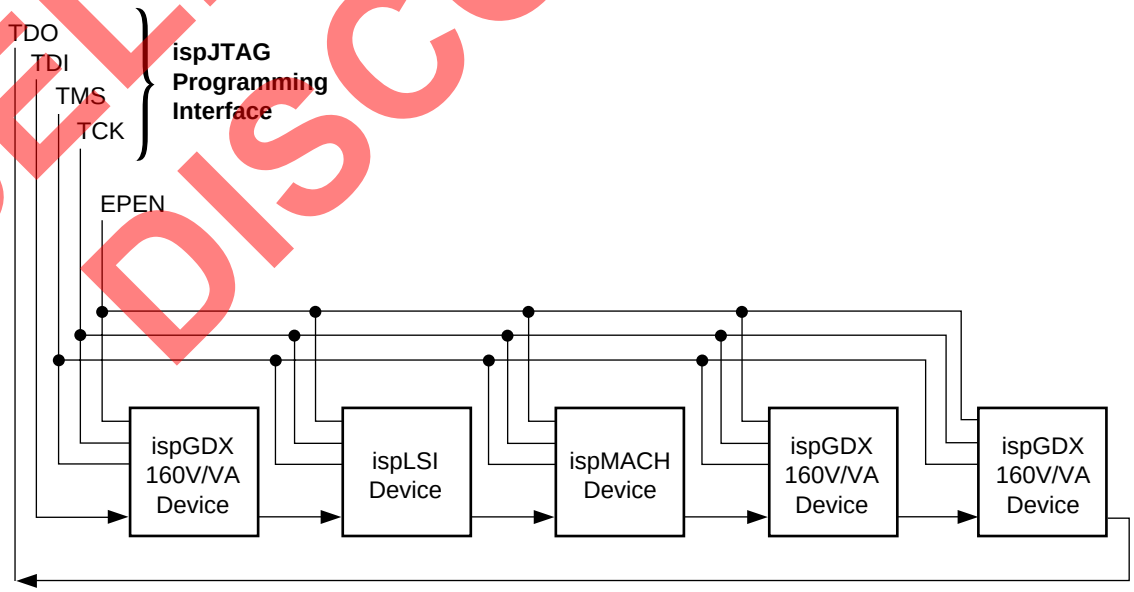
All necessary programming of the ispGDXV/VA is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming.

On-chip programming can be accomplished using an IEEE 1149.1 boundary scan protocol. The IEEE 1149.1-compliant interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. The EPEN pin is also used to enable or disable the JTAG port.

The embedded controller port enable pin (EPEN) is used to enable the JTAG tap controller and in that regard has similar functionality to a TRST pin. When the pin is driven high, the JTAG TAP controller is enabled. This is also true when the pin is left unconnected, in which case the pin is pulled high by the permanent internal pullup. This allows ISP programming and BSCAN testing to take place as specified by the Instruction Table.

When the pin is driven low, the JTAG TAP controller is driven to a reset state asynchronously. It stays there while the pin is held low. After pulling the pin high the JTAG controller becomes active. The intent of this feature is to allow the JTAG interface to be directly controlled by the data bus of an embedded controller (hence the name Embedded Port Enable). The EPEN signal is used as a “device select” to prevent spurious programming and/or testing from occuring due to random bit patterns on the data bus. Figure 9 illustrates the block diagram for the ispJTAG™ interface.

Figure 9. ispJTAG Device Programming Interface



The ispGDXV/VA devices provide IEEE1149.1a test capability and ISP programming through a standard Boundary Scan Test Access Port (TAP) interface.

The boundary scan circuitry on the ispGDXV/VA Family operates independently of the programmed pattern. This allows customers using boundary scan test to have full test capability with only a single BSDL file.

The ispGDXV/VA devices are identified by the 32-bit JTAG IDCODE register. The device ID assignments are listed in Table 4.

Figure 10. Boundary Scan Register Circuit for I/O Pins

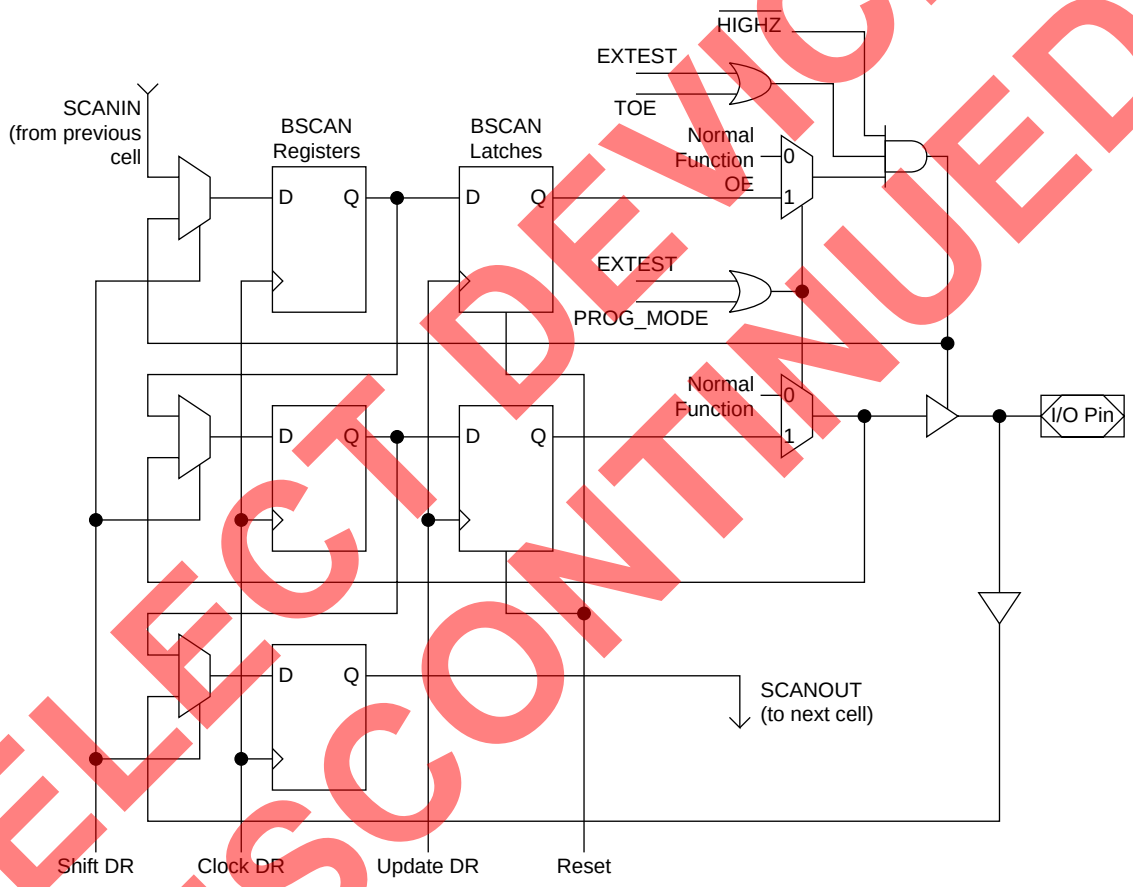


Table 3. I/O Shift Register Order

DEVICE	I/O SHIFT REGISTER ORDER
ispGDX160V/VA	TDI, TOE, Y2, Y3, $\overline{\text{RESET}}$, Y1, Y0, I/O B20 .. B39, I/O C0 .. C39, I/O D0 .. D19, I/O B19 .. B0, I/O A39.. A0, I/O D39 .. D20, TDO

I/O Shift Reg Order/ispGDXVA

Table 4. ispGDX160V/VA Device ID Codes

DEVICE	32-BIT BOUNDARY SCAN ID CODE
ispGDX160V	0000, 0000, 0011, 0101, 0011, 0000, 0100, 0011
ispGDX160VA	0001, 0000, 0011, 0101, 0011, 0000, 0100, 0011

ID Code/GDX160V/VA

The ispJTAG programming is accomplished by executing Lattice private instructions under the Boundary Scan State Machine.

Details of the programming sequence are transparent to the user and are handled by Lattice ISP Daisy Chain Downlowad (ispDCD™), ispCODE 'C' routines or any third-party programmers. Contact Lattice Technical Support to obtain more detailed programming information.

Figure 11. Boundary Scan Register Circuit for Input-Only Pins

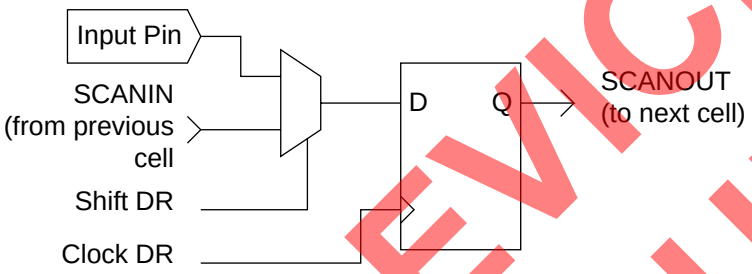


Figure 12. Boundary Scan State Machine

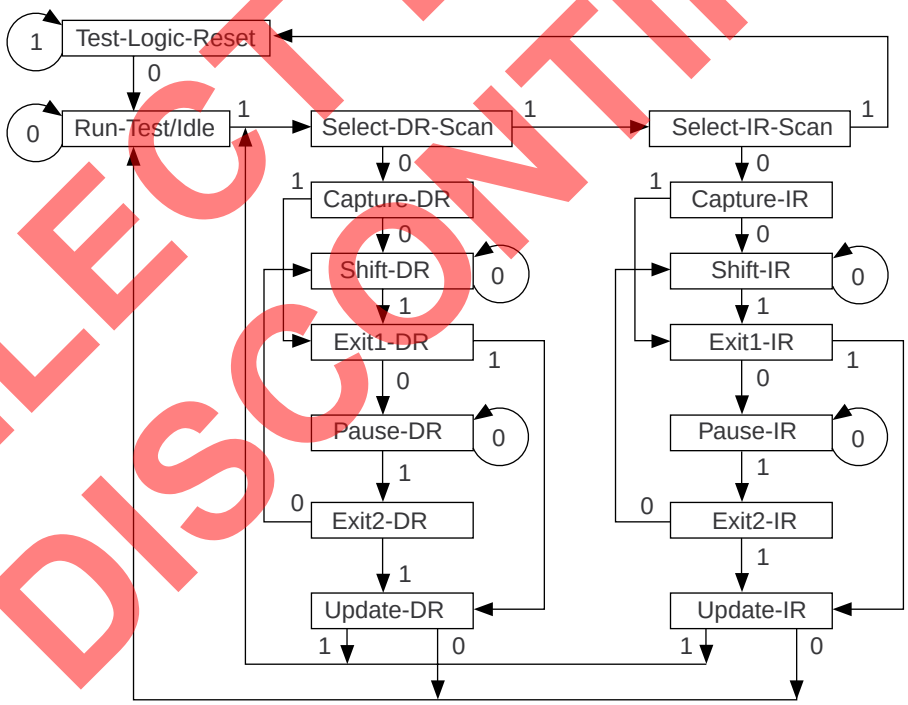
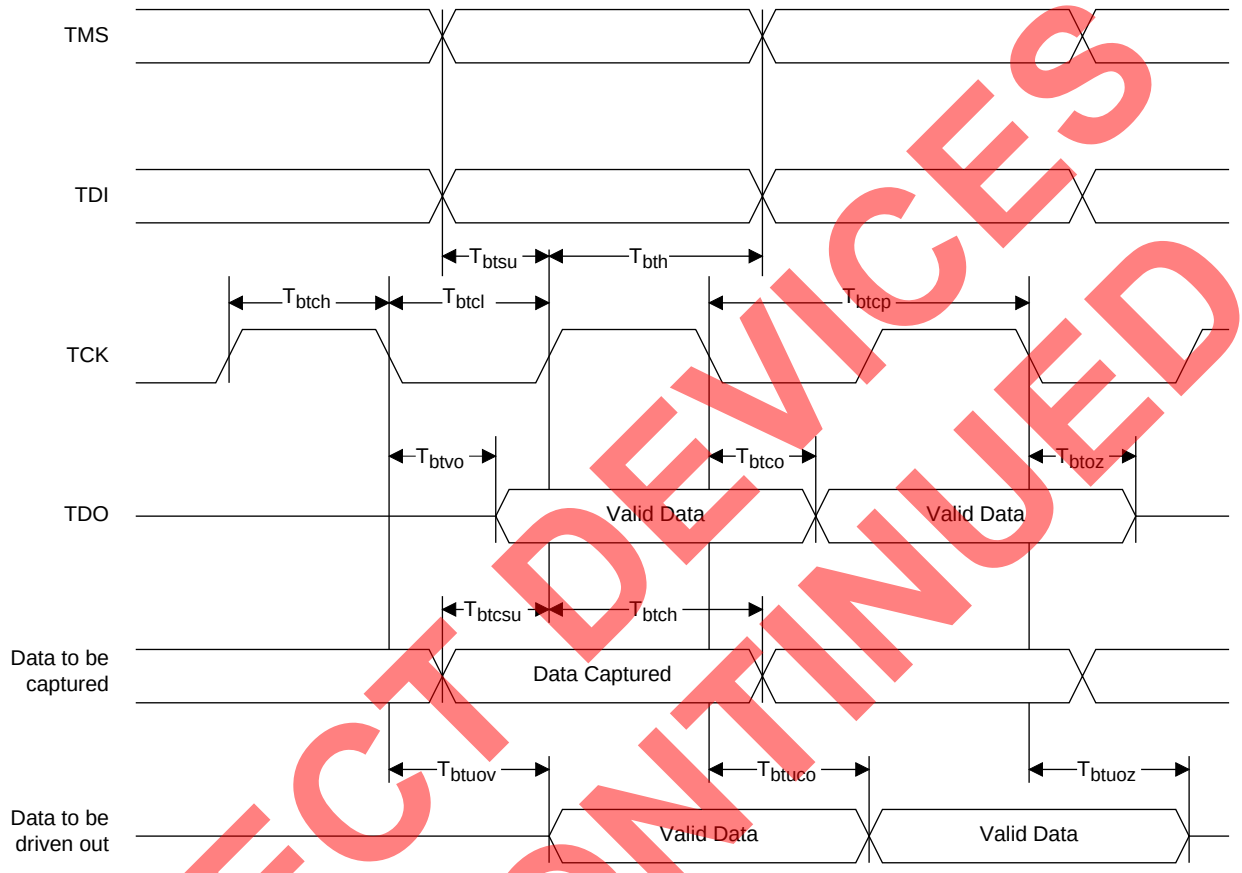


Figure 13. Boundary Scan Waveforms and Timing Specifications



Symbol	Parameter	Min	Max	Units
t_{btcp}	TCK [BSCAN test] clock pulse width	100	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	50	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	50	–	ns
t_{btsu}	TCK [BSCAN test] setup time	20	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsu}	BSCAN test Capture register setup time	20	–	ns
t_{btcph}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Signal Name	Description
I/O	Input/Output Pins – These are the general purpose bidirectional data pins. When used as outputs, each may be independently latched, registered or tristated. They can also each assume one other control function (OE, CLK/CLKEN, and MUXsel as described in the text).
TOE	Test Output Enable Pin – This pin tristates all I/P pins when a logic low is driven.
$\overline{\text{RESET}}$	Active LOW Input Pin – Resets all I/O register outputs when LOW.
Yx/CLKENx	Input Pins –These can be either Global Clocks or Clock Enables.
EPEN	Input Pin – JTAG TAP Controller Enable Pin. When high, JTAG operation is enabled. When low, JTAG TAP controller is driven to reset.
TDI	Input Pin – Serial data input during ISP programming or Boundary Scan mode.
TCK	Input Pin – Serial data clock during ISP programming or Boundary Scan mode.
TMS	Input Pin – Control input during ISP programming or Boundary Scan mode.
TDO	Output Pin – Serial data output during ISP programming or Boundary Scan mode.
GND	Ground (GND)
VCC	Vcc – Supply voltage (3.3V).
VCCIO[2]	Input – This pin is used if optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the VCC supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.
NC[1]	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.
2. "VA" version only.

Signal	208-Pin PQFP	208-Ball fpBGA	272-Ball BGA
TOE	178	D9	A12
$\overline{\text{RESET}}$	185	A8	D10
Y0/CLKEN0	75	N8	V10
Y1/CLKEN1	76	R8	Y10
Y2/CLKEN2	180	B9	C11
Y3/CLKEN3	181	C9	A11
EPEN	183	A9	B10
TDI	81	P9	Y12
TCK	80	T9	U11
TMS	79	T8	V11
TDO	78	P8	W11
GND	6, 15, 25, 35, 44, 54, 63, 77, 91, 100, 110, 119, 129, 139, 148, 159, 168, 182, 195, 204	D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, N4, N13	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	1, 17, 33, 49, 65, 89, 105, 121, 137, 153, 156[1], 170, 184, 193	E13[1], F4, F13, L4, L13, M4, M13, N5, N11, N12 D5, D6, D12, E4	C18[1], D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
VCCIO	156[1]	E13[1]	C18[1]
NC	73, 74, 179	A10, P7, T7	A2, A6, A7, A10, A15, A19, A20, B1, B2, B4, B11, B14, B18, B19, B20, C2, C3, C10, D2, D3, D16, E2, E17, E19, H1, H3, H18, H20, K20, L1, N1, N3, N18 N20, T2, T4, T19, U5, U18, U19, V3, V14, V18, V19, W1, W2, W3, W7, W10, W14, W19, W20, Y1, Y2, Y6, Y9, Y11, Y18, Y20

1. VCC on ispGDX160V, VCCIO on ispGDX160VA.

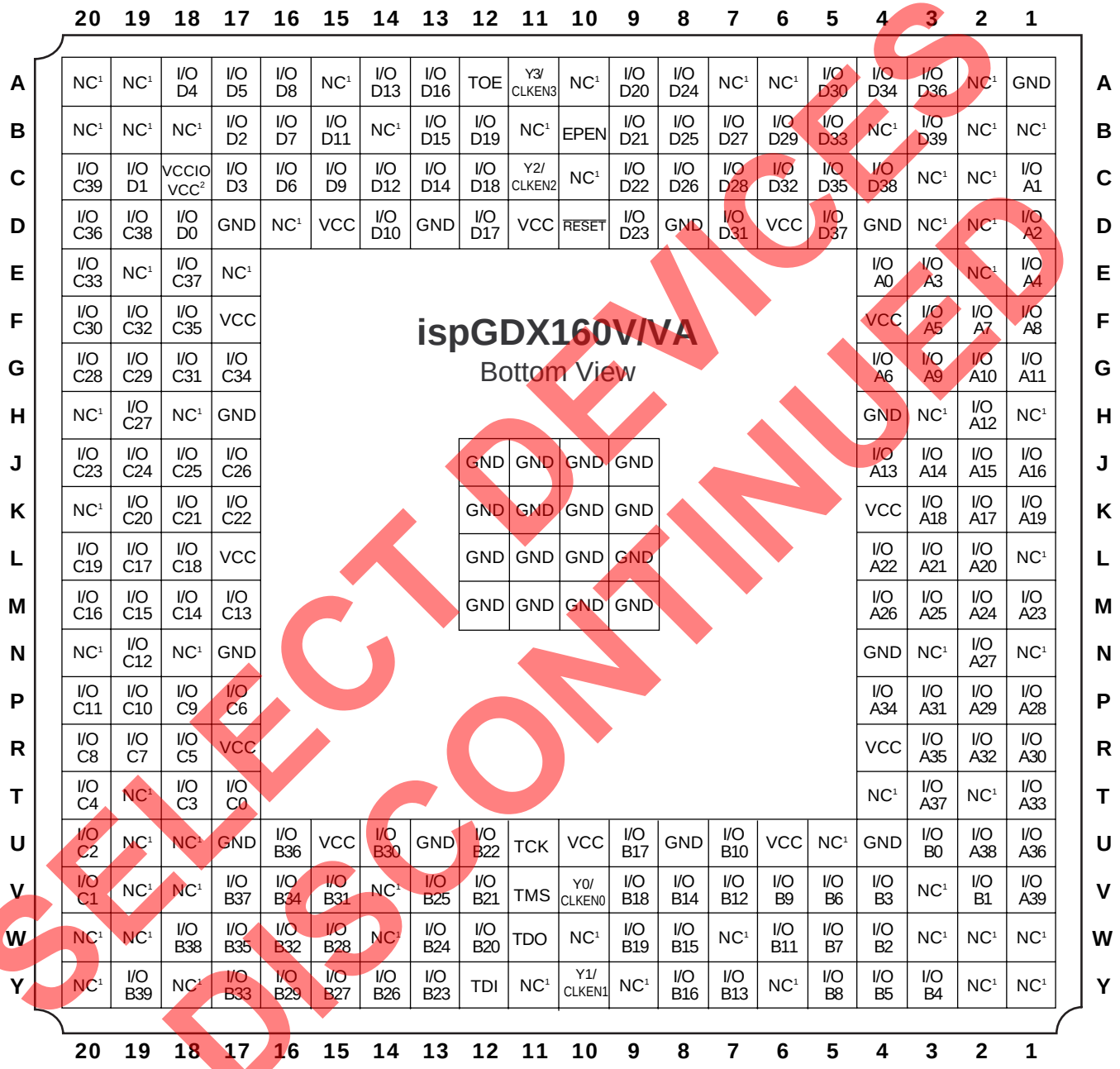
I/O Signal	Control Signal	208 PQFP	208 fpBGA	272 BGA
VCC				
I/O A0	CLK/CLKEN	2	B2	E4
I/O A1	OE	3	B1	C1
I/O A2	MUXsel1	4	C2	D1
I/O A3	MUXsel2	5	A1	E3
GND				
I/O A4	CLK/CLKEN	7	C1	E1
I/O A5	OE	8	D3	F3
I/O A6	MUXsel1	9	D2	G4
I/O A7	MUXsel2	10	D1	F2
I/O A8	CLK/CLKEN	11	E3	F1
I/O A9	OE	12	E2	G3
I/O A10	MUXsel1	13	E1	G2
I/O A11	MUXsel2	14	F3	G1
GND				
I/O A12	CLK/CLKEN	16	F2	H2
VCC				
I/O A13	OE	18	F1	J4
I/O A14	MUXsel1	19	G4	J3
I/O A15	MUXsel2	20	G2	J2
I/O A16	CLK/CLKEN	21	G3	J1
I/O A17	OE	22	G1	K2
I/O A18	MUXsel1	23	H4	K3
I/O A19	MUXsel2	24	H2	K1
GND				
I/O A20	CLK/CLKEN	26	H3	L2
I/O A21	OE	27	H1	L3
I/O A22	MUXsel1	28	J1	L4
I/O A23	MUXsel2	29	J3	M1
I/O A24	CLK/CLKEN	30	J2	M2
I/O A25	OE	31	J4	M3
I/O A26	MUXsel1	32	K1	M4
VCC				
I/O A27	MUXsel2	34	K3	N2
GND				
I/O A28	CLK/CLKEN	36	K2	P1
I/O A29	OE	37	K4	P2
I/O A30	MUXsel1	38	L1	R1
I/O A31	MUXsel2	39	L2	P3
I/O A32	CLK/CLKEN	40	L3	R2
I/O A33	OE	41	M1	T1
I/O A34	MUXsel1	42	M2	P4
I/O A35	MUXsel2	43	M3	R3
GND				
I/O A36	CLK/CLKEN	45	N1	U1
I/O A37	OE	46	N2	T3
I/O A38	MUXsel1	47	N3	U2
I/O A39	MUXsel2	48	P1	V1
VCC				
I/O B0	CLK/CLKEN	50	P2	U3
I/O B1	OE	51	R1	V2
I/O B2	MUXsel1	52	R2	W4
I/O B3	MUXsel2	53	T1	V4
GND				
I/O B4	CLK/CLKEN	55	P3	Y3
I/O B5	OE	56	T2	Y4
I/O B6	MUXsel1	57	R3	V5
I/O B7	MUXsel2	58	P4	W5
I/O B8	CLK/CLKEN	59	T3	Y5
I/O B9	OE	60	R4	V6
I/O B10	MUXsel1	61	T4	U7
I/O B11	MUXsel2	62	P5	W6
GND				
I/O B12	CLK/CLKEN	64	R5	V7
VCC				
I/O B13	OE	66	N6	Y7
I/O B14	MUXsel1	67	T5	V8
I/O B15	MUXsel2	68	R6	W8
I/O B16	CLK/CLKEN	69	P6	Y8
I/O B17	OE	70	T6	U9
I/O B18	MUXsel1	71	N7	V9
I/O B19	MUXsel2	72	R7	W9
GND				
I/O B20	CLK/CLKEN	82	R9	W12
I/O B21	OE	83	N9	V12
I/O B22	MUXsel1	84	T10	U12
I/O B23	MUXsel2	85	P10	Y13
I/O B24	CLK/CLKEN	86	R10	W13
I/O B25	OE	87	N10	V13
I/O B26	MUXsel1	88	T11	Y14
VCC				
I/O B27	MUXsel2	90	P11	Y15
GND				
I/O B28	CLK/CLKEN	92	R11	W15
I/O B29	OE	93	T12	Y16
I/O B30	MUXsel1	94	P12	U14
I/O B31	MUXsel2	95	R12	V15
I/O B32	CLK/CLKEN	96	T13	W16
I/O B33	OE	97	R13	Y17
I/O B34	MUXsel1	98	T14	V16
I/O B35	MUXsel2	99	P13	W17
GND				
I/O B36	CLK/CLKEN	101	R14	U16
I/O B37	OE	102	T15	V17
I/O B38	MUXsel1	103	T16	W18
I/O B39	MUXsel2	104	R15	Y19
VCC				
I/O C0	CLK/CLKEN	106	P14	T17
I/O C1	OE	107	P15	V20
I/O C2	MUXsel1	108	R16	U20
I/O C3	MUXsel2	109	N14	T18
GND				
I/O C4	CLK/CLKEN	111	P16	T20
I/O C5	OE	112	N15	R18
I/O C6	MUXsel1	113	N16	P17
I/O C7	MUXsel2	114	M14	R19
I/O C8	CLK/CLKEN	115	M15	R20
I/O C9	OE	116	M16	P18
I/O C10	MUXsel1	117	L15	P19
I/O C11	MUXsel2	118	L14	P20
GND				
I/O C12	CLK/CLKEN	120	L16	N19
VCC				
I/O C13	OE	122	K13	M17
I/O C14	MUXsel1	123	K15	M18
I/O C15	MUXsel2	124	K14	M19
I/O C16	CLK/CLKEN	125	K16	M20
I/O C17	OE	126	J13	L19
I/O C18	MUXsel1	127	J15	L18
I/O C19	MUXsel2	128	J14	L20
GND				
I/O C20	CLK/CLKEN	130	J16	K19
I/O C21	OE	131	H14	K18
I/O C22	MUXsel1	132	H16	K17
I/O C23	MUXsel2	133	H15	J20
I/O C24	CLK/CLKEN	134	H13	J19
I/O C25	OE	135	G16	J18
I/O C26	MUXsel1	136	G14	J17
VCC				
I/O C27	MUXsel2	138	G15	H19
GND				
I/O C28	CLK/CLKEN	140	G13	G20
I/O C29	OE	141	F16	G19
I/O C30	MUXsel1	142	F14	F20
I/O C31	MUXsel2	143	F15	G18
I/O C32	CLK/CLKEN	144	E16	F19
I/O C33	OE	145	E14	E20
I/O C34	MUXsel1	146	E15	G17
I/O C35	MUXsel2	147	D16	F18
GND				
I/O C36	CLK/CLKEN	149	C16	D20
I/O C37	OE	150	D15	E18
I/O C38	MUXsel1	151	D14	D19
I/O C39	MUXsel2	152	C15	C20
VCC				
I/O D0	CLK/CLKEN	154	B16	D18
I/O D1	OE	155	A16	C19
VCC/VCCIO[1]				
I/O D2	MUXsel1	157	B15	B17
I/O D3	MUXsel2	158	A15	C17
GND				
I/O D4	CLK/CLKEN	160	C14	A18
I/O D5	OE	161	B14	A17
I/O D6	MUXsel1	162	A14	C16
I/O D7	MUXsel2	163	C13	B16
I/O D8	CLK/CLKEN	164	B13	A16
I/O D9	OE	165	A13	C15
I/O D10	MUXsel1	166	C12	D14
I/O D11	MUXsel2	167	B12	B15
GND				
I/O D12	CLK/CLKEN	169	D11	C14
VCC				
I/O D13	OE	171	A12	A14
I/O D14	MUXsel1	172	C11	C13
I/O D15	MUXsel2	173	B11	B13
I/O D16	CLK/CLKEN	174	D10	A13
I/O D17	OE	175	A11	D12
I/O D18	MUXsel1	176	B10	C12
I/O D19	MUXsel2	177	C10	B12
GND				
VCC				
I/O D20	CLK/CLKEN	186	C8	A9
I/O D21	OE	187	B8	B9
I/O D22	MUXsel1	188	D8	C9
I/O D23	MUXsel2	189	A7	D9
I/O D24	CLK/CLKEN	190	C7	A8
I/O D25	OE	191	B7	B8
I/O D26	MUXsel1	192	D7	C8
VCC				
I/O D27	MUXsel2	194	A6	B7
GND				
I/O D28	CLK/CLKEN	196	C6	C7
I/O D29	OE	197	B6	B6
I/O D30	MUXsel1	198	A5	A5
I/O D31	MUXsel2	199	C5	D7
I/O D32	CLK/CLKEN	200	B5	C6
I/O D33	OE	201	A4	B5
I/O D34	MUXsel1	202	B4	A4
I/O D35	MUXsel2	203	C4	C5
GND				
I/O D36	CLK/CLKEN	205	A3	A3
I/O D37	OE	206	C3	D5
I/O D38	MUXsel1	207	B3	C4
I/O D39	MUXsel2	208	A2	B3

NOTE: VCC and GND Pads Shown for Reference, [1]VCC in ispGDX160V

I/O Signal	Control Signal	208 PQFP	208 fpBGA	272 BGA
I/O A3	MUXsel2	5	A1	E3
I/O D39	MUXsel2	208	A2	B3
I/O D36	CLK/CLKEN	205	A3	A3
I/O D33	OE	201	A4	B5
I/O D30	MUXsel1	198	A5	A5
I/O D27	MUXsel2	194	A6	B7
I/O D23	MUXsel2	189	A7	D9
I/O D17	OE	175	A11	D12
I/O D13	OE	171	A12	A14
I/O D9	OE	165	A13	C15
I/O D6	MUXsel1	162	A14	C16
I/O D3	MUXsel2	158	A15	C17
I/O D1	OE	155	A16	C19
I/O A1	OE	3	B1	C1
I/O A0	CLK/CLKEN	2	B2	E4
I/O D38	MUXsel1	207	B3	C4
I/O D34	MUXsel1	202	B4	A4
I/O D32	CLK/CLKEN	200	B5	C6
I/O D29	OE	197	B6	B6
I/O D25	OE	191	B7	B8
I/O D21	OE	187	B8	B9
I/O D18	MUXsel1	176	B10	C12
I/O D15	MUXsel2	173	B11	B13
I/O D11	MUXsel2	167	B12	B15
I/O D8	CLK/CLKEN	164	B13	A16
I/O D5	OE	161	B14	A17
I/O D2	MUXsel1	157	B15	B17
I/O D0	CLK/CLKEN	154	B16	D18
I/O A4	CLK/CLKEN	7	C1	E1
I/O A2	MUXsel1	4	C2	D1
I/O D37	OE	206	C3	D5
I/O D35	MUXsel2	203	C4	C5
I/O D31	MUXsel2	199	C5	D7
I/O D28	CLK/CLKEN	196	C6	C7
I/O D24	CLK/CLKEN	190	C7	A8
I/O D20	CLK/CLKEN	186	C8	A9
I/O D19	MUXsel2	177	C10	B12
I/O D14	MUXsel1	172	C11	C13
I/O D10	MUXsel1	166	C12	D14
I/O D7	MUXsel2	163	C13	B16
I/O D4	CLK/CLKEN	160	C14	A18
I/O C39	MUXsel2	152	C15	C20
I/O C36	CLK/CLKEN	149	C16	D20
I/O A7	MUXsel2	10	D1	F2
I/O A6	MUXsel1	9	D2	G4
I/O A5	OE	8	D3	F3
I/O D26	MUXsel1	192	D7	C8
I/O D22	MUXsel1	188	D8	C9
I/O D16	CLK/CLKEN	174	D10	A13
I/O D12	CLK/CLKEN	169	D11	C14
I/O C38	MUXsel1	151	D14	D19
I/O C37	OE	150	D15	E18
I/O C35	MUXsel2	147	D16	F18
I/O A10	MUXsel1	13	E1	G2
I/O A9	OE	12	E2	G3
I/O A8	CLK/CLK_EN	11	E3	F1
I/O C33	OE	145	E14	E20
I/O C34	MUXsel1	146	E15	G17
I/O C32	CLK/CLKEN	144	E16	F19
I/O A13	OE	18	F1	J4
I/O A12	CLK/CLKEN	16	F2	H2
I/O A11	MUXsel2	14	F3	G1
I/O C30	MUXsel1	142	F14	F20
I/O C31	MUXsel2	143	F15	G18
I/O C29	OE	141	F16	G19
I/O A17	OE	22	G1	K2
I/O A15	MUXsel2	20	G2	J2
I/O A16	CLK/CLKEN	21	G3	J1
I/O A14	MUXsel1	19	G4	J3
I/O C28	CLK/CLKEN	140	G13	G20
I/O C26	MUXsel1	136	G14	J17
I/O C27	MUXsel2	138	G15	H19
I/O C25	OE	135	G16	J18
I/O A21	OE	27	H1	L3
I/O A19	MUXsel2	24	H2	K1
I/O A20	CLK/CLKEN	26	H3	L2
I/O A18	MUXsel1	23	H4	K3
I/O C24	CLK/CLKEN	134	H13	J19
I/O C21	OE	131	H14	K18
I/O C23	MUXsel2	133	H15	J20
I/O C22	MUXsel1	132	H16	K17
I/O A22	MUXsel1	28	J1	L4
I/O A24	CLK/CLKEN	30	J2	M2
I/O A23	MUXsel2	29	J3	M1
I/O A25	OE	31	J4	M3
I/O C17	OE	126	J13	L19
I/O C19	MUXsel2	128	J14	L20
I/O C18	MUXsel1	127	J15	L18
I/O C20	CLK/CLKEN	130	J16	K19
I/O A26	MUXsel1	32	K1	M4
I/O A28	CLK/CLKEN	36	K2	P1
I/O A27	MUXsel2	34	K3	N2
I/O A29	OE	37	K4	P2
I/O C13	OE	122	K13	M17
I/O C15	MUXsel2	124	K14	M19
I/O C14	MUXsel1	123	K15	M18
I/O C16	CLK/CLKEN	125	K16	M20
I/O A30	MUXsel1	38	L1	R1
I/O A31	MUXsel2	39	L2	P3
I/O A32	CLK/CLKEN	40	L3	R2
I/O C11	MUXsel2	118	L14	P20
I/O C10	MUXsel1	117	L15	P19
I/O C12	CLK/CLKEN	120	L16	N19
I/O A33	OE	41	M1	T1
I/O A34	MUXsel1	42	M2	P4
I/O A35	MUXsel2	43	M3	R3
I/O C7	MUXsel2	114	M14	R19
I/O C8	CLK	115	M15	R20
I/O C9	OE	116	M16	P18
I/O A36	CLK/CLKEN	45	N1	U1
I/O A37	OE	46	N2	T3
I/O A38	MUXsel1	47	N3	U2
I/O B13	OE	66	N6	Y7
I/O B18	MUXsel1	71	N7	V9
I/O B21	OE	83	N9	V12
I/O B25	OE	87	N10	V13
I/O C3	MUXsel2	109	N14	T18
I/O C5	OE	112	N15	R18
I/O C6	MUXsel1	113	N16	P17
I/O A39	MUXsel2	48	P1	V1
I/O B0	CLK/CLKEN	50	P2	U3
I/O B4	CLK/CLKEN	55	P3	Y3
I/O B7	MUXsel2	58	P4	W5
I/O B11	MUXsel2	62	P5	W6
I/O B16	CLK/CLKEN	69	P6	Y8
I/O B23	MUXsel2	85	P10	Y13
I/O B27	MUXsel2	90	P11	Y15
I/O B30	MUXsel1	94	P12	U14
I/O B35	MUXsel2	99	P13	W17
I/O C0	CLK/CLKEN	106	P14	T17
I/O C1	OE	107	P15	V20
I/O C4	CLK/CLKEN	111	P16	T20
I/O B1	OE	51	R1	V2
I/O B2	MUXsel1	52	R2	W4
I/O B6	MUXsel1	57	R3	V5
I/O B9	OE	60	R4	V6
I/O B12	CLK/CLKEN	64	R5	V7
I/O B15	MUXsel2	68	R6	W8
I/O B19	MUXsel2	72	R7	W9
I/O B20	CLK/CLKEN	82	R9	W12
I/O B24	CLK/CLKEN	86	R10	W13
I/O B28	CLK/CLKEN	92	R11	W15
I/O B31	MUXsel2	95	R12	V15
I/O B33	OE	97	R13	Y17
I/O B36	CLK/CLKEN	101	R14	U16
I/O B39	MUXsel2	104	R15	Y19
I/O C2	MUXsel1	108	R16	U20
I/O B3	MUXsel2	53	T1	V4
I/O B5	OE	56	T2	Y4
I/O B8	CLK/CLKEN	59	T3	Y5
I/O B10	MUXsel1	61	T4	U7
I/O B14	MUXsel1	67	T5	V8
I/O B17	OE	70	T6	U9
I/O B22	MUXsel1	84	T10	U12
I/O B26	MUXsel1	88	T11	Y14
I/O B29	OE	93	T12	Y16
I/O B32	CLK/CLKEN	96	T13	W16
I/O B34	MUXsel1	98	T14	V16
I/O B37	OE	102	T15	V17
I/O B38	MUXsel1	103	T16	W18

I/O Signal	Control Signal	208 PQFP	208 fpBGA	272 BGA
I/O D36	CLK/CLKEN	205	A3	A3
I/O D34	MUXsel1	202	B4	A4
I/O D30	MUXsel1	198	A5	A5
I/O D24	CLK/CLKEN	190	C7	A8
I/O D20	CLK/CLKEN	186	C8	A9
I/O D16	CLK/CLKEN	174	D10	A13
I/O D13	OE	171	A12	A14
I/O D8	CLK/CLKEN	164	B13	A16
I/O D5	OE	161	B14	A17
I/O D4	CLK/CLKEN	160	C14	A18
I/O D39	MUXsel2	208	A2	B3
I/O D33	OE	201	A4	B5
I/O D29	OE	197	B6	B6
I/O D27	MUXsel2	194	A6	B7
I/O D25	OE	191	B7	B8
I/O D21	OE	187	B8	B9
I/O D19	MUXsel2	177	C10	B12
I/O D15	MUXsel2	173	B11	B13
I/O D11	MUXsel2	167	B12	B15
I/O D7	MUXsel2	163	C13	B16
I/O D2	MUXsel1	157	B15	B17
I/O A1	OE	3	B1	C1
I/O D38	MUXsel1	207	B3	C4
I/O D35	MUXsel2	203	C4	C5
I/O D32	CLK/CLKEN	200	B5	C6
I/O D28	CLK/CLKEN	196	C6	C7
I/O D26	MUXsel1	192	D7	C8
I/O D22	MUXsel1	188	D8	C9
I/O D18	MUXsel1	176	B10	C12
I/O D14	MUXsel1	172	C11	C13
I/O D12	CLK/CLKEN	169	D11	C14
I/O D9	OE	165	A13	C15
I/O D6	MUXsel1	162	A14	C16
I/O D3	MUXsel2	158	A15	C17
I/O D1	OE	155	A16	C19
I/O C39	MUXsel2	152	C15	C20
I/O A2	MUXsel1	4	C2	D1
I/O D37	OE	206	C3	D5
I/O D31	MUXsel2	199	C5	D7
I/O D23	MUXsel2	189	A7	D9
I/O D17	OE	175	A11	D12
I/O D10	MUXsel1	166	C12	D14
I/O D0	CLK/CLKEN	154	B16	D18
I/O C38	MUXsel1	151	D14	D19
I/O C36	CLK/CLKEN	149	C16	D20
I/O A4	CLK/CLK_EN	7	C1	E1
I/O A3	MUXsel2	5	A1	E3
I/O A0	CLK/CLKEN	2	B2	E4
I/O C37	OE	150	D15	E18
I/O C33	OE	145	E14	E20
I/O A8	CLK/CLKEN	11	E3	F1
I/O A7	MUXsel2	10	D1	F2
I/O A5	OE	8	D3	F3
I/O C35	MUXsel2	147	D16	F18
I/O C32	CLK/CLKEN	144	E16	F19
I/O C30	MUXsel1	142	F14	F20
I/O A11	MUXsel2	14	F3	G1
I/O A10	MUXsel1	13	E1	G2
I/O A9	OE	12	E2	G3
I/O A6	MUXsel1	9	D2	G4
I/O C34	MUXsel1	146	E15	G17
I/O C31	MUXsel2	143	F15	G18
I/O C29	OE	141	F16	G19
I/O C28	CLK/CLKEN	140	G13	G20
I/O A12	CLK/CLKEN	16	F2	H2
I/O C27	MUXsel2	138	G15	H19
I/O A16	CLK/CLKEN	21	G3	J1
I/O A15	MUXsel2	20	G2	J2
I/O A14	MUXsel1	19	G4	J3
I/O A13	OE	18	F1	J4
I/O C26	MUXsel1	136	G14	J17
I/O C25	OE	135	G16	J18
I/O C24	CLK/CLKEN	134	H13	J19
I/O C23	MUXsel2	133	H15	J20
I/O A19	MUXsel2	24	H2	K1
I/O A17	OE	22	G1	K2
I/O A18	MUXsel1	23	H4	K3
I/O C22	MUXsel1	132	H16	K17
I/O C21	OE	131	H14	K18
I/O C20	CLK/CLKEN	130	J16	K19
I/O A20	CLK/CLKEN	26	H3	L2
I/O A21	OE	27	H1	L3
I/O A22	MUXsel1	28	J1	L4
I/O C18	MUXsel1	127	J15	L18
I/O C17	OE	126	J13	L19
I/O C19	MUXsel2	128	J14	L20
I/O A23	MUXsel2	29	J3	M1
I/O A24	CLK/CLKEN	30	J2	M2
I/O A25	OE	31	J4	M3
I/O A26	MUXsel1	32	K1	M4
I/O C13	OE	122	K13	M17
I/O C14	MUXsel1	123	K15	M18
I/O C15	MUXsel2	124	K14	M19
I/O C16	CLK/CLKEN	125	K16	M20
I/O A27	MUXsel2	34	K3	N2
I/O C12	CLK/CLKEN	120	L16	N19
I/O A28	CLK/CLKEN	36	K2	P1
I/O A29	OE	37	K4	P2
I/O A31	MUXsel2	39	L2	P3
I/O A34	MUXsel1	42	M2	P4
I/O C6	MUXsel1	113	N16	P17
I/O C9	OE	116	M16	P18
I/O C10	MUXsel1	117	L15	P19
I/O C11	MUXsel2	118	L14	P20
I/O A30	MUXsel1	38	L1	R1
I/O A32	CLK/CLKEN	40	L3	R2
I/O A35	MUXsel2	43	M3	R3
I/O C5	OE	112	N15	R18
I/O C7	MUXsel2	114	M14	R19
I/O C8	CLK	115	M15	R20
I/O A33	OE	41	M1	T1
I/O A37	OE	46	N2	T3
I/O C0	CLK/CLKEN	106	P14	T17
I/O C3	MUXsel2	109	N14	T18
I/O C4	CLK/CLKEN	111	P16	T20
I/O A36	CLK/CLKEN	45	N1	U1
I/O A38	MUXsel1	47	N3	U2
I/O B0	CLK/CLKEN	50	P2	U3
I/O B10	MUXsel1	61	T4	U7
I/O B17	OE	70	T6	U9
I/O B22	MUXsel1	84	T10	U12
I/O B30	MUXsel1	94	P12	U14
I/O B36	CLK/CLKEN	101	R14	U16
I/O C2	MUXsel1	108	R16	U20
I/O A39	MUXsel2	48	P1	V1
I/O B1	OE	51	R1	V2
I/O B3	MUXsel2	53	T1	V4
I/O B6	MUXsel1	57	R3	V5
I/O B9	OE	60	R4	V6
I/O B12	CLK/CLKEN	64	R5	V7
I/O B14	MUXsel1	67	T5	V8
I/O B18	MUXsel1	71	N7	V9
I/O B21	OE	83	N9	V12
I/O B25	OE	87	N10	V13
I/O B31	MUXsel2	95	R12	V15
I/O B34	MUXsel1	98	T14	V16
I/O B37	OE	102	T15	V17
I/O C1	OE	107	P15	V20
I/O B2	MUXsel1	52	R2	W4
I/O B7	MUXsel2	58	P4	W5
I/O B11	MUXsel2	62	P5	W6
I/O B15	MUXsel2	68	R6	W8
I/O B19	MUXsel2	72	R7	W9
I/O B20	CLK/CLKEN	82	R9	W12
I/O B24	CLK/CLKEN	86	R10	W13
I/O B28	CLK/CLKEN	92	R11	W15
I/O B32	CLK/CLKEN	96	T13	W16
I/O B35	MUXsel2	99	P13	W17
I/O B38	MUXsel1	103	T16	W18
I/O B4	CLK/CLKEN	55	P3	Y3
I/O B5	OE	56	T2	Y4
I/O B8	CLK/CLKEN	59	T3	Y5
I/O B13	OE	66	N6	Y7
I/O B16	CLK/CLKEN	69	P6	Y8
I/O B23	MUXsel2	85	P10	Y13
I/O B26	MUXsel1	88	T11	Y14
I/O B27	MUXsel2	90	P11	Y15
I/O B29	OE	93	T12	Y16
I/O B33	OE	97	R13	Y17
I/O B39	MUXsel2	104	R15	Y19

ispGDX160V/VA 272-Ball BGA Signal Diagram



1. NCs are not to be connected to any active signals, Vcc or GND.
2. VCCIO on ispGDX160VA. VCC on ispGDX160V.

ispGDX160V/VA 208-Ball fpBGA Signal Diagram

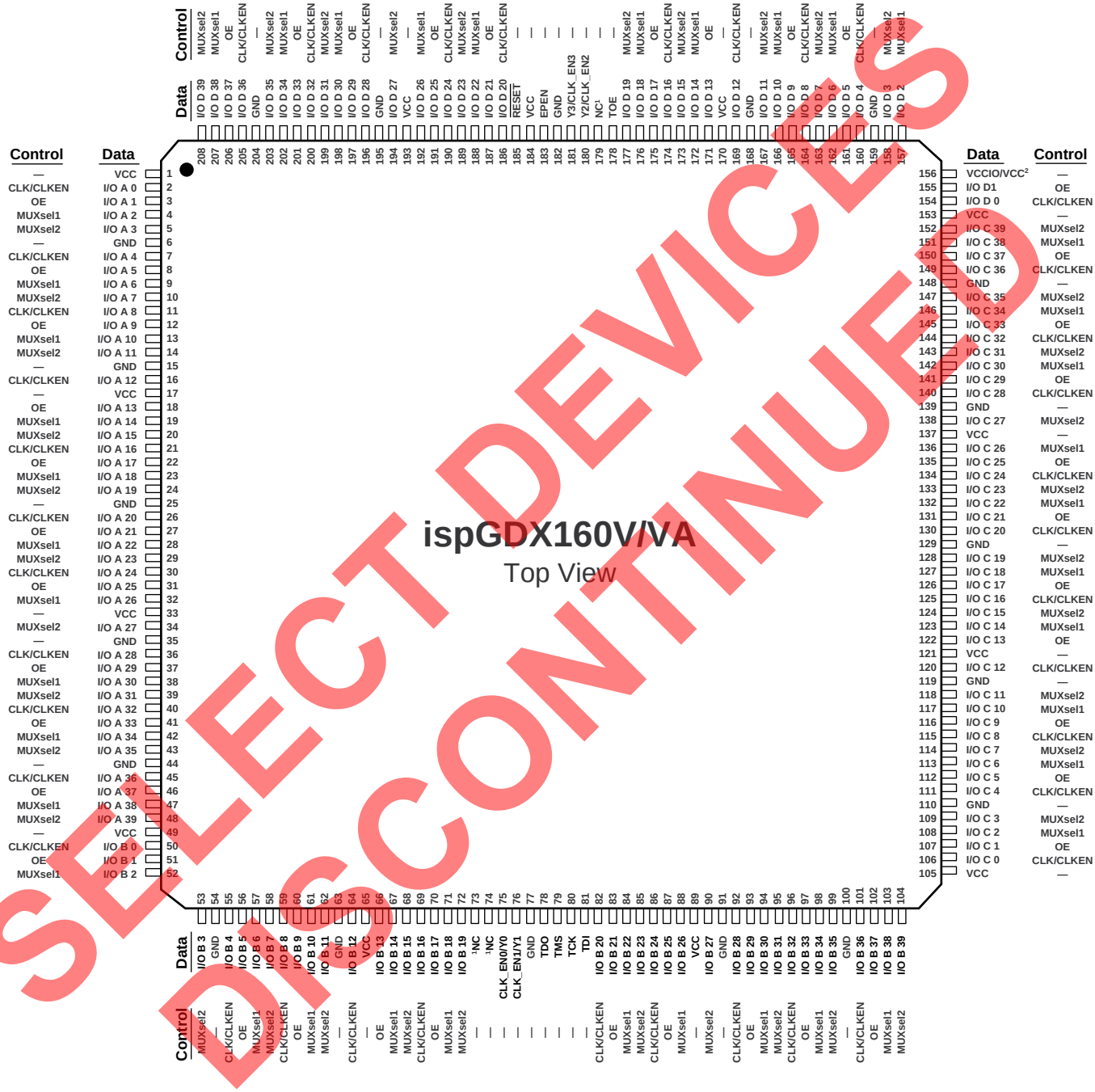
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O D1	I/O D3	I/O D6	I/O D9	I/O D13	I/O D17	NC [1]	EPEN	$\overline{\text{RESET}}$	I/O D23	I/O D27	I/O D30	I/O D33	I/O D36	I/O D39	I/O A3	A
B	I/O D0	I/O D2	I/O D5	I/O D8	I/O D11	I/O D15	I/O D18	Y2/ CLKEN2	I/O D21	I/O D25	I/O D29	I/O D32	I/O D34	I/O D38	I/O A0	I/O A1	B
C	I/O C36	I/O C39	I/O D4	I/O D7	I/O D10	I/O D14	I/O D19	Y3/ CLKEN3	I/O D20	I/O D24	I/O D28	I/O D31	I/O D35	I/O D37	I/O A2	I/O A4	C
D	I/O C35	I/O C37	I/O C38	GND	VCC	I/O D12	I/O D16	TOE	I/O D22	I/O D26	VCC	VCC	GND	I/O A5	I/O A6	I/O A7	D
E	I/O C32	I/O C34	I/O C33	VCCIO/ VCC [2]									VCC	I/O A8	I/O A9	I/O A10	E
F	I/O C29	I/O C31	I/O C30	VCC									VCC	I/O A11	I/O A12	I/O A13	F
G	I/O C25	I/O C27	I/O C26	I/O C28			GND	GND	GND	GND			I/O A14	I/O A16	I/O A15	I/O A17	G
H	I/O C22	I/O C23	I/O C21	I/O C24			GND	GND	GND	GND			I/O A18	I/O A20	I/O A19	I/O A21	H
J	I/O C20	I/O C18	I/O C19	I/O C17			GND	GND	GND	GND			I/O A25	I/O A23	I/O A24	I/O A22	J
K	I/O C16	I/O C14	I/O C15	I/O C13			GND	GND	GND	GND			I/O A29	I/O A27	I/O A28	I/O A26	K
L	I/O C12	I/O C10	I/O C11	VCC									VCC	I/O A32	I/O A31	I/O A30	L
M	I/O C9	I/O C8	I/O C7	VCC									VCC	I/O A35	I/O A34	I/O A33	M
N	I/O C6	I/O C5	I/O C3	GND	VCC	VCC	I/O B25	I/O B21	Y0/ CLKEN0	I/O B18	I/O B13	VCC	GND	I/O A38	I/O A37	I/O A36	N
P	I/O C4	I/O C1	I/O C0	I/O B35	I/O B30	I/O B27	I/O B23	TDI	TDO	NC [1]	I/O B16	I/O B11	I/O B7	I/O B4	I/O B0	I/O A39	P
R	I/O C2	I/O B39	I/O B36	I/O B33	I/O B31	I/O B28	I/O B24	I/O B20	Y1/ CLKEN1	I/O B19	I/O B15	I/O B12	I/O B9	I/O B6	I/O B2	I/O B1	R
T	I/O B38	I/O B37	I/O B34	I/O B32	I/O B29	I/O B26	I/O B22	TCK	TMS	NC [1]	I/O B17	I/O B14	I/O B10	I/O B8	I/O B5	I/O B3	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispGDX160V/VA

Bottom View

1. NCs are not to be connected to any active signals, Vcc or GND.
2. VCCIO on ispGDX160VA. VCC on ispGDX160V.

ispGDX160V/VA 208-Pin PQFP Pinout Diagram



1. No Connect Pins (NC) are not to be connected to any active signal, Vcc or GND.
2. VCCIO on ispGDX160VA. VCC on ispGDX160V.

ispGDX XXXXX - X XXXXX X

Device Family

Device Number
160V
160VA

Speed
3 = 3.5ns Tpd
5 = 5ns Tpd
7 = 7ns Tpd
9 = 9ns Tpd

Grade
Blank = Commercial
I = Industrial

Package
Q208 = 208-Pin PQFP
B208 = 208-Ball fpBGA
BN208 = Lead-Free 208-Ball fpBGA
B272 = 272-Ball BGA

0212/ispGDXVA

Conventional Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	3.5	ispGDX160VA-3Q208	208-Pin PQFP
	3.5	ispGDX160VA-3B208	208-Ball fpBGA
	3.5	ispGDX160VA-3B272	272-Ball BGA
	5	ispGDX160VA-5Q208	208-Pin PQFP
	5	ispGDX160VA-5B208	208-Ball fpBGA
	5	ispGDX160VA-5B272	272-Ball BGA
	7	ispGDX160VA-7Q208	208-Pin PQFP
	7	ispGDX160VA-7B208	208-Ball fpBGA
	7	ispGDX160VA-7B272	272-Ball BGA
ispGDXV*	5	ispGDX160V-5Q208	208-Pin PQFP
	5	ispGDX160V-5B208	208-Ball fpBGA
	5	ispGDX160V-5B272	272-Ball BGA
	7	ispGDX160V-7Q208	208-Pin PQFP
	7	ispGDX160V-7B208	208-Ball fpBGA
	7	ispGDX160V-7B272	272-Ball BGA

Table 2-0041A/ispGDXV/A

*Use ispGDX160VA for new designs.
Note: The ispGDX160VA devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, e.g. ispGDX160VA-3B208-5I.

Conventional Packaging (Cont.)

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	5	ispGDX160VA-5Q208I	208-Pin PQFP
	5	ispGDX160VA-5B208I	208-Ball fpBGA
	5	ispGDX160VA-5B272I	272-Ball BGA
	7	ispGDX160VA-7Q208I	208-Pin PQFP
	7	ispGDX160VA-7B208I	208-Ball fpBGA
	7	ispGDX160VA-7B272I	272-Ball BGA
	9	ispGDX160VA-9Q208I	208-Pin PQFP
	9	ispGDX160VA-9B208I	208-Ball fpBGA
	9	ispGDX160VA-9B272I	272-Ball BGA
ispGDXV*	7	ispGDX160V-7Q208I	208-Pin PQFP

*Use ispGDX160VA for new designs.

Table 2-0041C/ispGDXV

Note: The ispGDX160VA devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, e.g. ispGDX160VA-3B208-5I.

Lead-Free Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	3.5	ispGDX160VA-3BN208	Lead-Free 208-Ball fpBGA
	5	ispGDX160VA-5BN208	Lead-Free 208-Ball fpBGA
	7	ispGDX160VA-7BN208	Lead-Free 208-Ball fpBGA

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	5	ispGDX160VA-5BN208I	Lead-Free 208-Ball fpBGA
	7	ispGDX160VA-7BN208I	Lead-Free 208-Ball fpBGA
	9	ispGDX160VA-9BN208I	Lead-Free 208-Ball fpBGA

Note: The ispGDX160VA devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, e.g. ispGDX160VA-3B208-5I.