TEXAS INSTRUMENTS

TPS79301EVM
TPS79328EVM

LDO Linear Regulator Evaluation Module

User's Guide

June 2002 *Power Management Products Low Power*

SLVU060A

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DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7–5.5 V and the output current range of 0 mA to 200 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the TPS793xxEVM LDO regulator evaluation module (SLVP191). Each EVM package contains one SLVP191 test board, with either a TPS79301DBV linear regulator or a TPS79328DBV linear regulator, as well as supporting passive components. The SLVP191 test board provides a convenient method of evaluating the performance of the TPS793xx linear regulator family as well as other SOT–23 packaged linear regulators with the same pinout.

How to Use This Manual

- Chapter 1—Introduction
- Chapter 2—EVM Test Setup
- Chapter 3—Test Results

Related Documentation From Texas Instruments

- TPS793xx data sheet (literature number SLVS348)

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Chapter 1

Introduction

This user's guide describes the TPS793xxEVM LDO regulator evaluation module (SLVP191). Each EVM package contains one SLVP191 test board, with either a TPS79301DBV linear regulator or a TPS79328DBV linear regulator, as well as supporting passive components.

Topic **Page**

1.1 TPS793xx Family of LDO Regulators

Like all LDO linear regulators, the TPS793xx family of LDO regulators use a series pass element and feedback network, including an error amplifier and voltage reference, to provide a regulated output voltage from a slightly higher, possibly varying input voltage. However, these regulators have been optimized to reduce ripple and noise on the output. For example, advanced feedback compensation techniques were used to increase the bandwidth and open loop gain of the feedback network while maintaining stability with any 2.2-μF ceramic capacitor. Since PSRR is directly proportional to the frequency response of the loop of the error amplifier, these regulators' higher loop gain and larger bandwidth result in better PSRR over a wider range of frequencies than standard regulators. In addition to circuit design optimization to reduce circuit noise, the primary contributor to the noise of any regulator, the bandgap reference, has been pinned out to allow further noise reduction through the use of a filtering capacitor. Capabilities of this regulator include:

- 200-mA load current
- TPS793xx family is available in 1.8-V, 2.5 V, 2.8 V, 2.85 V, 3.0 V, 3.3-V, 4.75-V, and adjustable with positive ENABLE.
- PSRR of 75 dB at 10 kHz
- Approximately 30-μV output noise
- Start-up in approximately 60 μs
- Excellent line and load transient responses
- Very low dropout voltage
- 5-Pin SOT23 (DBV) package to minimize board space consumption

1.2 EVM Design Strategy

The purpose of this EVM is to facilitate evaluation of the TPS793xx family of LDO regulators. Each EVM package contains one SLVP191 test board, with either a TPS79301DBV linear regulator or a TPS79328DBV linear regulator, as well as supporting passive components. The TPS79301DBV adjustable device has been configured to provide 1.5-V output, and the TPS79328DBV provides a 2.8-V output. The board's small size and side clips facilitate attaching it to other PCBs as a power module.

The board has additional passive components that can be configured to test other SOT–23 packaged regulators with the same pin-out.

1.3 Schematic

Figures 1–1 and 1–2 show the SLVP191 schematic diagram that is used in the TPS793xxEVM.

Figure 1–1. TPS79301 Board Schematic

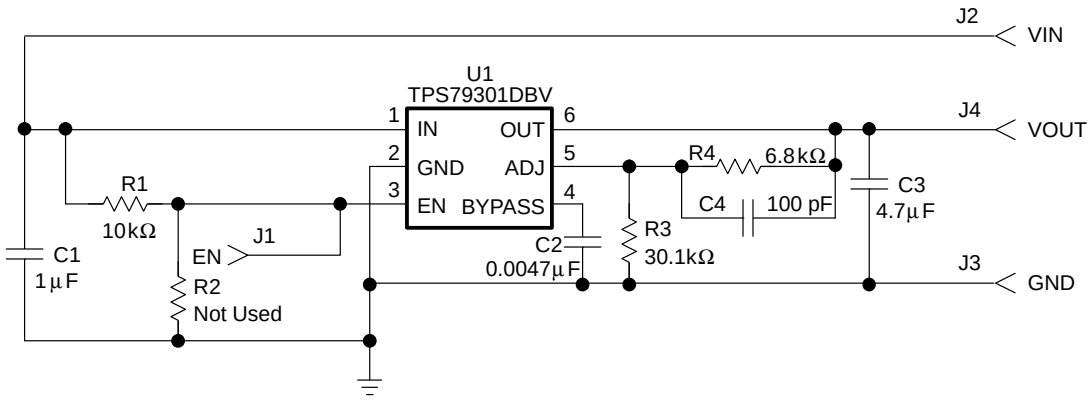
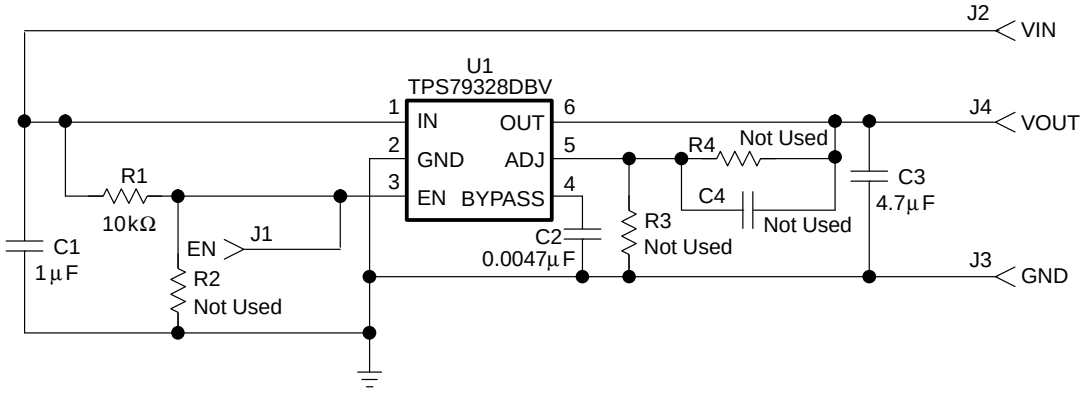


Figure 1–2. TPS79328 Board Schematic



1.4 Bill of Materials

Table 1–2 lists materials required for the SLVP191

Table 1–1. SLVP191 Bill of Materials

79301	79328	Ref Des	Description	Size	MFR	Part Number
1	1	C1	Capacitor, ceramic, 1.0 µF, 6.3 V, 10%	603	Murata	GRM39X7R105K6.3
1	1	C2	Capacitor, ceramic, 0.0047 µF, . . . 25 V, X7R, 10%	603	Murata	GRM39X7R472K25
1	1	C3	Capacitor, ceramic, 4.7 µF, 16 V, X5R, 15%	1206	Murata	GRM42–6X5R475K16
1		C4	Capacitor, ceramic, 100 pF, 50 V, C0G, 5%	603	Murata	GRM39C0G101J50
	0		Not used			
1	1	J1	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA–D36W–0FC
1	1	J2	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA–D36W–0FC
1	1	J3	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA–D36W–0FC
1	1	J4	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA–D36W–0FC
1	1	R1	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
0	0	R2	Not used			
1		R3	Resistor, chip, 30.1 kΩ,, 1/16 W, 1%	603	Std	Std
	0		Not used			
1		R4	Resistor, chip, 6.8 kΩ,, 1/16 W, 1%	603	Std	Std
	0		Not used			
1		U1	IC, high PSRR, low noise LDO, adj output, 100 mA	SOT23–6	TI	TPS79301DBV
	1		IC, high PSRR, low noise LDO, 2.8 V, 200 mA	SOT23–5	TI	TPS79328DBV
1	1		PCB, 0.705 in × 0.570 in × 0.031		Any	SLVP191

1.5 Board Layout

Figures 1–3 and 1–4 show the board layout for the TPS793xxEVM.

Figure 1–3. Top Layer

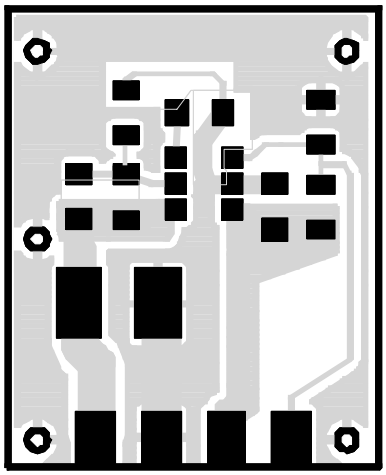


Figure 1–4. Bottom Layer

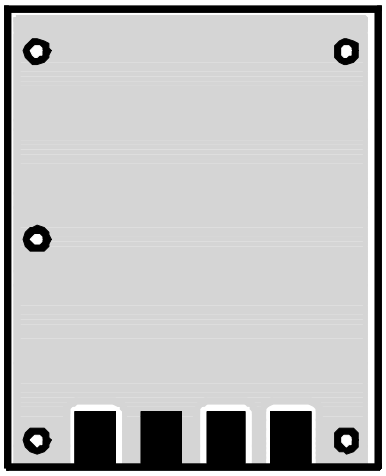
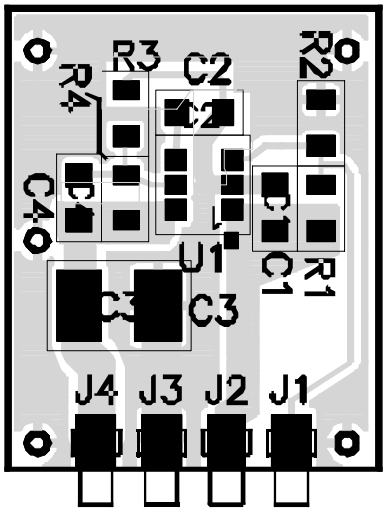


Figure 1–5. Assembly Drawing—Top

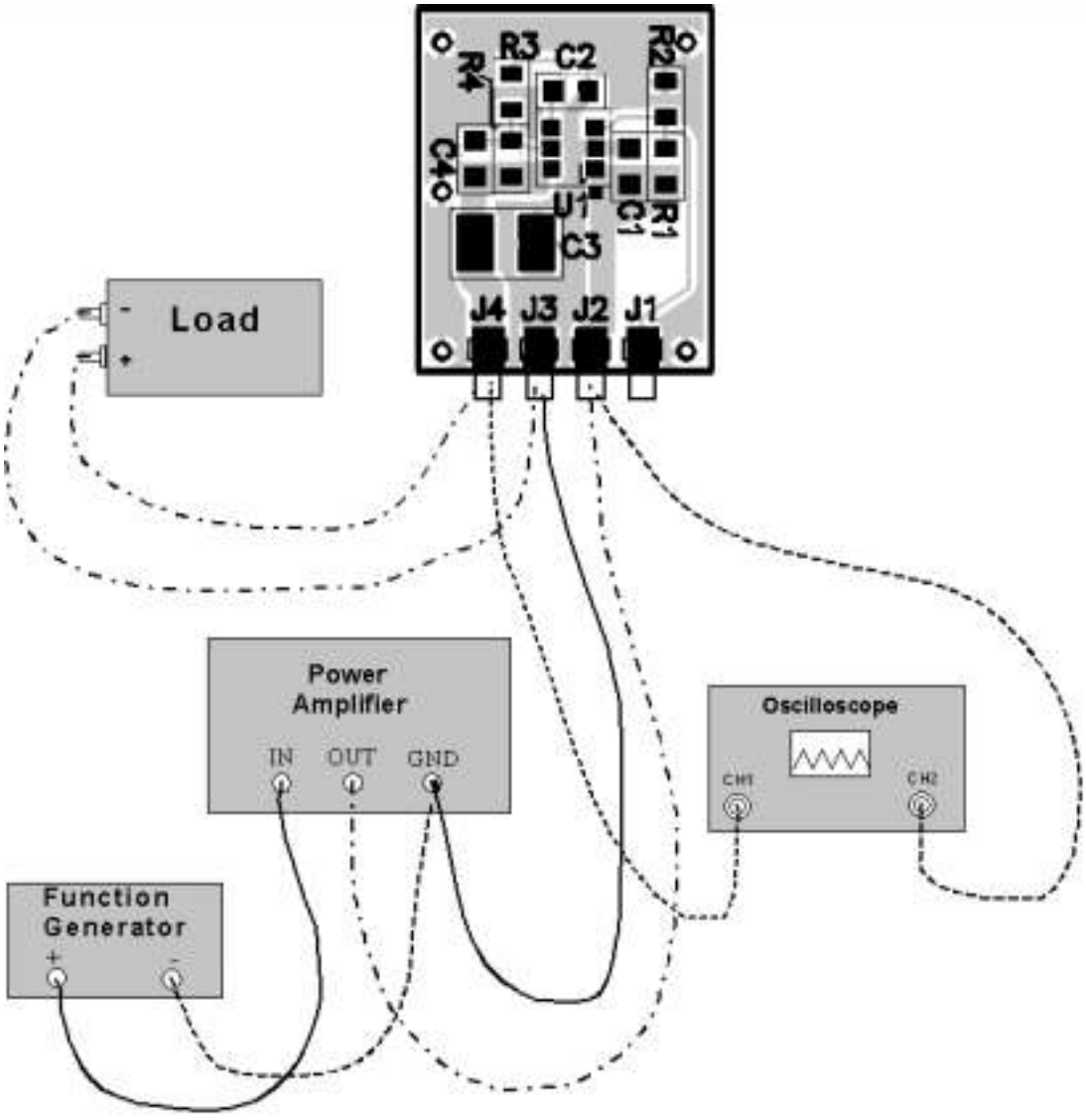


Chapter 2

EVM Test Setup

This chapter provides recommended test equipment and procedures for performing evaluations using the TPS793xxEVM. Figure 2–1 shows the test setup.

Figure 2–1. Recommended TPS793xxEVM Test Setup



The settings for the test equipment shown in Figure 2–1 are described below:

- Power amplifier capable of dv/dt = 1 V/μs and with at least 1-A current limit connected to IN (J2) and GND (J3).
- Function generator capable of generating both a 10-kHz, 1-V_{PP}, sine wave and a 1-V square wave connected to the input of the power amplifier.
- Oscilloscope with channel 1 connected to IN (J2), and channel 2 connected to OUT (J3). Set the oscilloscope to trigger off of the rising edge of channel 1 of the oscilloscope.
- Appropriately sized resistance for desired output current between OUT (J4) and GND (J3).

Powering up the device, the power amplifier, and function generator results in oscilloscope plots similar to those in Chapter 3.

Chapter 3

Test Results

This chapter provides laboratory test results of the TPS793xxEVM.

Figure 3–1 shows the line transient response of the TPS79328DBV device. The input voltage is set to 3.8 V and then a 1-V step is applied. The output load is 100 mA. Channel 1 is V_I. Channel 2 is V_O, ac-coupled.

Figure 3–1. Line Transient Response

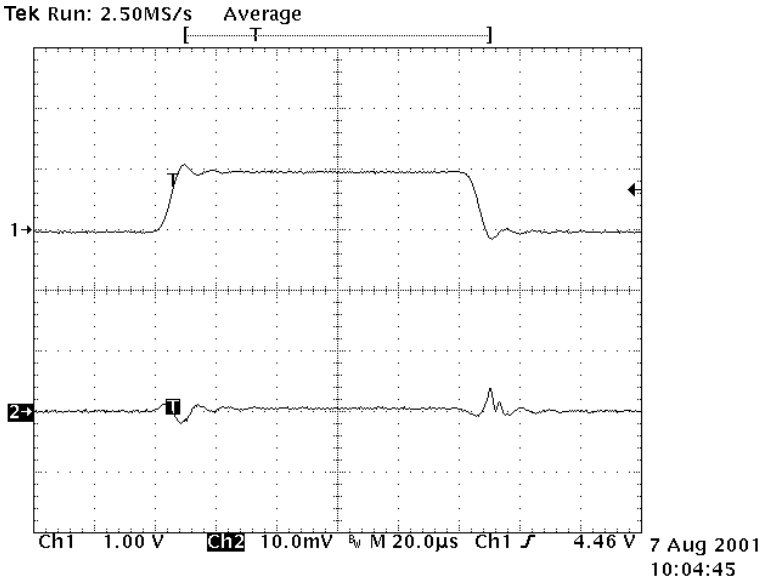


Figure 3–2 shows the ripple rejection capabilities of the TPS79328DBV device. The input voltage is set to 5 V and a 1-V_{PP} sine wave is added to the input dc voltage. The output load is 100 mA. Channel 1 is V_I. Channel 2 is V_O. Both are ac-coupled.

Figure 3–2. Ripple Rejection