SON8-P-0303-0.65A

Weight: 0.017 g (typ.)

Toshiba BiCD Integrated Circuit Silicon Monolithic

TB7102AF

Buck DC-DC Converter IC

The TB7102AF is a single-chip buck DC-DC converter IC. The TB7102AF contains high-speed and low-on-resistance power MOSFETs for the main switch and synchronous rectifier to achieve high efficiency.

Features

- Enables up to 1 A of load current (IOUT) with a minimum of external components.
- High efficiency ($\eta = 95\%$ typ.) (@VIN = 5 V, VOUT = 3.3 V and IOUT = 300 mA)
- Operating voltage (VIN) range: 2.7 V to 5.5 V
- A high 1-MHz oscillation frequency (typ.) allows the use of small external components.
- · Uses internal phase compensation to achieve high efficiency with a minimum of external components.
- Allows the use of a small surface-mount ceramic capacitor as an output filter capacitor.
- Enable threshold voltage : $V_{IH(EN)} = 1.5 \text{ V}$, $V_{IL(EN)} = 0.5 \text{ V} (@V_{IN} = 5 \text{ V})$
- Housed in a small surface-mount package (PS-8) with low thermal resistance.
- Undervoltage lockout (UVLO), thermal shutdown (TSD) and overcurrent protection (OCP)

Pin Assignment Part Marking Part Number (Abbrev.) N.C. N.C. V_{FB} 8 6 5 Lot No. 7102 3 4 The dot (•) on the top surface indicates pin 1. **PGND** V_{IN} **SGND**

*: The lot number consists of three digits. The first digit represents the last digit of the year of manufacture, and the following two digits indicates the week of manufacture between 01 and either 52 or 53.

Manufacturing week code

(The first week of the year is 01; the last week is 52 or 53.)

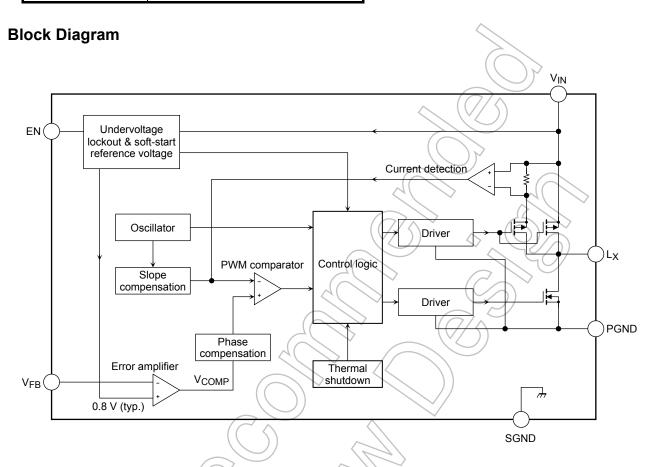
Manufacturing year code (last digit of the year of manufacture)

This product has a MOS structure and is sensitive to electrostatic discharge. Handle with care.

The product(s) in this document ("Product") contain functions intended to protect the Product from temporary small overloads such as minor short-term overcurrent, or overheating. The protective functions do not necessarily protect Product under all circumstances. When incorporating Product into your system, please design the system (1) to avoid such overloads upon the Product, and (2) to shut down or otherwise relieve the Product of such overload conditions immediately upon occurrence. For details, please refer to the notes appearing below in this document and other documents referenced in this document.

Ordering Information

Part Number	Shipping
TB7102AF (TE85L, F)	Embossed tape (3000 units per reel)

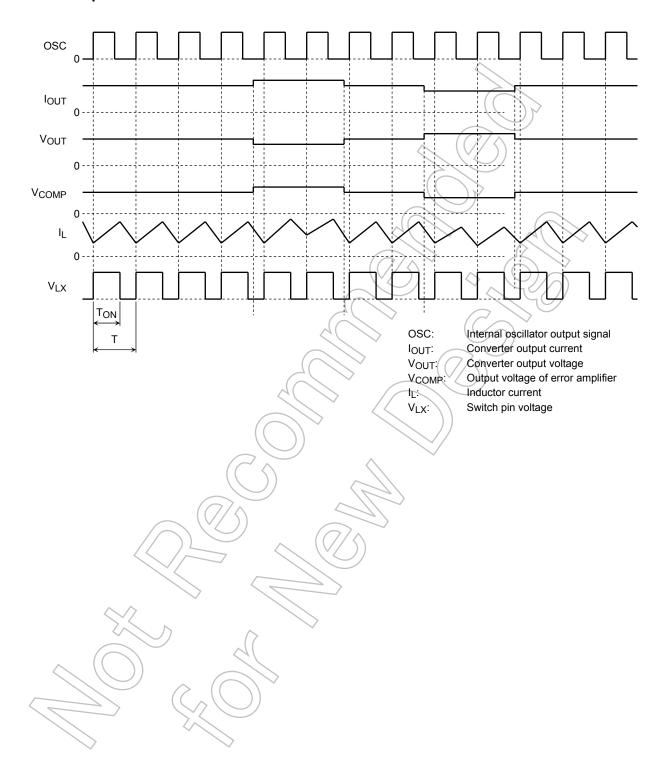


Pin Description

Pin No.	Symbol	Description
1	PGND	Ground for the output section
2	Z VIV	Input pin This pin is placed in the standby state if V_{EN} = low. Standby current is 1 μ A or less.
3	EN	Enable pin When EN \geq 1.5 V (@V _{IN} = 5 V), the control logic is allowed to operate and thus enable the switching operation of the output section.
4	SGND	Ground for the control logic
5	N.C.	No-connect
6	N.C.	No-connect
7	V _{FB}	Feedback pin This input is fed into an internal error amplifier with a reference voltage of 0.8 V (typ.).
8	L _X	Switch pin This output is connected to the high-side P-channel MOSFETs and low-side N-channel MOSFET.

Timing Diagram

Normal Operation



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Input voltage	V _{IN}	-0.3 to 6	٧
Enable pin voltage	V _{EN}	-0.3 to 6	٧
V _{EN} -V _{IN} voltage difference	V _{EN} – V _{IN}	$V_{EN}-V_{IN}<0.3$	٧
Feedback pin voltage	V _{FB}	-0.3 to 6	٧
Switch pin voltage	V_{LX}	-0.3 to 6	٧
Switch pin current	I _{LX}	±1.3	Α
Power dissipation (Note 1) P _D	0.7	V
Operating junction temperature	T _{jopr}	-40 to 125	°C
Junction temperature (Note 2	?) T _j	150	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

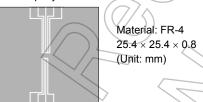
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Thermal Resistance Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, junction to ambient	Rth (j-a)	178.6 (Note 1)	°C/W

Note 1:

Glass epoxy board



Note 2: The TB7102AF may go into thermal shutdown at the rated maximum junction temperature. Thermal design is required to ensure that the rated maximum operating junction temperature, T_{jopr}, will not be exceeded.

4

Electrical Characteristics (unless otherwise specified: $T_j = 25^{\circ}\text{C}$ and $V_{IN} = 2.7$ to 5.5 V)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Operating input voltage		V _{IN (OPR)}	_	2.7	_	5.5	V
Operating current		I _{IN1}	V _{IN} = 5 V, V _{EN} = 5 V, V _{FB} = 5 V		0.68	0.9	mA
		I _{IN2}	V _{IN} = 2.7 V, V _{EN} = 2.7 V, V _{FB} = 2.7 V	/	0.55	0.69	mA
Otan dha assanant		In (STBY) 1	V _{IN} = 5 V, V _{EN} = 0 V, V _{FB} = 0 V		_	1	μА
Standby current		I _{IN} (STBY) 2	$V_{IN} = 2.7 \text{ V}, V_{EN} = 0 \text{ V}, V_{FB} = 0 \text{ V}$	(F)>	1	μА
		V _{IH} (EN) 1	V _{IN} = 5 V	1.5	_		>
EN threshold volta	ge.	V _{IH} (EN) 2	V _{IN} = 2.7 V	1.5	_		>
LIN (III estiola voita	y c	V _{IL (EN) 1}	V _{IN} = 5 V	\	_	0.5	٧
		V _{IL (EN) 2}	V _{IN} = 2.7 V		_	0.5	٧
EN input current		I _{IH} (EN) 1	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}$	7.6	£	12.4	μА
Liv input current		I _{IH} (EN) 2	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}$	4.1	4	6.7	μА
VFB input voltage		V _{FB1}	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}, I_{OUT} = 10 \text{ mA}$	0.776	0.8	0.824	V
VFB input voltage		V _{FB2}	$V_{IN} = 2.7 \text{ V, } V_{EN} = 2.7 \text{ V, } I_{OUT} = 10 \text{ mA}$	0.776	0,8	0.824	V
VFB input current		I _{FB1}	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}$	1	90)	1	μА
VFB input current		I _{FB2}	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}$	1	>_	1	μА
High-side switch on-state resistance		R _{DS} (ON) (H) 1	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}, I_{LX} = -0.5 \text{ A}$	/ / /	0.27	_	Ω
riigii-side switch o	n-state resistance	R _{DS} (ON) (H) 2	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}, I_{LX} = -0.5 \text{ A}$	\ <u> </u>	0.36	_	Ω
Low-side switch or	n-state resistance	R _{DS} (ON) (L) 1	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}, I_{LX} = 0.5 \text{ A}$	/ —	0.27	_	Ω
LOW-SIGE SWITCH OF	i-state resistance	R _{DS} (ON) (L) 2	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}, I_{LX} = 0.5 \text{ A}$	_	0.36	_	Ω
High-side switch le	eakage current	ILEAK (H)	$V_{IN} = 5 \text{ V}, V_{EN} = 0 \text{ V}, V_{LX} = 0 \text{ V}$	_	_	-1	μА
Low-side switch le	akage current	ILEAK (L)	$V_{IN} = 5 \text{ V}, V_{EN} = 0 \text{ V}, V_{LX} = 5 \text{ V}$	_	_	1	μΑ
Oscillation frequer	ICV	fosc1	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}$	0.85	1	1.15	MHz
Communicity in equal	loy	fosc2	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}$	0.85	1	1.15	MHz
Soft-start time		7/ ⟨t _{ss1}	$V_{IN} = 5 \text{ V}, V_{EN} = 5 \text{ V}, I_{OUT} = 0 \text{ A}$	1	2	_	ms
Soit-start time		t _{ss2}	$V_{IN} = 2.7 \text{ V}, V_{EN} = 2.7 \text{ V}, I_{OUT} = 0 \text{ A}$	1.3	2.4	_	ms
Thermal shutdown (TSD)	Detection temperature	T _{SD}	VIN = 5 V		160	l	°C
	Hysteresis	ΔT _{SD}	V _{IN} = 5 V	_	20	_	°C
Undervoltage lockout (UVLO)	Detection votage	V _{UV}	V _{IN} = V _{EN}	2.2	2.4	2.6	V
	Recovery voltage	V _{UVR}	$V_{IN} = V_{EN}$	2.3	2.5	2.7	V
	Hysteresis	ΔVuv	$V_{IN} = V_{EN}$		0.1	_	V
LX current limit		ILIM	V _{IN} = 5 V	1.3	2.8	_	Α

Note on Electrical Characteristics

The test condition T_j = 25°C means a state where any drifts in electrical characteristics incurred by an increase in the chip's junction temperature can be ignored during pulse testing.

Application Circuit Example

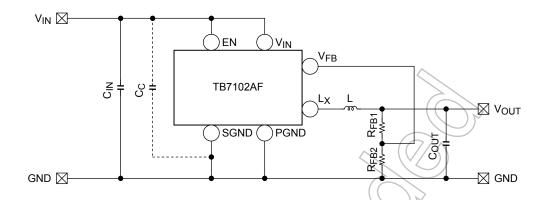


Figure 1 TB7102AF Application Circuit Example

Component values ($@V_{IN} = 5 \text{ V}, V_{OUT} = 3.3 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}$)

These values are presented only as a guide.

 C_{IN} : Input filter capacitor = 10 μ F

(ceramic capacitor: GRM21BB30J106K from Murata Manufacturing Co., Ltd.)

C_{OUT}: Output filter capacitor = 10 μF

(ceramic capacitor: GRM21BB30J106K from Murata Manufacturing Co., Ltd.)

R_{FB1}: Output voltage setting resistor = $7.5 \text{ k}\Omega$

R_{FB2}: Output voltage setting resistor = $2.4 \text{ k}\Omega$

Inductor = 3.3 μH (NP04SB3R3N from Taiyo Yuden Co., Ltd.)

Component values (@ $V_{IN} = 5 \text{ V}$, $V_{OUT} = 1.2 \text{ V}$, Ta = 25°C)

These values are presented only as a guide.

C_{IN}: Input filter capacitor = 10 μF

(ceramic capacitor: GRM21BB30J106K from Murata Manufacturing Co., Ltd.)

C_{OUT}: Output filter capacitor = 22 μF

(ceramic capacitor: GRM31CB30J226K from Murata Manufacturing Co., Ltd.)

R_{FB1}: Output voltage setting resistance = $1.2 \text{ k}\Omega$

R_{FB2}: Output voltage setting resistance = $2.4 \text{ k}\Omega$

Inductor = 3.3 µH (NP04SB3R3N from Taiyo Yuden Co., Ltd.) L:

Component values need to be adjusted, depending on the TB7102AF's input/output conditions and the board layout.

Application Notes

Inductor Selection

The inductance required for inductor L can be calculated as follows:

$$L = \frac{V_{IN} - V_{OUT}}{f_{osc} \cdot \Delta I_{I}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \dots (1)$$

$$V_{IN}: \quad \text{Input voltage (V)}$$

$$V_{OUT}: \quad \text{Output voltage (V)}$$

$$f_{osc}: \quad \text{Oscillation frequent}$$

Oscillation frequency = 1 MHz (typ.) f_{osc} :

> ΔII : Inductor ripple current (A)

*: Generally, ΔI_L should be set to approximately 30% of the maximum output current. Since the maximum output current of the TB7102AF is 1 A, ΔI_L should be 0.3 A or so. Therefore, the inductor should have a current rating greater than the peak output current of 1.15 A. If the inductor current rating is exceeded, the inductor becomes saturated, leading to an unstable DC-DC converter operation.

When $V_{IN} = 5 \text{ V}$ and $V_{OUT} = 3.3 \text{ V}$, the required inductance can be calculated as follows. Be sure to select an appropriate inductor, taking the V_{IN} range into account.

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$$\begin{split} L &= \frac{V_{IN} - V_{OUT}}{f_{osc} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \\ &= \frac{5 \ V - 3.3 \ V}{1 \ MHz \cdot 300 \ mA} \cdot \frac{3.3 \ V}{5 \ V} \quad \cdots \cdots (2) \\ &= 3.7 \ \mu H \end{split}$$

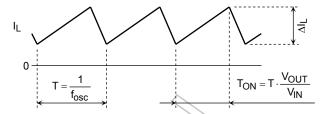


Figure 2 Inductor Current Waveform

Setting the Output Voltage

A resistive voltage divider is connected as shown in Figure 3 to set the output voltage; it is given by Equation 3 based on the reference voltage of the error amplifier, which is connected to the Feedback pin, VFB. RFB1 should be up to $10~\text{k}\Omega$ or so, because an extremely large value RFB1 incurs a delay due to parasitic capacitance at the VFB pin. If the difference between the input and output voltages is small, the output voltage may drop, depending on the load current conditions. For optimal operation, output voltage should be set to 0.8~V (typ.) at the minimum and to $(V_{IN}-1)~\text{V}$ at the maximum. It is recommended that resistors with a precision of $\pm 1\%$ or higher be used for RFB1 and RFB2.

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

$$= 0.8 \text{ V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \cdot \cdot \cdot \cdot \cdot (3)$$

Figure 3 Output Voltage Setting Resistors

Output Capacitor Selection

Use a ceramic capacitor as the output filter capacitor. Since a ceramic capacitor is generally sensitive to temperature, choose one with excellent temperature characteristics (such as the JIS B characteristic). As a rule of thumb, its capacitance should be 10 μF or greater for applications where Vout ≥ 2.0 V, and 20 μF or greater for applications where Vout ≤ 2.0 V. The capacitance should be set to an optimal value that meets the system's ripple voltage requirement and transient load response characteristics. Since the ceramic capacitor has a very low ESR value, it helps reduce the output ripple voltage; however, because the ceramic capacitor provides less phase margin, it should be thoroughly evaluated.

Component Values (@V_{IN} = 5 V, Ta = 25°C)

These values are presented only as a guide.

The following values may need tuning depending on the TB7102AF's input/output conditions and the board layout.

Output Voltage Setting	Inductance	Input Capacitance	Output Capacitance	Feedback Resistor	Feedback Resistor
V _{OUT}	L	C _{IN}	C _{OUT}	R _{FB1}	R _{FB2}
1.2 V	3.3 μΗ	10 μF	22 μF	1.2 kΩ	2.4 kΩ
1.5 V	3.3 μΗ	10 μF	22 μF	2.1 kΩ	2.4 kΩ
1.8 V	3.3 μΗ	10 μF	22 μF	3.0 kΩ	2.4 kΩ
2.5 V	3.3 μΗ	10 μF	10 μF	5.1 kΩ	2.4 kΩ
3.3 V	3.3 μΗ	10 μF	10 μF	7.5 kΩ	2.4 kΩ

Undervoltage Lockout (UVLO)

The TB7102AF has undervoltage lockout (UVLO) protection circuitry. The TB7102AF does not provide output voltage (V_{OUT}) until the input voltage has reached V_{UVR} (2.5 V typ.). UVLO has hysteresis of 0.1 V (typ.). After the switch turns on, if V_{IN} drops below V_{UV} (2.4 V typ.), UVLO shuts off the switch at V_{OUT} .

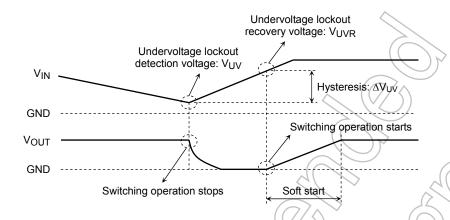


Figure 4 Undervoltage Lockout Operation

Thermal Shutdown (TSD)

The TB7102AF provides thermal shutdown. When the junction temperature continues to rise and reaches TSD (160°C typ.), the TB7102AF goes into thermal shutdown and shuts off the power supply. TSD has a hysteresis of about 20°C. The device is enabled again when the junction temperature has dropped by approximately 20°C from the TSD trip point. The device resumes the power supply when the soft-start circuit is used upon recovery from the TSD state .

Thermal shutdown is intended to protect the device against abnormal system conditions. It should be ensured that the TSD circuit will not be activated during normal operation of the system.

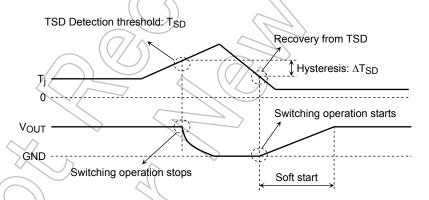


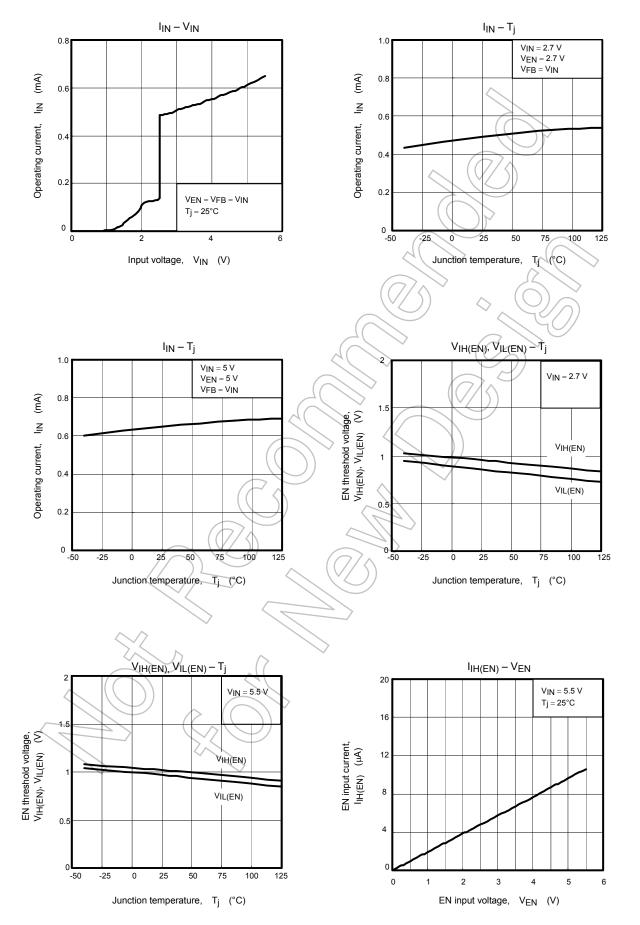
Figure 5 Thermal Shutdown Operation

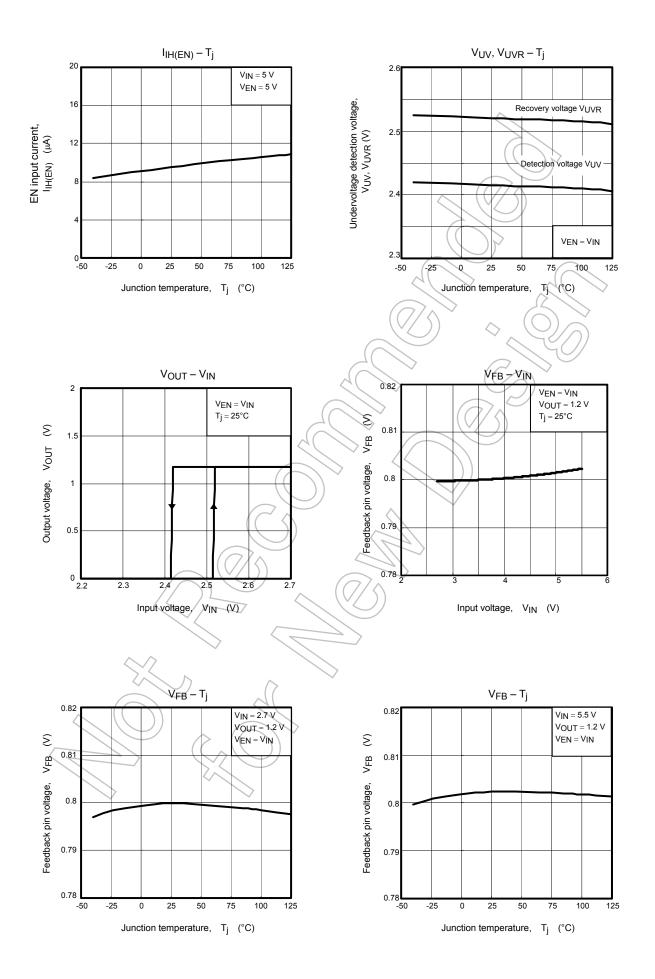
Usage Precautions

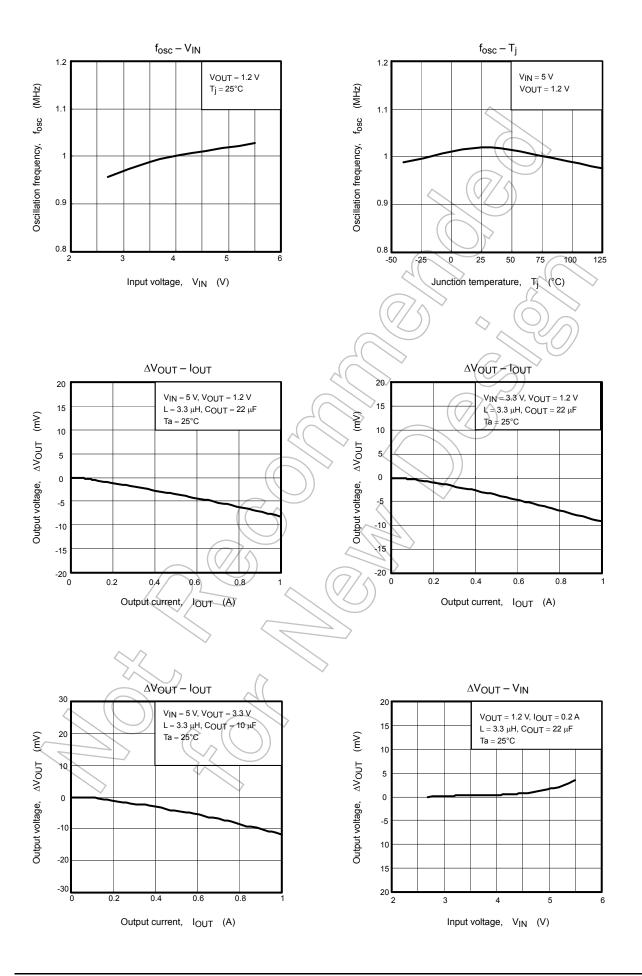
- The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.
- External components such as capacitors, inductor and resistors should be placed as close to the TB7102AF as possible.
- The TB7102AF has an ESD diode between the EN and V_{IN} pins. The voltage between these pins should satisfy $V_{EN} V_{IN} < 0.3 \text{ V}$.
- Operation might become unstable due to board layout. In that case, add a decoupling capacitor (C_C) of 0.1 μF to $1\mu F$ between the SGND and V_{IN} pins.
- The overcurrent protection circuits in the Product are designed to temporarily protect Product from minor overcurrent of brief duration. When the overcurrent protective function in the Product activates, immediately cease application of overcurrent to Product. Improper usage of Product, such as application of current to Product exceeding the absolute maximum ratings, could cause the overcurrent protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.
- The thermal shutdown circuits in the Product are designed to temporarily protect Product from minor overheating of brief duration. When the overheating protective function in the Product activates, immediately correct the overheating situation. Improper usage of Product, such as the application of heat to Product exceeding the absolute maximum ratings, could cause the overheating protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.

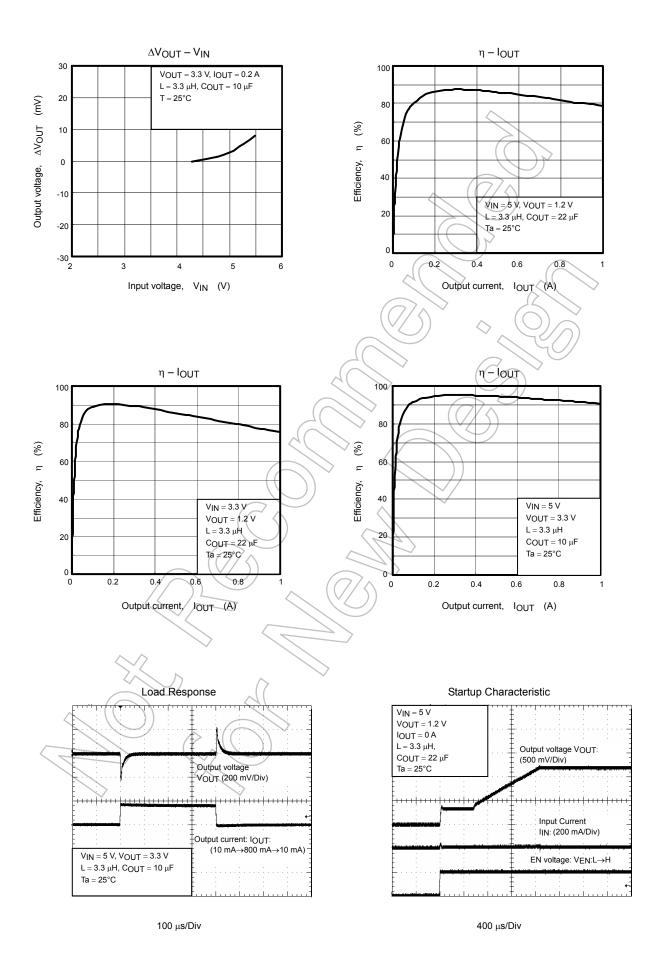


Typical Performance Characteristics

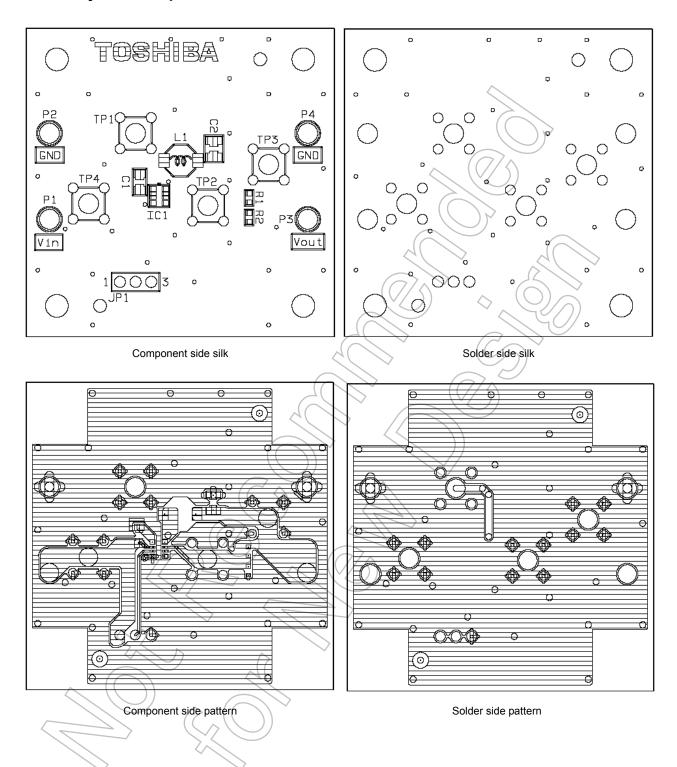








Board Layout Example



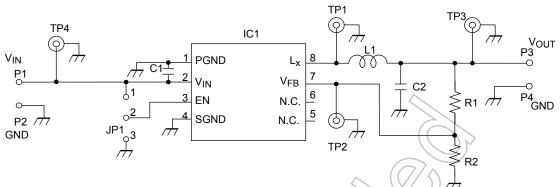


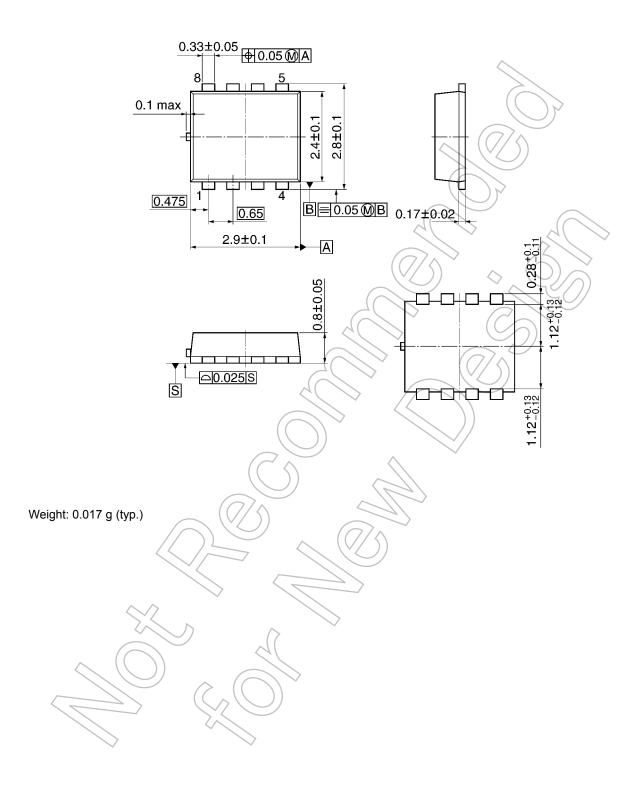
Figure 6 Circuit of the Board Layout Example

External Component Examples

Label	Vendor	Part Number
IC1	Toshiba Corporation	TB7102AF
C1	Murata Manufacturing Co., Ltd.	GRM21BB30J106K
C2	Murata Manufacturing Co., Ltd.	GRM21BB30J106K
R1	KOA Corporation	RK73H1ET
R2	KOA Corporation	RK73H1ET
L1	Taiyo Yuden Co., Ltd.	NP04SB3R3N

Package Dimensions

SON8-P-0303-0.65A Unit: mm



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