

LTC3314A 3.3V to 1V 8A, 2MHz Dual-Phase Low Ripple Step-Down DC/DC Regulator

DESCRIPTION

Demo circuit 3205A features the LTC3314A, 5V, dual 4A/dual-phase 8A step-down DC/DC regulator IC. This demo circuit is configured as a 2-phase, 2MHz, 3.3V input, single 1V output, 8A buck regulator. The top switches are 180-degree out of phase to reduce the output ripple.

The [LTC®3314A](#) features dual monolithic synchronous 4A step-down power stages in a 30-ball, 2.2mm × 2.7mm WLCSP package for space saving applications with demanding performance requirements. Both bucks achieve high efficiency and fast transient response with small external components. The LTC3314A can also be configured as a dual output, 4A per output, step-down converter. Please refer to DC3204A as a dual output application example. The LTC3314A data sheet gives a complete description of its operation and application information. The data sheet must be read in conjunction

with this demo manual when evaluating or modifying this demo circuit.

DC3205A supports three operation modes, including pulse-skipping, forced continuous and Burst Mode® operation. The clock frequency and the operation mode are shared by both regulators. User can select desired operation mode with JP1 jumper. Setting JP1 to FC/SYNC position also allows the LTC3314A to sync to a clock frequency from 1MHz to 3MHz, operating in forced continuous mode.

An EMI filter is included in this demo circuit for noise sensitive applications. To power with EMI filter, please apply input voltage via VIN EMI terminal.

[Design files for this circuit board are available.](#)

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN} /V _{IN EMI}	DC3205A Input Voltage Range		2.25		5.5	V
V _{OUT}	DC3205A Output Voltage Range		0.98	1	1.02	V
I _{OUT}	DC3205A Output Current (Each Output)				8	A
f _{SW}	Switching Frequency		1.8		2.2	MHz
EFF	Efficiency	V _{IN} = 3.3V, I _{OUT} = 4A		91		%

BOARD PHOTO Part marking is either ink mark or laser mark

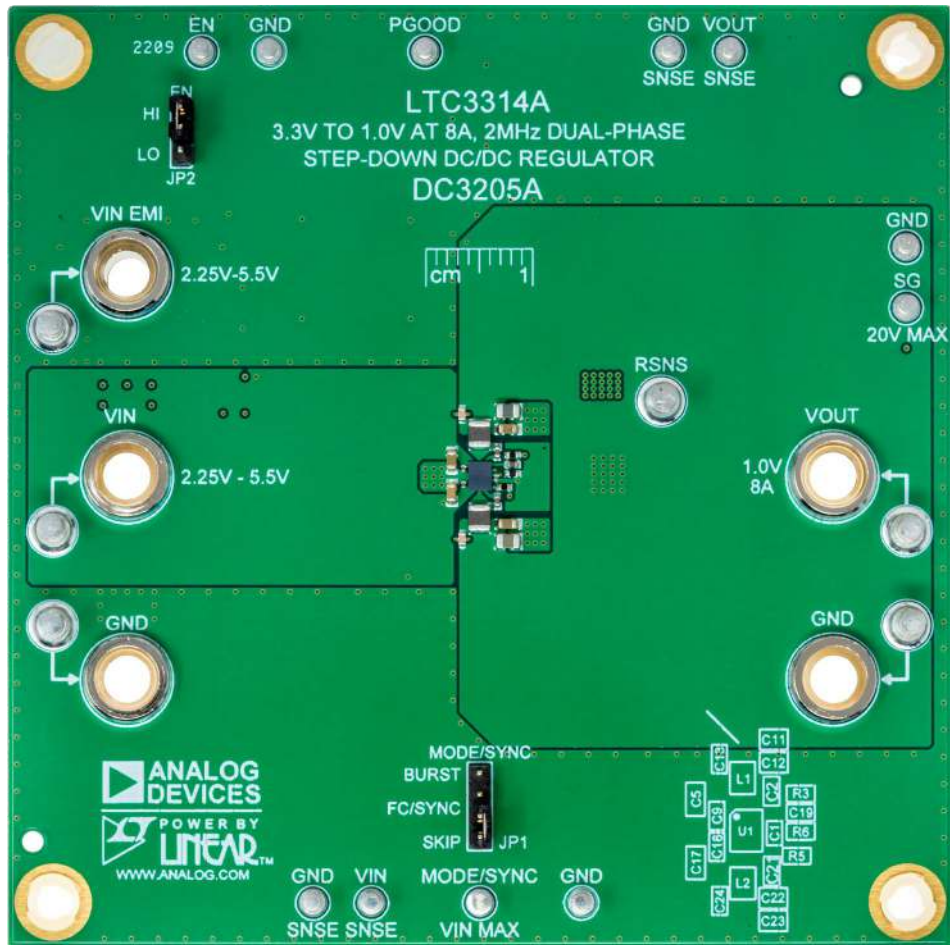


Figure 1. DC3205A Demo Board

QUICK START PROCEDURE

Refer to Figure 2 for the proper measurement equipment setup and follow the procedure below:

NOTE: For accurate V_{IN} , V_{OUT} and efficiency measurements, measure V_{IN} at the VIN SNSE and GND SNSN turrets, and measure V_{OUT} at the VOUT SNSE and GND SNSE turrets. When measuring the input or output ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. It is recommended to use technique shown in Figure 3 and Figure 4 for basic ripple measurement.

Prepare for the Test

- A. Select a power supply PS1 that can handle 5V of output voltage and 10A of output current, with internal current meter. If possible, connect PS1 Kelvin Sense terminals with VIN SNSE and GND SNSE turrets.
 - B. Select an electronic load LD1 can handle 1.5V of load voltage and up to 8A of load current in constant current mode.
 - C. Select an oscilloscope with two or more channels and two voltage probes.
1. Connect PS1, LD1, VM1, VM2 and VM3 as shown in Figure 2. If the input EMI filter is desired, connect the input power supply to VIN EMI and GND.
 2. Set the JP2 to HI position. Set LD1 to 0A. Slowly increase PS1 to 1V. If PS1 current reads less than 20mA, increase PS1 to 3.3V until VM1 reads $3.3V \pm 10mV$. VM2 should read between 0.98V to 1.02V. VM3 should read above 3V.
 3. Connect an oscilloscope voltage probe as shown in Figure 3, between VOUT SNSE and GND SNSE turrets. Set channel to AC-coupled, voltage scale to 20mV, and time base to $10\mu s/div$. Check V_{OUT} ripple voltage. Output voltage ripple can also be measured with a low inductance connector on TP1, as shown in Figure 4.
 4. Increase the load by 1A intervals up to 8A and observe the voltage output regulation, ripple voltage and SW behavior.

5. If other operation modes are desired. Turn off PS1, set LD1 to 0A and set JP1 to FC/SYNC or BURST position. Turn on PS1, slowly increase LD1 and observe the change in PS1 output current, SW behavior and output ripple.
6. Optional: To change the frequency, remove R5. Install the desired R_T resistor in the R8 location. Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output. Refer to the LTC3314A data sheet and LTPowerCAD for more information on choosing the required components.
7. Optional: To SYNC to a specific frequency, set JP1 to FC/SYNC position. Connect a waveform generator to MODE/SYNC turret. Please refer to LTC3314A data sheet for synchronization signal requirements.
8. To test the transient response with a base load, add the desired resistor to produce a minimum load between VOUT and RSNS turrets (R_L shown on Figure 2). Note that the total load resistance will be R_L plus R_{11} ($20m\Omega$). Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.
9. Measure the R_{SNS} voltage to observe the current, $V_{RSNS}/20m\Omega$. Adjust the amplitude of the pulse to provide the desired transient. Connect signal generator SG1 between SG_INPUT and GND turrets. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Refer to the following equation for output current measurement:

$$I_{OUT} = \frac{V_{RSNS1}}{20m\Omega} \quad (1)$$

10. When done, turn off SG1, PS1 and Load.

TEST SETUP

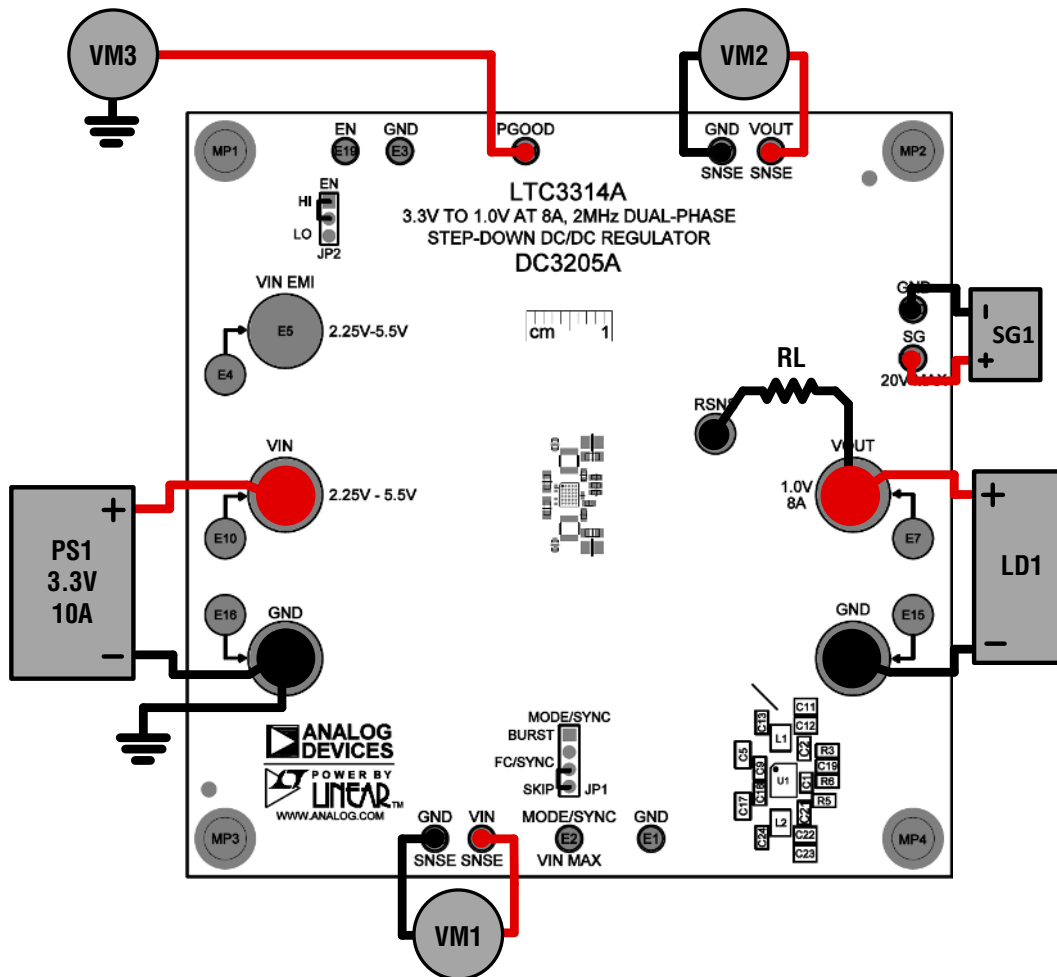


Figure 2. Test Setup for DC3205A Demo Board

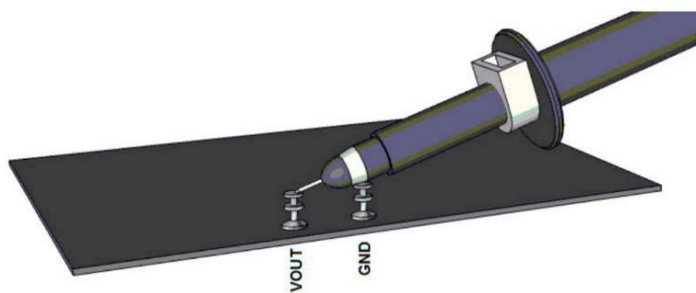


Figure 3. Technique for Measuring Output Ripple and Step Response

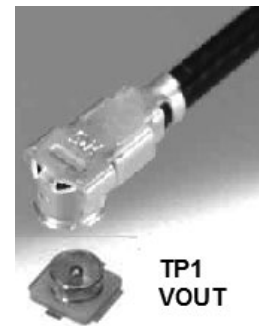


Figure 4. Technique for Measuring Output Ripple and Step Response with a Low Inductance Connector (Not Supplied)

THEORY OF OPERATION

Introduction to the DC3205A

The DC3205A demonstration circuit features the LTC3314A, 5V, dual 4A/dual-phase 8A step-down DC/DC regulator. The LTC3314A contains two monolithic, constant frequency, current mode step-down DC/DC converters. An oscillator, shared by two converters, with frequency set by a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. The beginning of each clock cycle of the two converters are 180-degree out of phase. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current, at which the top switch turns off, is controlled by the voltage on the internal V_C node, which is the output of the error amplifier. When operating in dual-phase mode, V_C of Buck1 is used to control the peak current for both buck power stages. The internal V_C node is connected with internal compensator to stabilize the control loop. The error amplifier servos the V_C node by comparing the voltage on the FB pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous bottom power switch turns on until the next clock cycle begins. In pulse-skipping mode and Burst mode, the bottom switch also turns off when inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level. In Burst Mode, the error amplifier and most part of the internal circuitry can be turned off until output voltage trips an output low comparator, during extreme light load condition, to improve light load efficiency.

If the EN1 pin is low, the DC3205A is in shutdown and in a low quiescent current state. When the EN1 pin is above its threshold, the DC3205A will be enabled.

The MODE/SYNC pin synchronizes the switching frequency to an external clock. It also sets the PWM mode. The PWM modes of operation are Burst, pulse-skipping

and forced continuous. See the LTC3314A data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of V_{OUT} to V_{IN} and the available inductor values. The maximum allowable operating frequency may be calculated in the formula below.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot t_{ON(MIN)}} \quad (2)$$

Select an operating switching frequency below $f_{SW(MAX)}$. Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3314A operating load, 4A. Use the formulas below to calculate the inductor value to obtain a 30% (1.2A) inductor ripple for the operating frequency.

$$L \geq \frac{V_{OUT}}{1.2A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \quad \text{for} \quad (3)$$

$$\frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5$$

$$L \geq \frac{0.25 \cdot V_{IN(MAX)}}{1.2A \cdot f_{SW}} \quad \text{for} \quad \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (4)$$

The overall control loop of the converter can be tuned by output capacitors and a feedforward capacitor. The LTC3314A has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces required output capacitance to meet the desired transient voltage range. Feedforward capacitor C19 along with R3 provides a phase lead which will improve the phase margin.

Loop stability is generally measured using the Bode Plot method of plotting loop gain in dB and phase shift in degrees. The 0dB crossover frequency should be less than 1/6 of the operating frequency to reduce the effects of added phase shift of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

TYPICAL PERFORMANCE CHARACTERISTICS

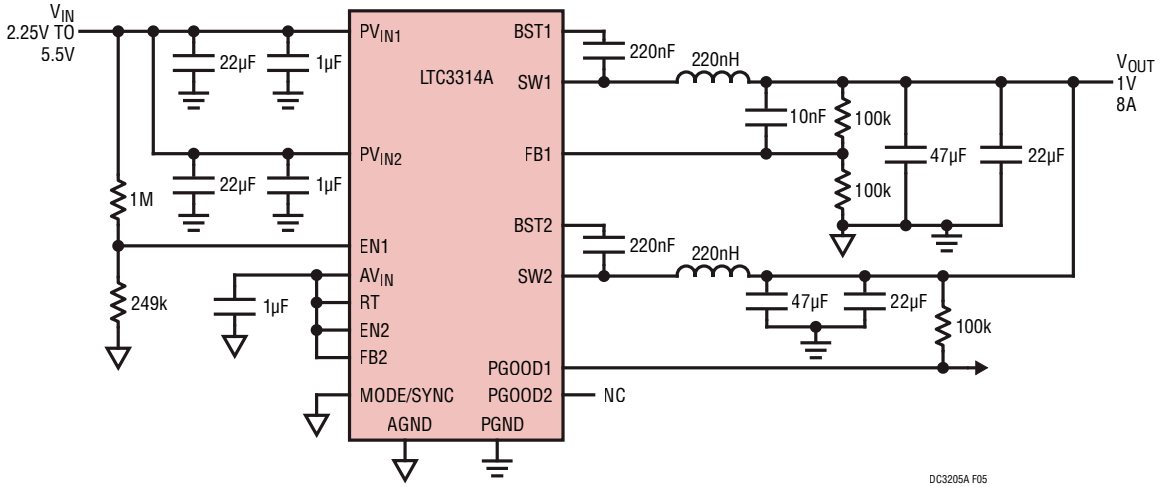


Figure 5. LTC3314A 2-Phase 2MHz 8A Buck Typical Application Schematic

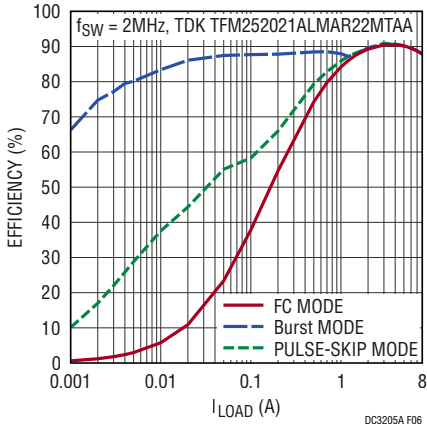


Figure 6. Efficiency vs Load

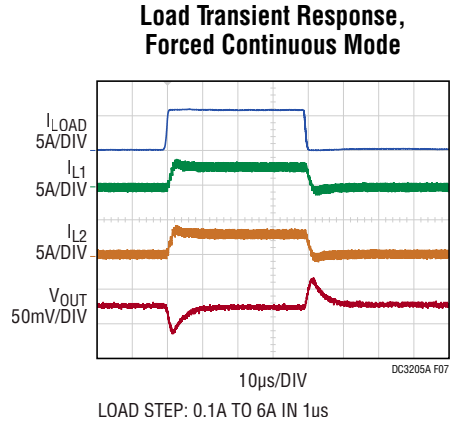


Figure 7. Load Step Response in Forced Continuous Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response,
Pulse-Skipping Mode

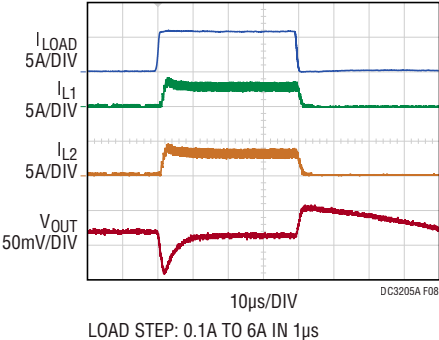


Figure 8. Load Step Response in Pulse-Skipping Mode with $V_{IN} = 3.3V$

Load Transient Response,
Burst Mode Operation

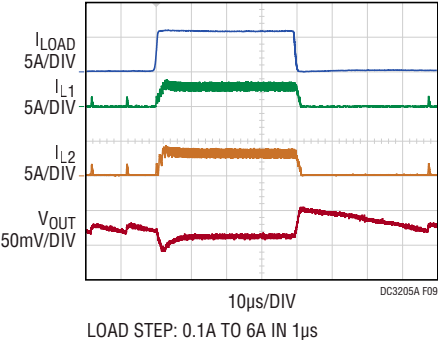


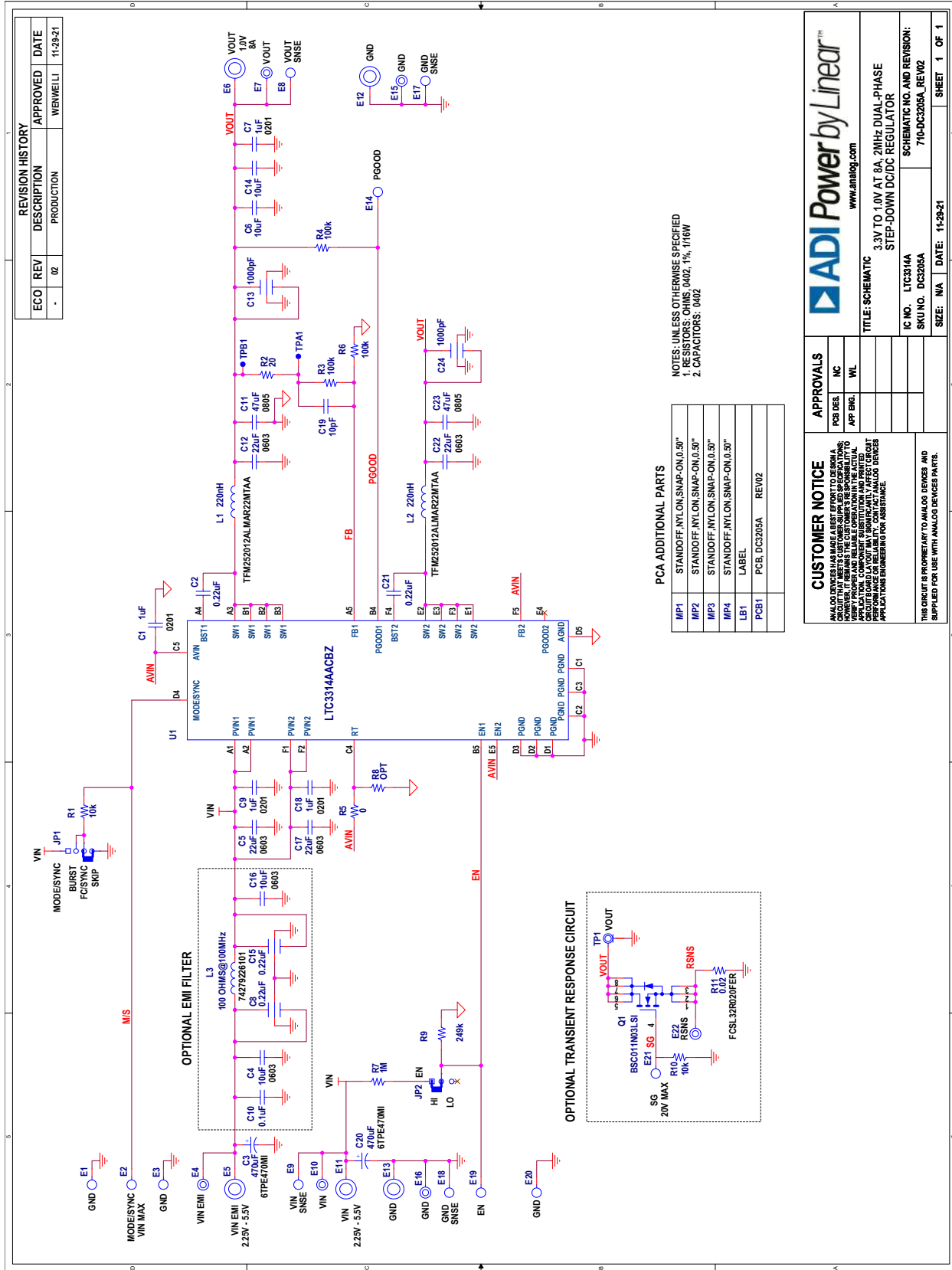
Figure 9. Load Step Response in Burst Mode with $V_{IN} = 3.3V$

DEMO MANUAL DC3205A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	4	C1, C7, C9, C18	CAP, 1 μ F, X7T, 6.3V, 20%, 0201	MURATA, GRM033D70J105ME01D
2	2	C2, C21	CAP, 0.22 μ F, X7R, 16V, 10%, 0402, AEC-Q200	MURATA, GCM155R71C224KE02D
3	4	C5, C12, C17, C22	CAP, 22 μ F, X5R, 10V, 20%, 0603	AVX, 0603ZD226MAT2A
4	2	C11, C23	CAP, 47 μ F, X6S, 6.3V, 20%, 0805	TAIYO YUDEN, JMK212BC6476MG-T
5	1	C19	CAP, 10pF, C0G/NPO, 25V, 10%, 0402	AVX, 04023A100KAT2A
6	2	L2, L3	IND., 220nH, PWR, 20%, 6.7A, 13m Ω , 2.5mm \times 2.00mm, SMD, AEC-Q200	TDK, TFM252012ALMAR22MTAA
7	1	Q1	XSTR., MOSFET, N-CH, 30V, 37A, PG-TDSON-8	INFINEON, BSC011N03LSI
8	2	R3, R6	RES., 100k, 1%, 1/10W, 0402, AEC-Q200	KOA SPEER, RK73H1ETTP1003F
9	1	U1	IC, DUAL 2MHz, 4A STEP-DOWN DC/DC REGULATOR	ANALOG DEVICES INC., LTC3314AACBZ-R7
Additional Demo Board Circuit Components				
1	2	C3, C20	CAP, 470 μ F, TANT, POSCAP, 6.3V, 20%, 7343, 18m Ω , TPE	PANASONIC, 6TPE470MI
2	2	C4, C16	CAP, 10 μ F, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
3	2	C6, C14	CAP CER 10 μ F 6.3V X5R 0402	Murata Electronics, GRM155R60J106ME47D
4	1	C7	CAP, 1 μ F, X7T, 6.3V, 20%, 0201	MURATA, GRM033D70J105ME01D
5	2	C8, C15	CAP, 0.22 μ F, X7R, 6.3V, 20%, 0603	JOHANSON DIELECTRICS, 6R3X14W224MV4T
6	1	C10	CAP, 0.1 μ F, X7R, 25V, 10%, 0402, AEC-Q200	MURATA, GCM155R71E104KE02D
7	2	C13, C24	CAP, 1000pF, X7R, 50V, 20%, 0402, 3-TERM, X2Y EMI FILTER	JOHANSON DIELECTRICS, 500X07W102MV4T
8	1	L1	IND., 100 Ω AT 100MHz, FERRITE BEAD, 25%, 8A, 6m Ω , 1812	WURTH ELEKTRONIK, 74279226101
9	2	R1, R10	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J103TRF
10	1	R2	RES., 20 Ω , 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F20R0TRF
11	1	R4	RES., 100k, 5%, 1/16W, 0402	YAGEO, RC0402JR-07100KL
12	1	R5	RES., 0 Ω , 1/16W, 0402	VISHAY, CRCW04020000Z0ED
13	1	R7	RES., 1M, 1%, 1/16W, 0402, AEC-Q200	STACKPOLE ELECTRONICS, INC., RMCF0402FT1M00
14	1	R9	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F2493TRF
15	1	R11	RES 0.02 Ω 1% 1.5W 1206	Ω ITE, FCSL32R020FER
17	1	Q1	XSTR., MOSFET, N-CH, 30V, 37A, PG-TDSON-8	INFINEON, BSC011N03LSI
18	0	TP1	CONN., U.FL, RECEPT, ST SMD, 0Hz to 6GHz 50 Ω	HIROSE ELECTRIC, U.FL-R-SMT-1(10)
Hardware: For Demo Board Only				
1	11	E1-E3, E8, E9, E14, E17-E21	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E10, E15, E16, E22	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E5, E6, E11-E13	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1 \times 4, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000411121
5	1	JP2	CONN., HDR, MALE, 1 \times 3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
6	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	WURTH ELEKTRONIK, 702935000
7	2	XJP1, XJP2	CONN., SHUNT, FEMALE, 2-POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM





ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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