

# FDZ372NZ

## N-Channel 1.5 V Specified PowerTrench® Thin WL-CSP MOSFET 20 V, 4.7 A, 50 mΩ

### Features

- Max  $r_{DS(on)}$  = 50 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 2$  A
- Max  $r_{DS(on)}$  = 60 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 2$  A
- Max  $r_{DS(on)}$  = 72 mΩ at  $V_{GS} = 1.8$  V,  $I_D = 1$  A
- Max  $r_{DS(on)}$  = 93 mΩ at  $V_{GS} = 1.5$  V,  $I_D = 1$  A
- Occupies only 1.0 mm<sup>2</sup> of PCB area. Less than 30% of the area of 2x2 BGA
- **Ultra-thin package:** less than 0.4 mm height when mounted to PCB
- HBM ESD protection level > 3200V (Note3)
- RoHS Compliant

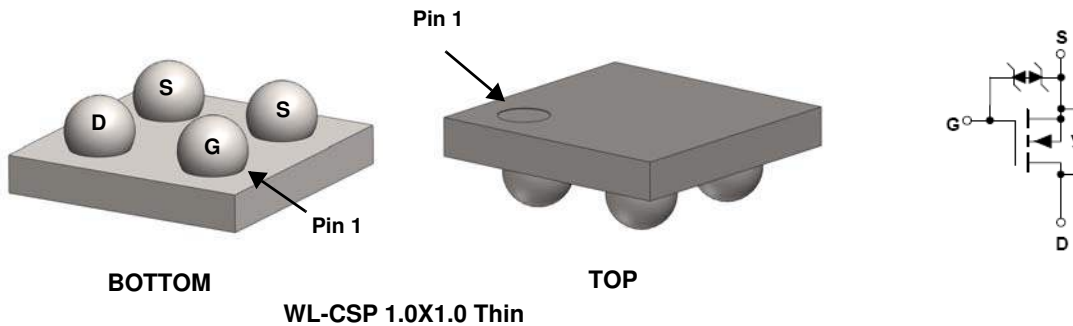


### General Description

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" **Thin** WLCSP packaging process, the FDZ372NZ minimizes both PCB space and  $r_{DS(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low  $r_{DS(on)}$ .

### Applications

- Battery management
- Load switch
- Battery protection



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated Value	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current -Continuous $T_A = 25$ °C (Note 1a)	4.7	A
	-Pulsed	12	
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	1.7	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	260	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
L	FDZ372NZ	WL-CSP 1.0x1.0 Thin	7"	8 mm	5000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		18		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		40	50	m $\Omega$
		$V_{GS} = 2.5\text{ V}$ , $I_D = 2\text{ A}$		45	60	
		$V_{GS} = 1.8\text{ V}$ , $I_D = 1\text{ A}$		53	72	
		$V_{GS} = 1.5\text{ V}$ , $I_D = 1\text{ A}$		63	93	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		57	81	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 4.7\text{ A}$		22		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		515	685	pF
$C_{oss}$	Output Capacitance			85	115	pF
$C_{rss}$	Reverse Transfer Capacitance			65	100	pF

### Switching Characteristics

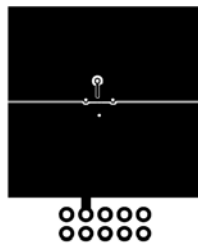
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}$ , $I_D = 4.7\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6.2	12	ns
$t_r$	Rise Time			3.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns
$t_f$	Fall Time			5.6	12	ns
$Q_g$	Total Gate Charge			7	9.8	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{GS} = 4.5\text{ V}$ , $V_{DD} = 10\text{ V}$ $I_D = 4.7\text{ A}$		0.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.6		nC

### Drain-Source Diode Characteristics

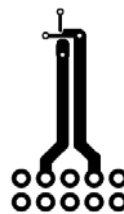
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 1.4\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 4.7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		11	20	ns
$Q_{rr}$	Reverse Recovery Charge			2.6	10	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $75\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.

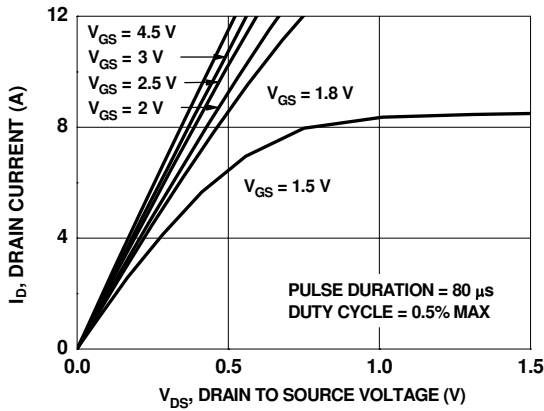


b.  $260\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

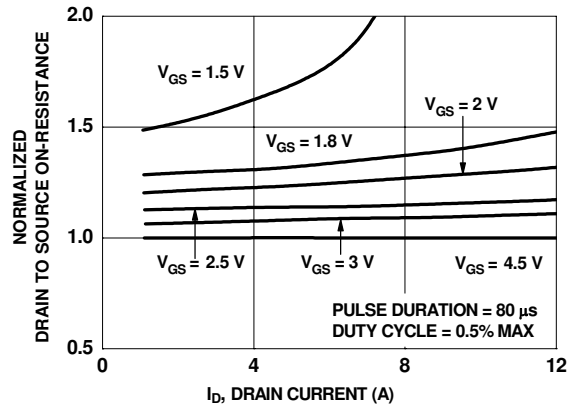
2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

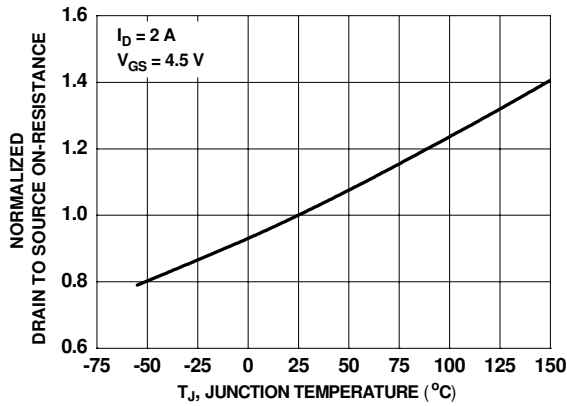
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



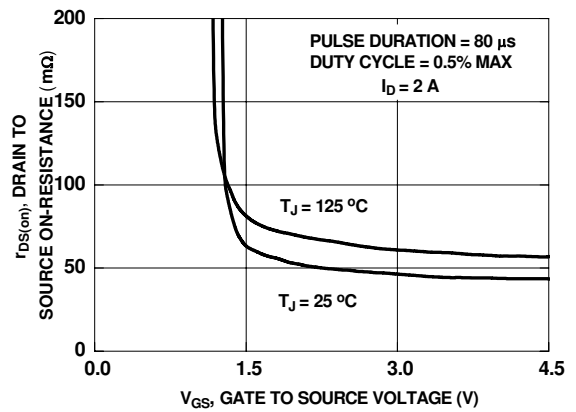
**Figure 1. On-Region Characteristics**



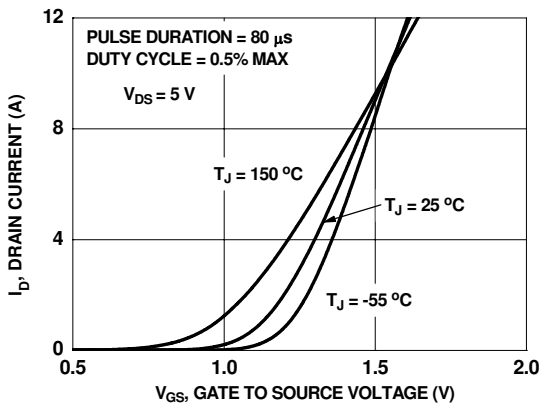
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



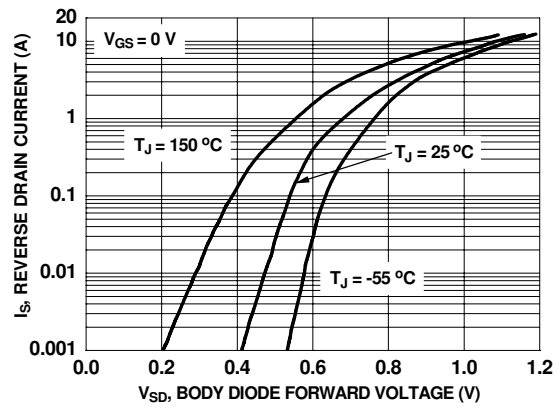
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

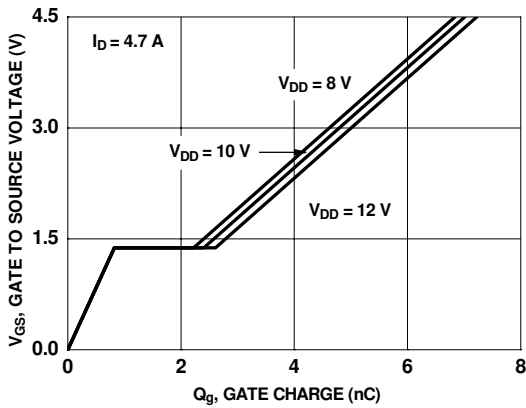


**Figure 5. Transfer Characteristics**

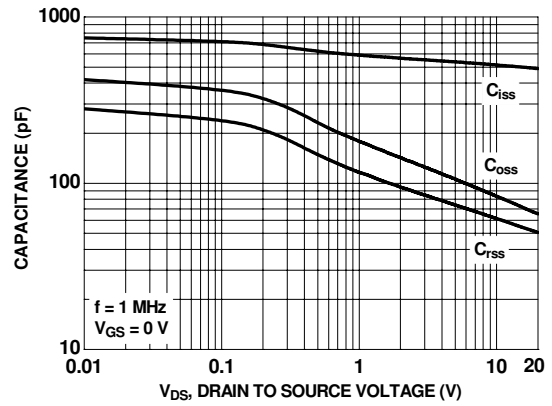


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

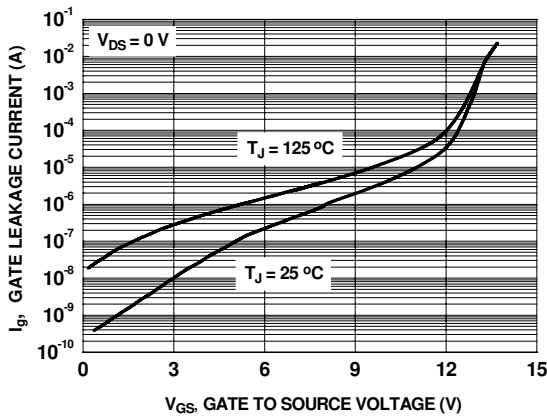
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



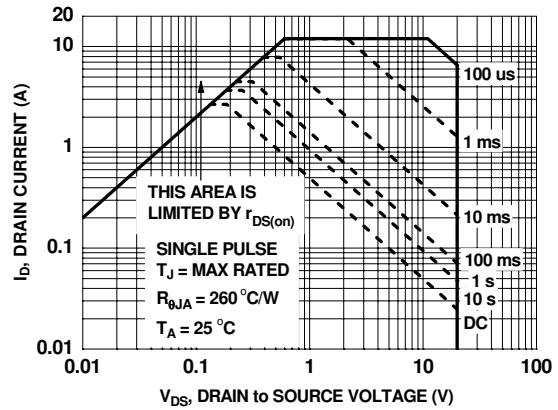
**Figure 7. Gate Charge Characteristics**



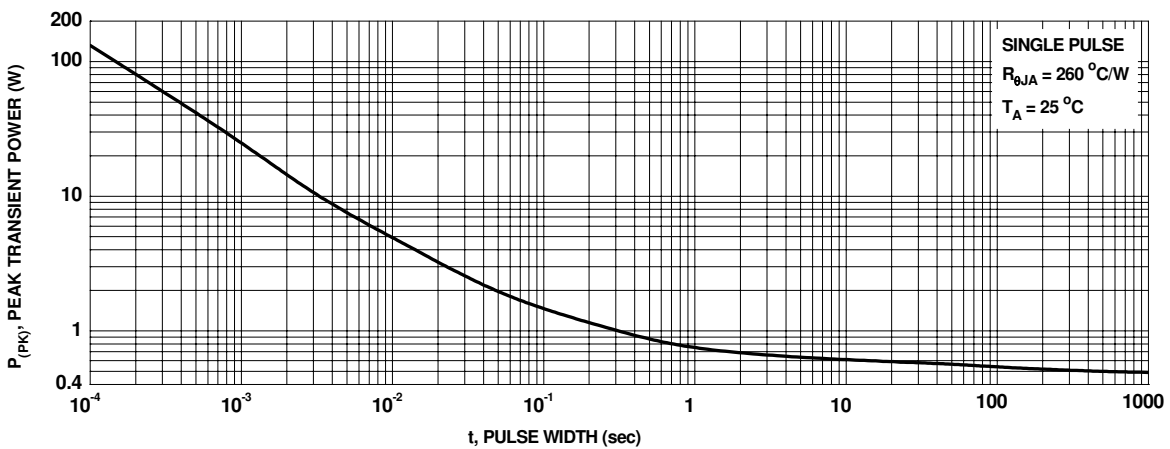
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

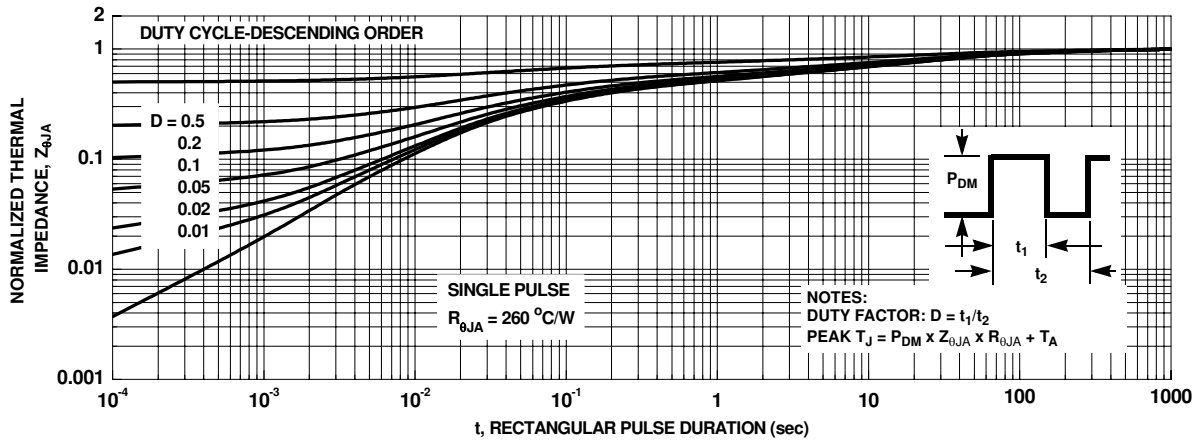


**Figure 10. Forward Bias Safe Operating Area**



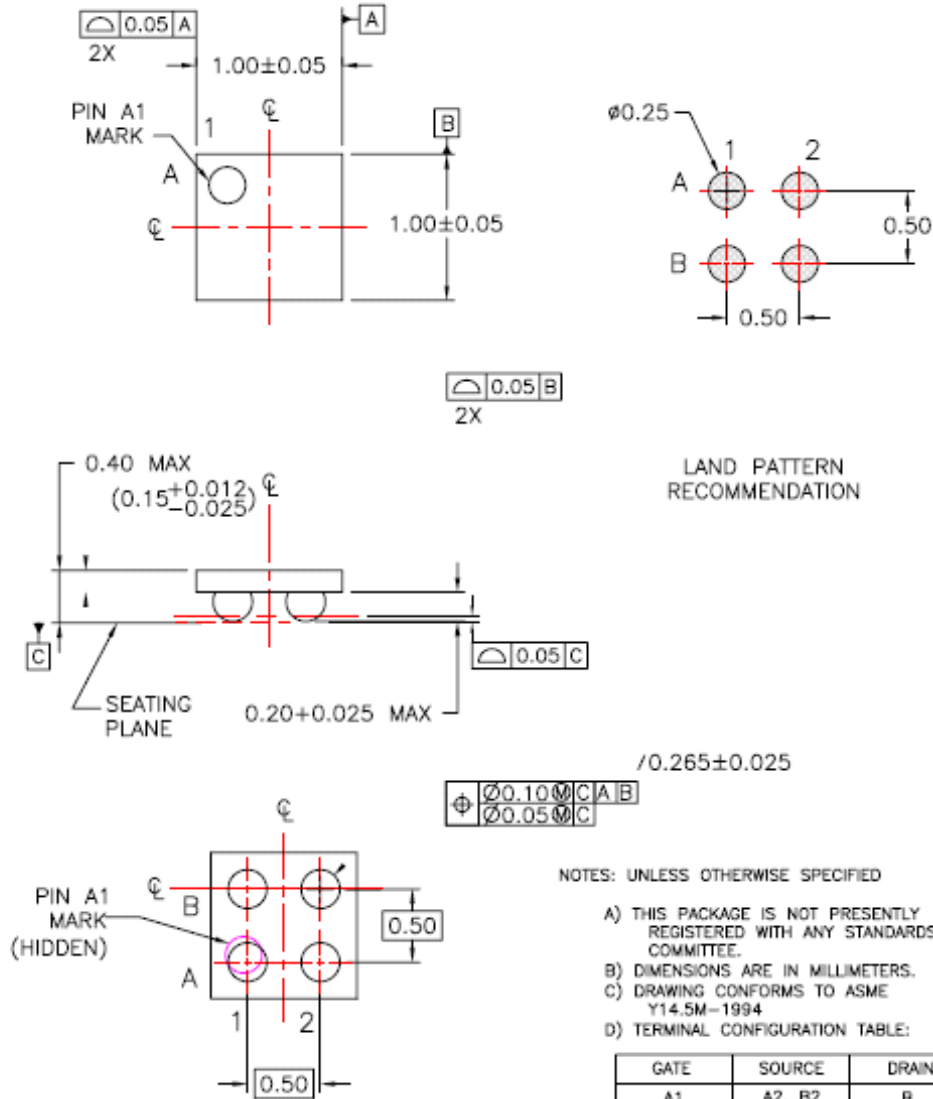
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout





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