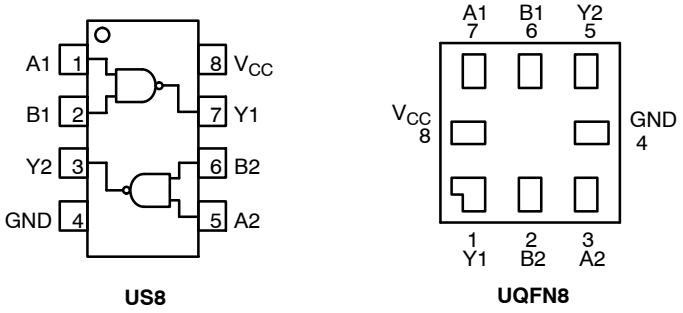
TinyLogic ULP-A Dual 2-Input NAND Gate

NC7WP00

The NC7WP00 is a dual 2−input NAND gate in tiny footprint packages. The device is designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 2.1 ns t_{PD} at 3.3 V (Typ)
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 2.6 mA at 3.3 V
- Available in US8 and MicroPak™ Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



US8 UQFN8

Figure 1. Pinout Diagrams (Top Views)

Figure 2. Logic Symbol

ON Semiconductor®

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MARKING DIAGRAMS

UQFN8
1.6X1.6, 0.5P
CASE 523AY

CCKK
XYZ

US8
CASE 846AN

CC, XXXX	= Specific Device Code
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code Format
Z	= Assembly Plant Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

PIN ASSIGNMENT

Pin	US8	UQFN8
1	A1	Y1
2	B1	B2
3	Y2	A2
4	GND	GND
5	A2	Y2
6	B2	B1
7	Y1	A1
8	V_{CC}	V_{CC}

FUNCTION TABLE (Y = $\overline{AB}$)

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: H = HIGH Logic Level
L = LOW Logic Level

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.3	V
V_{IN}	DC Input Voltage		−0.5 to +4.3	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	US8 MicroPak	250 210	°C/W
P_D	Power Dissipation in Still Air	US8 MicroPak	500 595	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		0.9	3.6	V
V_{IN}	DC Input Voltage		0	3.6	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	
T_A	Operating Temperature Range		−40	+85	°C
t_r , t_f	Input Transition Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V	0	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		0.9	_	0.5	–	_	–	V
			1.1 to 1.3	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			1.4 to 1.6	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			1.65 to 1.95	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			2.3 to 2.7	1.6	–	–	1.6	–	
			3.0 to 3.6	2.1	–	–	2.1	–	
V_{IL}	Low−Level Input Voltage		0.9	–	0.5	–	–	–	V
			1.1 to 1.3	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			1.4 to 1.6	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			1.65 to 1.95	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			2.3 to 2.7	–	–	0.7	–	0.7	
			3.0 to 3.6	–	–	0.9	–	0.9	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −20 μA	0.9	–	V_{CC} − 0.1	–	–	–	
			1.1 to 1.3	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.4 to 1.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.65 to 1.95	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			2.3 to 2.7	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			3.0 to 3.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
		I_{OH} = −0.5 mA	1.1 to 1.3	0.75 x V_{CC}	–	–	0.70 x V_{CC}	–	
		I_{OH} = −1 mA	1.4 to 1.6	1.07	–	–	0.99	–	
		I_{OH} = −1.5 mA	1.65 to 1.95	1.24	–	–	1.22	–	
		I_{OH} = −2.1 mA	2.3 to 2.7	1.95	–	–	1.87	–	
		I_{OH} = −2.6 mA	3.0 to 3.6	2.61	–	–	2.55	–	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OL} = 20 μA	0.9	–	0.1	–	–	–	
			1.1 to 1.3	–	–	0.1	–	0.1	
			1.4 to 1.6	–	–	0.1	–	0.1	
			1.65 to 1.95	–	–	0.1	–	0.1	
			2.3 to 2.7	–	–	0.1	–	0.1	
			3.0 to 3.6	–	–	0.1	–	0.1	
		I_{OL} = 0.5 mA	1.1 to 1.3	–	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
		I_{OL} = 1 mA	1.4 to 1.6	–	–	0.31	–	0.37	
		I_{OL} = 1.5 mA	1.65 to 1.95	–	–	0.31	–	0.35	
		I_{OL} = 2.1 mA	2.3 to 2.7	–	–	0.31	–	0.33	
		I_{OL} = 2.6 mA	3.0 to 3.6	–	–	0.31	–	0.33	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±0.5	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V or V_{OUT} = 0 V to 3.6 V	0	–	–	0.5	–	0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	0.9 to 3.6	–	–	0.9	–	0.9	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

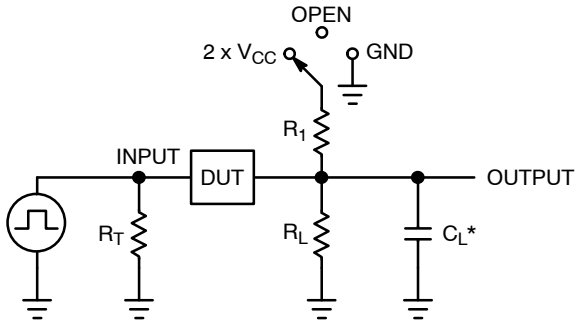
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	R_L = 1 MΩ, C_L = 10 pF	0.9	–	40.7	–	–	–	ns
			1.10 to 1.30	–	10.9	23.5	–	31.0	
			1.40 to 1.60	–	5.6	12.0	–	14.0	
			1.65 to 1.95	–	3.7	10.0	–	12.0	
			2.3 to 2.7	–	2.7	7.0	–	8.0	
			3.0 to 3.6	–	2.1	6.0	–	7.0	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	0.9	–	42.2	–	–	–	ns
			1.10 to 1.30	–	11.4	24.9	–	34.0	
			1.40 to 1.60	–	6.0	13.0	–	16.0	
			1.65 to 1.95	–	4.0	10.0	–	12.0	
			2.3 to 2.7	–	3.0	7.0	–	8.0	
			3.0 to 3.6	–	2.3	6.0	–	7.0	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	R_L = 1 MΩ, C_L = 30 pF	0.9	–	46.4	–	–	–	ns
			1.10 to 1.30	–	13.0	28.9	–	43.0	
			1.40 to 1.60	–	7.3	16.0	–	18.0	
			1.65 to 1.95	–	5.1	12.0	–	14.0	
			2.3 to 2.7	–	3.7	9.0	–	10.0	
			3.0 to 3.6	–	2.9	7.0	–	9.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	2.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, V_{CC} = 0.9 to 3.6 V, V_{IN} = 0 V or V_{CC}	6.0	pF

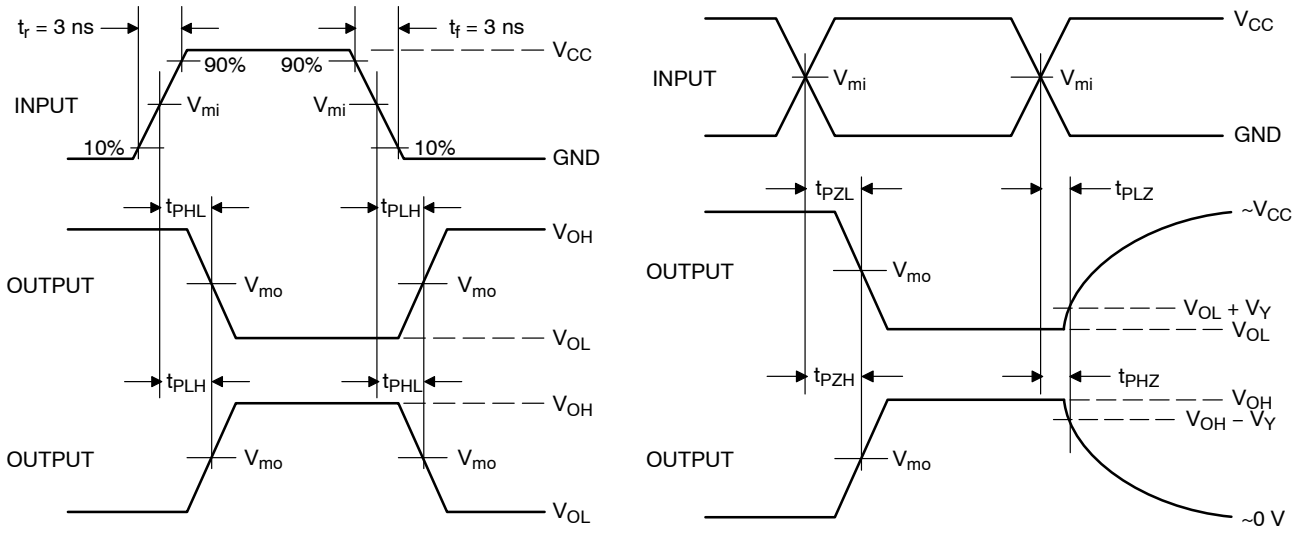
5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

Figure 3. Test Circuit



V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	V_{CC} / 2	V_{CC} / 2	0.1
1.1 to 1.3	V_{CC} / 2	V_{CC} / 2	0.1
1.4 to 1.6	V_{CC} / 2	V_{CC} / 2	0.1
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	1.5	1.5	0.3

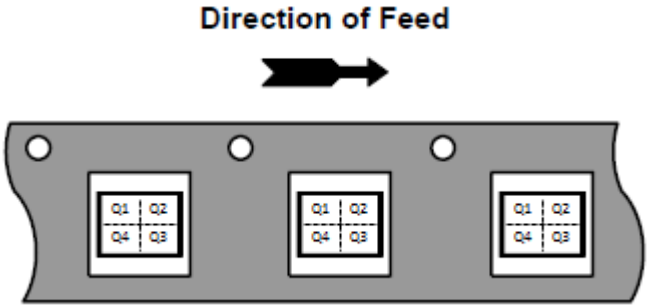
Figure 4. Switching Waveforms

ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NC7WP00K8X	US8	WP00	Q4	3000 / Tape & Reel
NC7WP00L8X	MicroPak, UQFN8	Y3	Q4	5000 / Tape & Reel

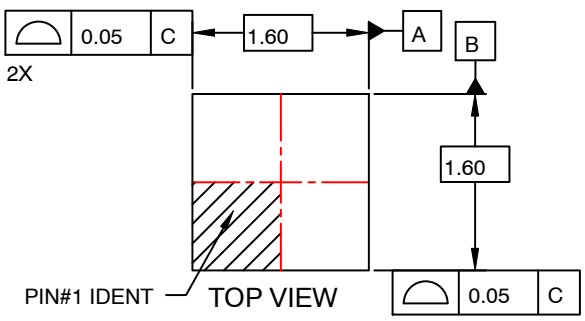
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

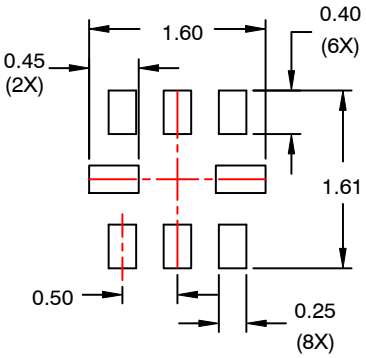
Pin 1 Orientation in Tape and Reel



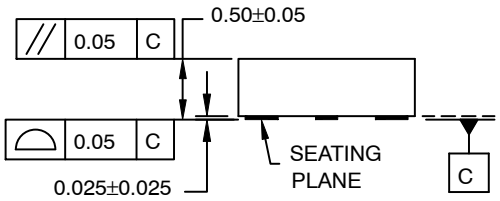
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016





RECOMMENDED
LAND PATTERN



SIDE VIEW

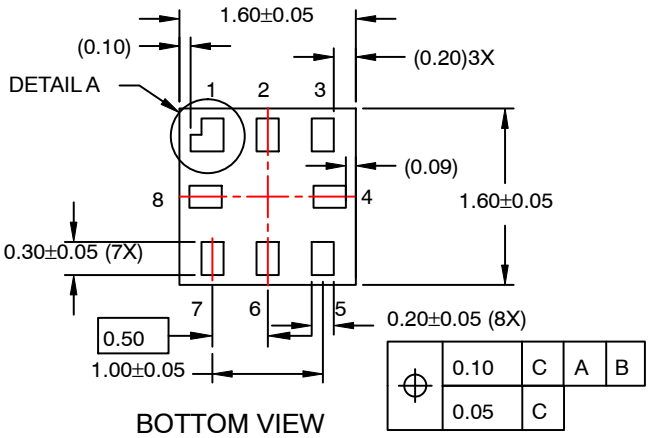
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

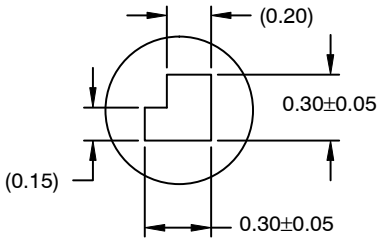
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



DETAIL A
SCALE : 2X

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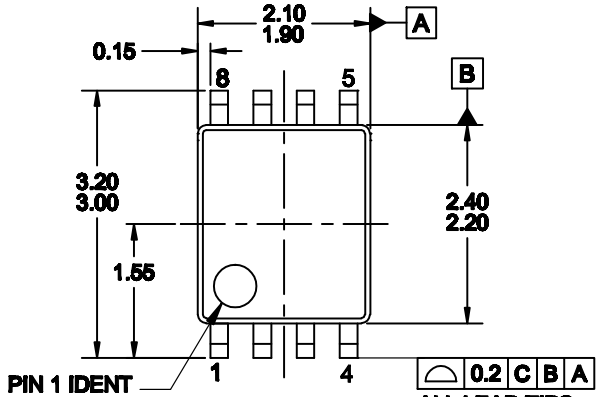
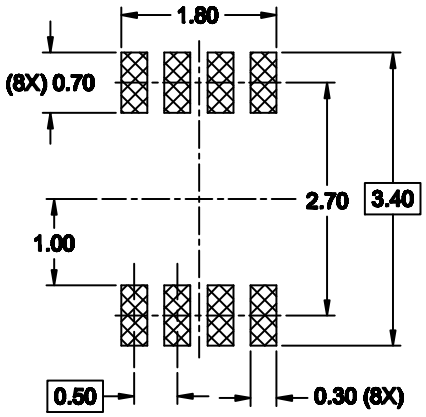
US8
CASE 846AN
ISSUE O

DATE 31 DEC 2016



TOP VIEW



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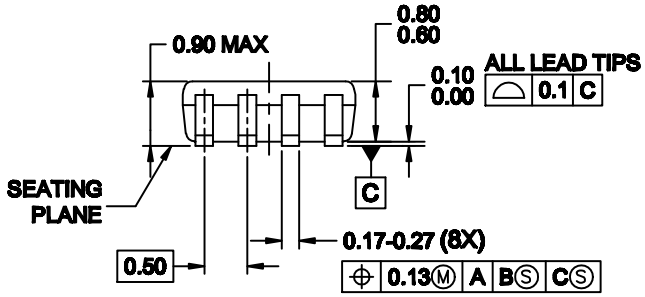


SIDE VIEW

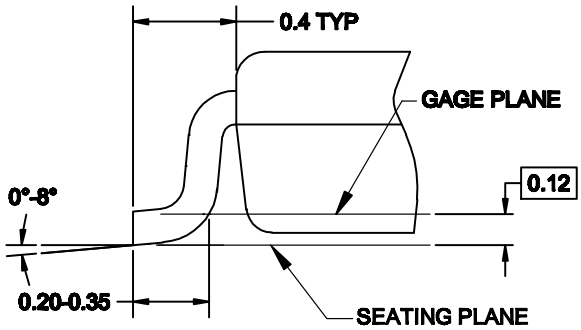
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187

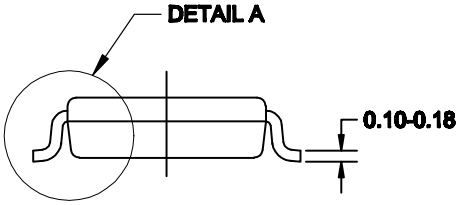
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



DETAIL A



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