28 Gbps, 5-Bit, Digital Time Delay with Programmable Output Voltage

Data Sheet **HMC856**

FEATURES

- Differential and single-ended operation
- Supports data rates up to 28 Gbps
- Fast rise/fall time: 20 ps/18 ps
- Low power consumption: 610 mW typical
- Programmable differential
- Output voltage swing: 500 mV p-p to 1350 mV p-p
- Single supply: −3.3 V
- 5 mm × 5 mm, 32-terminal ceramic leadless chip carrier (LCC) package: 25 mm²

APPLICATIONS

- SONET OC-192
- High speed serial logic
- Clock and data recovery
- Broadband test and measurement equipment
- Frequency synthesis
- Matched timing

FUNCTIONAL BLOCK DIAGRAM

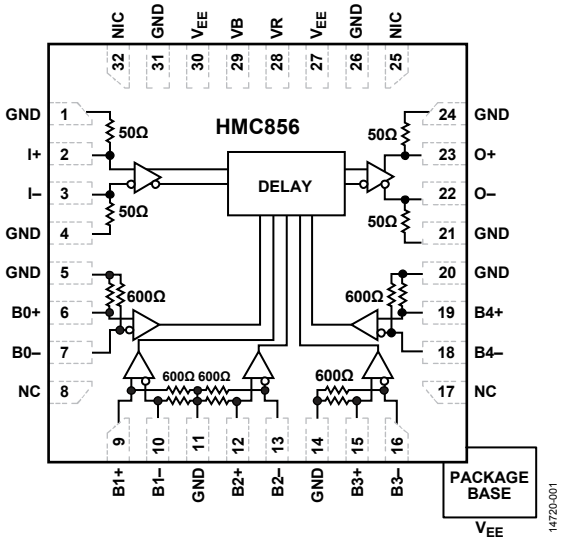

Figure 1.

GENERAL DESCRIPTION

The HMC856 is a wideband time delay device with a 5-bit digital control designed for timing compensation or clock skew management applications. The time delay provides nearly 100 ps (maximum) of delay range with 3 ps resolution and supports 28 Gbps data. The monotonic delay is compensated for stable operation over both power supply and temperature variation.

All differential inputs to the HMC856 are current mode logic (CML) and terminated on chip with 50 Ω to the positive supply ground, GND, and can be ac or dc-coupled. The differential CML outputs are source terminated to 50 Ω and can also be ac or dc-coupled. Connect outputs directly to a 50 Ω ground terminated system or drive devices with CML logic input. The control lines, B4 to B0, are differential CML inputs terminated with 600 Ω to the positive rail, which supports lower power control options. The HMC856 features an output level control pin, VR, that allows loss compensation or signal level optimization. The HMC856 operates from a single −3.3 V supply and is available in a 5 mm × 5 mm LCC package.

Rev. D

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Technical Support
www.analog.com

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This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

12/2016—Rev. 01.0611 to Rev. C

Updated Format ... Universal
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{EE} = −3.3 V, VR = 0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Voltage	V_{EE}		−3.7	−3.3	−2.9	V
Current				185		mA
POWER CONSUMPTION				610		mW
MAXIMUM DATA RATE					28	Gbps
INPUT VOLTAGE		CML logic input				
Single-Ended			−1.5		+0.5	V
Differential			0.1		2.0	V
OUTPUT						
Rise/Fall Time	t_R, t_F	Differential, 20% to 80%		20/18		ps
Single-Ended Amplitude				565		mV p-p
Differential Amplitude			500	1130	1350	mV p-p
High Voltage				−20		mV
Low Voltage				−585		mV
RETURN LOSS		Frequency <12 GHz				
Input				10		dB
Output				10		dB
JITTER						
Random	J_R	RMS		0.2		ps rms
Deterministic	J_D	2^{15} − 1 pseudo random binary sequence (PRBS) 28 Gbps input		<2		ps p-p
VR PIN CURRENT		VR = 0 V		3		mA
		VR = 0.4 V			4.25	mA
DELAY						
Propagation Delay Data to Data	t_{PROP}			255		ps
Control Range				92		ps
Temperature Variation		T_A = 85°C	9		12	ps
		T_A = −40°C	4		8	ps
Resolution	t_{PROG_DELAY}			3		ps

TIMING DIAGRAM

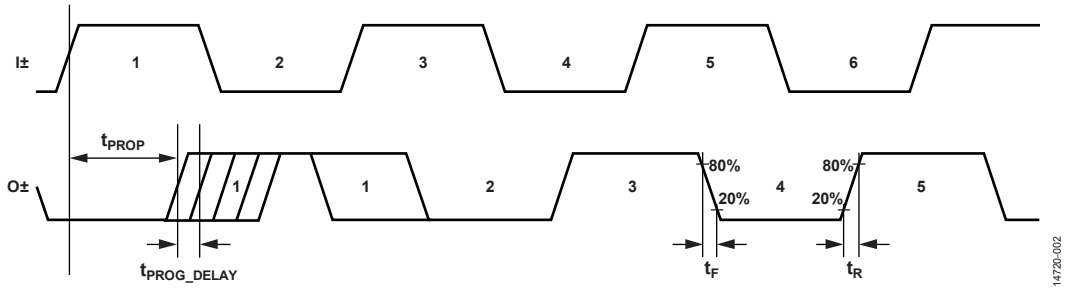

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Power Supply Voltage (V_{EE})	−3.75 V to +0.5 V
Input Signals	−2 V to +0.5 V
Output Signals	−1.5 V to 0.5 V
Maximum Junction Temperature	125°C
Continuous Power Dissipation, P_{DISS} (T = 85°C, Derate 33 mW/°C Above 85°C)	1.33 W
Thermal Resistance, θ_{JC} (Worst Case Device to Package Exposed Paddle)	30°C/W
Temperature	
Storage	−65°C to +150°C
Operating	−40°C to +85°C
Reflow (MSL3 Rating)	260°C
ESD Sensitivity Human Body Model (HBM)	Class 1C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

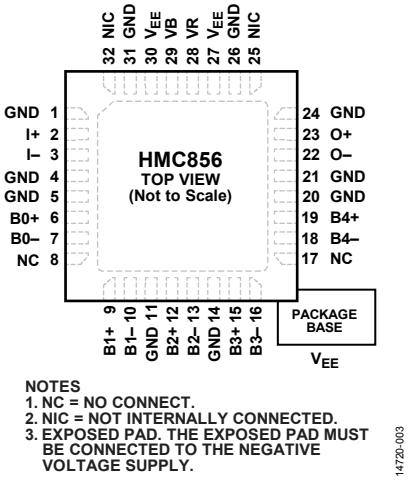

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 4, 5, 11, 14, 20, 21, 24	GND	Signal Ground.
2, 3	I+, I–	Differential Data Inputs. CML referenced to positive supply.
6, 7, 9, 10, 12, 13, 15, 16, 18, 19	B0+, B0–, B1+, B1–, B2+, B2–, B3+, B3–, B4–, B4+	Differential Digital Control Inputs. CML referenced to positive supply.
8, 17	NC	No Connect. These pins are internally connected to the device. These pins can be connected to radio frequency (RF)/dc ground without affecting performance.
25, 32	NIC	Not Internally Connected. These pins can be connected to radio frequency (RF)/dc ground without affecting performance.
22, 23	O–, O+	Differential Data Outputs. CML referenced to positive supply, 50 Ω termination.
26, 31	GND	Supply Ground.
27, 30	V_{EE}	Negative Supply Voltage. These pins and the exposed pad must be connected to the negative voltage supply.
28	VR	Output Level Control. Output levels can be increased or decreased by applying voltage to VR, as shown in Figure 12.
29	VB	DC Bias Voltage. VB must be connected to ground.
	EPAD (V_{EE})	Exposed Pad. The exposed pad must be connected to the negative voltage supply.

INTERFACE SCHEMATICS

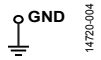

Figure 4. GND Interface Schematic

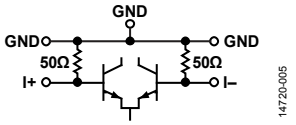

Figure 5. I+, I– Interface Schematic

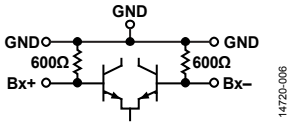

Figure 6. B_X+, B_X– Interface Schematic

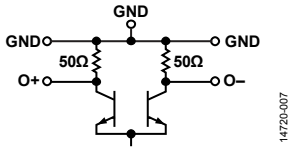

Figure 7. O+, O– Interface Schematic

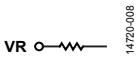

Figure 8. VR Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

V_{EE} = −3.3 V, VR = 0 V, 400 mV, 28 Gbps, PRBS $2^{15} - 1$, input applied, unless otherwise noted.

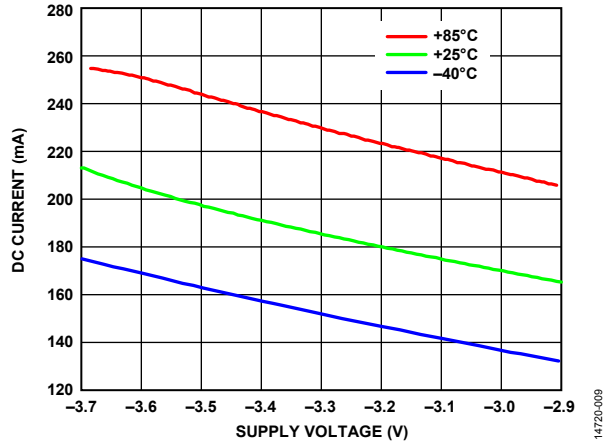

Figure 9. DC Current vs. Supply Voltage, VR = 0 V at Various Temperatures

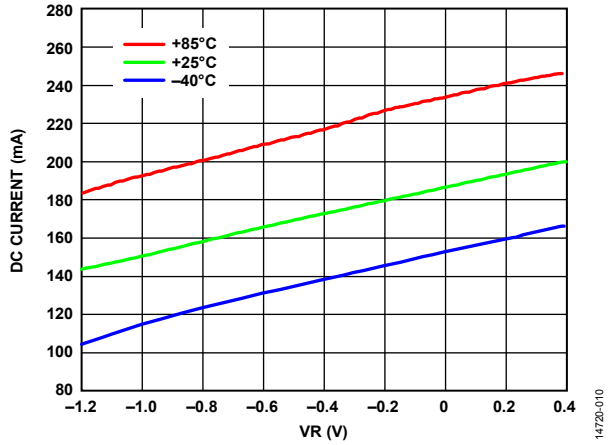

Figure 10. DC Current vs. VR at Various Temperatures

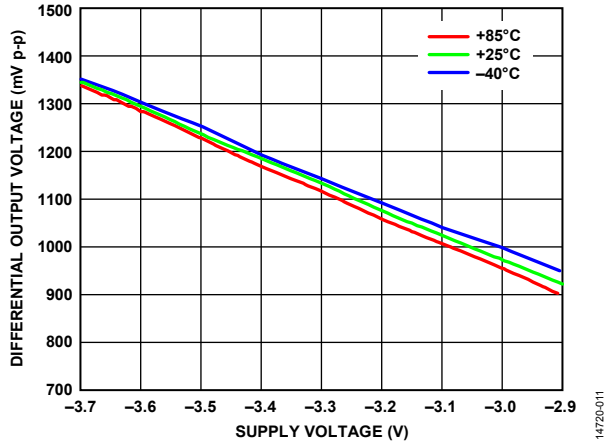

Figure 11. Differential Output Voltage vs. Supply Voltage at Various Temperatures

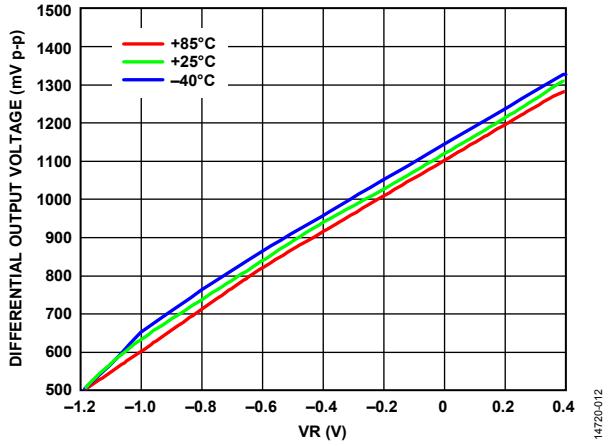

Figure 12. Differential Output Voltage vs. VR at Various Temperatures

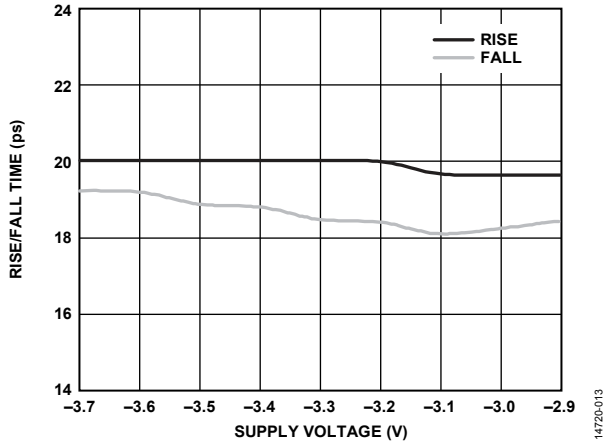

Figure 13. Rise/Fall Time vs. Supply Voltage

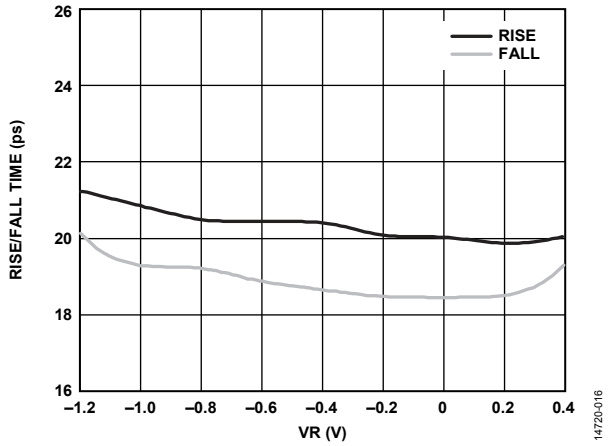

Figure 14. Rise/Fall Time vs. VR

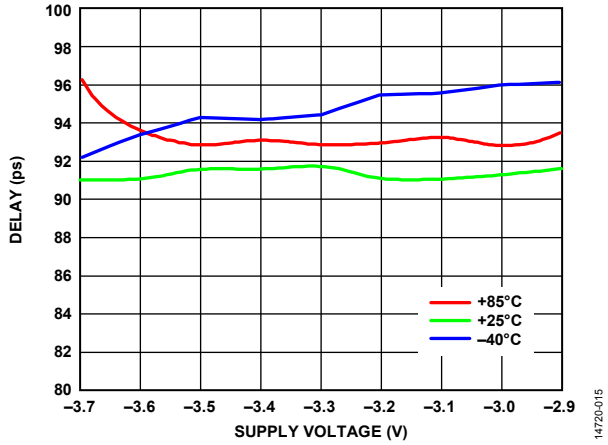

Figure 15. Delay vs. Supply Voltage at Various Temperatures

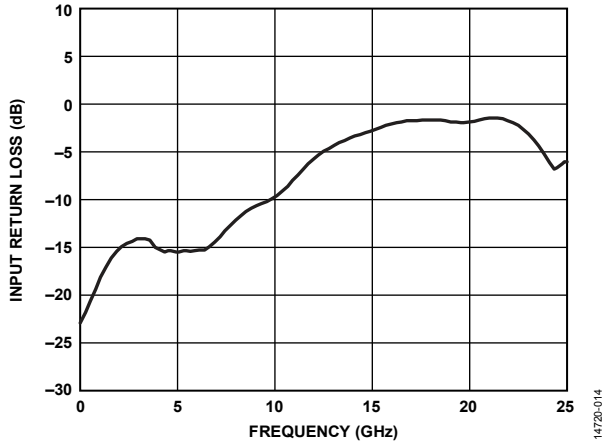

Figure 16. Input Return Loss vs. Frequency
(Device Measured on an Evaluation Board with Port Extensions)

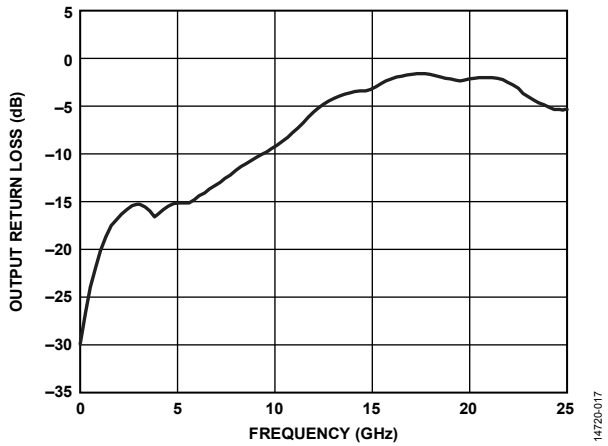

Figure 17. Output Return Loss vs. Frequency
(Device Measured on an Evaluation Board with Port Extensions)

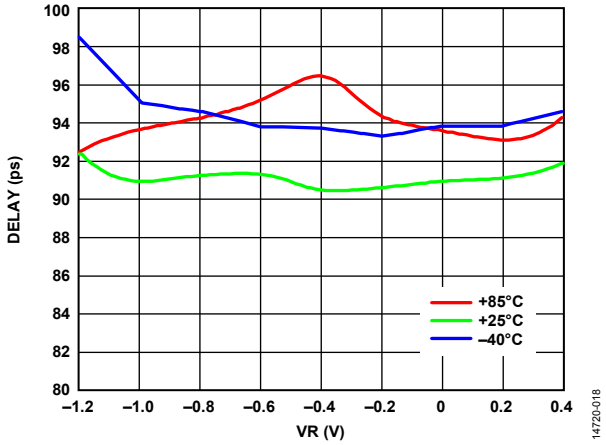

Figure 18. Delay vs. VR at Various Temperatures

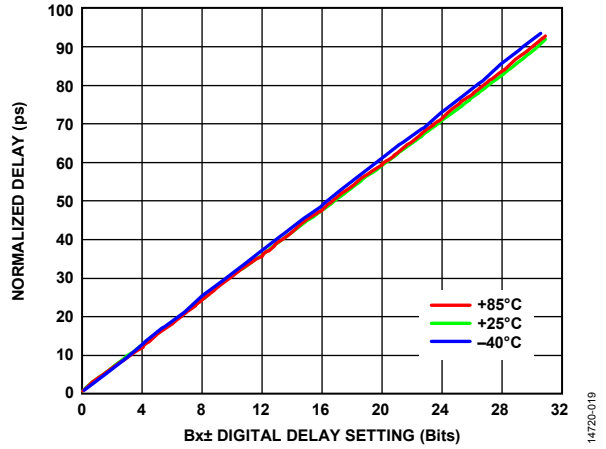

Figure 19. Normalized Delay vs. Bx± Digital Delay Setting
(Device Measured on an Evaluation Board with Port Extensions Normalized to Minimum Delay, 0 Setting (B4±:B0± = 00000), at its Respective Temperature)

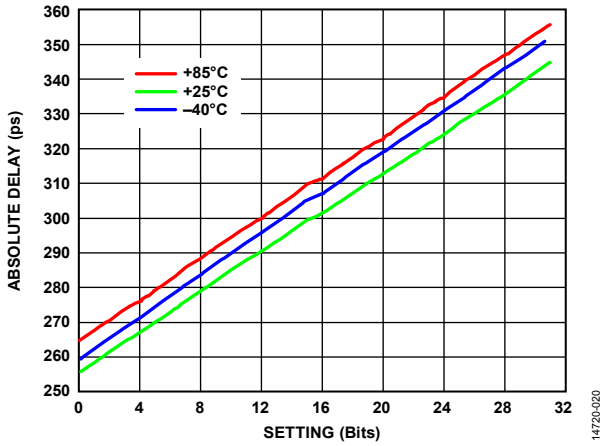

Figure 20. Absolute Delay vs. Setting
(Normalized to 0 Setting at its Respective Temperature)

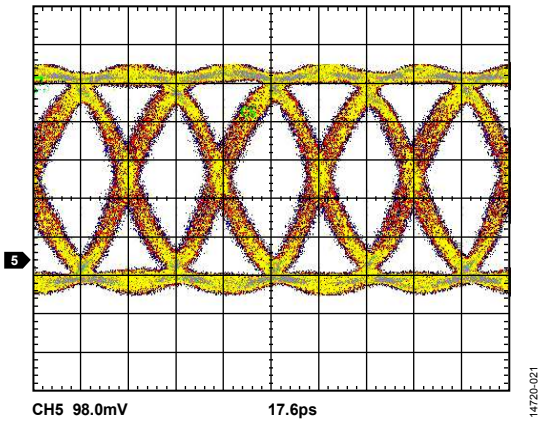

Figure 21. Single-Ended Output Eye Diagram at 28 Gbps, Measured V_{OUT} = 550 mV p-p

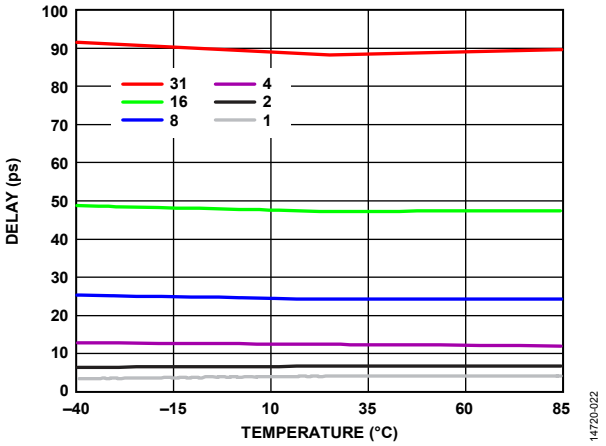

Figure 22. Delay vs. Temperature at Various Bit Settings (Device Measured on an Evaluation Board with Port Extensions)

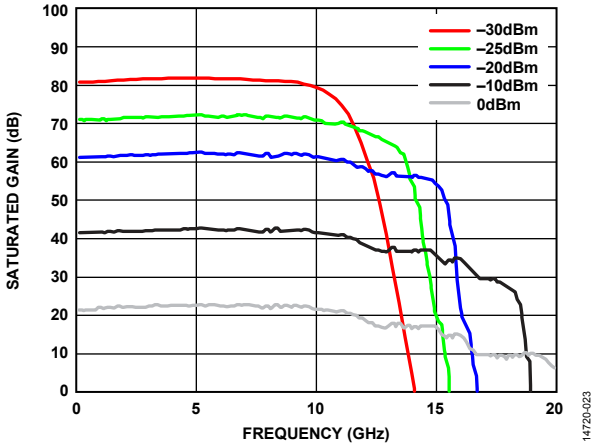

Figure 23. Saturated Gain vs. Frequency at Various Input Powers (Device Measured on an Evaluation Board with Port Extensions), The Output is Saturated, Limiting the Gain for Larger Input Signals, Gain ≈ Saturated Output Power – Input Power

THEORY OF OPERATION

The HMC856 is a wideband time delay device with a 5-bit digital control designed for timing compensation or clock skew management applications. The HMC856 operates from a single −3.3 V supply and is available in a 5 mm × 5 mm LCC package.

The HMC856 can support data rates up to 28 Gbps and is able to provide 100 ps variable delay with 3 ps resolution. The total propagation delay of the HMC856 varies between 250 ps and 350 ps. The maximum achievable bandwidth of the HMC856 depends on the power of the input signal. The highest bandwidth of the device is at the larger input power levels, as shown in Figure 23.

The HMC856 uses a CML interface, which uses 50 Ω internal terminations to the ground. The input and output pins can be interfaced with either ac or dc coupling. For ac coupling, using a series resistor, which is effectively short circuit, and an ac load of 50 Ω is recommended. For dc coupling, inputs and outputs can be directly interfaced with another CML circuit. The control lines, B4 to B0, are also CML, but they are terminated with 600 Ω to the positive rail for low power operation.

The HMC856 features an output level control pin, VR, that allows loss compensation or signal level optimization. VR can have a voltage value between −1.2 V and 0.4 V, which results in a differential output swing of 500 mV p-p and 1350 mV p-p. Increasing the output swing affects the rise and fall times. As VR becomes higher, the rise and fall times increase. Changing the VR pin also changes the power dissipation because the HMC856 can consume between 140 mA and 200 mA at room temperature depending on the VR pin.

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The evaluation PCB of the HMC856 uses RF circuit design techniques. Signal lines must have 50 Ω impedance whereas the package ground leads must connect directly to the ground plane similar to that shown in Figure 25. The exposed metal package base must connect to V_{EE}. A sufficient number of via holes must connect the top and bottom ground planes. The evaluation PCB shown in Figure 24 is available from Analog Devices, Inc., upon request. Install a jumper on the JP1 header to short VR to GND for normal operation.

Table 4. Bill of Materials for the Evaluation PCB 127102-HMC856LC5[1]

Item	Description
J1 to J4	K connectors
J5	0.1 inch 2 × 5 header
J7 to J14	0.04 inch dc pin
JP1	0.1 inch 2 position header with shunt
C1, C2	4.7 µF capacitor, Case A
C3 to C5	100 pF capacitor, 0402 package
R1, R8	10 Ω resistor, 0603 package
R2	1.2 kΩ resistor, 0603 package
R3 to R7	2.7 kΩ resistor, 0603 package
U1	28 Gbps digital time delay HMC856
PCB[2]	127100 evaluation board PCB

[1] 127100 is the raw bare PCB. Reference 127102-HMC856LC5 when ordering the complete evaluation PCB.
[2] Use Arlon 25FR or Rogers 4350 for circuit board material.

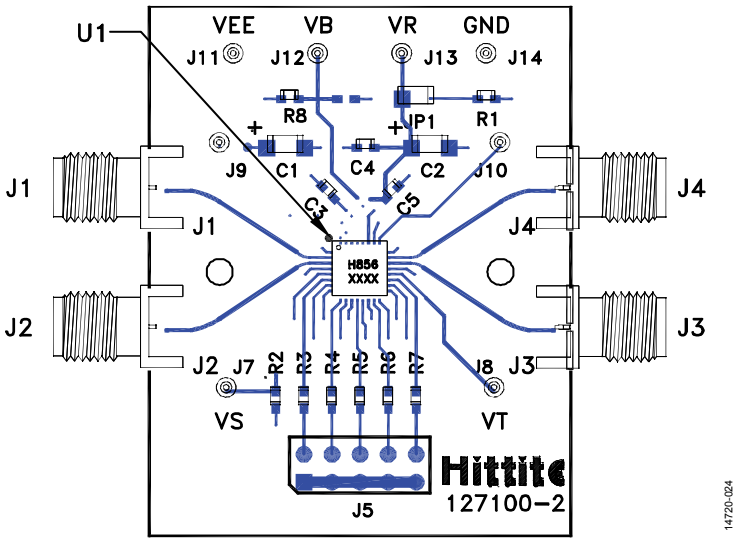

Figure 24. Evaluation Board Layout, Top Side

TYPICAL APPLICATION CIRCUIT

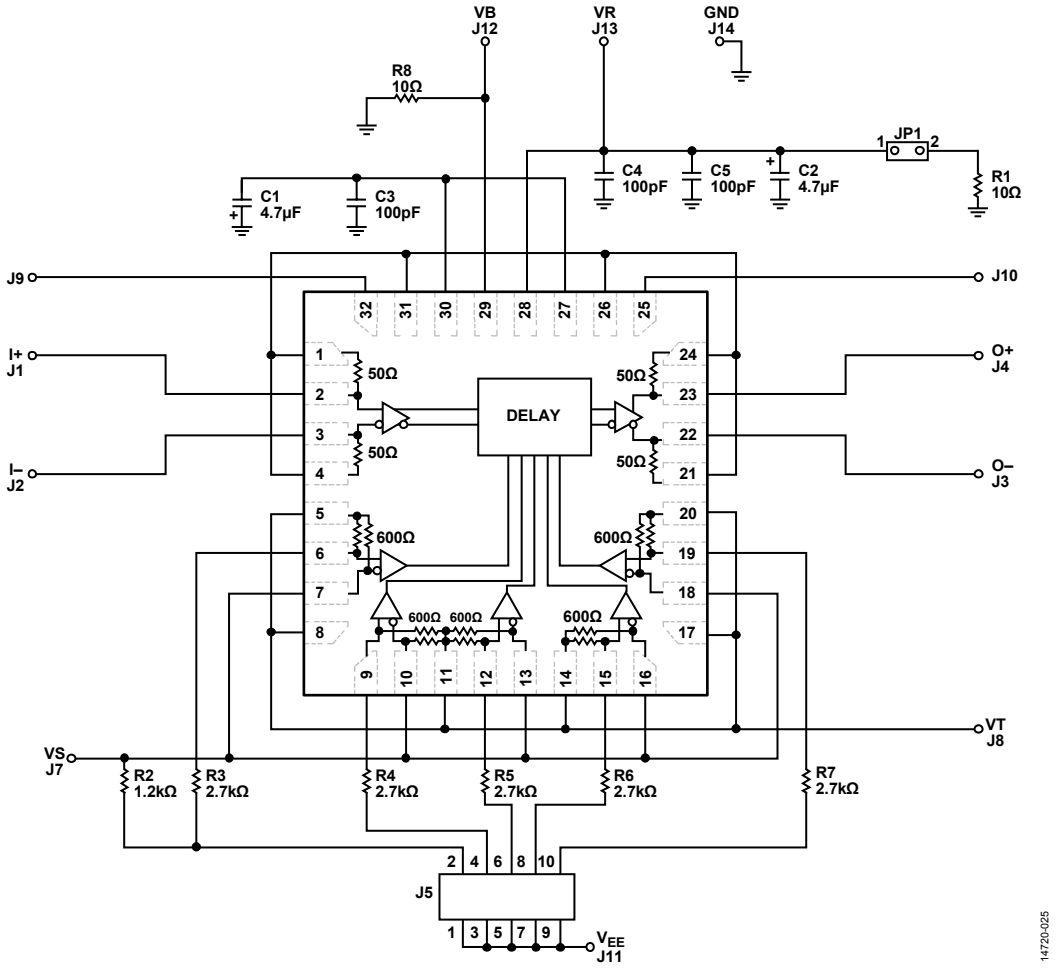

Figure 25. Typical Application Circuit

OUTLINE DIMENSIONS

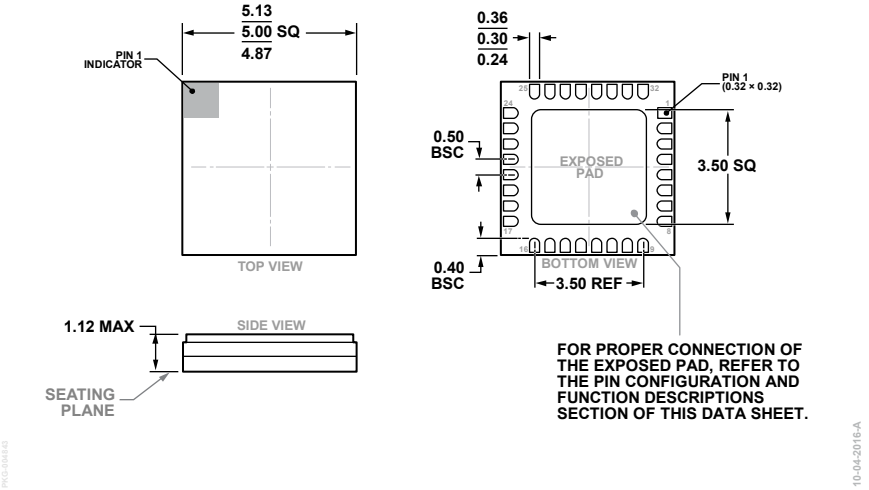

Figure 26. 32-Terminal Ceramic Leadless Chip Carrier [LCC]
(HE-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Moisture Sensitivity Level (MSL) Rating[2]	Package Description	Package Option
HMC856LC5	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	HE-32-1
HMC856LC5TR	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	HE-32-1
HMC856LC5TR-R5	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	HE-32-1
127102-HMC856LC5			Evaluation Board	

[1] All models are RoHS compliant parts.
[2] See the Absolute Maximum Ratings section.