DUAL OUTPUT SPREAD SPECTRUM CLOCK SYNTHESIZER

IDT6V40088

Description

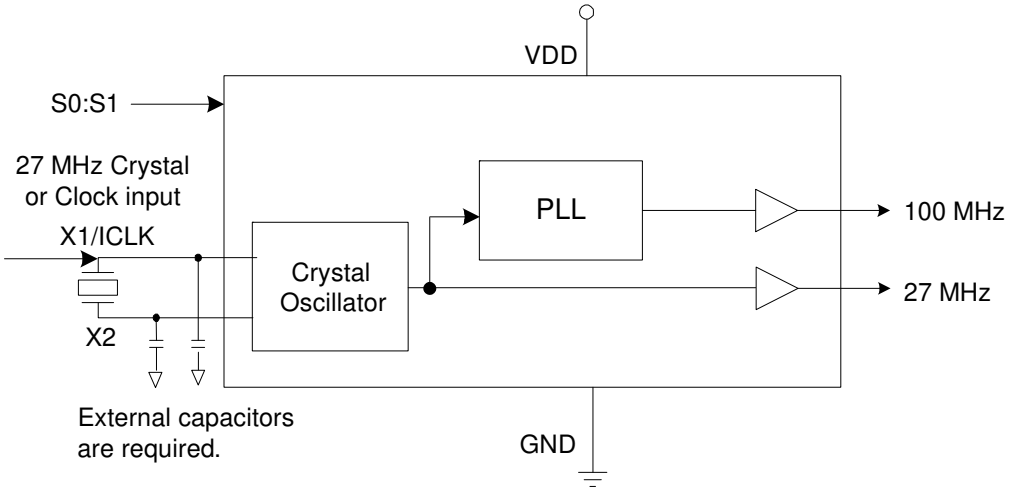
The IDT6V40088 is a low cost, dual-output clock synthesizer. The IDT6V40088 generates a 100 MHz and 27 MHz output from a 27 MHz crystal or clock input. The 100 MHz output may employ Spread Spectrum to reduce system electro-magnetic interference (EMI).

The device employs Phase-Locked Loop (PLL) techniques to run from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

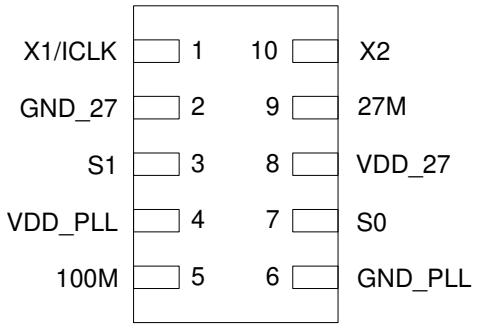
Features

- 10-pin 3x3mm DFN package
- Input crystal or clock frequency of 27 MHz
- 32 kHz Spread Spectrum Modulation
- Adjustable down spread
- Operating voltage of 3.3 V
- Replaces multiple crystals and oscillators
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



10-pin DFN (3x3mm)

100 MHz Spread Selection Table

S1	S0	Down Spread%
		-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Connect this pin to a 27 MHz crystal or external clock input.
2	GND_27	Power	27 MHz ground. Connect to ground.
3	S1	Input	Down spread select pin. See table above.
4	VDD_PLL	Power	PLL VDD. Connect to +3.3 V.
5	100M	Output	100 MHz clock output.
6	GND_PLL	Power	PLL ground. Connect to ground.
7	S0	Input	Down spread select pin. See table above.
8	VDD_27	Power	27 MHz VDD. Connect to +3.3 V.
9	27M	Output	27 MHz clock output.
10	X2	XO	Connect this pin to a 27 MHz crystal, or float for clock input.
11	GPAD	NC	Thermal ground pad. Electrically isolated from die.

External Components

The IDT6V40088 requires a minimum number of external components for proper operation.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high-performance mixed-signal IC, the IDT6V40088 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane. A 1Ω isolation resistor between VDD_27 and VDD_PLL will improve performance.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT6V40088. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Spread Spectrum Modulation

The IDT6V40088 utilizes frequency modulation (FM) to distribute energy over a range of frequencies. By modulating the output clock frequencies, the device effectively lowers energy across a broader range of frequencies; thus, lowering a system's electro-magnetic interference (EMI). The modulation rate is the time from transitioning from a minimum frequency to a maximum frequency and then back to the minimum.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6V40088. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND	-0.5		7	V
Inputs	Referenced to GND	-0.5		VDD+ 0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+2.97	+3.3	+3.63	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.97	3.3	3.63	V
Operating Supply Current	IDD	C_L = 15 pF, VDD = 3.63 V, T_A = +85°C		47	55	mA
		C_L = 5 pF, VDD = 3.63 V, T_A = +85°C		44	47	
Input High Voltage	V_{IH}		VDD-0.8			V
Input Low Voltage	V_{IL}	S0:S1			0.8	V
Input Mid Voltage	V_{IM}	S0:S1	VDD/2-0.4		VDD/2+0.4	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}			±70		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-down Resistor	R_{PD}	S0, S1		200	260	kΩ
Input Capacitance	C_{IN}	inputs			5	pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C, C_L = 5 pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental Crystal		27		MHz
		Input Clock		27		MHz
Output Rise/Fall Time	t_{RF5}	20% to 80%, Note 1		1	1.5	ns
	t_{RF15}	80% to 20%, Note 2		1.5	2	ns
	t_{RF5}	20% to 80%, Note 3		0.75	1	ns
	t_{RF15}	20% to 80%, Note 4		1.5	1.75	ns
Synthesis Error	t_{PPM}	100M output		0		ppm
Duty Cycle	t_{DC}		45	50	55	%
Modulation Frequency	f_{MOD}	100M		32		kHz
Modulation Type Slew Rate		100M output, triangular*			0.125	%/µs
Power-up Time		PLL lock time from power-up			5	ms
Cycle-to-cycle Jitter				125	200	ps
Long-term Jitter (10,000 cycles)		S0=S1=0, 100M, 27M		200	300	ps

Note 1: 27M measured with 5 pF load.

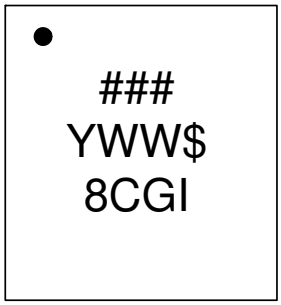
Note 2: 27M measured with 15 pF load.

Note 3: 100M measured with 5 pF load.

Note 4: 100M measured with 15 pF load.

* Spread 2% and below.

Marking Diagram

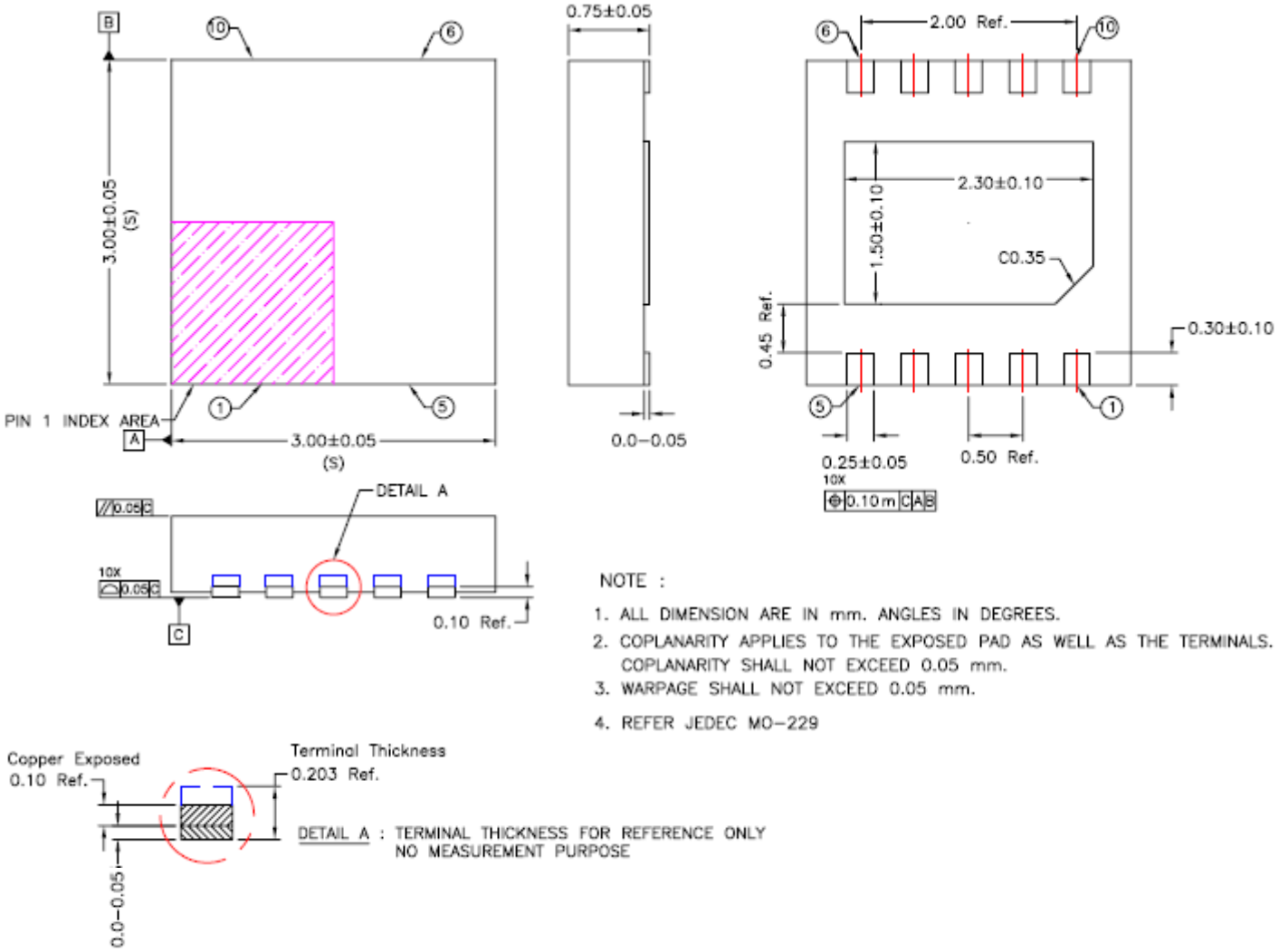


Notes:

1. ### is the lot number.
2. YYW is the last digit of the year and week that the part was assembled. “$” is the assembler mark code.
3. “8C” is the truncated part number and revision ID.
4. “G” denotes RoHS compliant package.
5. “I” denotes industrial temperature range.
6. Bottom marking: country of origin.

Package Outline and Package Dimensions (10-pin DFN 3x3mm)

Package dimensions are kept current with JEDEC Publication No. 95,



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. REFER JEDEC MO–229

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
6V40088CNBGI	See Page 6	Tubes	10-pin DFN	-40 to +85° C
6V40088CNBGI8		Tape and Reel	10-pin DFN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	P.Keyashian	10/29/08	New device; Preliminary release.
B	R. Wade	11/13/08	Updated pinout/pin description table; added text to “Decoupling Capacitor” section; various updates to AC/DC char tables.
C	R. Wade	03/26/09	Removed Low Drive reference in DC char table; added top-side marking; update duty cycle specs; changed orderable part number to reflect “C” revision of device; released to final.
D	R. Wade	03/31/09	Added IDD for C_L = 5 pF.
E		12/14/09	Various updates to AC/DC char tables.

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