8-Bit Shift Register with Output Register

MC74VHC594

The MC74VHC594 is an 8−bit shift register designed for 2.0 V to 5.5 V V_{CC} operation. The device contain an 8−bit serial−in, parallel−out shift register that feeds an 8−bit D−type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on the shift and storage registers. A serial output (Q_H’) is provided for cascading purposes.

The shift−register (SRCLK) and storage−register (RCLK) clocks are positive−edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

Features

- 2.0 V to 5.5 V V_{CC} Operation
- High Speed: f_{max} = 185 MHz (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 1.0 V (Max)
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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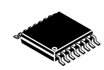
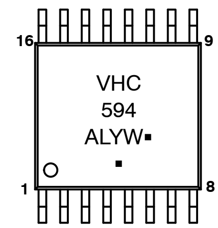
MARKING DIAGRAM

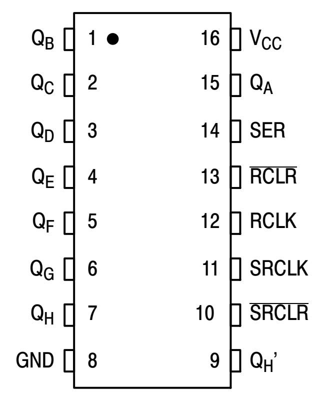


TSSOP−16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC594DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel
NLV74VHC594DTR2G*	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

August, 2021 − Rev. 1

Publication Order Number:
MC74VHC594/D

FUNCTION TABLE

INPUT					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{RCLR}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

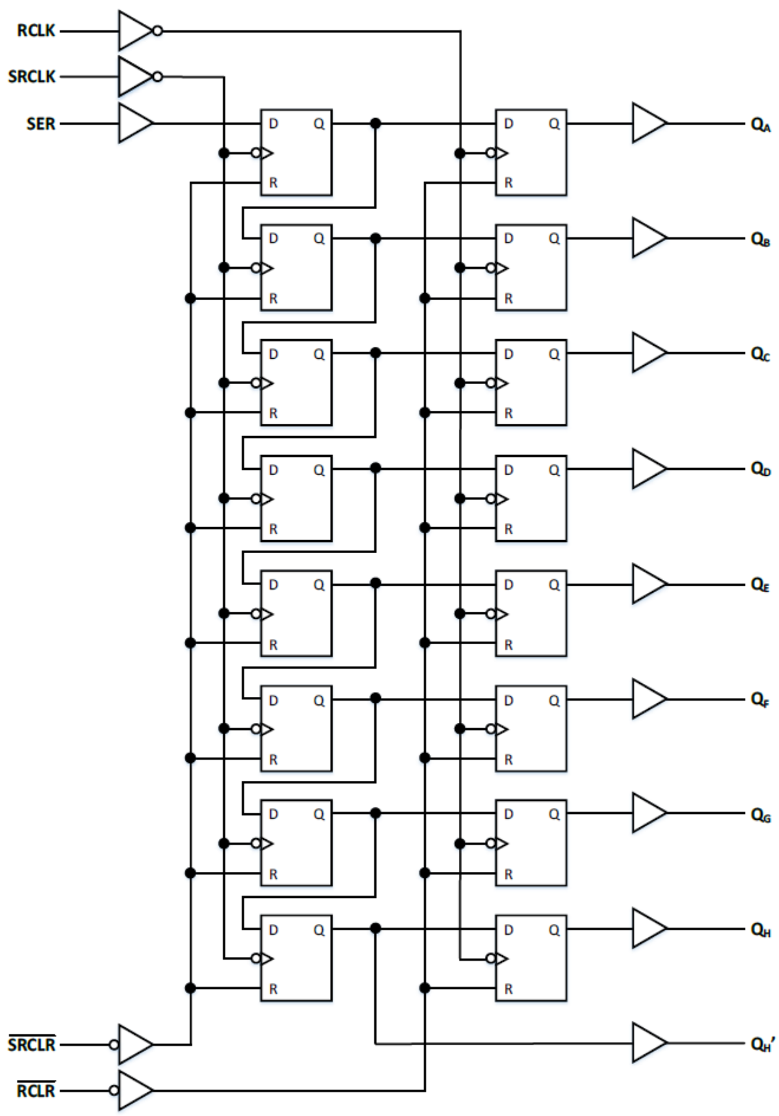


Figure 1. Logic Diagram

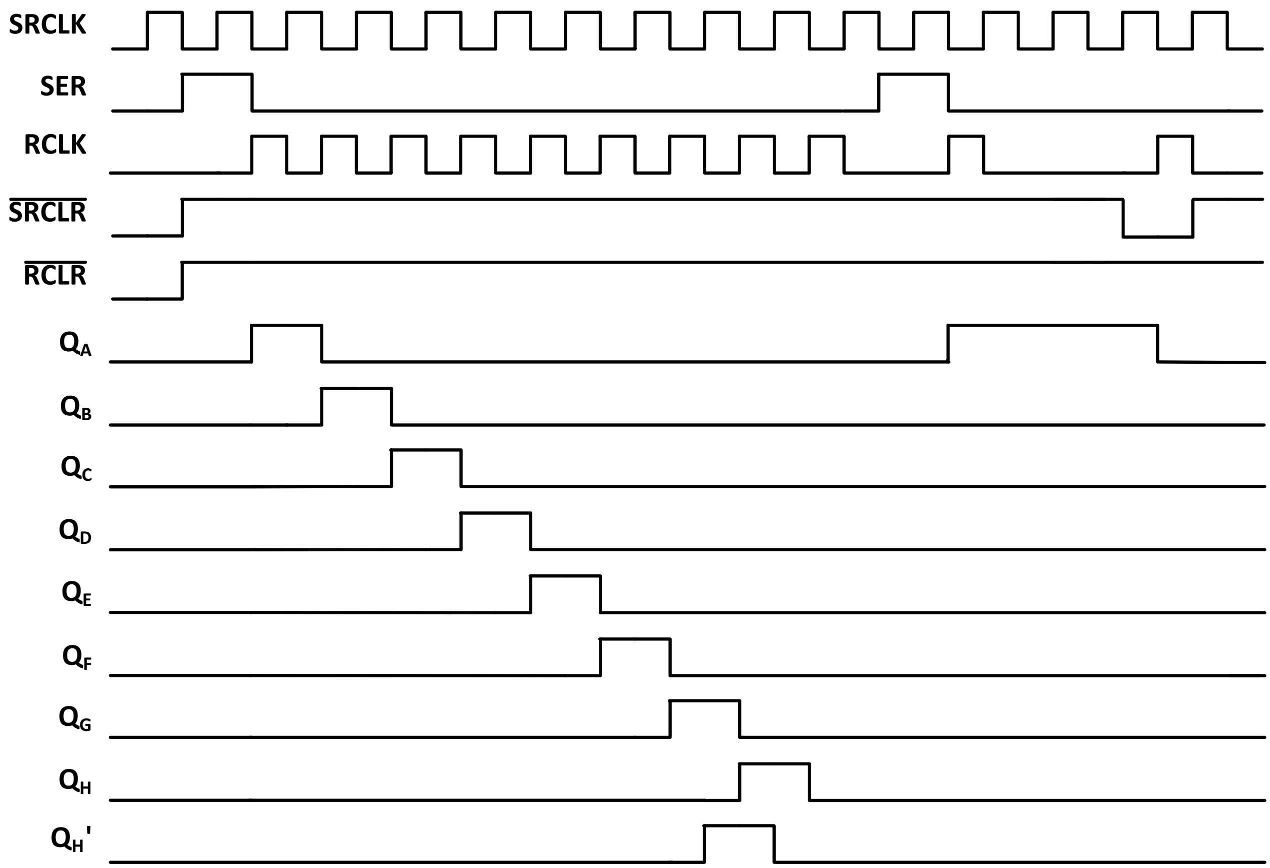


Figure 2. Timing Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_O	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Clamp Current		−20	mA
I_{OK}	DC Output Clamp Current		±20	mA
I_{IN}	DC Input Current		±20	mA
I_O	DC Output Source / Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
I_{GND}	DC Ground Current per Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)		62.2	°C/W
P_D	Power Dissipation in Still Air		2	W
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 254 mm^2, 2 ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	5.5	V
V_{IN}	DC Input Voltage (Referenced to GND)		0	5.5	V
V_O	DC Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 2.0 V	0	20	nS/V
		V_{CC} = 2.3 V to 2.7 V	0	20	
		V_{CC} = 3.0 V to 3.6 V	0	10	
		V_{CC} = 4.5 V to 5.5 V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \le$ 85°C Min	Max	$T_A \le$ 125°C Min	Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 4.5 5.5			0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = − 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		
V_{OL}	Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	2.0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V	0			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Supply Current	$V_I = V_{CC}$ or GND, I_O = 0 A	5.5			4.0		40.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0 ns, Figures 3 to 7)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = 25°C Limit	$T_A \le$ 85°C Limit	$T_A \le$ 125°C Limit	Unit
t_{su}	Setup Time, SER before SRCLK↑↓	3.3 5.0	– –	3.5 3.0	3.5 3.0	3.5 3.0	ns
	Setup Time, SRCLK↑ to RCLK↑	3.3 5.0	– –	8.0 5.0	8.5 5.0	8.5 5.0	ns
	Setup Time, $\overline{SRCLR}$ low to RCLK↑	3.3 5.0	– –	8.0 5.0	9.0 5.0	9.0 5.0	ns
t_h	Hold Time, SER before SRCLK↑↓	3.3 5.0	– –	2.0 2.0	2.0 2.0	2.0 2.0	ns
	Hold Time, $\overline{SRCLR}$ low to RCLK↑	3.3 5.0	– –	0.0 0.0	0.0 0.0	1.0 1.0	ns
t_{rec}	Recovery Time, $\overline{SRCLR}$ high to SRCLK↑	3.3 5.0	– –	3.0 2.5	3.0 2.5	3.0 2.5	ns
	Recovery Time, $\overline{RCLR}$ high to RCLK↑	3.3 5.0	– –	3.0 2.5	3.0 2.5	3.0 2.5	ns
t_W	Pulse Width, SRCLK or RCLK	3.3 5.0	– –	5.0 5.0	5.0 5.0	5.0 5.0	ns
	Pulse Width, $\overline{SRCLR}$ or $\overline{RCLR}$	3.3 5.0	– –	5.0 5.0	5.0 5.0	5.0 5.0	ns

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns, Figures 3 to 8)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)		3.0 to 3.6	80	150		70		70		MHz
			4.5 to 5.5	135	185		115		115		
t_{PLH}, t_{PHL}	Propagation Delay, SRCLK to Q_H'	C_L = 15pF C_L = 50pF	3.0 to 3.6		8.8 11.3	13.0 16.5	1.0 1.0	15.0 18.5	1.0 1.0	15.0 18.5	ns
		C_L = 15pF C_L = 50pF	4.5 to 5.5		6.2 7.7	8.2 10.2	1.0 1.0	9.4 11.4	1.0 1.0	9.4 11.4	
t_{PLH}, t_{PHL}	Propagation Delay, RCLK to Q_A–Q_H	C_L = 15pF C_L = 50pF	3.0 to 3.6		7.7 10.2	11.9 15.4	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		C_L = 15pF C_L = 50pF	4.5 to 5.5		5.4 6.9	7.4 9.4	1.0 1.0	8.5 10.5	1.0 1.0	8.5 10.5	
t_{PHL}	Propagation Delay, $\overline{SRCLR}$ to Q_H'	C_L = 15pF C_L = 50pF	3.0 to 3.6		8.4 10.9	12.8 16.3	1.0 1.0	13.7 17.2	1.0 1.0	13.7 17.2	ns
		C_L = 15pF C_L = 50pF	4.5 to 5.5		5.9 7.4	8.0 10.0	1.0 1.0	9.1 11.1	1.0 1.0	9.1 11.1	
t_{PHL}	Propagation Delay, $\overline{RCLR}$ to Q_A–Q_H	C_L = 15pF C_L = 50pF	3.0 to 3.6		7.7 10.2	11.9 15.4	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		C_L = 15pF C_L = 50pF	4.5 to 5.5		5.4 6.9	7.4 9.4	1.0 1.0	8.5 10.5	1.0 1.0	8.5 10.5	
C_{IN}	Input Capacitance				4	10		10		10	pF

Symbol	Parameter	V_{CC} (V)	Typ (T_A = 25°C)	Unit
C_{PD}	Power Dissipation Capacitance (Note 1)	5.0	87	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OLP}	Quiet Output, Dynamic V_{OL}		0.8	1.0	V
V_{OLV}	Quiet Output, Dynamic V_{OL}	–1.0	–0.8		V
V_{IHD}	High–Level Dynamic Input Voltage	3.5			V
V_{ILD}	Low–Level Dynamic Input Voltage			1.5	V

SWITCHING WAVEFORMS

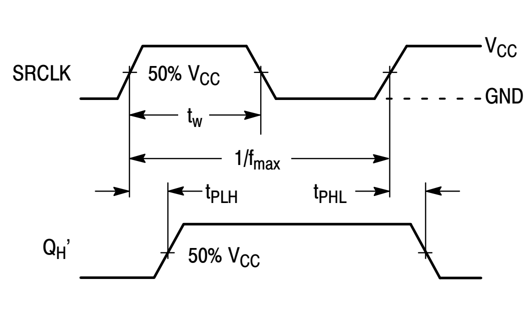


Figure 3.

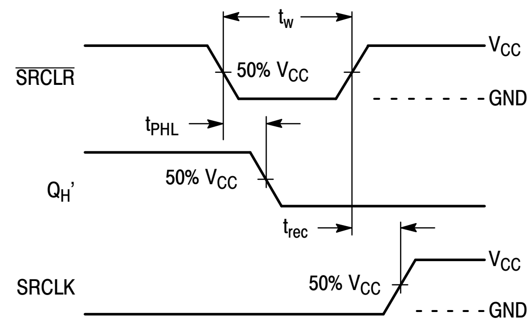


Figure 4.

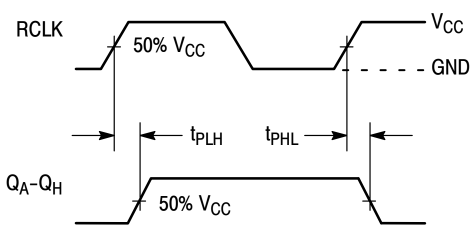


Figure 5.

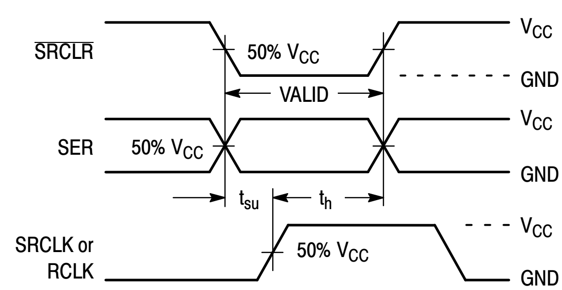


Figure 6.

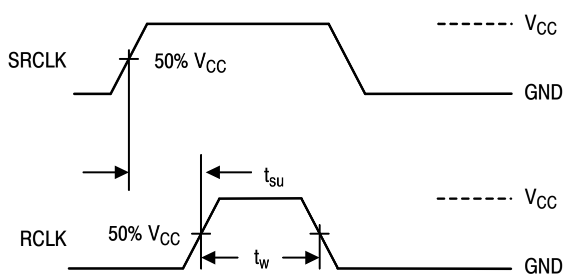
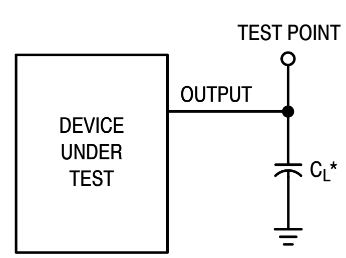


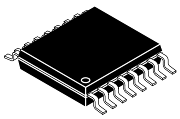
Figure 7.

TEST CIRCUIT



*Includes all probe and jig capacitance

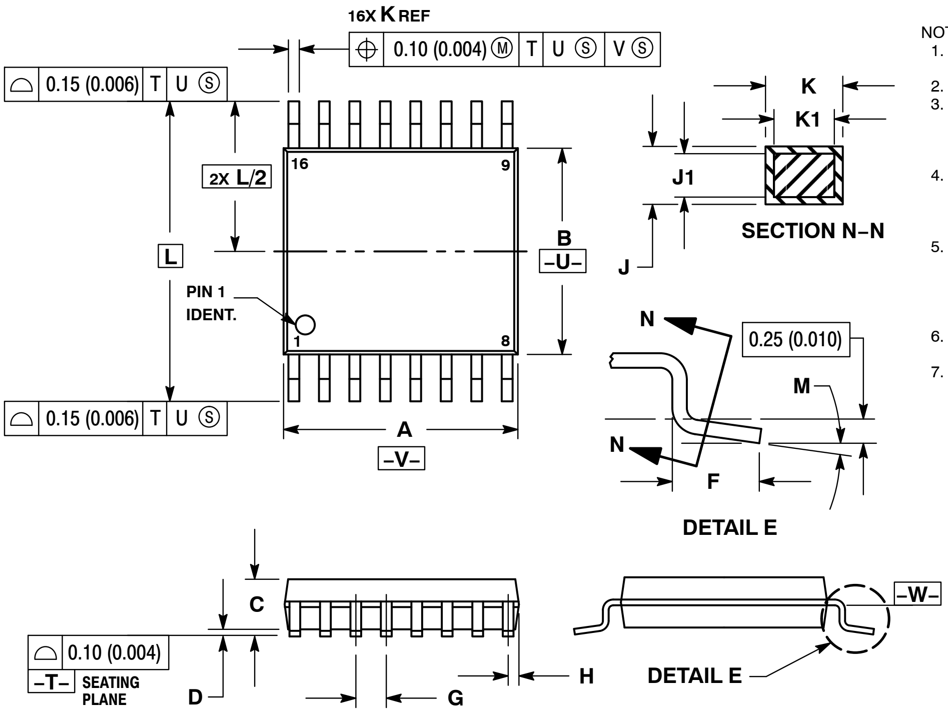
Figure 8. Test Circuit



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

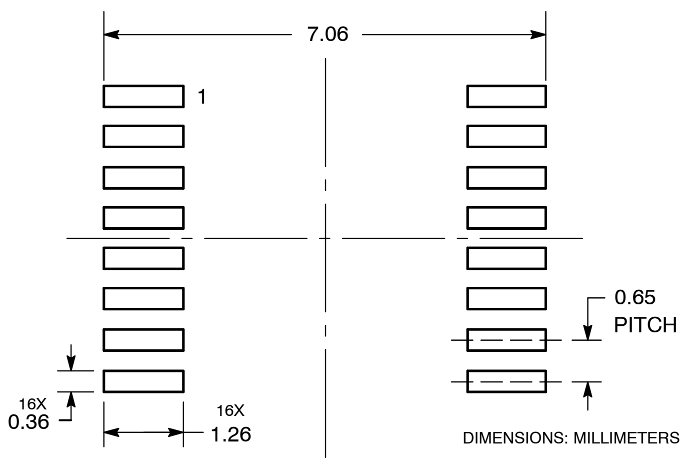
DATE 19 OCT 2006



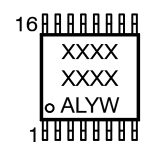
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−16**	**PAGE 1 OF 1**

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