# TS5A22362 0.65-Ω 2-channel SPDT Analog Switches With Negative Signaling Capability

## 1 Features

- Specified break-before-make switching
- Negative signaling capability: maximum swing from –2.75 V to 2.75 V ($V_{CC}$ = 2.75 V)
- Low ON-state resistance (0.65 Ω typical)
- Low charge injection
- Excellent ON-state resistance matching
- 2.3-V to 5.5-V Power supply ($V_{CC}$)
- Latch-Up performance exceeds 100 mA Per JESD 78, Class II
- ESD Performance tested per JESD 22
  - 2500-V Human-body model (A114-B, class II)
  - 1500-V Charged-device model (C101)
  - 200-V Machine model (A115-A)

## 2 Applications

- Cell phones
- Personal digital assistant (PDAs)
- Portable instrumentation
- Audio routing
- Medical imaging

## 3 Description

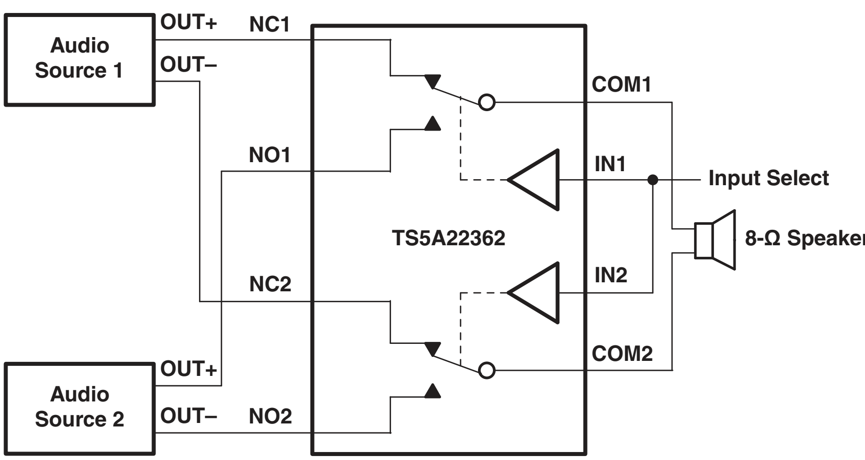
The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications. The 3.00 mm × 3.00 mm DRC package is also available as a nonmagnetic package for medical imaging application.

**Device Information[(1)]**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TS5A22362 | VSON (10) | 3.00 mm × 3.00 mm |
| | DSBGA (10) | 1.86 mm × 1.36 mm |
| | VSSOP (10) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (March 2018) to Revision E | Page |
|---|---|
| • Changed the YZP Package view From: Top View To: Bottom View | 3 |

| Changes from Revision C (June 2017) to Revision D | Page |
|---|---|
| • Changed the YZP Package From: Laser Marketing View and Bump View To: Top View | 3 |
| • Changed the $Q_C$ TYP value From: 10 pC To: 150 pC in the *Electrical Characteristics for 5-V Supply* table | 8 |

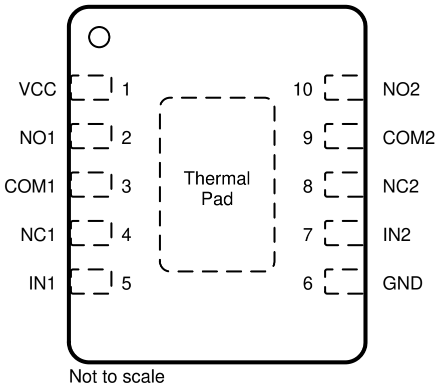
| Changes from Revision B (September 2015) to Revision C | Page |
|---|---|
| • Changed the $V_{IN}$ MAX value From: $V_{CC}$ To: 5.5 V in the *Recommended Operating Conditions* table | 4 |

| Changes from Revision A (August 2015) to Revision B | Page |
|---|---|
| • Changed $C_L$ TEST CONDITION value for all THD PARAMETERs from 15 pf to 35 pf. | 6 |

| Changes from Original (June 2015) to Revision A | Page |
|---|---|
| • Changed the Functional Block Diagram. | 15 |

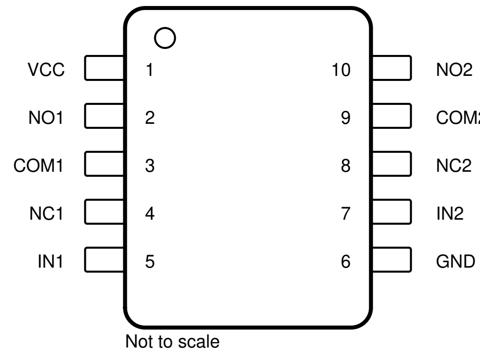
# 5 Pin Configuration and Functions

**DRC Package**
**10-Pin VSON**
**Top View**

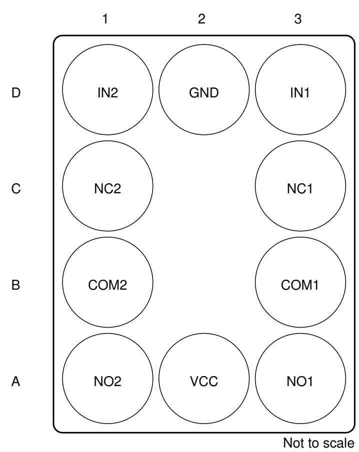



The exposed center pad, if used, must be connected as a secondary GND or left electrically open.

**DGS Package**
**10-Pin VSSOP**
**Top View**




**YZP Package**
**10-Pin DSBGA**
**Bottom View**




**Pin Functions**

| PIN | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | VSON | VSSOP | DSBGA | | |
| VCC | 1 | 1 | A2 | — | Power Supply |
| NO1 | 2 | 2 | A3 | I/O | Normally Open (NO) signal path, Switch 1 |
| COM1 | 3 | 3 | B3 | I/O | Common signal path, Switch 1 |
| NC1 | 4 | 4 | C3 | I/O | Normally Closed (NC) signal path, Switch 1 |
| IN1 | 5 | 5 | D3 | I | Digital control pin , Switch 1 |
| GND | 6 | 6 | D2 | — | Ground |
| IN2 | 7 | 7 | D1 | I | Digital control pin, Switch 2 |
| NC2 | 8 | 8 | C1 | I/O | Normally Closed (NC) signal path, Switch 2 |
| COM2 | 9 | 9 | B1 | I/O | Common signal path, Switch 2 |
| NO2 | 10 | 10 | A1 | I/O | Normally Open (NO) signal Path, Switch 2 |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ [2] | Supply voltage [3] | | –0.5 | 6 | V |
| $V_{NC}$<br>$V_{NO}$<br>$V_{COM}$ | Analog voltage [3] [4] [5] | | $V_{CC}$ – 6 | $V_{CC}$ + 0.5 | V |
| $I_{I/OK}$ | Analog port diode current | $V_{NC}$, $V_{NO}$, $V_{COM}$ < 0<br>or<br>$V_{NC}$, $V_{NO}$, $V_{COM}$ > $V_{CC}$ | –50 | 50 | mA |
| $I_{NC}$<br>$I_{NO}$<br>$I_{COM}$ | ON-state switch current | $V_{NC}$, $V_{NO}$, $V_{COM}$ = 0 to $V_{CC}$ | –150 | 150 | mA |
| | ON-state peak switch current [6] | | –300 | 300 | |
| $I_{NC}$ [3] [7] [8]<br>$I_{NO}$ [3] [7] [8]<br>$I_{COM}$ [3] [7] [8] | ON-state switch current | $V_{NC}$, $V_{NO}$, $V_{COM}$ = 0 to $V_{CC}$ | –350 | 350 | mA |
| | ON-state peak switch current [6] | | –500 | 500 | |
| $V_I$ | Digital input voltage | | –0.5 | 6.5 | V |
| $I_{IK}$ | Digital input clamp current [3] [4] | $V_I$ < 0 | –50 | 50 | mA |
| $I_{CC}$<br>$I_{GND}$ | Continuous current through $V_{CC}$ or GND | | –100 | 100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.
(7) $V_{CC}$ = 3.0 V to 5.0 V, $T_A$ = –40°C to 85°C.
(8) For YZP package only.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±2500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.3 | 5.5 | V |
| $V_{NC}$<br>$V_{NO}$<br>$V_{COM}$ | Signal path voltage | $V_{CC}$ – 5.5 | $V_{CC}$ | V |
| $V_{IN}$ | Digital control | GND | 5.5 | V |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TS5A22362 DGS (VSSOP) 10 PINS | TS5A22362 DRC (VSON) 10 PINS | TS5A22362 YZP (DSBGA) 10 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 163.3 | 44.3 | 90.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.4 | 70.1 | 0.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 83.1 | 19.3 | 8.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.8 | 2.0 | 3.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 81.8 | 19.4 | 8.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics for 2.5-V Supply

$V_{CC}$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal range | | | | | $V_{CC}$ – 5.5 | | $V_{CC}$ | V |
| $R_{on}$ | ON-state resistance | $V_{NC}$ or $V_{NO}$ = $V_{CC}$, 1.5 V, $V_{CC}$ – 5.5 V $I_{COM}$ = –100 mA, | COM to NO or NC, see Figure 13 | 25°C | 2.7 V | | 0.65 | 0.94 | Ω |
| | | | | Full | | | | 1.3 | |
| $\Delta R_{on}$ | ON-state resistance match between channels | $V_{NC}$ or $V_{NO}$ = 1.5 V, $I_{COM}$ = –100 mA, | COM to NO or NC, see Figure 13 | 25°C | 2.7 V | | 0.023 | 0.11 | Ω |
| | | | | Full | | | | 0.15 | |
| $R_{on(flat)}$ | ON-state resistance flatness | $V_{NC}$ or $V_{NO}$ = $V_{CC}$, 1.5 V, $V_{CC}$ – 5.5 V $I_{COM}$ = –100 mA, | COM to NO or NC, see Figure 13 | 25°C | 2.7 V | | 0.18 | 0.46 | Ω |
| | | | | Full | | | | 0.5 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{NC}$ = 2.25 V, $V_{CC}$ – 5.5 V $V_{COM}$ = $V_{CC}$ – 5.5 V, 2.25 V $V_{NO}$ = Open COM to NO or $V_{NO}$ = 2.25 V, $V_{CC}$ – 5.5 V, $V_{COM}$ = $V_{CC}$ – 5.5 V, 2.25 V $V_{NC}$ = Open COM to NC | See Figure 14 | 25°C | 2.7 | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{NC}$ and $V_{NO}$ = Floating, $V_{COM}$ = $V_{CC}$,$V_{CC}$ – 5.5 V | See Figure 15 | 25°C | 2.7 V | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |
| **Digital Control Inputs (IN)** (2) | | | | | | | | | |
| $V_{IH}$ | Input logic high | | | Full | | 1.4 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | | | | | | 0.6 | |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{IN}$ = $V_{CC}$ or 0 | | 25°C | 2.7 V | –250 | | 250 | nA |
| | | | | Full | | –250 | | 250 | |
| **Dynamic** | | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 17 | 25°C | 2.5 V | | 44 | 80 | ns |
| | | | | Full | 2.3 V to 2.7 V | | | 120 | |
| $t_{OFF}$ | Turnoff time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 17 | 25°C | 2.5 V | | 22 | 70 | ns |
| | | | | Full | 2.3 V to 2.7 V | | | 70 | |
| $t_{BBM}$ | Break-before-make time | See Figure 18 | | 25°C | 2.5 V | 1 | 7 | | ns |
| $Q_C$ | Charge injection | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 1 nF, see Figure 22 | 25°C | 2.5 V | | 150 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, | See Figure 16 | 25°C | 2.5 V | | 70 | | pF |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## Electrical Characteristics for 2.5-V Supply (continued)

$V_{CC}$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $C_{COM(ON)}$ | NC, NO, COM ON capacitance | $V_{COM}$ = $V_{CC}$ or GND, Switch ON, f = 10 MHz | See Figure 16 | 25°C | 2.5 V | | 370 | | pF |
| $C_I$ | Digital input capacitance | $V_I$ = $V_{CC}$ or GND | See Figure 16 | 25°C | 2.5 V | | 2.6 | | pF |
| BW | Bandwidth | $R_L$ = 50 Ω, –3 dB | See Figure 18 | 25°C | 2.5 V | | 17 | | MHz |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω | f = 100 kHz, see Figure 20 | 25°C | 2.5 V | | –66 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω | f = 100 kHz, see Figure 21 | 25°C | 2.5 V | | –75 | | dB |
| THD | Total harmonic distortion | $R_L$ = 600 Ω, $C_L$ = 35 pF | f = 20 Hz to 20 kHz, see Figure 23 | 25°C | 2.5 V | | 0.01% | | |
| **Supply** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{COM}$ and $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | 25°C | 2.7 V | | 0.2 | 1.1 | µA |
| | | | | Full | | | | 1.3 | |
| $I_{CC}$ | Positive supply current | $V_{COM}$ = $V_{CC}$ – 5.5 V, $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | Full | 2.7 V | | | 3.3 | µA |

## 6.6 Electrical Characteristics for 3.3-V Supply

$V_{CC}$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal range | | | | | $V_{CC}$ – 5.5 | | $V_{CC}$ | V |
| $R_{on}$ | ON-state resistance | $V_{NC}$ or $V_{NO}$ ≤ $V_{CC}$, 1.5 V, $V_{CC}$ – 5.5 V, $I_{COM}$ = –100 mA | COM to NO or NC, see Figure 13 | 25°C | 3 V | | 0.61 | 0.87 | Ω |
| | | | | Full | | | | 0.97 | |
| $\Delta R_{on}$ | ON-state resistance match between channels | $V_{NC}$ or $V_{NO}$ = 1.5 V, $I_{COM}$ = –100 mA, | COM to NO or NC, see Figure 13 | 25°C | 3 V | | 0.024 | 0.13 | Ω |
| | | | | Full | | | | 0.13 | |
| $R_{on(flat)}$ | ON-state resistance flatness | $V_{NC}$ or $V_{NO}$ ≤ $V_{CC}$, 1.5 V, $V_{CC}$ – 5.5 V, $I_{COM}$ = –100 mA | COM to NO or NC, see Figure 13 | 25°C | 3 V | | 0.12 | 0.46 | Ω |
| | | | | Full | | | | 0.5 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{NC}$ = 3 V, $V_{CC}$ – 5.5 V $V_{COM}$ = $V_{CC}$ – 5.5 V, 3 V $V_{NO}$ = Open COM to NO or $V_{NO}$ = 3 V, $V_{CC}$ – 5.5 V, $V_{COM}$ = $V_{CC}$ – 5.5 V, 3 V $V_{NC}$ = Open COM to NC | See Figure 14 | 25°C | 3.6 V | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{NC}$ and $V_{NO}$ = Floating, $V_{COM}$ = $V_{CC}$,$V_{CC}$ – 5.5 V | COM to NO or NC, see Figure 15 | 25°C | 3.6 V | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |
| **DIGITAL CONTROL INPUTS (IN) (2)** | | | | | | | | | |
| $V_{IH}$ | Input logic high | | | Full | | 1.4 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | | | | | | 0.8 | |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{IN}$ = $V_{CC}$ or 0 | | 25°C | 3.6 V | –250 | | 250 | nA |
| | | | | Full | | –250 | | 250 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics for 3.3-V Supply (continued)

$V_{CC}$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **DYNAMIC** | | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω | $C_L$ = 35 pF, see Figure 17 | 25°C | 3.3 V | | 34 | 80 | ns |
| | | | | Full | 3 V to 3.6 V | | | 120 | |
| $t_{OFF}$ | Turnoff time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω | $C_L$ = 35 pF, see Figure 17 | 25°C | 3.3 V | | 19 | 70 | ns |
| | | | | Full | 3 V to 3.6 V | | | 70 | |
| $t_{BBM}$ | Break-before-make time | See Figure 18 | | 25°C | 3.3 V | 1 | 7 | | ns |
| $Q_C$ | Charge injection | $V_{GEN}$ = 0, $R_{GEN}$ = 0 | $C_L$ = 1 nF, see Figure 22 | 25°C | 3.3 V | | 150 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or $V_{CC}$ – 5.5 V | See Figure 16 | 25°C | 3.3 V | | 70 | | pF |
| $C_{COM(ON)}$ | NC, NO, COM ON capacitance | $V_{COM}$ = $V_{CC}$ or GND, f = 10 MHz | See Figure 16 | 25°C | 3.3 V | | 370 | | pF |
| $C_I$ | Digital input capacitance | $V_I$ = $V_{CC}$ or GND | See Figure 16 | 25°C | 3.3 V | | 2.6 | | pF |
| BW | Bandwidth | $R_L$ = 50 Ω, –3 dB | Switch ON, see Figure 18 | 25°C | 3.3 V | | 17.5 | | MHz |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω | f = 100 kHz, see Figure 20 | 25°C | 3.3 V | | –68 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω | f = 100 kHz, see Figure 21 | 25°C | 3.3 V | | –76 | | dB |
| THD | Total harmonic distortion | $R_L$ = 600 Ω, $C_L$ = 35 pF | f = 20 Hz to 20 kHz, see Figure 23 | 25°C | 3.3 V | | 0.008% | | |
| **SUPPLY** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{COM}$ and $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | 25°C | 3.6 V | | 0.1 | 1.2 | µA |
| | | | | Full | | | | 1.3 | |
| | | $V_{COM}$ = $V_{CC}$ – 5.5 V, $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | Full | 3.6 V | | | 3.4 | µA |

## 6.7 Electrical Characteristics for 5-V Supply

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal range | | | | | $V_{CC}$ – 5.5 | | $V_{CC}$ | V |
| $R_{on}$ | ON-state resistance | $V_{NC}$ or $V_{NO}$ = $V_{CC}$, 1.6 V, $V_{CC}$ = –5.5 V, $I_{COM}$ = –100 mA | COM to NO or NC, see Figure 13 | 25°C | 4.5 V | | 0.52 | 0.74 | Ω |
| | | | | Full | | | | 0.83 | |
| $\Delta R_{on}$ | ON-state resistance match between channels | $V_{NC}$ or $V_{NO}$ = 1.6 V, $I_{COM}$ = –100 mA | COM to NO or NC, see Figure 13 | 25°C | 4.5 V | | 0.04 | 0.23 | Ω |
| | | | | Full | | | | 0.30 | |
| $R_{on(flat)}$ | ON-state resistance flatness | $V_{NC}$ or $V_{NO}$ = $V_{CC}$, 1.6 V, $V_{CC}$ = –5.5 V, $I_{COM}$ = –100 mA | COM to NO or NC, see Figure 13 | 25°C | 4.5 V | | 0.076 | 0.46 | Ω |
| | | | | Full | | | | 0.5 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{NC}$ = 4.5 V, $V_{CC}$ – 5.5 V, $V_{COM}$ = $V_{CC}$ – 5.5 V, 4.5 V, $V_{NO}$ = Open, COM to NO or $V_{NO}$ = 4.5 V, $V_{CC}$ – 5.5 V, $V_{COM}$ = $V_{CC}$ – 5.5 V, 4.5 V, $V_{NC}$ = Open, COM to NC | See Figure 14 | 25°C | 5.5 V | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{NC}$ and $V_{NO}$ = Floating, $V_{COM}$ = $V_{CC}$, $V_{CC}$ – 5.5 V | See Figure 15 | 25°C | 5.5 V | –50 | | 50 | nA |
| | | | | Full | | –375 | | 375 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 5-V Supply (continued)

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **DIGITAL CONTROL INPUTS (IN)** (2) | | | | | | | | | |
| $V_{IH}$ | Input logic high | | | Full | | 2.4 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | | Full | | | | 0.8 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{IN}$ = $V_{CC}$ or 0 | | 25°C | 5.5 V | –250 | | 250 | nA |
| | | | | Full | | –250 | | 250 | |
| **DYNAMIC** | | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω | $C_L$ = 35 pF, see Figure 17 | 25°C | 5 V | | 27 | 80 | ns |
| | | | | Full | 4.5 V to 5.5 V | | | 80 | |
| $t_{OFF}$ | Turnoff time | $V_{COM}$ = $V_{CC}$, $R_L$ = 300 Ω | $C_L$ = 35 pF, see Figure 17 | 25°C | 5 V | | 13 | 70 | ns |
| | | | | Full | 4.5 V to 5.5 V | | | 70 | |
| $t_{BBM}$ | Break-before-make time | $V_{NC}$ = $V_{NO}$ = $V_{CC}$/2 $R_L$ = 300 Ω | $C_L$ = 35 pF, see Figure 18 | 25°C | 5 V | 1 | 3.5 | | ns |
| $Q_C$ | Charge injection | $V_{GEN}$ = 0, $R_{GEN}$ = 0 | $C_L$ = 1 nF, see Figure 22 | 25°C | 5 V | | 150 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or $V_{CC}$ – 5.5 V | See Figure 16 | 25°C | 5 V | | 70 | | pF |
| $C_{COM(ON)}$ | NC, NO, COM ON capacitance | $V_{COM}$ = $V_{CC}$ or GND, | See Figure 16 | 25°C | 5 V | | 370 | | pF |
| $C_I$ | Digital input capacitance | $V_I$ = $V_{CC}$ or GND | See Figure 16 | 25°C | 5 V | | 2.6 | | pF |
| BW | Bandwidth | $R_L$ = 50 Ω | See Figure 18 | 25°C | 5 V | | 18.3 | | MHz |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω | f = 100 kHz, see Figure 20 | 25°C | 5 V | | –70 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω | f = 100 kHz, see Figure 21 | 25°C | 5 V | | –78 | | dB |
| THD | Total harmonic distortion | $R_L$ = 600 Ω, $C_L$ = 35 pF | f = 20 Hz to 20 kHz, see Figure 23 | 25°C | 5 V | | 0.009% | | |
| **SUPPLY** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{COM}$ and $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | 25°C | 5.5 V | | 0.2 | 1.3 | µA |
| | | | | Full | | | | 3.5 | |
| | | $V_{COM}$ = $V_{CC}$ – 5.5 V, $V_{IN}$ = $V_{CC}$ or GND, $V_{NC}$ and $V_{NO}$ = Floating | | Full | | | | 5 | |

(2) All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.8 Typical Characteristics

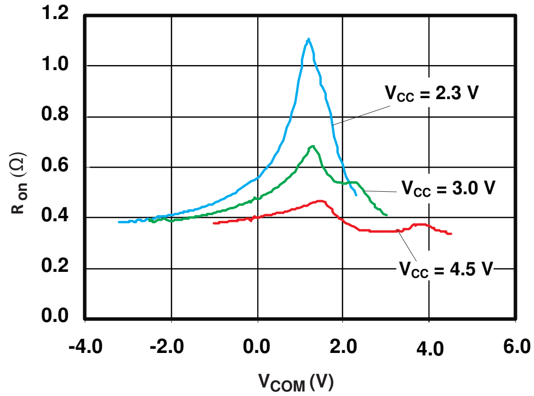



Figure 1. $R_{on}$ vs $V_{COM}$

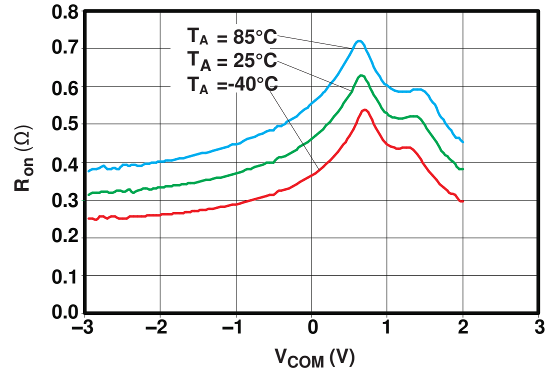



Figure 2. $R_{on}$ vs $V_{COM}$ ($V_{CC}$ = 2.7 V)

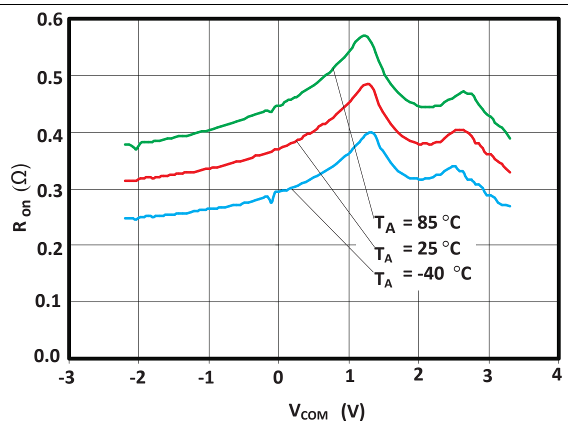



Figure 3. $R_{on}$ vs $V_{COM}$ ($V_{CC}$ = 3.3 V)

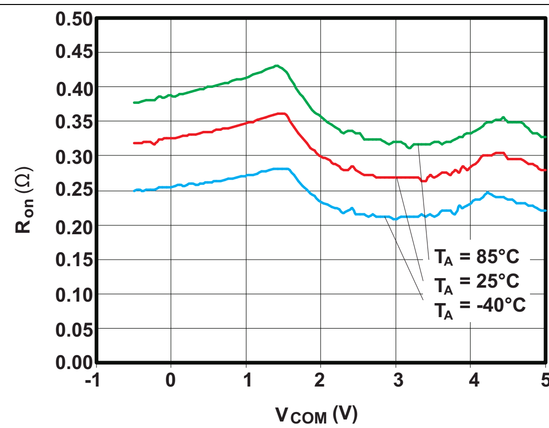



Figure 4. $R_{on}$ vs $V_{COM}$ ($V_{CC}$ = 5 V)

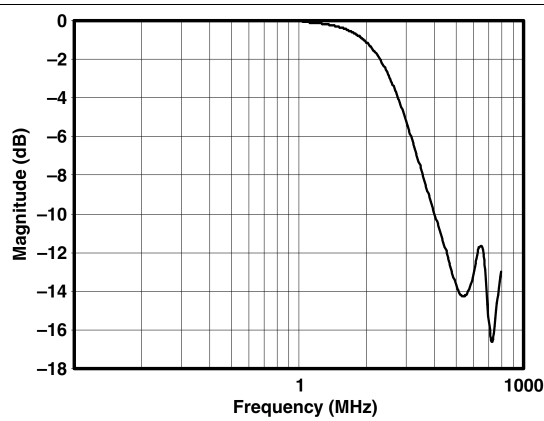



Figure 5. Insertion Loss

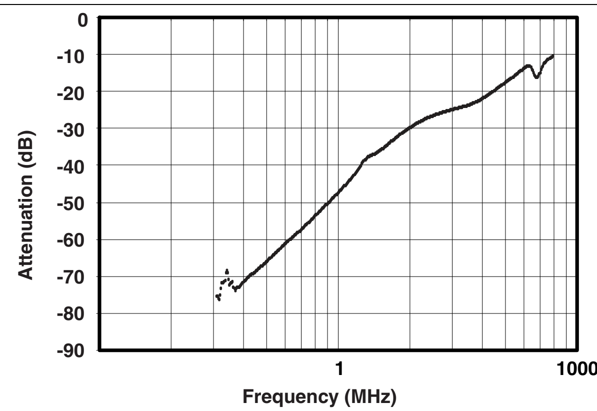



Figure 6. Off Isolation vs Frequency

## Typical Characteristics (continued)

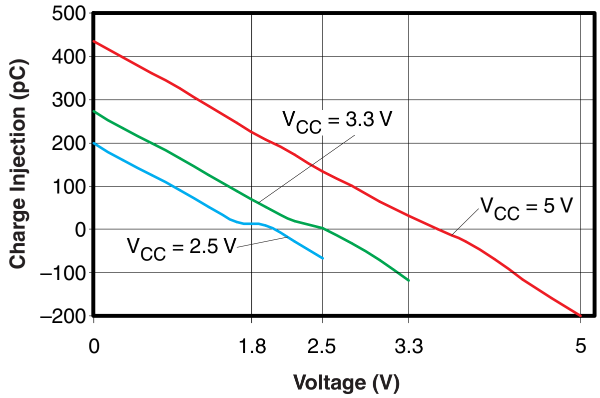



**Figure 7. Charge Injection ($Q_C$) vs $V_{COM}$**

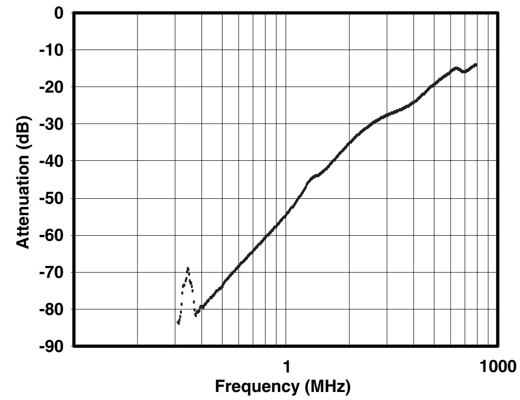



**Figure 8. Crosstalk ($V_{CC}$ = 3.3 V)**

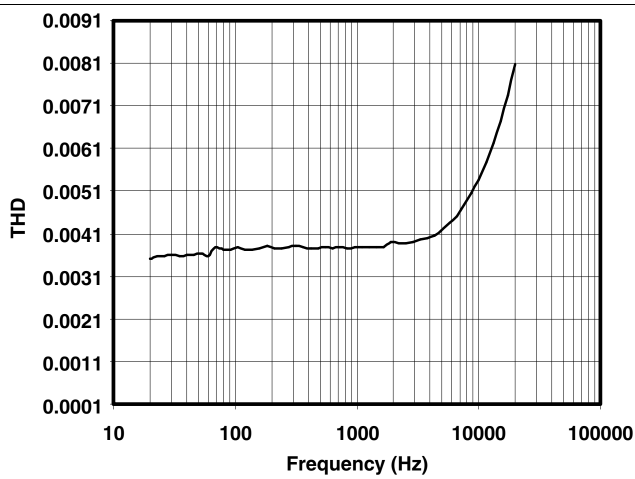



**Figure 9. Total Harmonic Distortion vs Frequency**

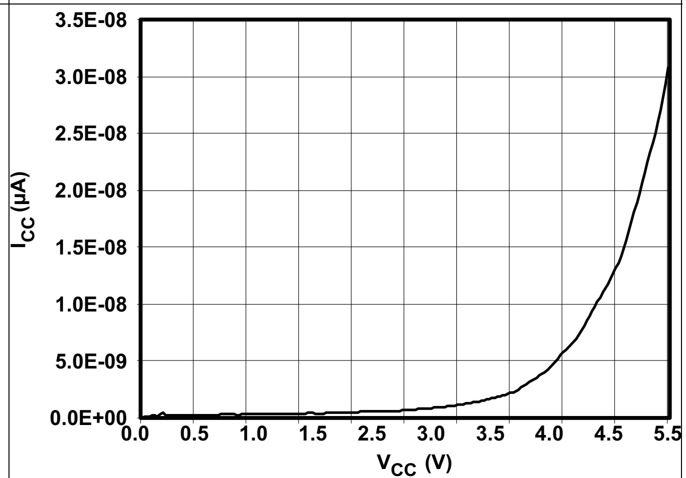



**Figure 10. Power-Supply Current vs $V_{CC}$**

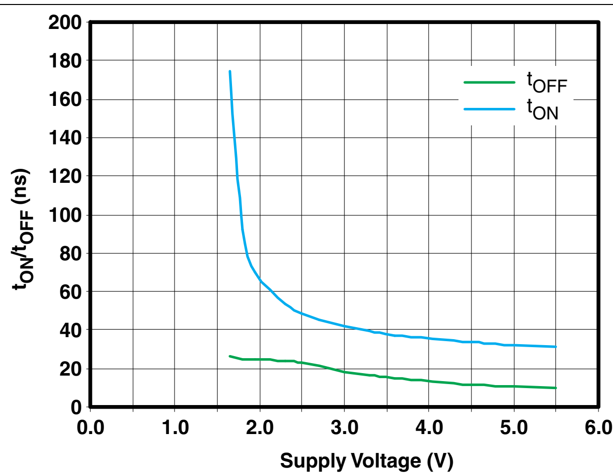



**Figure 11. $t_{ON}$ And $t_{OFF}$ vs Supply Voltage**

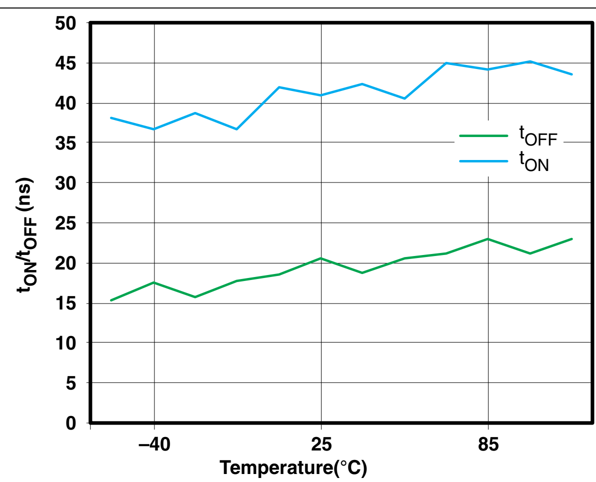



**Figure 12. $t_{ON}$ And $t_{OFF}$ vs Temperature (2.5-V Supply)**

# 7 Parameter Measurement Information

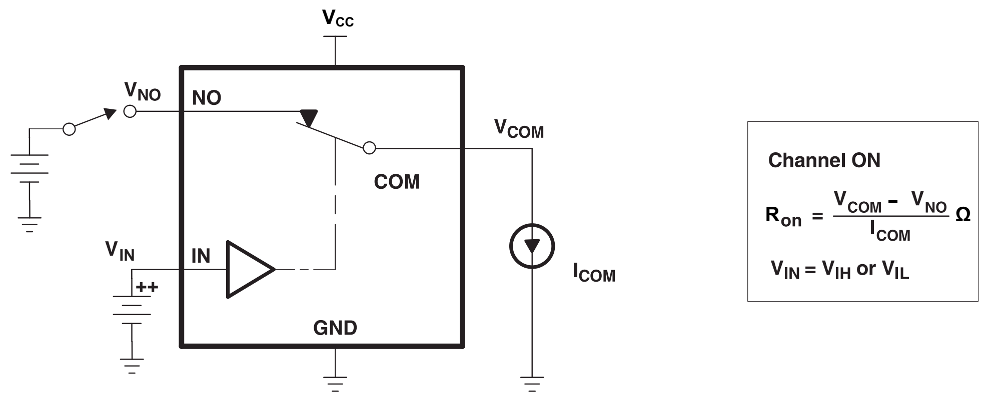



**Figure 13. ON-state resistance ($R_{on}$)**

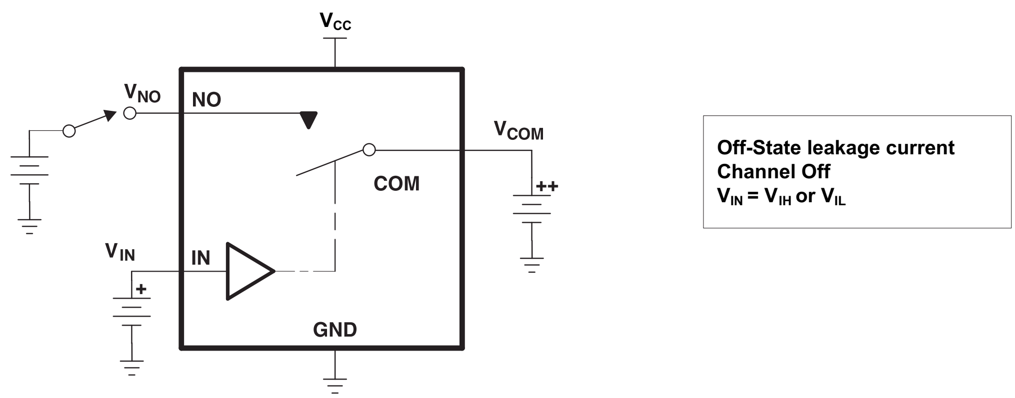



**Figure 14. OFF-state leakage current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)**

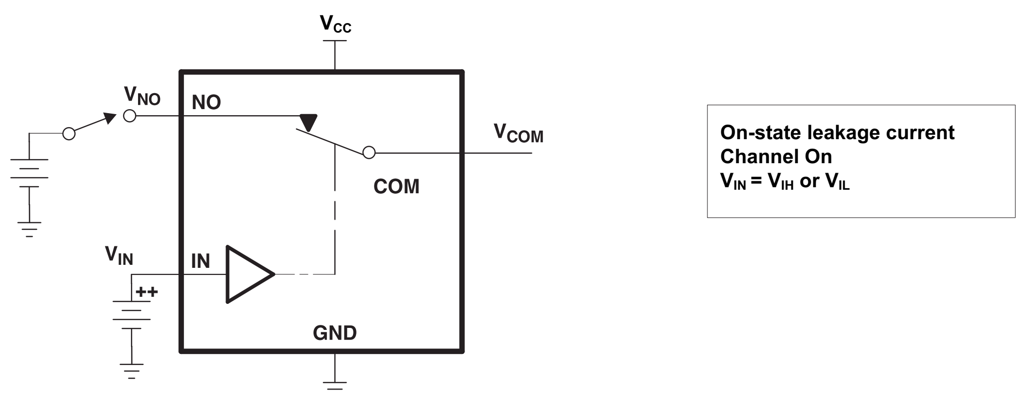



**Figure 15. ON-state leakage current ($I_{COM(ON)}$, $I_{NO(ON)}$)**

## Parameter Measurement Information (continued)

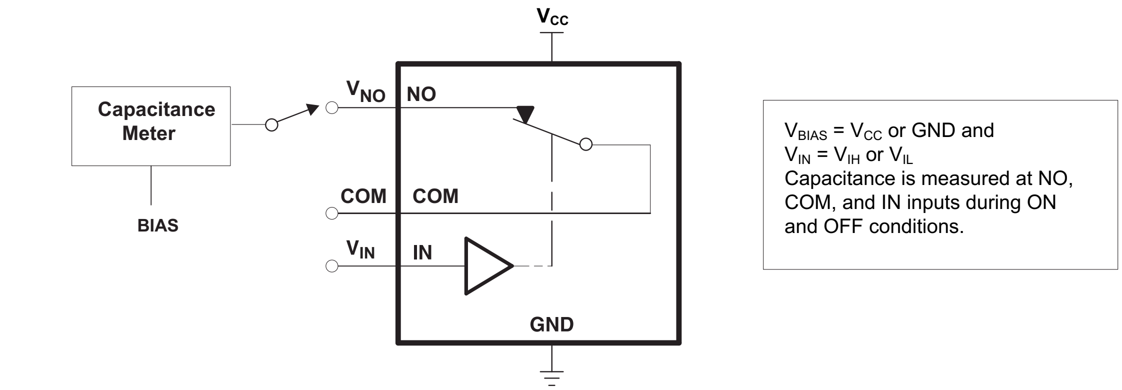
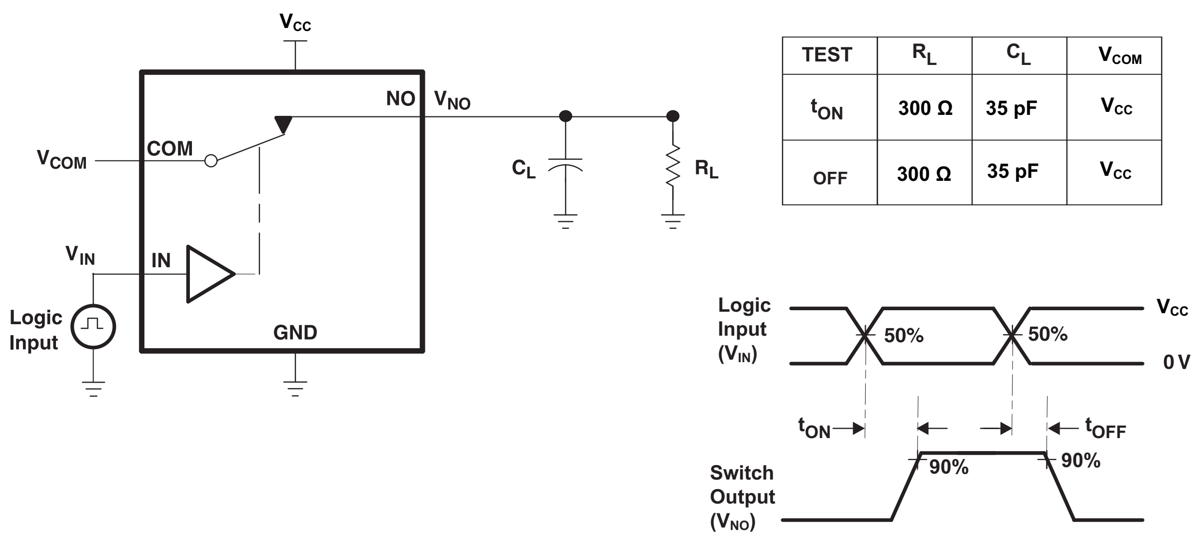



**Figure 16. Capacitance ($C_I$, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)**



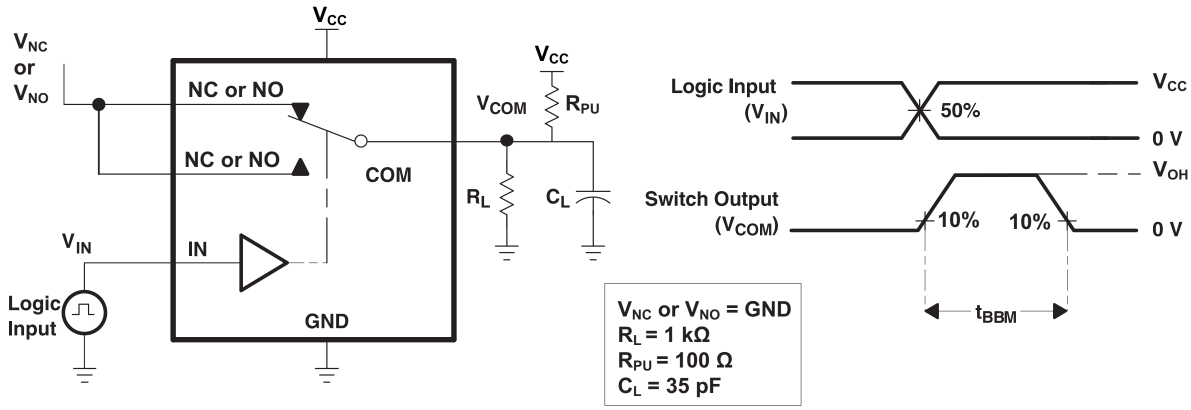

| TEST | $R_L$ | $C_L$ | $V_{COM}$ |
|---|---|---|---|
| $t_{ON}$ | 300 Ω | 35 pF | $V_{CC}$ |
| OFF | 300 Ω | 35 pF | $V_{CC}$ |

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 17. Turnon ($t_{ON}$) and Turnoff time ($t_{OFF}$)**

## Parameter Measurement Information (continued)




A. $C_L$ includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

**Figure 18. Break-Before-Make Time ($t_{BBM}$)**

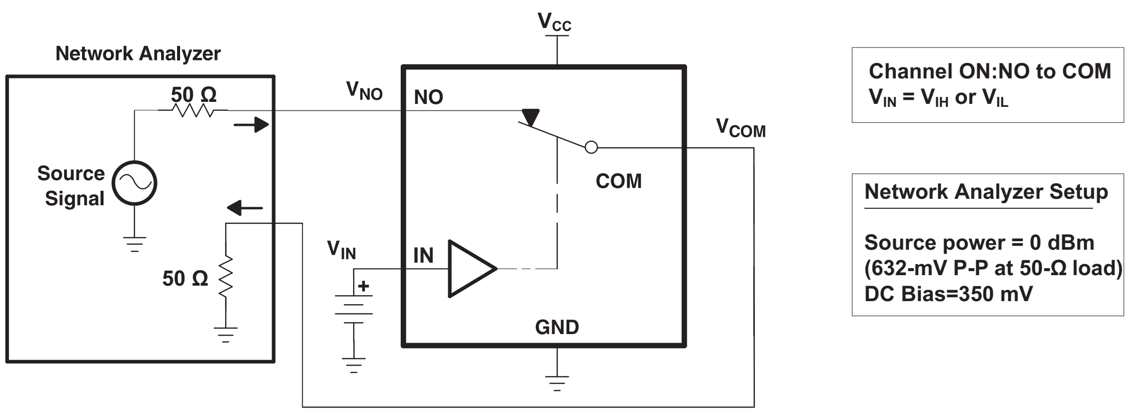



**Figure 19. Bandwidth (BW)**

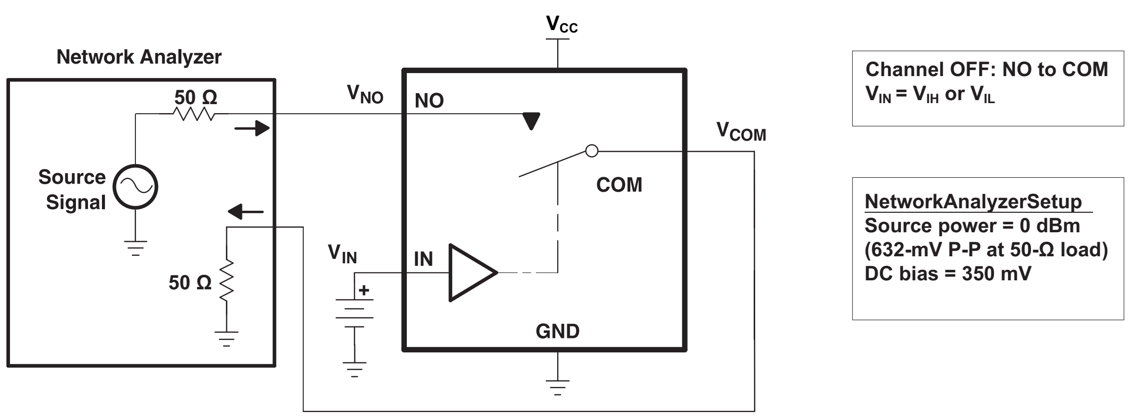



**Figure 20. OFF isolation ($O_{ISO}$)**

## Parameter Measurement Information (continued)

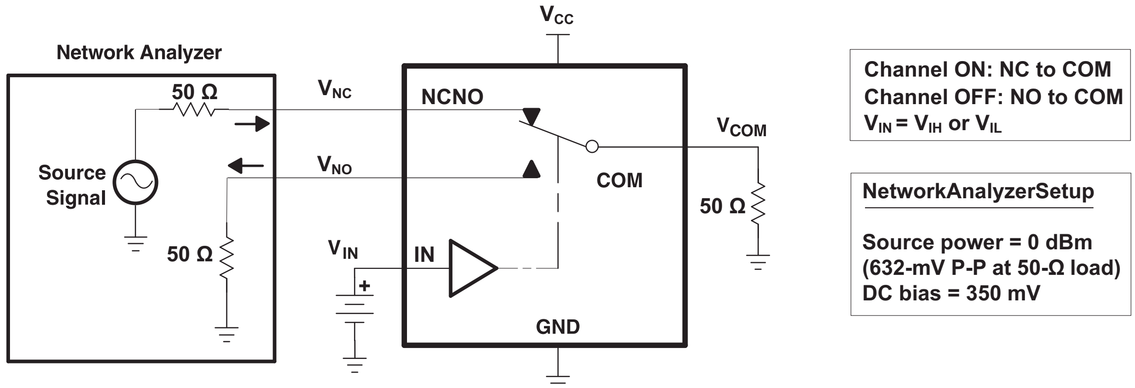
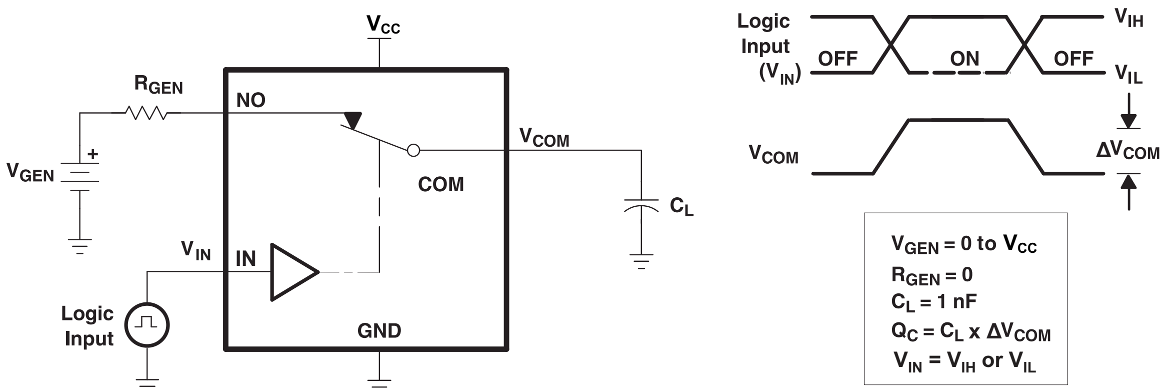


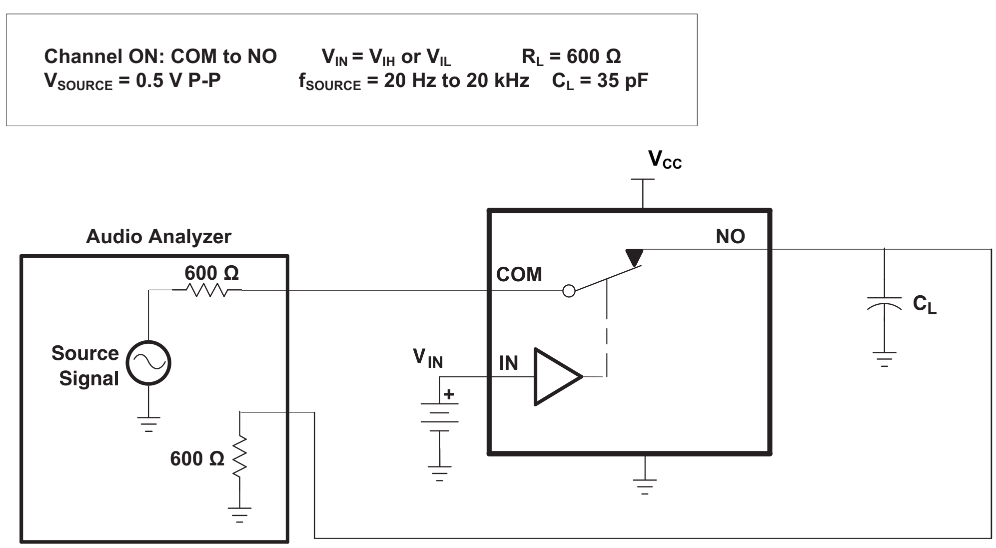

**Figure 21. Crosstalk ($X_{TALK}$)**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 22. Charge injection ($Q_C$)**




A. $C_L$ includes probe and jig capacitance.

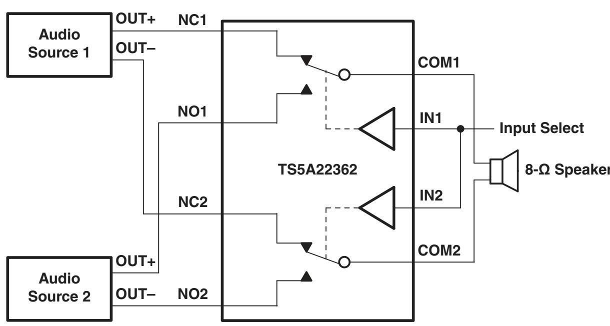
**Figure 23. Total Harmonic Distortion (THD)**

# 8 Detailed Description

## 8.1 Overview

The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switches designed to operate from 2.3 V to 5.5 V. The devices feature negative signal capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Negative Signaling Capacity

The TS5A22362 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input and output signal swing of the device is dependant of the supply voltage $V_{CC}$: the devices pass signals as high as $V_{CC}$ and as low as $V_{CC}$ – 5.5 V, including signals below ground with minimal distortion.

Table 1 shows the input/output signal swing the user can get with different supply voltages.

**Table 1. Input/Output signal swing**

| SUPPLY VOLTAGE, $V_{CC}$ | MINIMUM ($V_{NC}$, $V_{NO}$, $V_{COM}$) = $V_{CC}$ – 5.5 | MAXIMUM ($V_{NC}$, $V_{NO}$, $V_{COM}$) = $V_{CC}$ |
|---|---|---|
| 5.5 V | 0 V | 5.5 V |
| 4.5 V | –1.9 V | 4.5 V |
| 3.6 V | –2.5 V | 3.6 V |
| 3.0 V | –2.5 V | 3.0 V |
| 2.7 V | –2.8 V | 2.7 V |
| 2.3 V | –3.2 V | 2.3 V |

## 8.4 Device Functional Modes

The function table for TS5A22362 is shown in Table 2

**Table 2. Function Table**

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|---|---|---|
| L | ON | OFF |
| H | OFF | ON |

# 9 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Tie the digitally controlled inputs select pins IN1 and IN2 to $V_{CC}$ or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 9.2 Typical Application

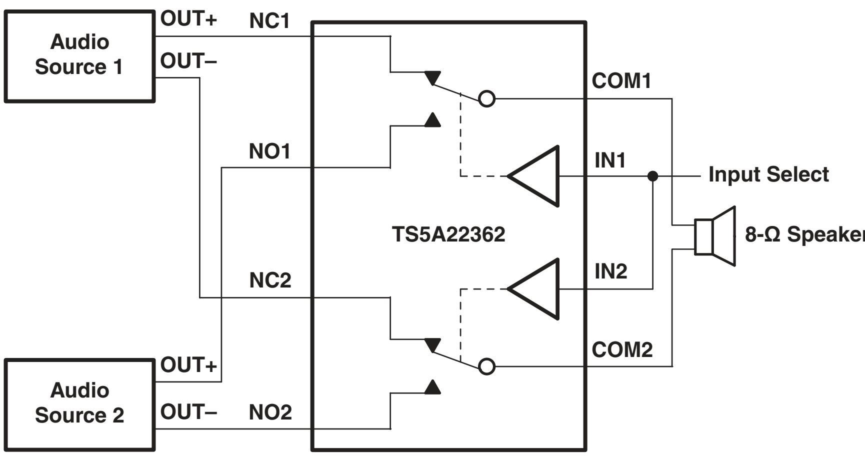



**Figure 24. Typical Application**

### 9.2.1 Design Requirements

Tie the digitally controlled inputs select pins IN1 and IN2 to $V_{CC}$ or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

### 9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22362 operates from a single +2.3-V to +5.5-V supply and the input/output signal swing of the device is dependant of the supply voltage $V_{CC}$. The device will pass signals as high as $V_{CC}$ and as low as $V_{CC}$ – 5.5 V. Use table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

## Typical Application (continued)

### 9.2.3 Application Curve

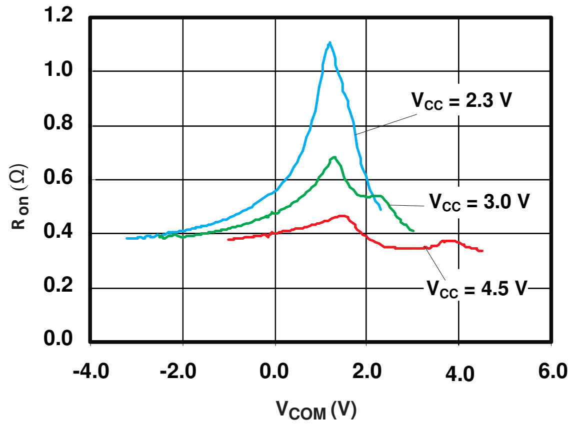



**Figure 25. $R_{on}$ vs $V_{COM}$**

## 10 Power Supply Recommendations

The TS5A22362 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100-µs delay after VCC is at voltage before applying a signal on NC and NO paths

It is also good practice to place a 0.1-µF bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

### 11.2 Layout Example

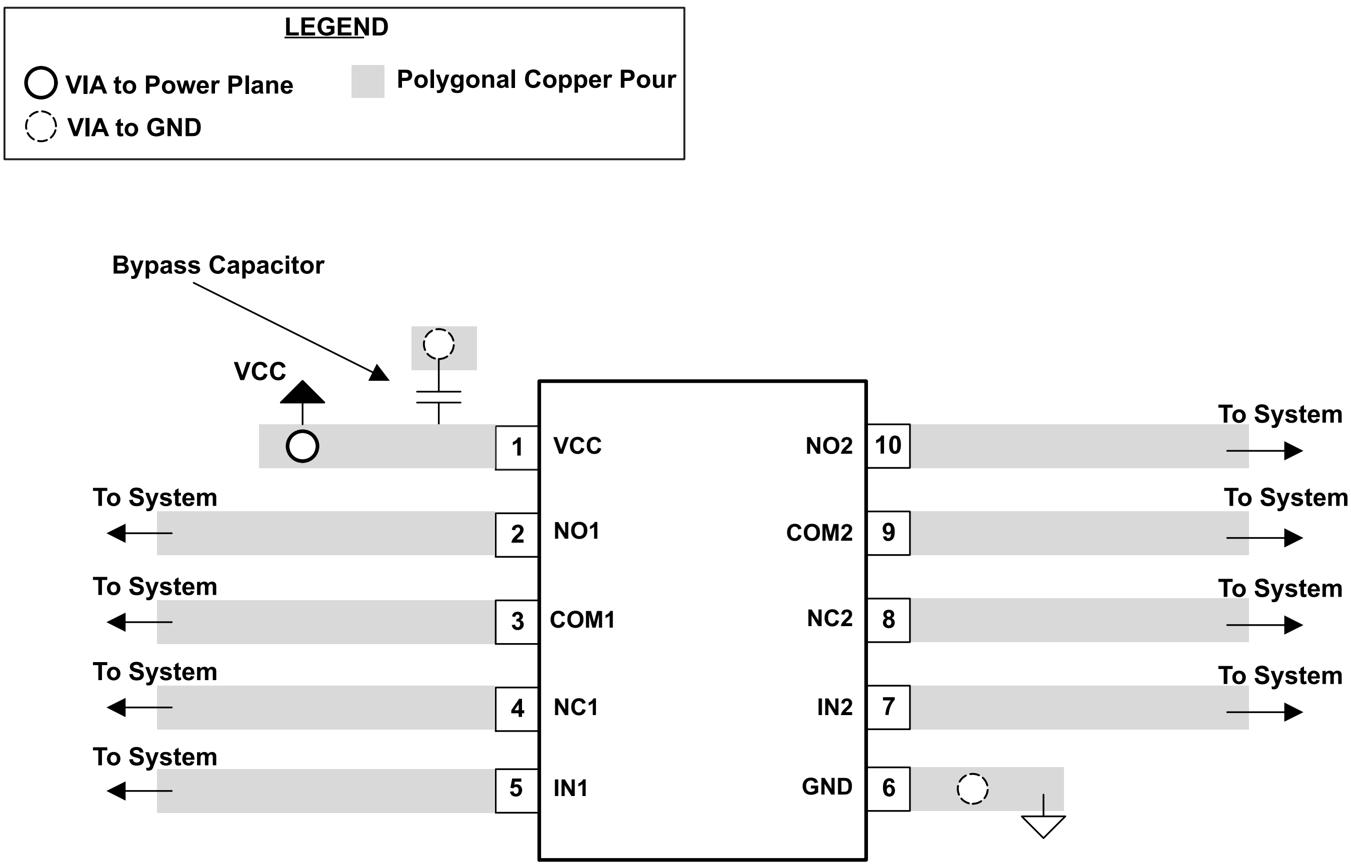



**Figure 26. Layout example of TS5A22362**

# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5A22362DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 39R | Samples |
| TS5A22362DGSRG4 | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 39R | Samples |
| TS5A22362DRCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ZVG | Samples |
| TS5A22362DRCT-NM | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | ZVGNM | Samples |
| TS5A22362YZPR | ACTIVE | DSBGA | YZP | 10 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (39, 392) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

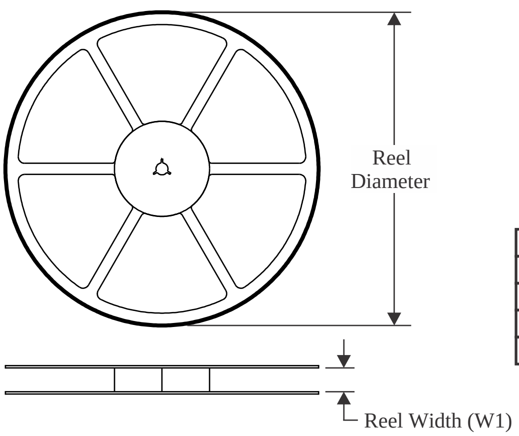
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

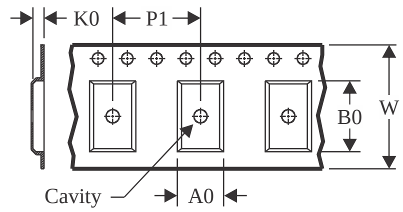
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

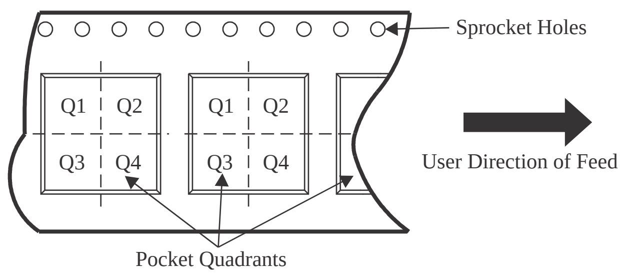



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

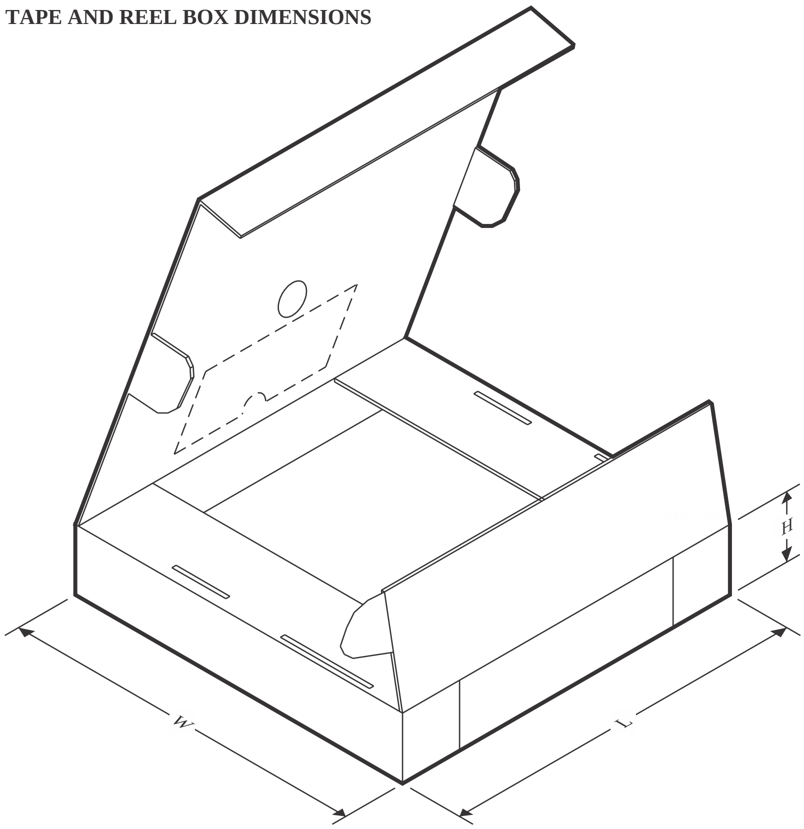
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

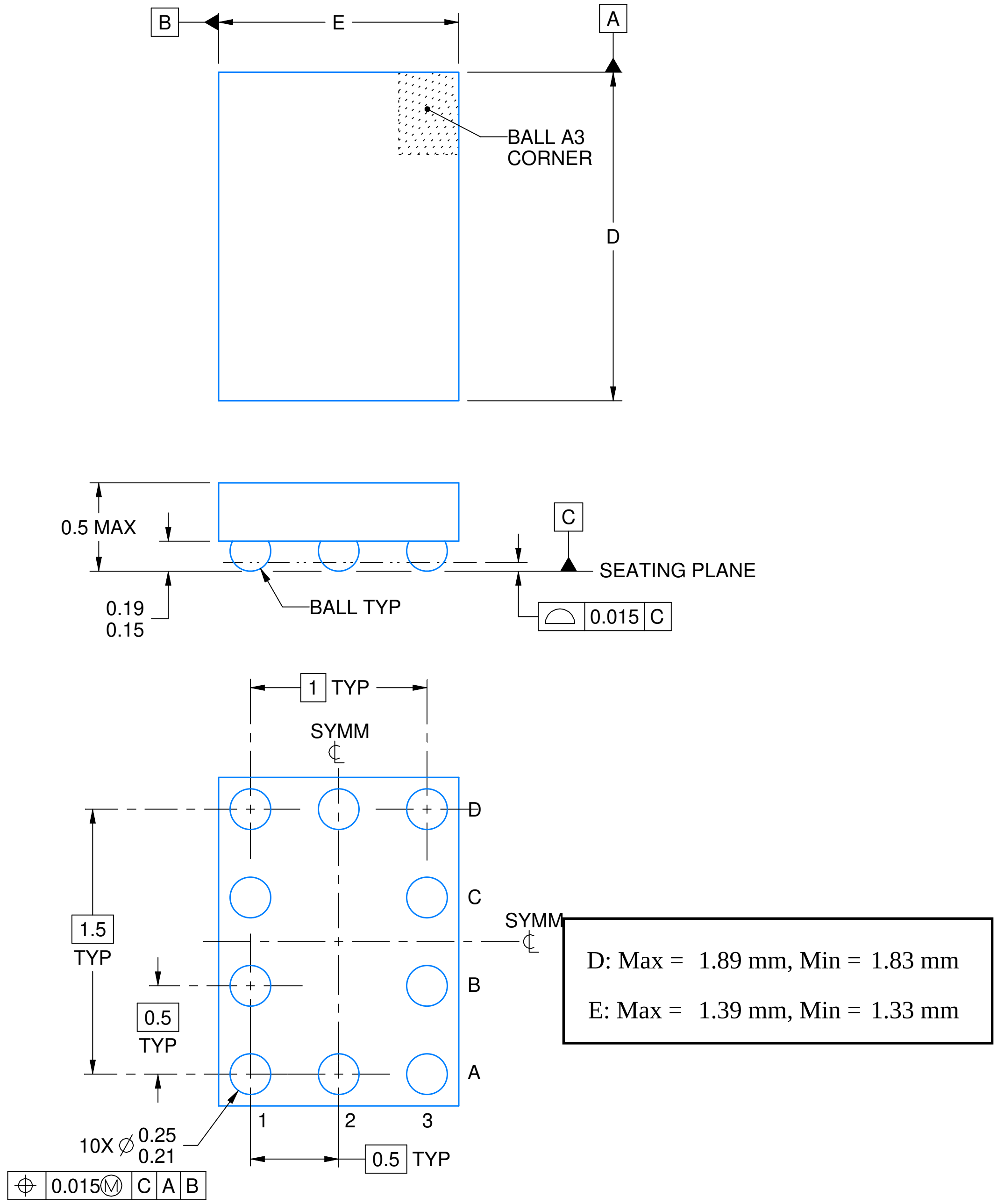
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5A22362DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TS5A22362DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TS5A22362DRCT-NM | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TS5A22362YZPR | DSBGA | YZP | 10 | 3000 | 178.0 | 9.2 | 1.49 | 1.99 | 0.63 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



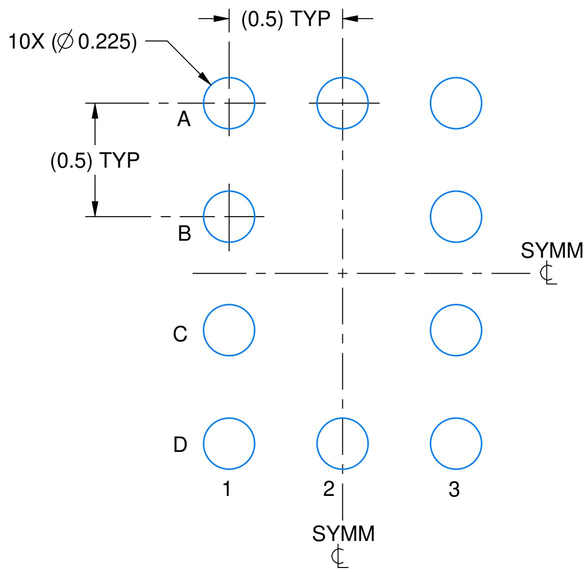

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS5A22362DGSR | VSSOP | DGS | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TS5A22362DRCR | VSON | DRC | 10 | 3000 | 356.0 | 356.0 | 35.0 |
| TS5A22362DRCT-NM | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| TS5A22362YZPR | DSBGA | YZP | 10 | 3000 | 220.0 | 220.0 | 35.0 |

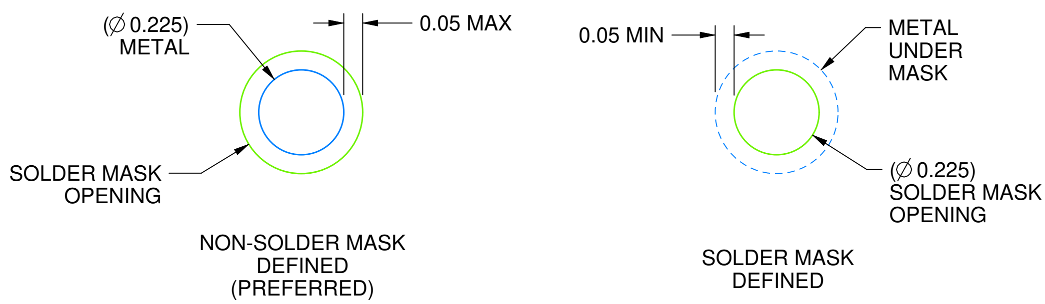



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:30X

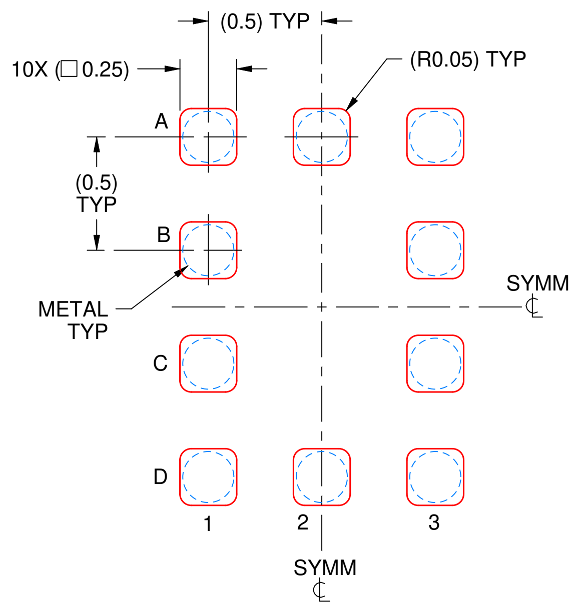



SOLDER MASK DETAILS
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

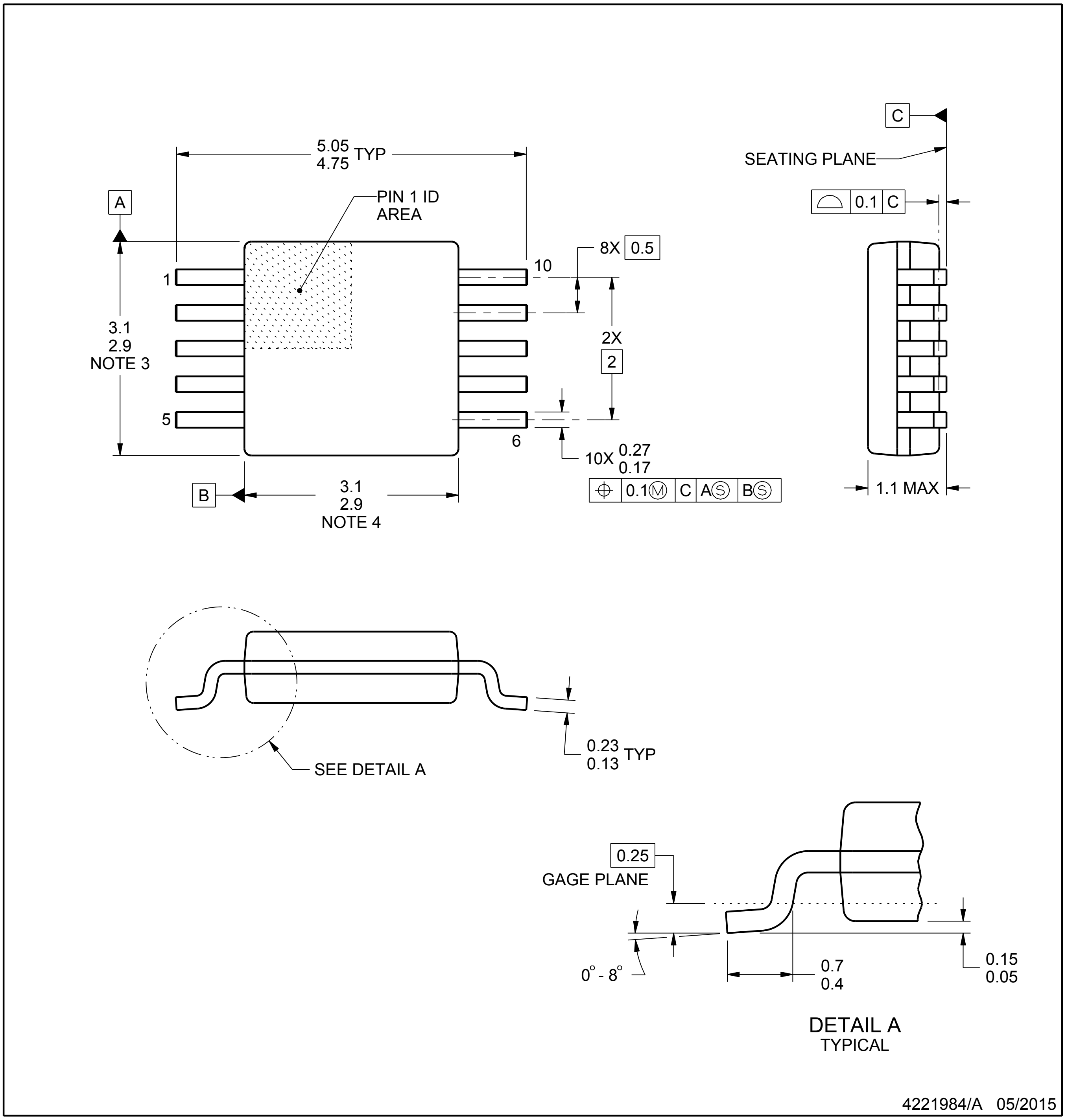



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219350/B 11/2017

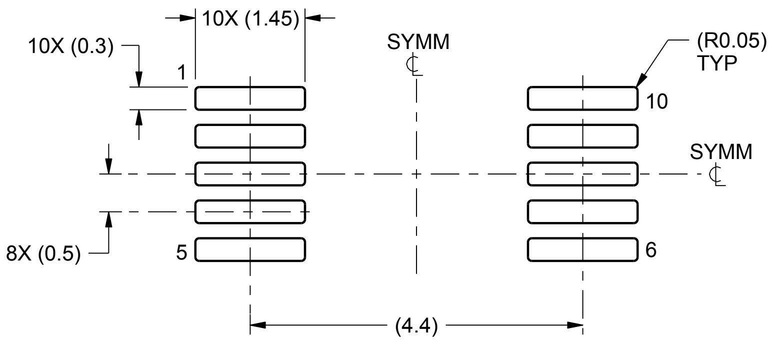
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

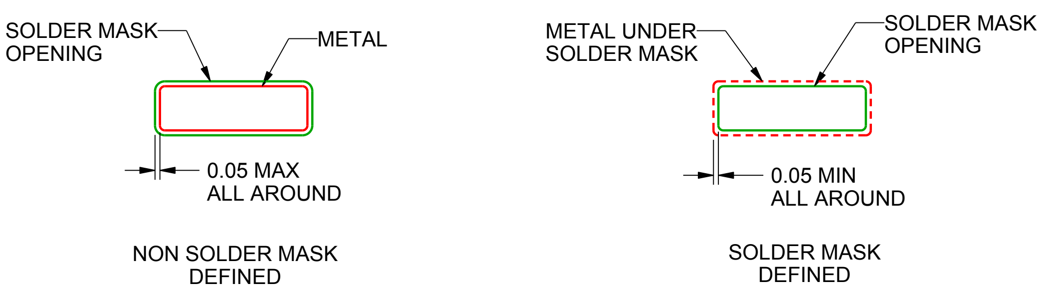



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

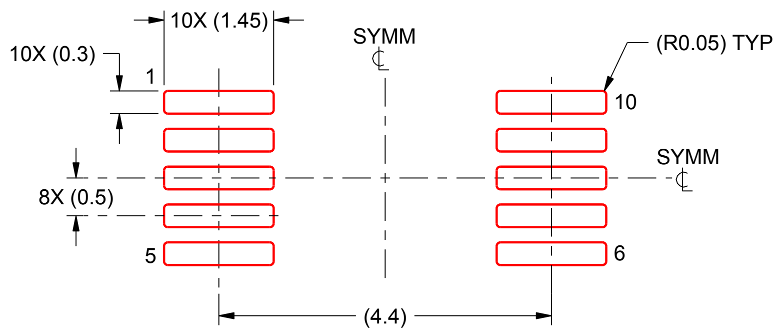



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



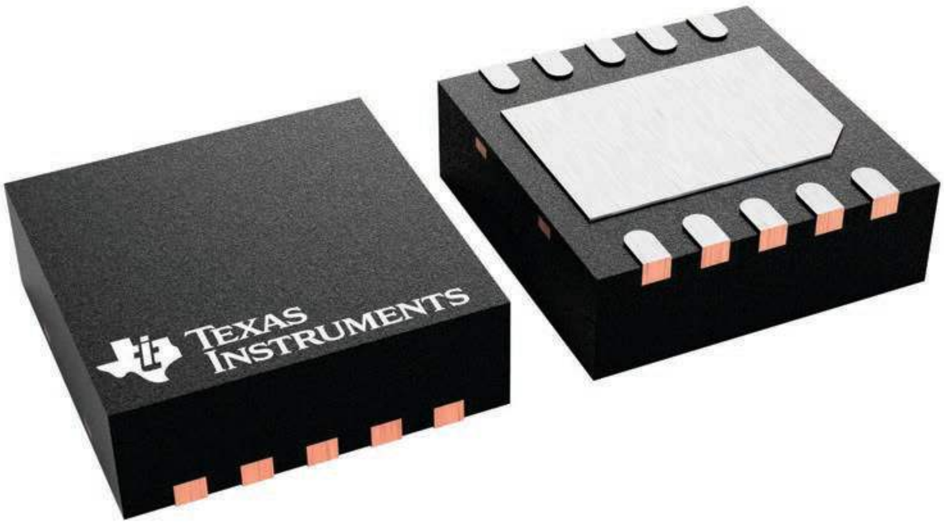

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

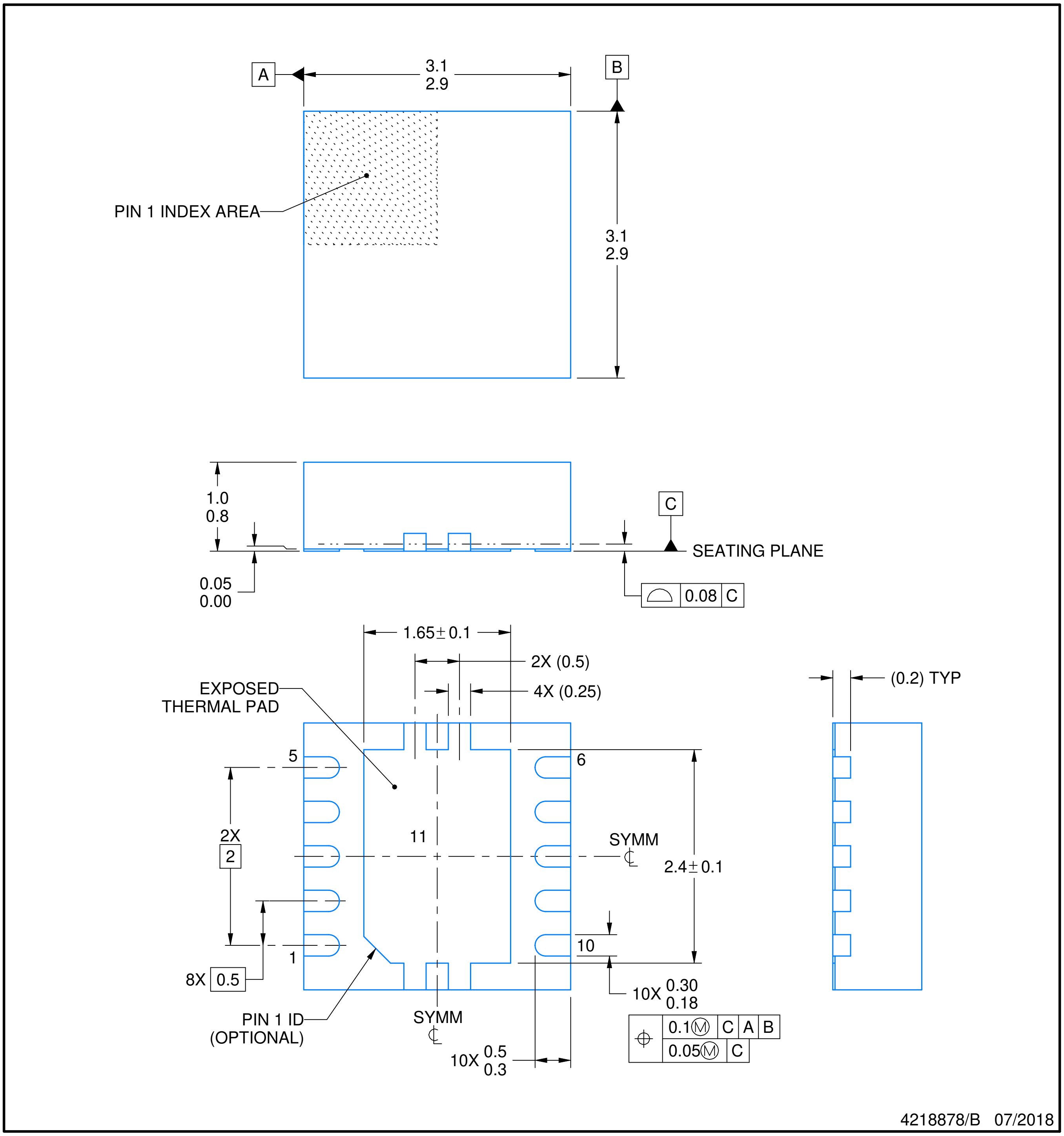
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

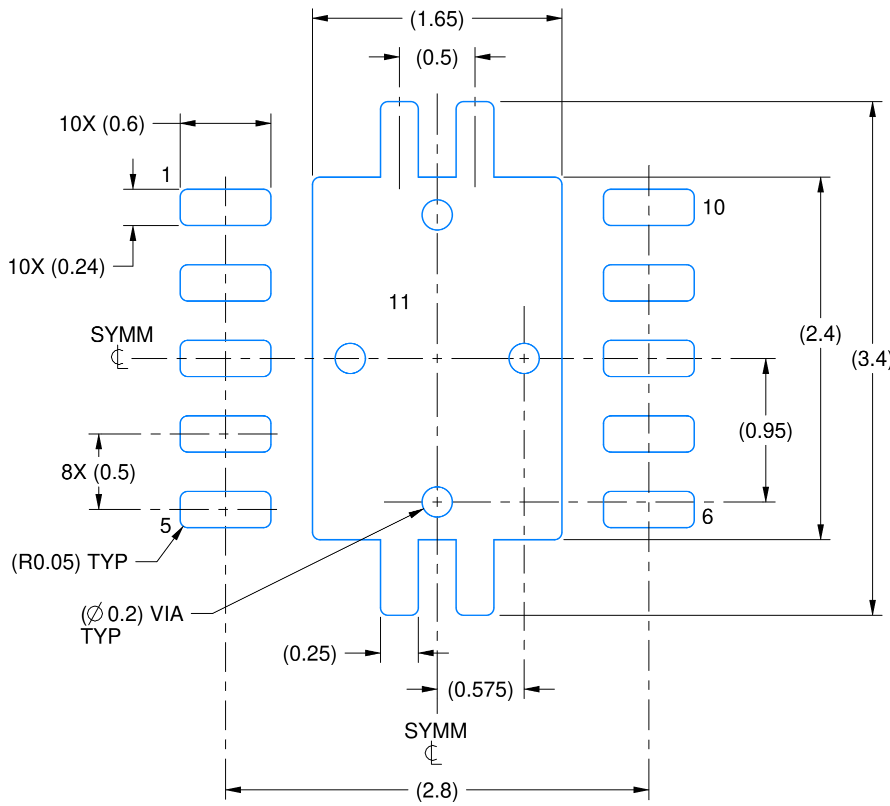



4226193/A

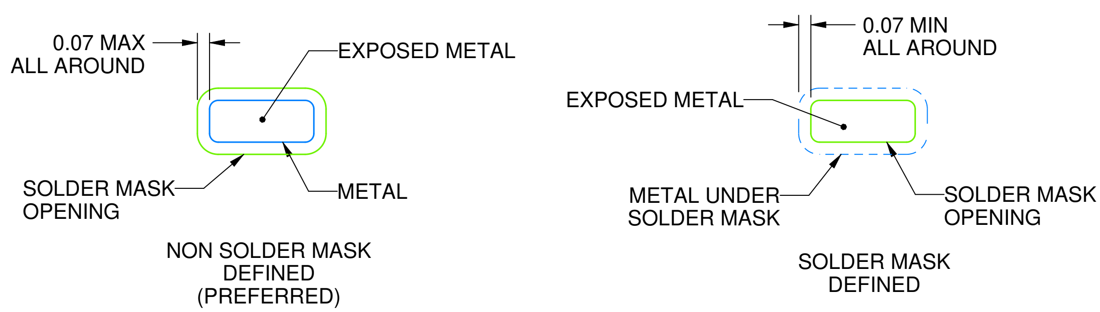



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

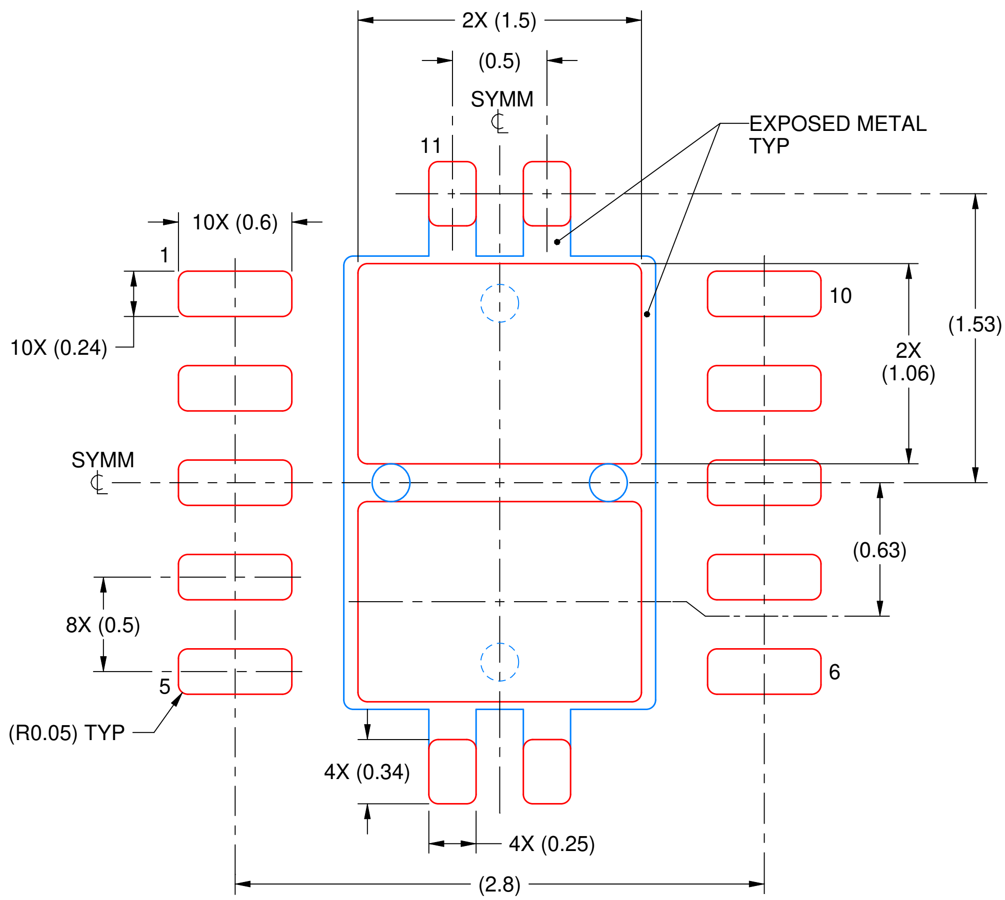



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



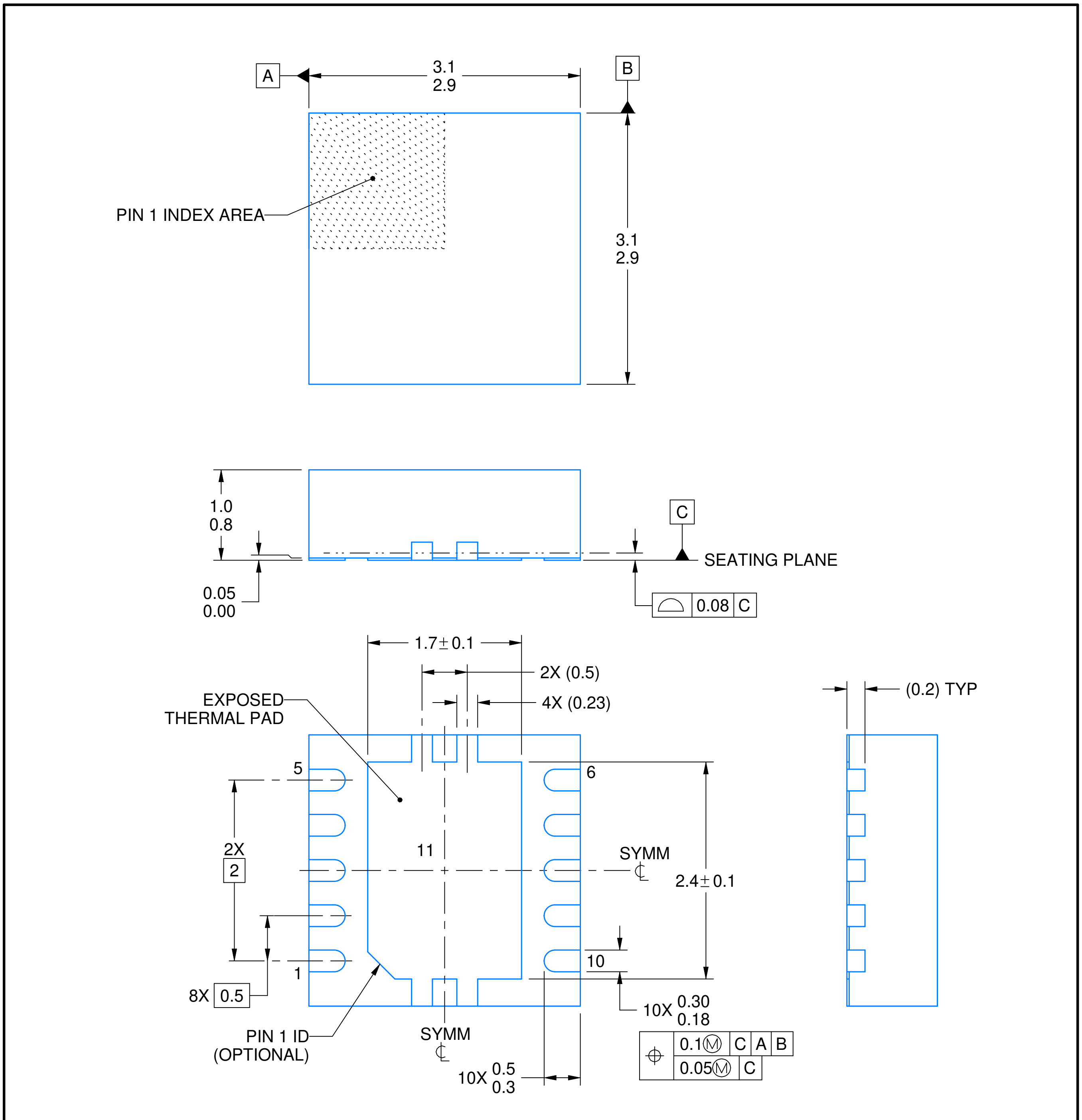

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

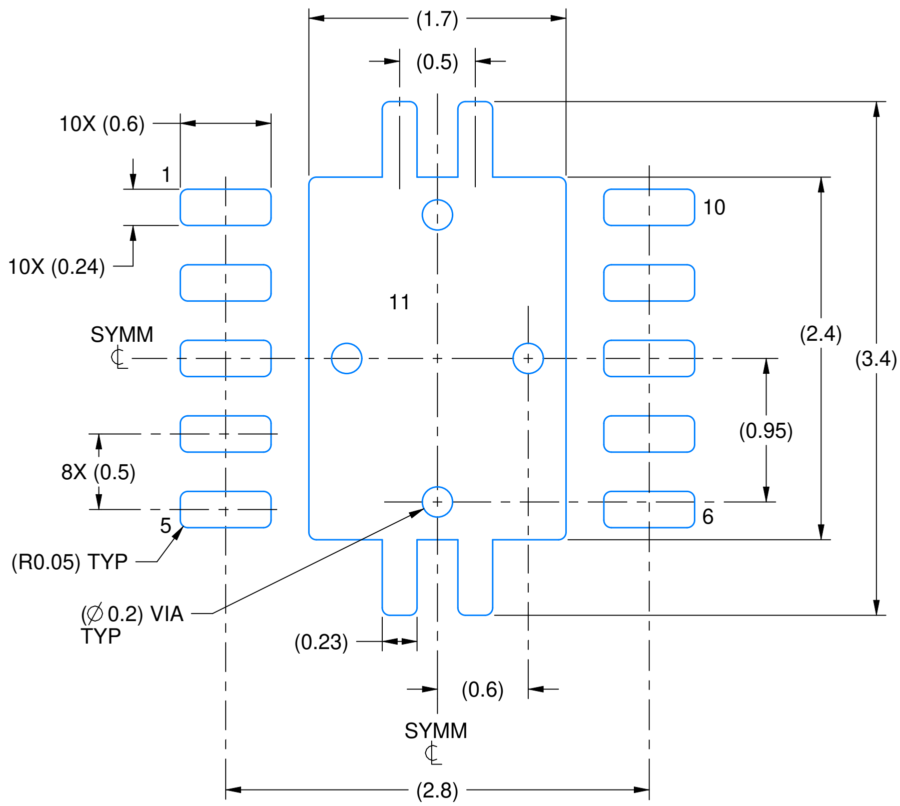
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



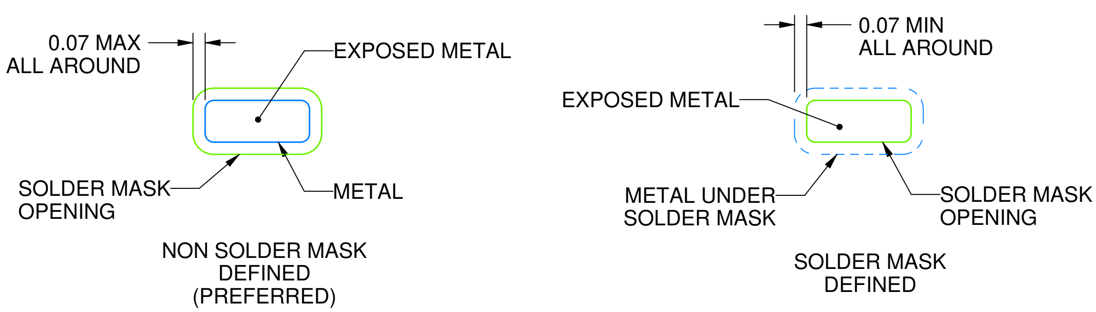

4218883/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

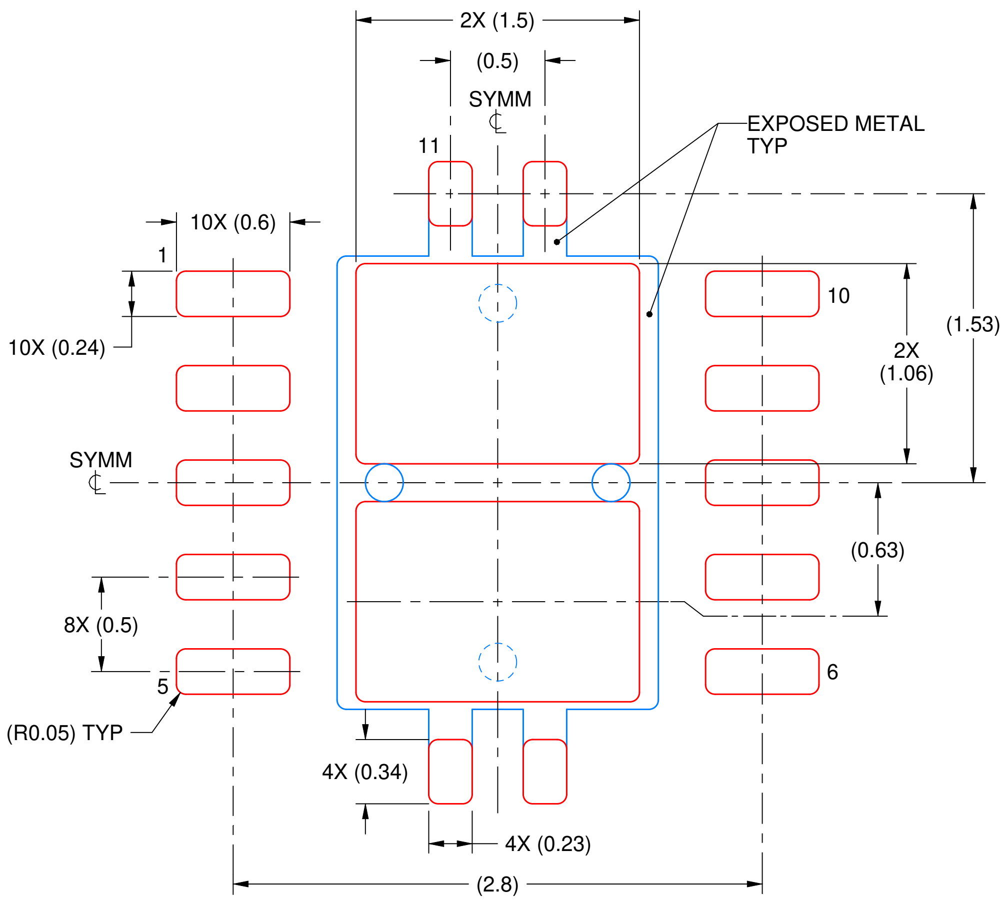



SOLDER MASK DETAILS

4218883/A 12/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218883/A 12/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.