MICROCHIP

TC1302A/B

Low Quiescent Current Dual Output LDO

Features

- Dual Output LDO:
  - V_{OUT1} = 1.5V to 3.3V @ 300 mA
  - V_{OUT2} = 1.5V to 3.3V @ 150 mA
- Output Voltage (See Table 8-1)
- Low Dropout Voltage:
  - V_{OUT1} = 104 mV @ 300 mA Typical
  - V_{OUT2} = 150 mV @ 150 mA Typical
- Low Supply Current: 116 µA Typical TC1302A/B with both output voltages available
- Reference Bypass Input for Low-Noise Operation
- Both Output Voltages Stable with a Minimum of 1 µF Ceramic Output Capacitor
- Separate V_{OUT1} and V_{OUT2} $\overline{SHDN}$ pins (**TC1302B**)
- Power-Saving Shutdown Mode of Operation
- Wake-up from $\overline{SHDN}$: 5.3 µs. Typical
- Small 8-pin DFN or MSOP Package Options
- Operating Junction Temperature Range:
  - -40°C to +125°C
- Overtemperature and Overcurrent Protection

Applications

- Cellular/GSM/PHS Phones
- Battery-Operated Systems
- Hand-Held Medical Instruments
- Portable Computers/PDAs
- Linear Post-Regulators for SMPS
- Pagers

Related Literature

- AN765, “Using Microchip’s Micropower LDOs”, DS00765, Microchip Technology Inc., 2002
- AN766, “Pin-Compatible CMOS Upgrades to BiPolar LDOs”, DS00766, Microchip Technology Inc., 2002
- AN792, “A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”, DS00792, Microchip Technology Inc., 2001

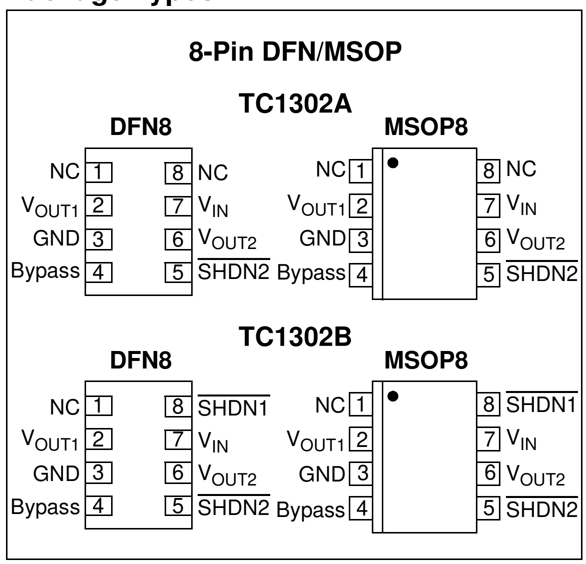
Description

The TC1302A/B combines two Low Dropout (LDO) regulators into a single 8-pin MSOP or DFN package. Both regulator outputs feature low dropout voltage, 104 mV @ 300 mA for V_{OUT1}, 150 mV @ 150 mA for V_{OUT2}, low quiescent current consumption, 58 µA each and a typical regulation accuracy of 0.5%. Several fixed-output voltage combinations are available. A reference bypass pin is available to further reduce output noise and improve the power supply rejection ratio of both LDOs.

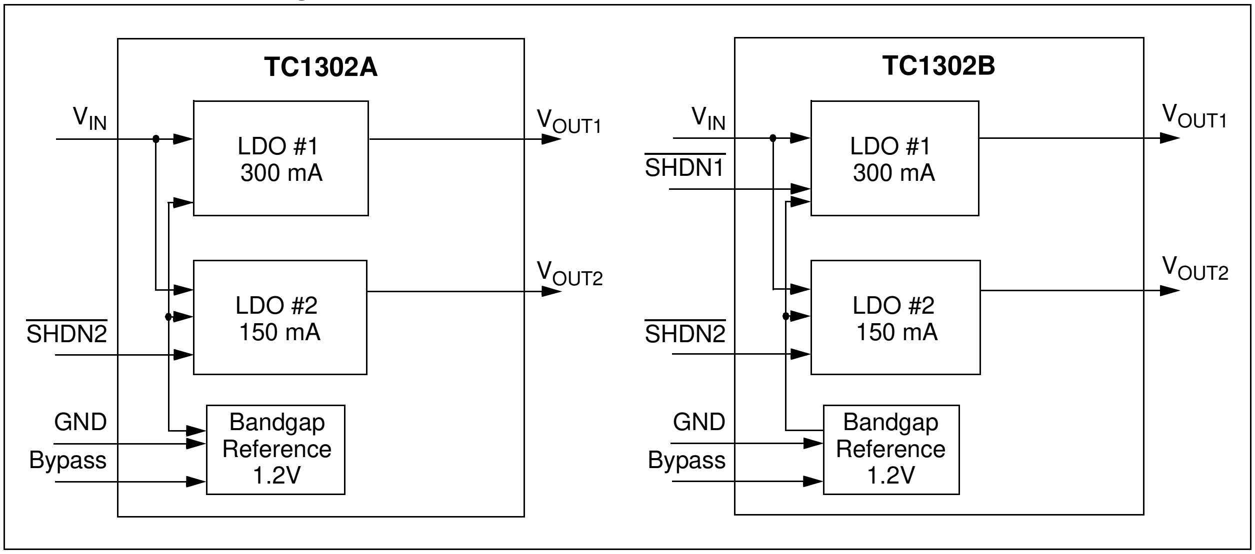
The TC1302A/B is stable over all line and load conditions, with a minimum of 1 µF of ceramic output capacitance, and utilizes a unique compensation scheme to provide fast dynamic response to sudden line voltage and load current changes.

Additional features include an overcurrent limit and overtemperature protection that combine to provide a robust design for all load fault conditions.

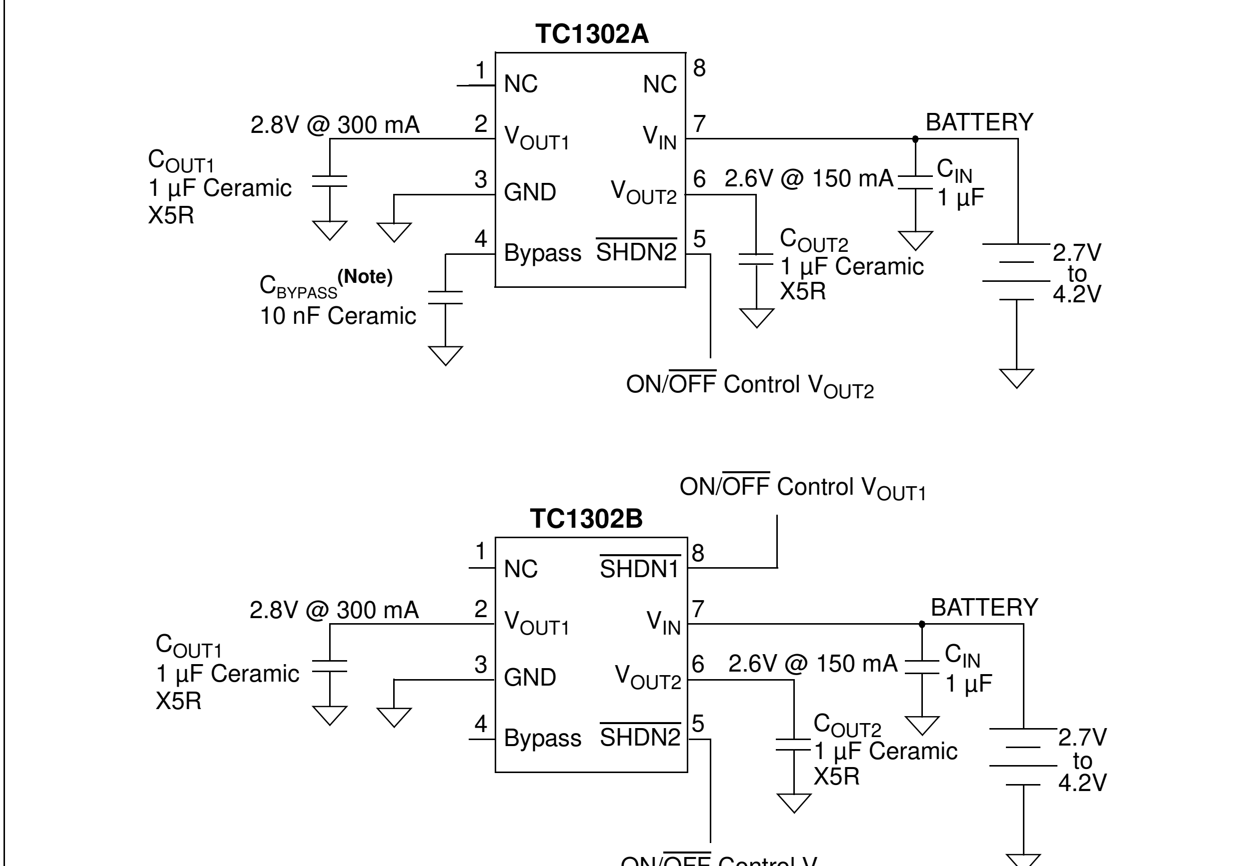
Package Types



Functional Block Diagrams



Typical Application Circuits



Note: C_{BYPASS} is optional

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V
Maximum Voltage on Any Pin ...... (V_{SS} – 0.3) to (V_{IN} + 0.3)V
Power Dissipation ....Internally Limited **(Note 7)**
Storage temperature ....-65°C to +150°C
Maximum Junction Temperature, T_J ....+150°C
Continuous Operating Temperature Range ..-40°C to +125°C
ESD protection on all pins, HBM, MM .... 4 kV, 400V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF, C_{BYPASS} = 10 nF, $\overline{SHDN} > V_{IH}$, T_A = +25°C.
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 1**
Maximum Output Current	$I_{OUT1Max}$	**300**	—	—	mA	V_{IN} = 2.7V to 6.0V **(Note 1)**
Maximum Output Current	$I_{OUT2Max}$	**150**	—	—	mA	V_{IN} = 2.7V to 6.0V **(Note 1)**
Output Voltage Tolerance (V_{OUT1} and V_{OUT2})	V_{OUT}	**V_R – 2.5**	V_R±0.5	**V_R + 2.5**	%	**Note 2**
Temperature Coefficient (V_{OUT1} and V_{OUT2})	TCV_{OUT}	—	25	—	ppm/°C	**Note 3**
Line Regulation (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.02	**0.2**	%/V	$(V_R + 1V) \le V_{IN} \le 6V$
Load Regulation, $V_{OUT} \ge 2.5V$ (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/V_{OUT}$	**-1**	0.1	**+1**	%	I_{OUTX} = 0.1 mA to I_{OUTMax}, **(Note 4)**
Load Regulation, $V_{OUT} < 2.5V$ (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/V_{OUT}$	**-1.5**	0.1	**+1.5**	%	I_{OUTX} = 0.1 mA to I_{OUTMax}, **(Note 4)**
Thermal Regulation	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	%/W	**Note 5**
Dropout Voltage (Note 6)						
V_{OUT1} > 2.7V	$V_{IN} - V_{OUT}$	—	104	**180**	mV	I_{OUT1} = 300 mA
V_{OUT2} > 2.6V	$V_{IN} - V_{OUT}$	—	150	**250**	mV	I_{OUT2} = 150 mA
Supply Current						
TC1302A	$I_{IN(A)}$	—	103	**180**	µA	$\overline{SHDN2} = V_{IN}$, $I_{OUT1} = I_{OUT2}$ = 0 mA
TC1302B	$I_{IN(B)}$	—	114	**180**	µA	$\overline{SHDN1} = \overline{SHDN2} = V_{IN}$, $I_{OUT1} = I_{OUT2}$ = 0 mA

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \ge 2.7V$ and $V_{IN} \ge V_R + V_{DROPOUT}$.
2: V_R is defined as the higher of the two regulator nominal output voltages (V_{OUT1} or V_{OUT2}).
3: $TCV_{OUT} = ((V_{OUTmax} - V_{OUTmin}) * 10^6)/(V_{OUT} * \Delta T)$.
4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 msec.
6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.
7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

DC CHARACTERISTICS (Continued)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF, C_{BYPASS} = 10 nF, $\overline{SHDN} > V_{IH}$, T_A = +25°C. **Boldface** type specifications apply for junction temperatures of -40°C to +125°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Shutdown Supply Current **TC1302A**	$I_{IN\_\overline{SHDNA}}$	—	58	**90**	µA	$\overline{SHDN2}$ = GND
Shutdown Supply Current **TC1302B**	$I_{IN\_\overline{SHDNB}}$	—	0.1	1	µA	$\overline{SHDN1} = \overline{SHDN2}$ = GND
Power Supply Rejection Ratio	PSRR	—	58	—	dB	f ≤ 100 Hz, $I_{OUT1} = I_{OUT2}$ = 50 mA, C_{IN} = 0 µF
Output Noise	eN	—	830	—	$nV/(Hz)^{½}$	f ≤ 1 kHz, $I_{OUT1} = I_{OUT2}$ = 50 mA, C_{IN} = 0 µF
Output Short Circuit Current (Average)						
V_{OUT1}	I_{OUTsc1}	—	200	—	mA	$R_{LOAD1} \leq 1\Omega$
V_{OUT2}	I_{OUTsc2}	—	140	—	mA	$R_{LOAD2} \leq 1\Omega$
$\overline{SHDN}$ Input High Threshold	V_{IH}	**45**	—	—	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V
$\overline{SHDN}$ Input Low Threshold	V_{IL}	—	—	**15**	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V
Wake Up Time (From $\overline{SHDN}$ mode), (V_{OUT2})	t_{WK}	—	5.3	20	µs	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 30 mA, **See Figure 5-1**
Settling Time (From $\overline{SHDN}$ mode), (V_{OUT2})	t_S	—	50	—	µs	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 50 mA, **See Figure 5-2**
Thermal Shutdown Die Temperature	T_{SD}	—	150	—	°C	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 100 µA
Thermal Shutdown Hysteresis	T_{HYS}	—	10	—	°C	V_{IN} = 5V

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_R + V_{DROPOUT}$.

2: V_R is defined as the higher of the two regulator nominal output voltages (V_{OUT1} or V_{OUT2}).

3: $TCV_{OUT} = ((V_{OUTmax} - V_{OUTmin}) * 10^6)/(V_{OUT} * \Delta T)$.

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 msec.

6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits are specified for: V_{IN} = +2.7V to +6.0V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_A	-40	—	+125	°C	Steady State
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Thermal Package Resistances						
Thermal Resistance, MSOP8	θ_{JA}	—	208	—	°C/W	Typical 4-Layer Board
Thermal Resistance, DFN8	θ_{JA}	—	41	—	°C/W	Typical 4-Layer Board with Vias

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$, $T_A = +25°C$.

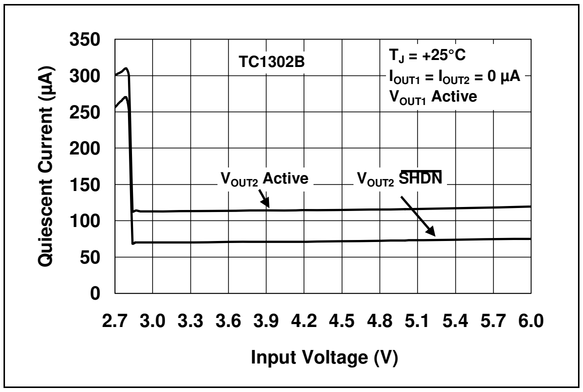


FIGURE 2-1: Quiescent Current vs. Input Voltage.

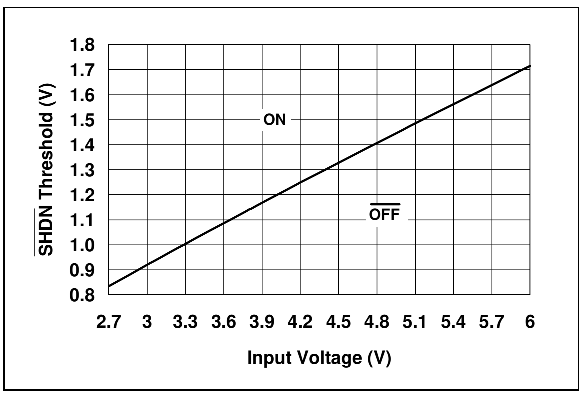


FIGURE 2-2: $\overline{SHDN}$ Voltage Threshold vs. Input Voltage.

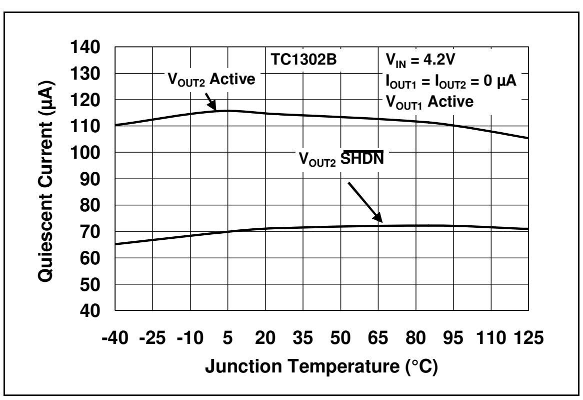


FIGURE 2-3: Quiescent Current vs. Junction Temperature.

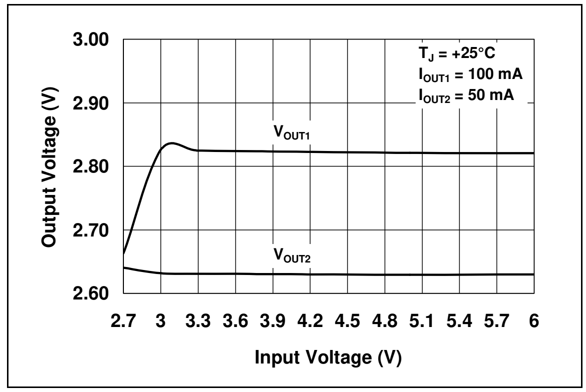


FIGURE 2-4: Output Voltage vs. Input Voltage.

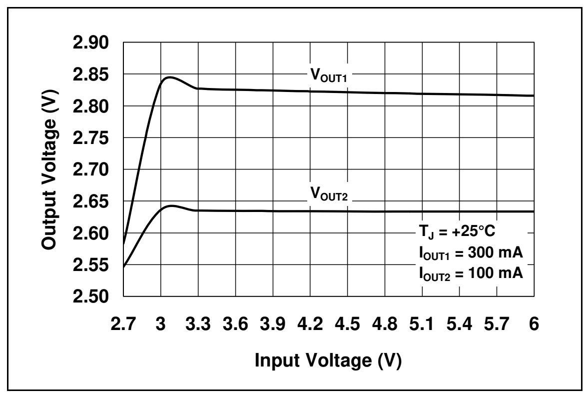


FIGURE 2-5: Output Voltage vs. Input Voltage.

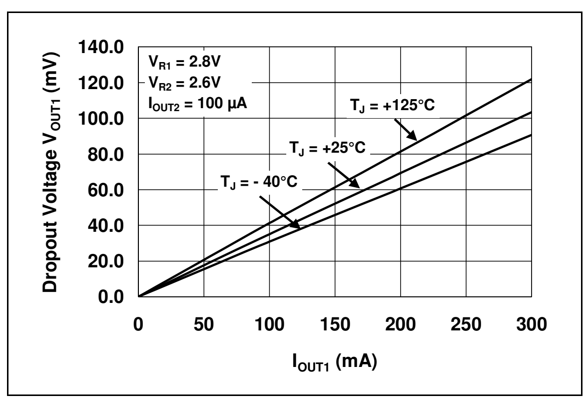


FIGURE 2-6: Dropout Voltage vs. Output Current (V_{OUT1}).

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$, $T_A = +25°C$.

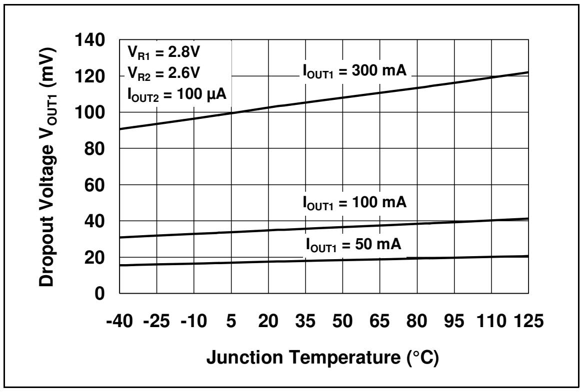


FIGURE 2-7: Dropout Voltage vs. Junction Temperature (V_{OUT1}).

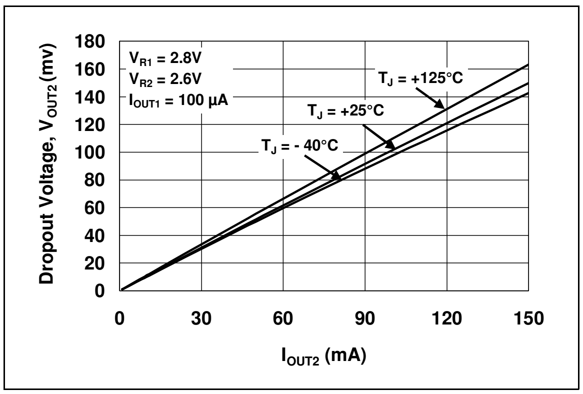


FIGURE 2-8: Dropout Voltage vs. Output Current (V_{OUT2}).

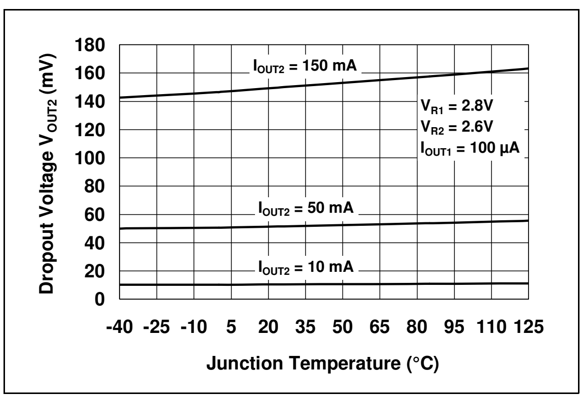


FIGURE 2-9: Dropout Voltage vs. Junction Temperature (V_{OUT2}).

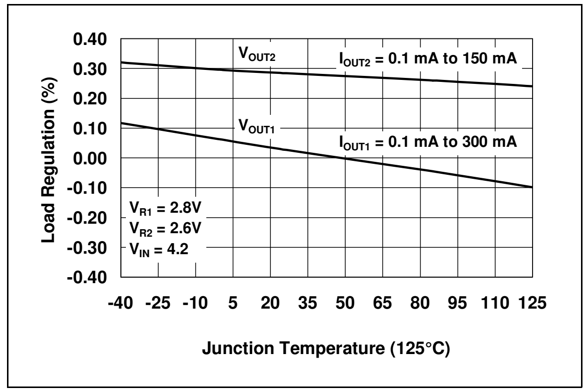


FIGURE 2-10: V_{OUT1} and V_{OUT2} Load Regulation vs. Junction Temperature.

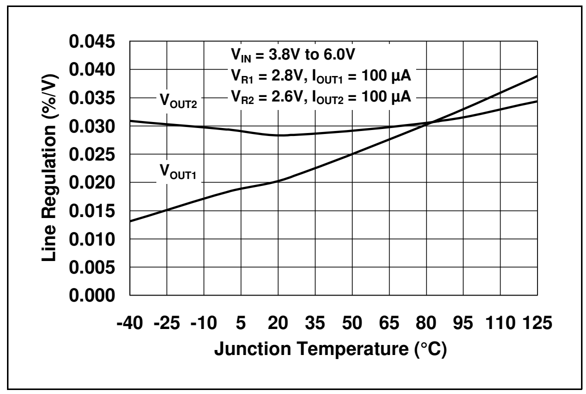


FIGURE 2-11: V_{OUT1} and V_{OUT2} Line Regulation vs. Junction Temperature.

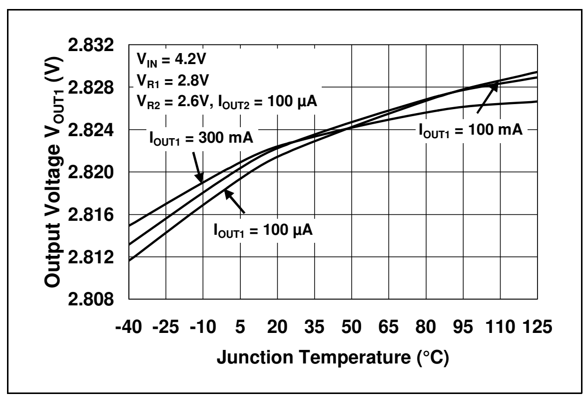


FIGURE 2-12: V_{OUT1} vs. Junction Temperature.

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$, $T_A = +25°C$.

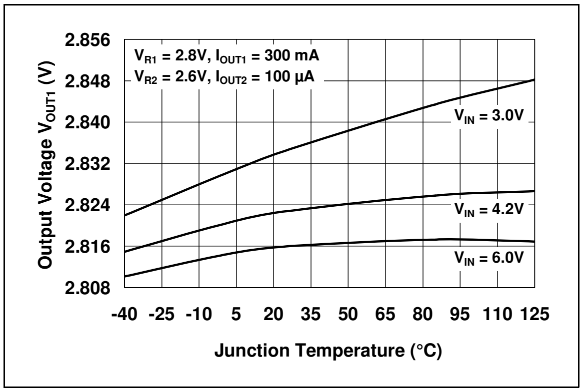


FIGURE 2-13: *V_{OUT1} vs. Junction Temperature.*

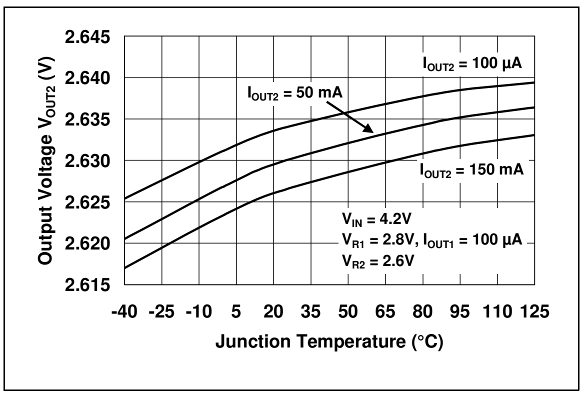


FIGURE 2-14: *V_{OUT2} vs. Junction Temperature.*

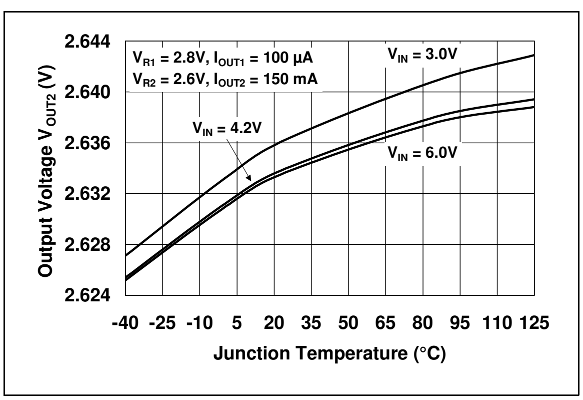


FIGURE 2-15: *V_{OUT2} vs. Junction Temperature.*

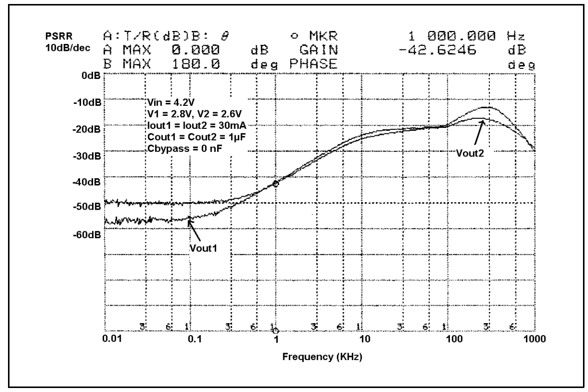


FIGURE 2-16: *Power Supply Rejection Ratio vs. Frequency (without bypass capacitor).*

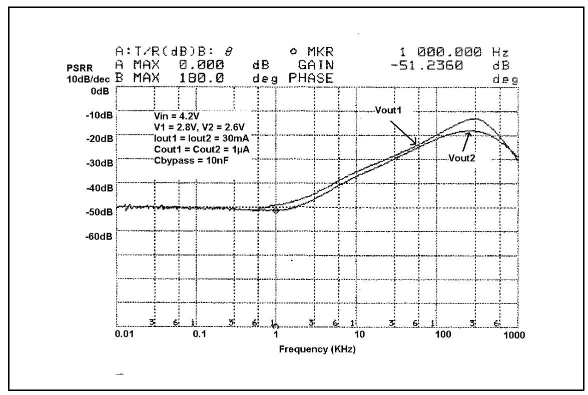


FIGURE 2-17: *Power Supply Rejection Ratio vs. Frequency (with bypass capacitor).*

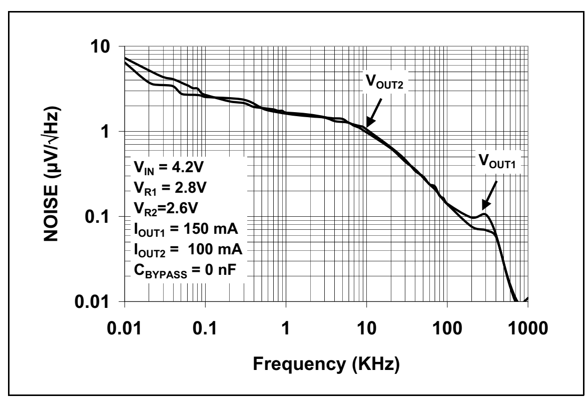


FIGURE 2-18: *V_{OUT1} and V_{OUT2} Noise vs. Frequency (without bypass capacitor).*

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0\ pF$, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$, $T_A = +25°C$.

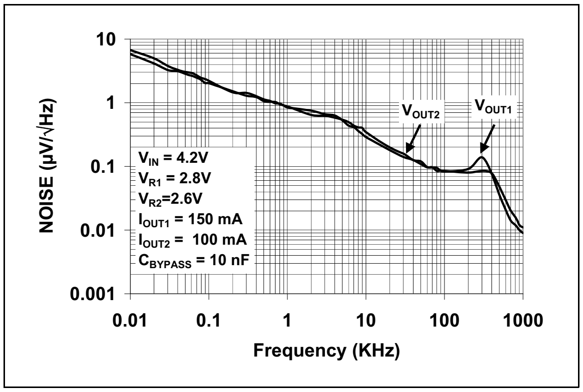


FIGURE 2-19: *V_{OUT1} and V_{OUT2} Noise vs. Frequency (with bypass capacitor).*

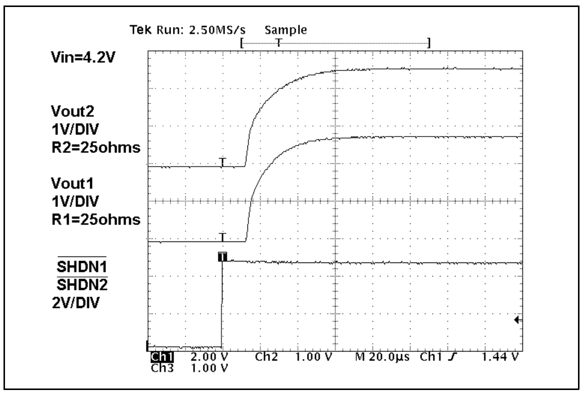


FIGURE 2-20: *V_{OUT1} and V_{OUT2} Power-up from Shutdown TC1302B.*

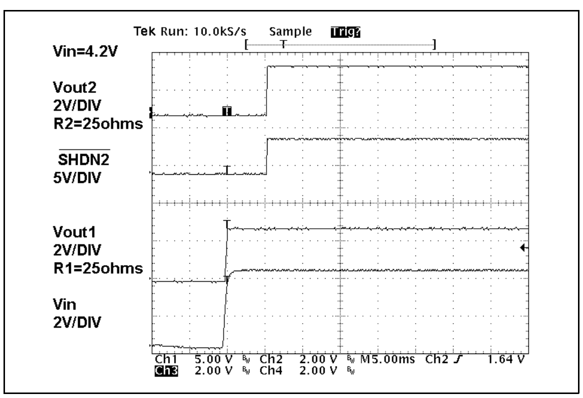


FIGURE 2-21: *V_{OUT2} Power-up from Shutdown Input TC1302A.*

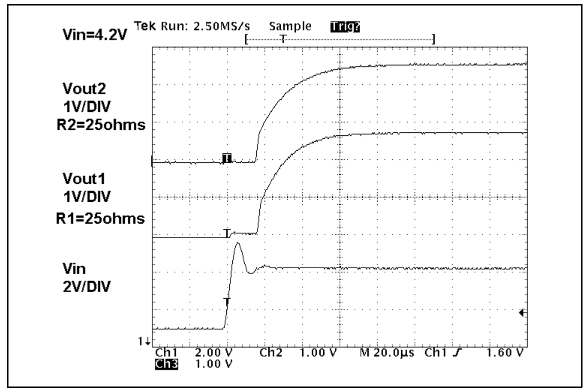


FIGURE 2-22: *V_{OUT1} and V_{OUT2} Power-up from Input Voltage TC1302B.*

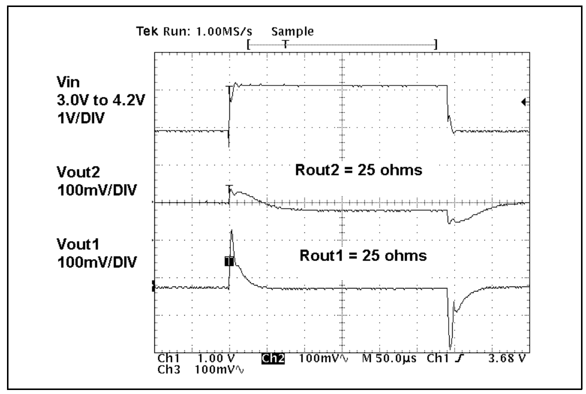


FIGURE 2-23: *Dynamic Line Response.*

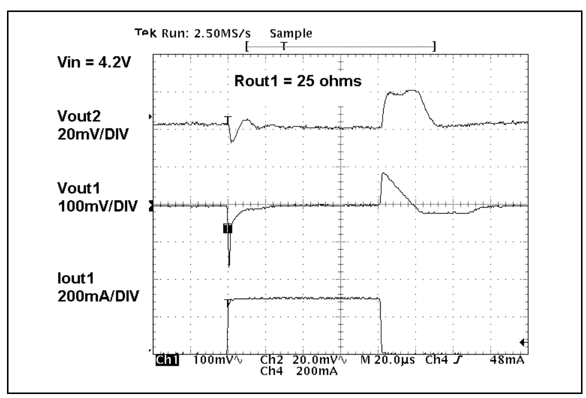


FIGURE 2-24: *300 mA Dynamic Load Step V_{OUT1}.*

Note: Unless otherwise indicated, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF (X5R or X7R), C_{BYPASS} = 0 pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$, T_A = +25°C.

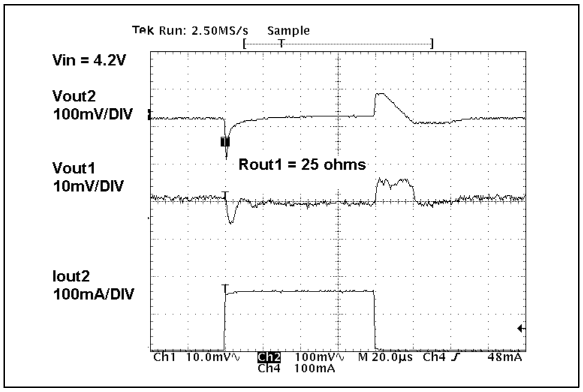


FIGURE 2-25: *150 mA Dynamic Load Step V_{OUT2}.*

3.0 TC1302A PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: TC1302A PIN FUNCTION TABLE

Pin No.	Name	Function
1	NC	No connect.
2	V_{OUT1}	Regulated output voltage #1, capable of 300 mA.
3	GND	Circuit ground pin.
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.
5	$\overline{SHDN2}$	Output #2 shutdown control input.
6	V_{OUT2}	Regulated output voltage #2, capable of 150 mA.
7	V_{IN}	Unregulated input voltage pin.
8	NC	No connect.

3.1 Regulated Output Voltage #1 (V_{OUT1})

Connect V_{OUT1} to the positive side of the V_{OUT1} capacitor and load. Capable of 300 mA maximum output current. V_{OUT1} output is available when V_{IN} is available; there is no pin to turn it $\overline{OFF}$. See TC1302B if ON/$\overline{OFF}$ control of V_{OUT1} is desired.

3.2 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 µA maximum).

3.3 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the Bypass Input, both outputs (V_{OUT1} and V_{OUT2}) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

3.4 Output Voltage #2 Shutdown ($\overline{SHDN2}$)

ON/$\overline{OFF}$ control is performed by connecting $\overline{SHDN2}$ to its proper level. When the input of this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT2} will be $\overline{OFF}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT2} will be turned ON.

3.5 Regulated Output Voltage #2 (V_{OUT2})

Connect V_{OUT2} to the positive side of the V_{OUT2} capacitor and load. This pin is capable of a maximum output current of 150 mA. V_{OUT2} can be turned ON and $\overline{OFF}$ using $\overline{SHDN2}$.

3.6 Unregulated Input Voltage Pin (V_{IN})

Connect the unregulated input voltage source to V_{IN}. If the input voltage source is located more than several inches away or is a battery, a typical input capacitance of 1 µF to 4.7 µF is recommended.

4.0 TC1302B PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: TC1302B PIN FUNCTION TABLE

Pin No.	Name	Function
1	NC	No connect.
2	V_{OUT1}	Regulated output voltage #1, capable of 300 mA.
3	GND	Circuit ground pin.
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.
5	$\overline{SHDN2}$	Output #2 shutdown control input.
6	V_{OUT2}	Regulated output voltage #2, capable of 150 mA.
7	V_{IN}	Unregulated Input voltage pin.
8	$\overline{SHDN1}$	Output #1 shutdown control input.

4.1 Regulated Output Voltage #1 (V_{OUT1})

Connect V_{OUT1} to the positive side of the V_{OUT1} capacitor and load. Capable of 300 mA maximum output current. For the TC1302B, V_{OUT1} can be turned ON and $\overline{OFF}$ using the $\overline{SHDN1}$ input pin.

4.2 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 µA maximum).

4.3 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the bypass input, both outputs (V_{OUT1} and V_{OUT2}) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage startup time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the startup time will be minimized.

4.4 Output Voltage #2 Shutdown ($\overline{SHDN2}$)

ON/$\overline{OFF}$ control is performed by connecting $\overline{SHDN2}$ to its proper level. When this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT2} will be $\overline{OFF}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT2} will be turned ON.

4.5 Regulated Output Voltage #2 (V_{OUT2})

Connect V_{OUT2} to the positive side of the V_{OUT2} capacitor and load. This pin is capable of a maximum output current of 150 mA. V_{OUT2} can be turned ON and $\overline{OFF}$ using $\overline{SHDN2}$.

4.6 Unregulated Input Voltage Pin (V_{IN})

Connect the unregulated input voltage source to V_{IN}. If the input voltage source is located more than several inches away, or is a battery, a typical minimum input capacitance of 1 µF and 4.7 µF is recommended.

4.7 Output Voltage #1 Shutdown ($\overline{SHDN1}$)

ON/$\overline{OFF}$ control is performed by connecting $\overline{SNDN1}$ to its proper level. When this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT1} will be $\overline{OFF}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT1} will be turned ON.

5.0 DETAILED DESCRIPTION

5.1 Device Overview

The TC1302A/B is a combination device consisting of one 300 mA LDO regulator with a fixed output voltage V_{OUT1} (1.5V – 3.3V) and one 150 mA LDO regulator with a fixed output voltage V_{OUT2} (1.5V – 3.3V).

For the TC1302A, the 300 mA output (V_{OUT1}) is always present, independent of the level of $\overline{SHDN2}$. The 150 mA output (V_{OUT2}) can be turned ON/$\overline{OFF}$ by controlling the level of $\overline{SHDN2}$.

For the TC1302B, V_{OUT1} and V_{OUT2} each have independent shutdown input pins ($\overline{SHDN1}$ and $\overline{SHDN2}$) to control their respective outputs.

5.2 LDO Output #1

LDO output #1 is rated for 300 mA of output current. The typical dropout voltage for V_{OUT1} = 104 mV @ 300 mA. A 1 µF (minimum) output capacitor is needed for stability and should be located as close to the V_{OUT1} pin and ground as possible.

5.3 LDO Output #2

LDO output #2 is rated for 150 mA of output current. The typical dropout voltage for V_{OUT2} = 150 mV. A 1 µF (minimum) capacitor is needed for stability and should be located as close to the V_{OUT2} pin and ground as possible.

5.4 Input Capacitor

Low input source impedance is necessary for the two LDO outputs to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications. When using large capacitors on the LDO outputs, larger capacitance is recommended on the LDO input. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

5.5 Output Capacitor

A minimum output capacitance of 1 µF for each of the TC1302A/B LDO outputs is necessary for stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities. Tantalum or aluminum electrolytic capacitors can be used on the LDO outputs as well. The Equivalent Series Resistance (ESR) requirements on the electrolytic output capacitor's are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 uF X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger LDO output capacitors can be used with the TC1302A/B to improve dynamic performance and power supply ripple rejection performance. A maximum of 10 µF is recommended. Aluminum electrolytic capacitors are not recommended for low temperature applications of < -25 °C.

5.6 Bypass Input

The Bypass pin is connected to the internal LDO reference. By adding capacitance to this pin, the LDO ripple rejection, input voltage transient response and output noise performance are all increased. A typical bypass capacitor between 470 pF to 10 nF is recommended. Larger bypass capacitors can be used, but result in a longer time period for the LDO outputs to reach their rated output voltage when started from $\overline{SHDN}$ or V_{IN}.

5.7 GND

For the optimal noise and PSRR performance, the GND pin of the TC1302A/B should be tied to a quiet circuit ground. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

5.8 $\overline{SHDN1}$/$\overline{SHDN2}$ Operation

The TC1302A $\overline{SHDN2}$ pin is used to turn V_{OUT2} ON and $\overline{OFF}$. A logic-high level on $\overline{SHDN2}$ will enable the V_{OUT2} output, while a logic-low on the $\overline{SHDN2}$ pin will disable the V_{OUT2} output. For the TC1302A, V_{OUT1} is not affected by $\overline{SHDN2}$ and will be enabled as long as the input voltage is present.

The TC1302B $\overline{SHDN1}$ and $\overline{SHDN2}$ pins are used to turn V_{OUT1} and V_{OUT2} ON and $\overline{OFF}$. They operate independent of each other.

5.9 TC1302A $\overline{SHDN2}$ Timing

V_{OUT1} will rise independent of the level of $\overline{SHDN2}$ for the TC1302A. Figure 5-1 is used to define the wake-up time from shutdown (t_{WK}) and the settling time (t_S). The wake-up time is dependant upon the frequency of operation. The faster the $\overline{SHDN}$ pin is pulsed, the shorter the wake-up time will be.

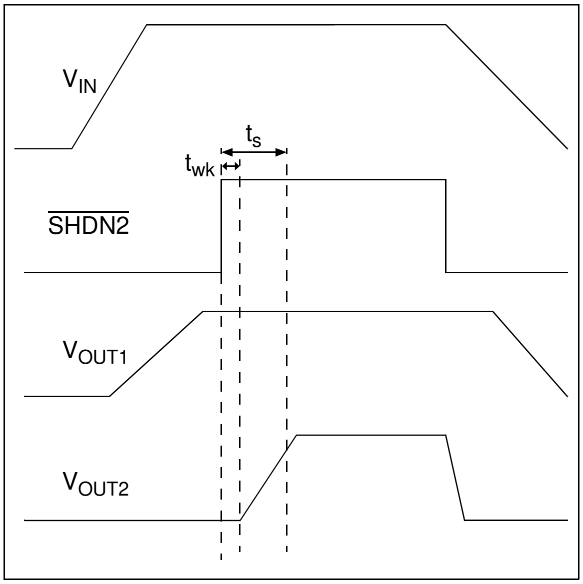


FIGURE 5-1: *TC1302A Timing.*

5.10 TC1302B $\overline{SHDN1}$/$\overline{SHDN2}$ Timing

For the TC1302B, the $\overline{SHDN1}$ input pin is used to control V_{OUT1}. The $\overline{SHDN2}$ input pin is used to control V_{OUT2}, independent of the logic input on $\overline{SHDN1}$.

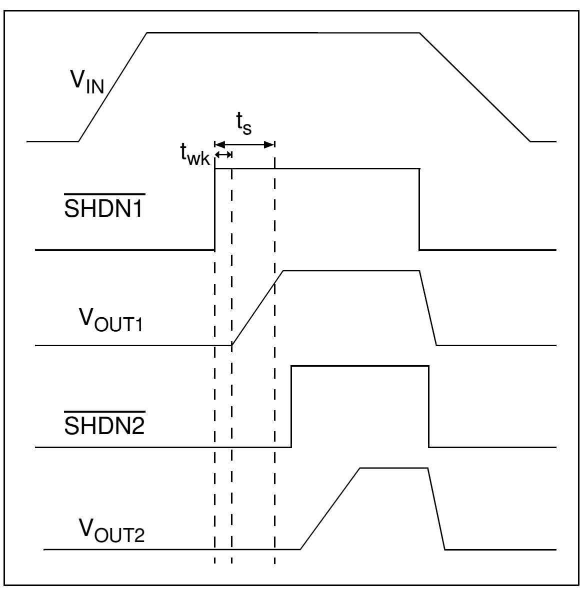


FIGURE 5-2: *TC1302B Timing.*

5.11 Device Protection

5.11.1 OVERCURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO output will permit to flow is limited internally for each of the TC1302A/B outputs. The peak current limit for V_{OUT1} is typically 1.1A, while the peak current limit for V_{OUT2} is typically 0.5A. During short-circuit operation, the average current is limited to 200 mA for V_{OUT1} and 140 mA for V_{OUT2}.

5.11.2 OVERTEMPERATURE PROTECTION

If the internal power dissipation within the TC1302A/B is excessive due to a faulted load or higher-than-specified line voltage, an internal temperature-sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does reach 150°C, both outputs will be disabled until the junction temperature cools to approximately 140°C and the device resumes normal operation. If the internal power dissipation continues to be excessive, the device will again shut off.

6.0 APPLICATION CIRCUITS/ ISSUES

6.1 Typical Application

The TC1302A/B is used for applications that require the integration of two LDOs.

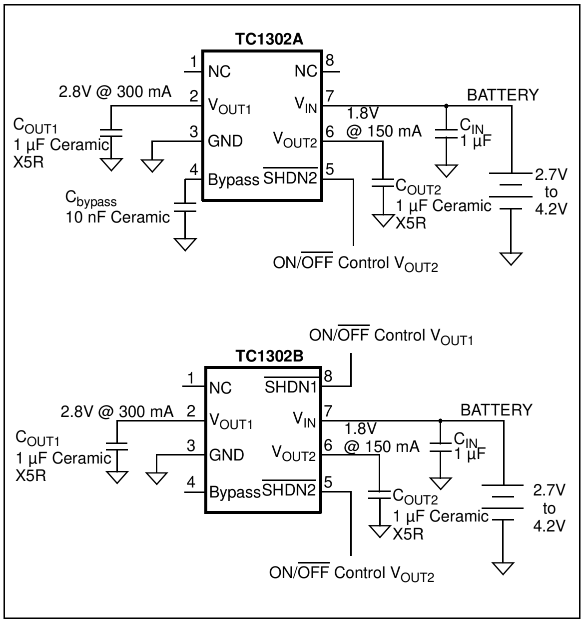


FIGURE 6-1: *Typical Application Circuit TC1302A/B.*

6.1.1 APPLICATION INPUT CONDITIONS

Package Type = 3x3DFN8

Input Voltage Range = 2.7V to 4.2V

V_{IN} maximum = 4.2V

V_{IN} typical = 3.6V

V_{OUT1} = 300 mA maximum

V_{OUT2} = 150 mA maximum

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation within the TC1302A/B is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for each LDO.

EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

P_{LDO} = LDO Pass device internal power dissipation

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the TC1302A/B as a result of quiescent or ground current. The power dissipation, as a result of the ground current, can be calculated using the following equation.

EQUATION 6-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

$P_{I(GND)}$ = Total current in ground pin.

$V_{IN(MAX)}$ = Maximum input voltage.

I_{VIN} = Current flowing in the V_{IN} pin with no output current on either LDO output.

The total power dissipated within the TC1302A/B is the sum of the power dissipated in both of the LDOs and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the TC1302A/B is 116 µA. Operating at a maximum of 4.2V results in a power dissipation of 0.5 milliWatts. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the TC1302A/B is +125°C. To estimate the internal junction temperature of the TC1302A/B, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction-to-ambient for the 3x3DFN8 pin package is estimated at 41° C/W.

EQUATION 6-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature.

P_{TOTAL} = Total device power dissipation.

$R\theta_{JA}$ = Thermal resistance from junction to ambient.

T_{AMAX} = Maximum Ambient Temperature.

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 6-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = maximum device power dissipation.
$T_{J(MAX)}$ = maximum continuous junction temperature.
$T_{A(MAX)}$ = maximum ambient temperature.
$R\theta_{JA}$ = Thermal resistance from junction to ambient.

EQUATION 6-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature.
$P_{D(MAX)}$ = Maximum device power dissipation.
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient.

EQUATION 6-6:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction temperature.
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature.
T_A = Ambient Temperature.

6.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 3x3DFN8

Input Voltage

V_{IN} = 2.7V to 4.2V

LDO Output Voltages and Currents

V_{OUT1} = 2.8V

I_{OUT1} = 300 mA

V_{OUT2} = 1.8V

I_{OUT2} = 150 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = 50°C

Internal Power Dissipation

Internal power dissipation is the sum of the power dissipation for each LDO pass device.

$P_{LDO1(MAX)}$ = ($V_{IN(MAX)}$ - $V_{OUT1(MIN)}$) x $I_{OUT1(MAX)}$

P_{LDO1} = (4.2V - (0.975 x 2.8V)) x 300 mA

P_{LDO1} = 441.0 milliWatts

P_{LDO2} = (4.2V - (0.975 X 1.8V)) x 150 mA

P_{LDO2} = 366.8 milliWatts

P_{TOTAL} = P_{LDO1} + P_{LDO2}

P_{TOTAL}= 807.8 milliWatts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7 "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application", (DS00792), for more information regarding this subject.

$T_{J(RISE)}$ = P_{TOTAL} x Rq_{JA}

T_{JRISE} = 807.8 milliWatts x 41.0° C/W

T_{JRISE} = 33.1°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

T_J = T_{JRISE} + $T_{A(MAX)}$

T_J = 83.1°C

Maximum Package Power Dissipation at 50°C Ambient Temperature

3x3DFN8 (41°C/Watt $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 50°C)/41° C/W

$P_{D(MAX)}$ = 1.83 Watts

MSOP8 (208°C/Watt $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 50°C)/208° C/W

$P_{D(MAX)}$ = 0.360 Watts

7.0 TYPICAL LAYOUT

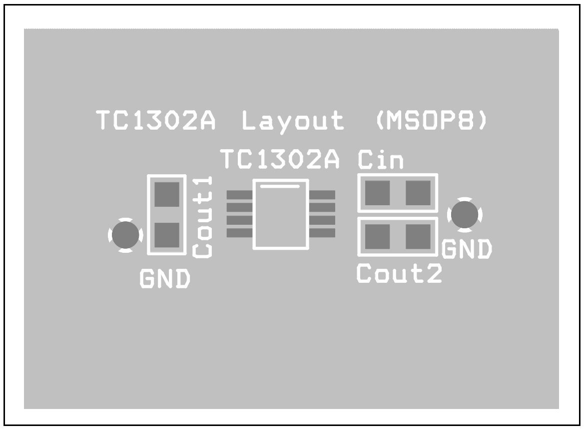


FIGURE 7-1: MSOP8 Silk-screen Layer.

When designing the physical layout for the TC1302A/B, the highest priority should be placed on positioning the input and output capacitors as close to the device pins as is practical. Figure 7-1 above represents a typical placement of the components when using the SMT0805 capacitors.

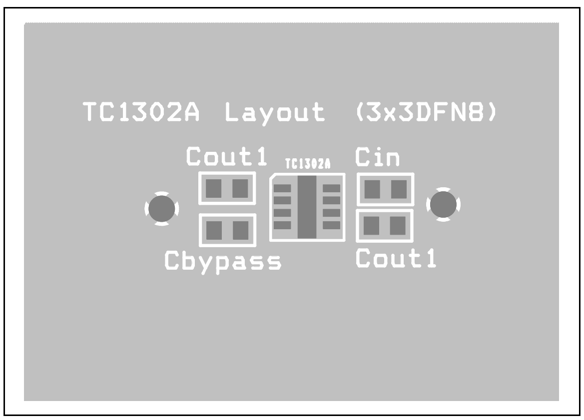


FIGURE 7-2: DFN3x3 Silk-screen Example.

Figure 7-2 above represents a typical placement of the components when using the SMT0603 capacitors.

8.0 ADDITIONAL OUTPUT VOLTAGES

8.1 Output Voltage Options

Table 8-1 describes the range of output voltage options available for the TC1302A/B. V_{OUT1} and V_{OUT2} can be factory preset from 1.5V to 3.3V in 100 mV increments.

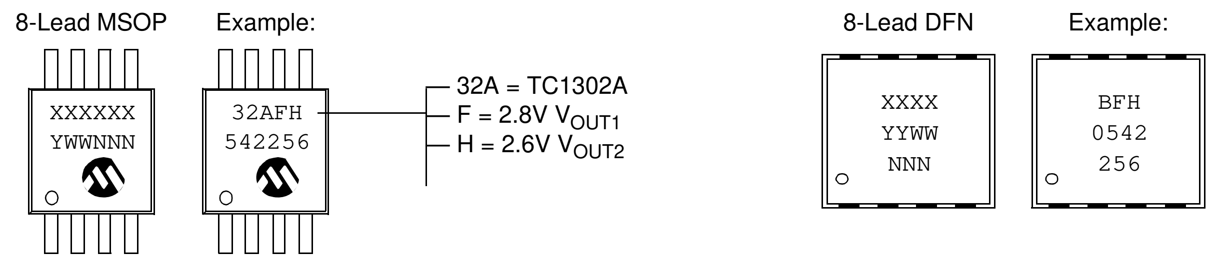
TABLE 8-1: CUSTOM OUTPUT VOLTAGES

V_{OUT1}	V_{OUT2}
1.5V to 3.3V	1.5V to 3.3V

For a listing of TC1302A/B standard parts, refer to the Product Identification System on page 23.

9.0 PACKAGING INFORMATION

9.1 Package Marking Information



X1 represents V_{OUT1} configuration:

Code	V_{OUT1}	Code	V_{OUT1}	Code	V_{OUT1}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

X2 represents V_{OUT2} configuration:

Code	V_{OUT2}	Code	V_{OUT1}	Code	V_{OUT2}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

For a listing of TC1302A/B standard parts, refer to the Product Identification System on page 23.

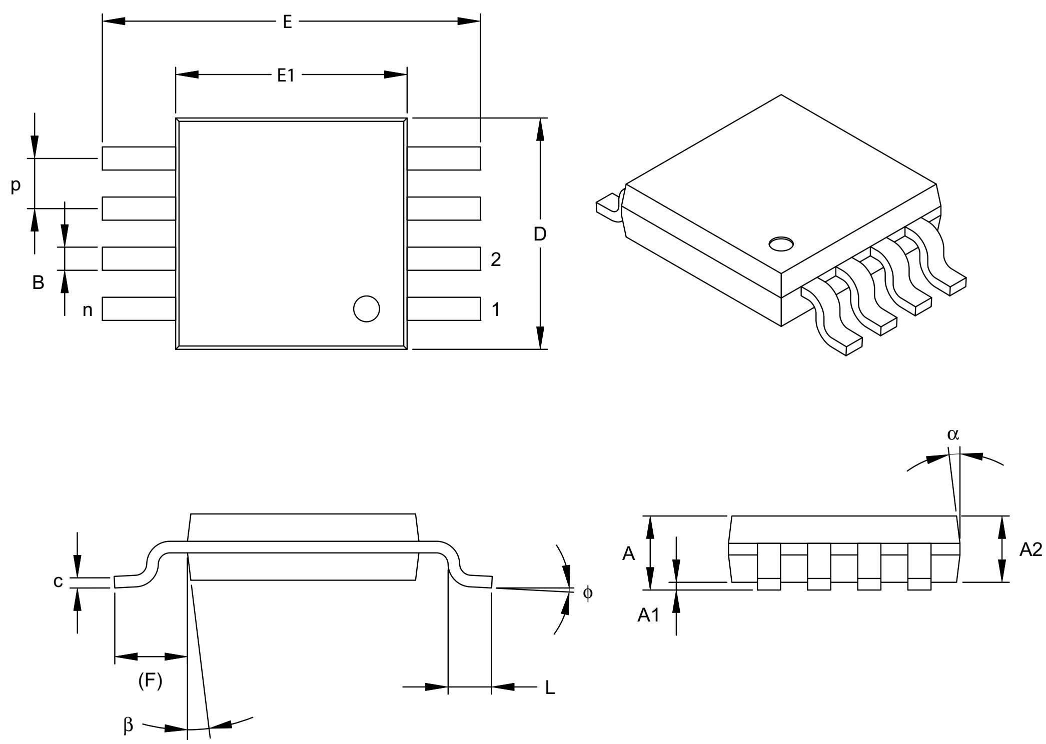
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

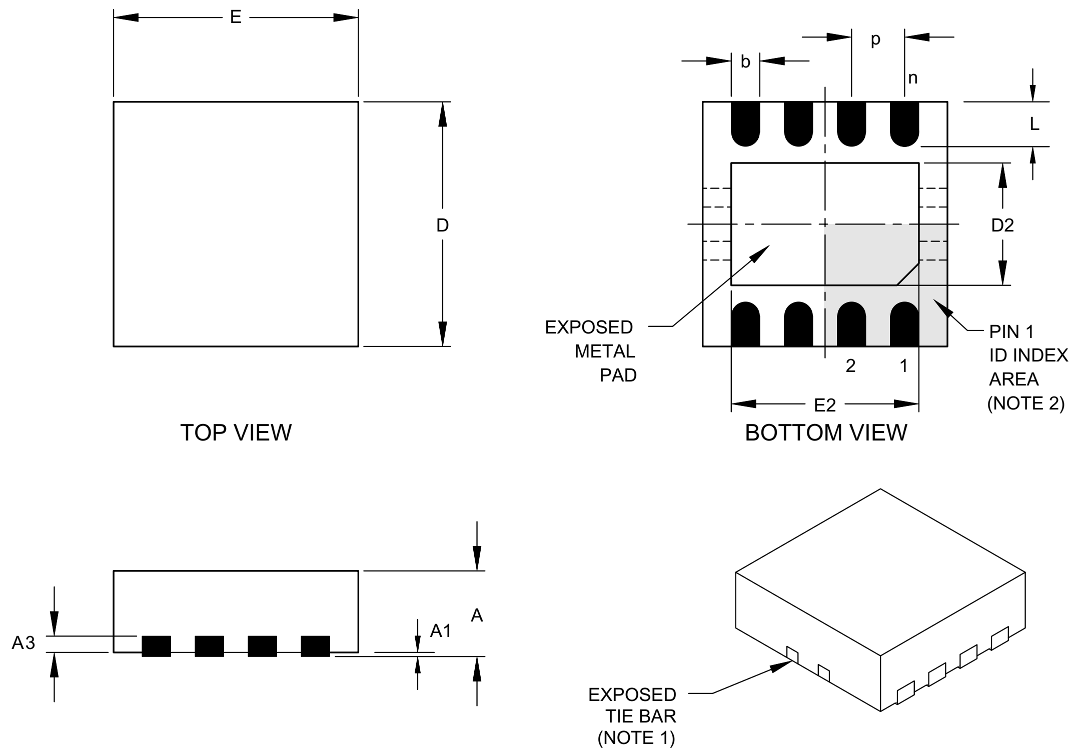
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

8-Lead Plastic Dual Flat No Lead Package (MF) 3x3x0.9 mm Body (DFN)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Lead Thickness	A3		.008 REF.			0.20 REF.	
Overall Length	E		.118 BSC			3.00 BSC	
Exposed Pad Length (Note 4)	E2	.055		.096	1.39		2.45
Overall Width	D		.118 BSC			3.00 BSC	
Exposed Pad Width (Note 4)	D2	.047		.069	1.20		1.75
Lead Width	b	.007	.010	.015	0.23	0.26	0.37
Lead Length	L	.012	.019	.022	0.30	0.48	0.55

*Controlling Parameter

Notes:

1. Package may have one or more exposed tie bars at ends.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.
3. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
4. Exposed pad dimensions vary with paddle size.
5. JEDEC equivalent: Pending

Drawing No. C04-062

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2003)

Original data sheet release.

Revision B (January 2005)

The following is the list of modifications:

1. Correct the incorrect part number options shown on the Product Identification System page and change the “standard” output voltage and reset voltage combinations.
2. Added Appendix A: Revision History.

Revision C (November 2012)

Added a note to each package outline drawing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	X	X	XX	XX
TC1302	Type A/B	V_{OUT1}	V_{OUT2}	Temp Range	Package	Tube or Tape & Reel

(V_{OUT1} and V_{OUT2}: Standard Configurations)

Device: TC1302A: Dual Output LDO with Single Shutdown input.
TC1302B: Dual Output LDO with Dual Shutdown Inputs.

Standard Configurations: *	V_{OUT1}/V_{OUT2}	Configuration Code
TC1302A	3.0/1.65	DT
TC1302B	3.0/1.65	DT
	2.6/1.8	HP
	2.5/1.8	IP

* Contact Factory for Alternate Output Voltage Configurations.

Temperature Range: V = -40°C to +125°C

Package: MF = Dual Flat, No Lead (3x3 mm body), 8-lead
UA = Plastic Micro Small Outline (MSOP), 8-lead

Tube or Tape and Reel: Blank = Tube
TR = Tape and Reel

Examples:

a) TC1302ADTVMF: 3.0, 1.65, 8LD DFN pkg.

a) TC1302BDTVMF: 3.0, 1.65, 8LD DFN pkg.

b) TC1302BHPVMFTR: 2.6, 1.8, 8LD DFN pkg, Tape and Reel.

c) TC1302BIPVUA: 2.5, 1.8, 8LD MSOP pkg.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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