Data Sheet November 12, 2010 FN7172.2

Sync Separator, 50% Slice, S-H, Filter

The EL4581 extracts timing information from standard negative going video sync found in NTSC, PAL and SECAM broadcast systems. It can also be used in non standard formats and with computer graphics systems at higher scan rates, by adjusting a single external resistor. When the input does not have correct serration pulses in the vertical interval, a default vertical output is produced.

Outputs are composite sync, vertical sync, burst/back porch output, and odd/even output. The later operates only in interlaced scan formats.

The EL4581 provides a reliable method of determining correct sync slide level by setting it to the mid-point between sync tip and blanking level at the back porch. This 50% level is determined by two internal self timing sample and hold circuits that track sync tip and back porch levels. This also provides a degree of hum and noise rejection to the input signal, and compensates for varying input levels of $0.5V_{P-P}$ to $2.0V_{P-P}$.

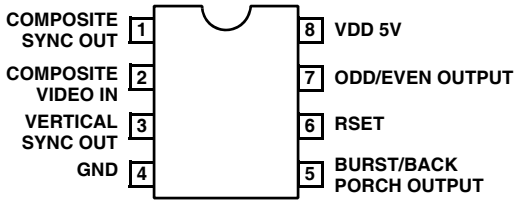
A built in linear phase, third order, low pass filter attenuates the chroma signal in color systems to prevent incorrectly set color burst from disturbing the 50% sync slide.

This device may be used to replace the industry standard LM1881, offering improved performance and reduced power consumption.

The EL4581 video sync separator is manufactured using Elantec's high performance analog CMOS process.

Pinout

EL4581
(8 LD SOIC, PDIP)
TOP VIEW



Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V
- Precision 50% slicing, internal caps
- Built-in color burst filter
- Decodes non-standard verticals
- Pin compatible with LM1881
- Low power
- Typically 1.5mA supply current
- Resistor programmable scan rate
- Few external components
- Available in 8 Ld PDIP and SOIC packages
- Pb-free available (RoHS compliant)

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE	PACKAGE	PKG. DWG. #
EL4581CN	EL4581CN	-40°C to +85°C	8 Ld PDIP	MDP0031
EL4581CS*	4581CS	-40°C to +85°C	8 Ld SOIC	MDP0027
EL4581CSZ* (Note)	4581CSZ	-40°C to +85°C	8 Ld SOIC (Pb-free)	MDP0027

*Add "-T7" or "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Demo Board

A dedicated demo board is not available. However, this device can be placed on the EL4584/5 Demo Board.

Absolute Maximum Ratings (T_A = +25°C)

V_{CC} Supply 7V
Storage Temperature . . . . . .-65°C to +150°C
Pin Voltages . . . . . -0.5V to V_{CC} +0.5V

Thermal Information

Maximum Power Dissipation. . . . . See Curves
Maximum Junction Temperature. . . . . +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Operating Temperature Range . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5V, T_A = +25°C, R_{SET} = 680kΩ.

PARAMETER	DESCRIPTION	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
I_{DD}	V_{DD} = 5V (Note 1)	+25	0.75	1.7	3	mA
Clamp Voltage	Pin 2, Unloaded	+25	1.3	1.5	1.9	V
Discharge Current	Pin 2 = 2V	+25	6	10	20	µA
Clamp Charge Current	Pin 2, V_{IN} = 1V	+25	2	3		mA
Ref Voltage	Pin 6, V_{DD} = 5V (Note 2)	+25	1.5	1.8	2.1	V
V_{OL} Output Low Voltage	I_{OL} = 1.6mA	+25			800	mV
V_{OH} Output High Voltage	I_{OH} = -40µA	+25	4			V
	I_{OH} = -1.6mA	+25	2.4			V

NOTES:
1. No video signal, outputs unloaded.
2. Tested for V_{DD} 5V ±5%.

Dynamic Specifications

V_{DD} = 5V, IV_{P-P} video, T_A = +25°C, C_L = 15pF, I_{OH} = -1.6mA, I_{OL} = 1.6mA. Signal voltages are peak to peak.

PARAMETER	DESCRIPTION	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Vertical Sync Width, t_{VS}	(Note 3)	+25	190	230	300	µs
Burst/Back Porch Width, t_B	(Note 3)	+25	2.5	3.5	4.5	µs
Vertical Sync Default Delay t_{VSD}		+25	40	55	70	µs
Filter Attenuation	F_{IN} = 3.4MHz (Note 4)	+25		24		dB
Composite Sync Prop Delay	V_{IN}- Composite Sync (Note 3)	+25		260	400	ns
Input Dynamic Range	Peak-to-Peak NTSC Signal (Note 5)	+25	0.5		2	V
Slice Level	Input Voltage = $1V_{P-P}$	+25	40	50	60	%
	(Note 6)	Full	40	50	60	%

NOTES:
3. C/S, Vertical and Burst outputs are all active low (V_{OH} = 2.4V, V_{OL} = 0.8V).
4. Attenuation is a function of R_{SET} (PIN 6).
5. Typical min is $0.3V_{P-P}$.
6. Refers to threshold level of sync tip to back porch amplitude.
7. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video in	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	GND	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	RSET (Note 8)	An external resistor to ground sets all internal timing. 681k, 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. Low during odd fields, high during even fields. Transitions occur at start of Vert Sync pulse.
8	VDD 5V	Positive supply. (5V)

NOTE:

8. R_{SET} must be a 1% resistor.

Typical Performance Curves

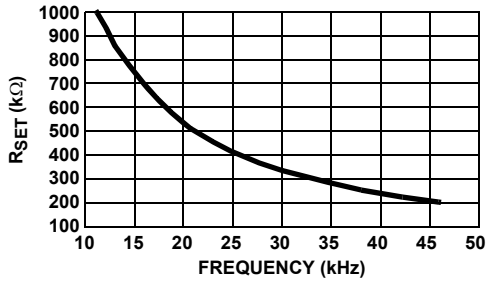


FIGURE 1. R_{SET} vs HORIZONTAL FREQUENCY

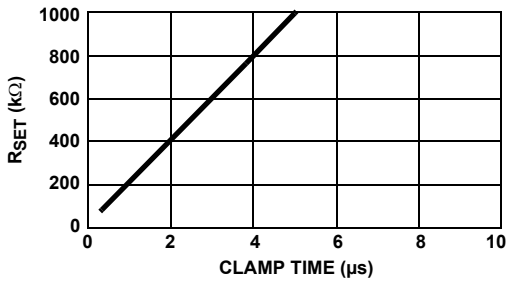


FIGURE 2. BACK PORCH CLAMP, ON-TIME vs R_{SET}

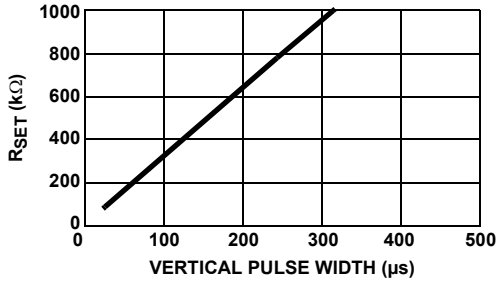


FIGURE 3. VERTICAL PULSE WIDTH vs R_{SET}

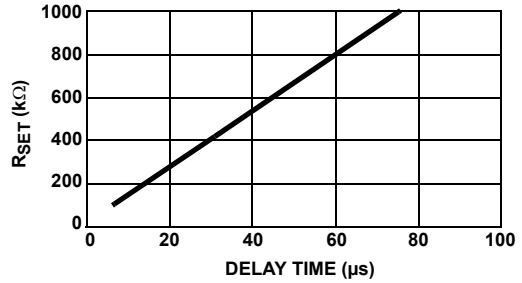


FIGURE 4. VERTICAL DEFAULT DELAY, TIME vs R_{SET}

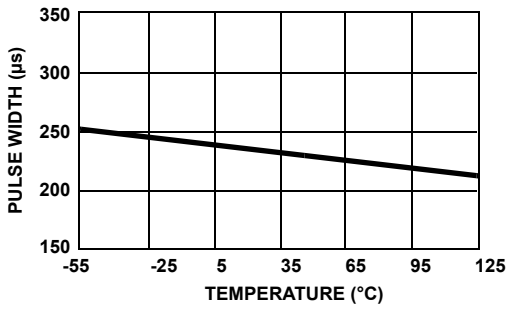


FIGURE 5. VERTICAL PULSE WIDTH vs TEMPERATURE

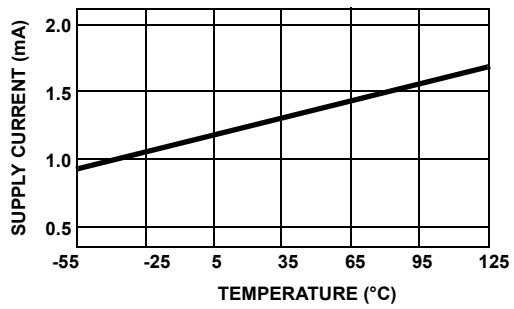


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves

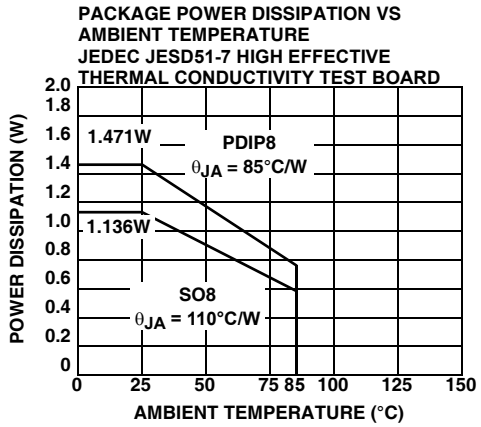


FIGURE 7. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

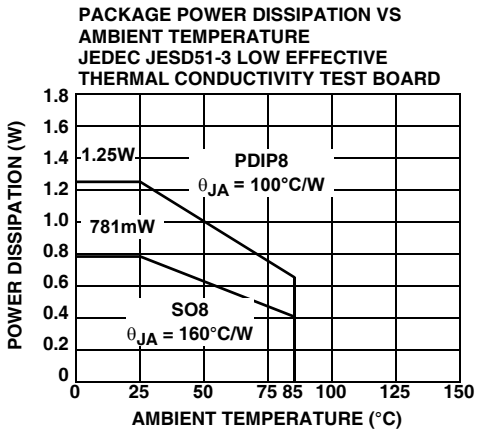


FIGURE 8. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

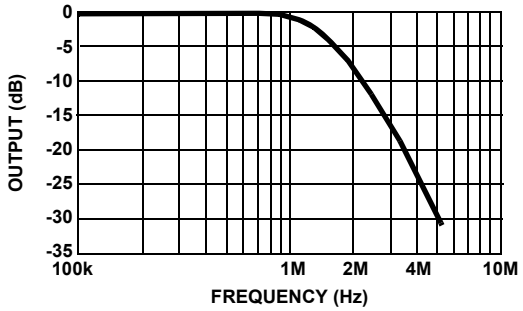
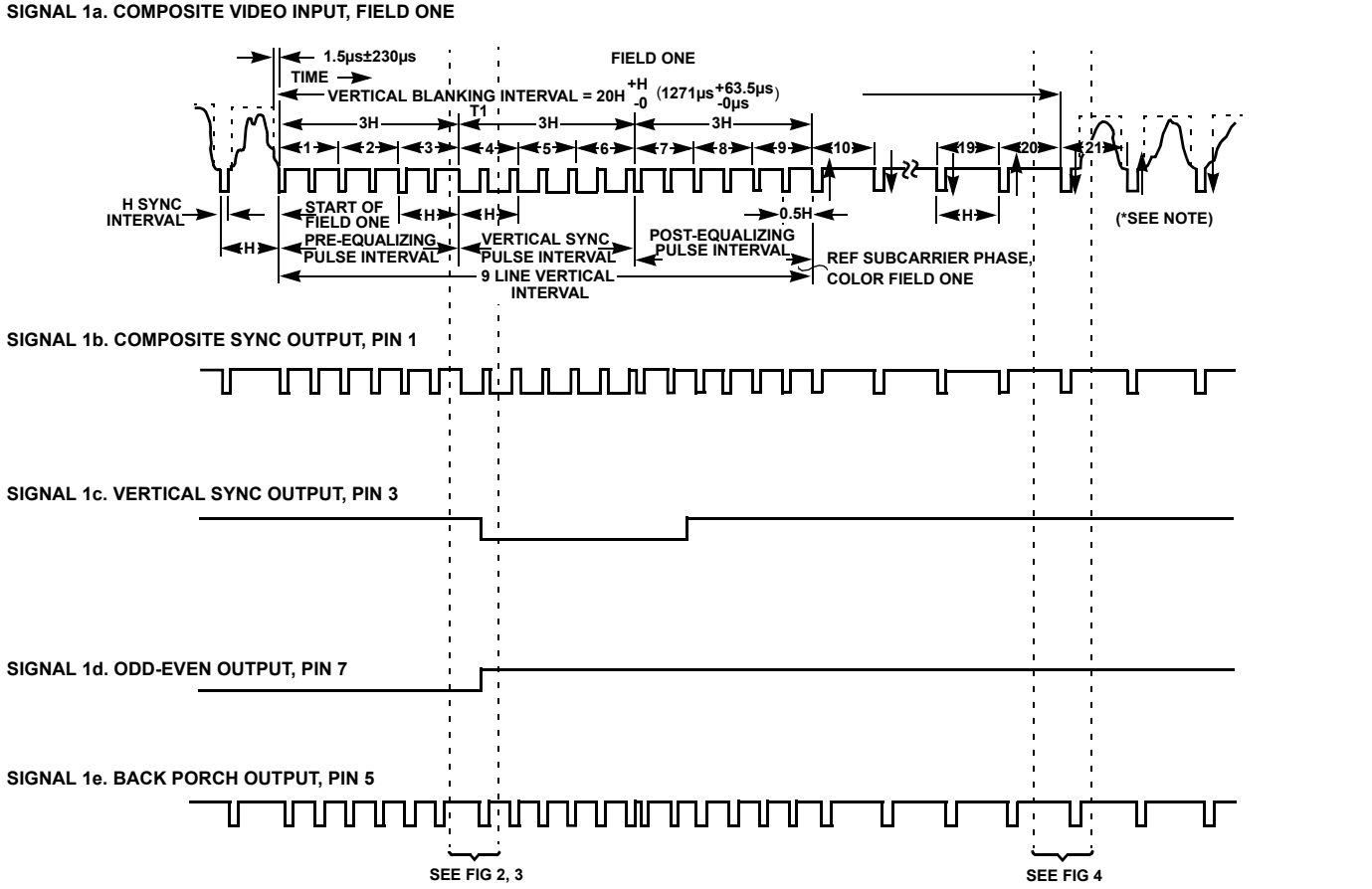


FIGURE 9. INPUT SIGNAL = 300mV$_{P-P}$, EL4581 FILTER CHARACTERISITIC CONSTANT DELAY 240ns

Timing Diagrams



NOTES:

9. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
10. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.
11. Odd-even output is low for even field, and high for odd field.
12. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

FIGURE 10.

Timing Diagrams (Continued)

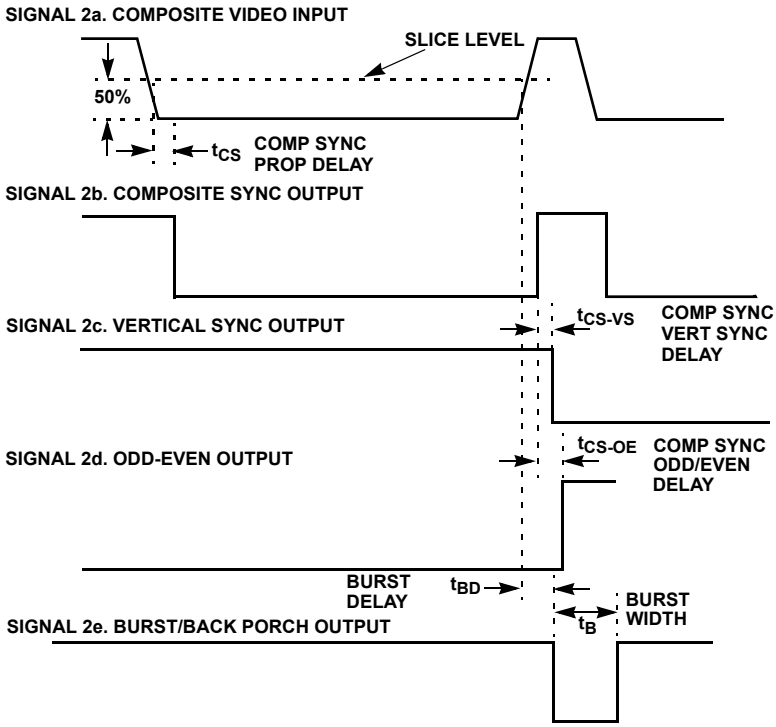


FIGURE 10.

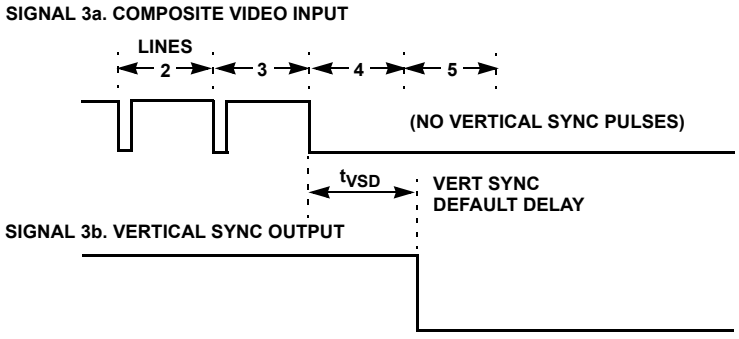


FIGURE 11.

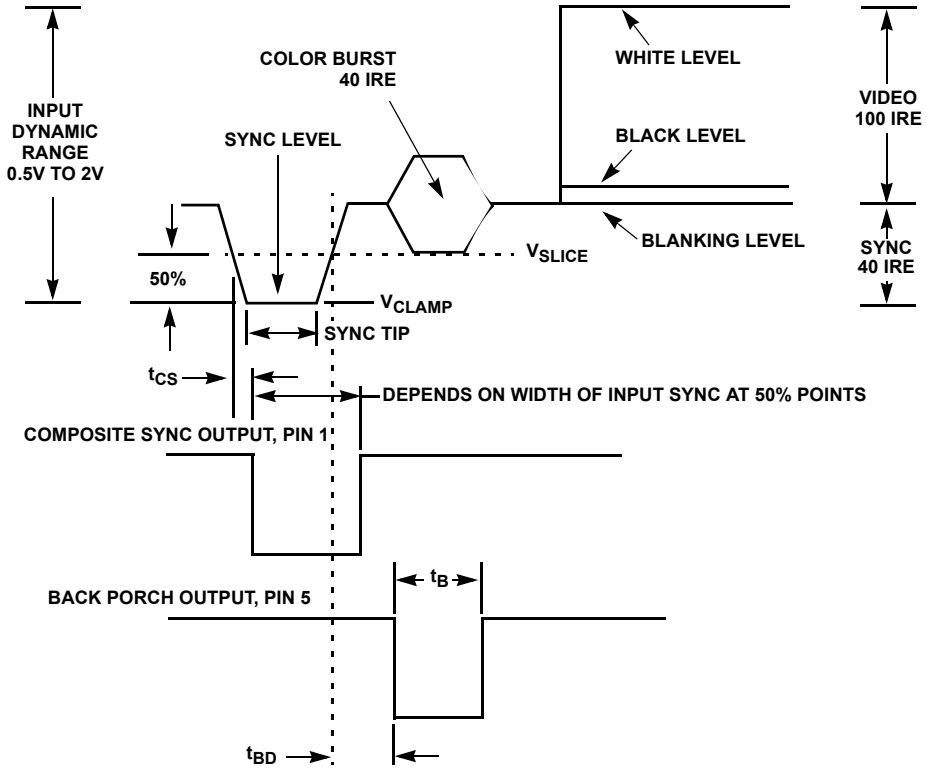


FIGURE 12. STANDARD (NTSC INPUT) H. SYNC DETAIL

Description of Operation

A simplified block diagram is shown in Figure 13. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 2 via the capacitor C_1, nominally 0.1µF. The clamp circuit A1 will prevent the input signal on pin 2 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10µA, charges the coupling capacitor during the remaining portion of the H line, approximately 58µs for a 15.75kHz timebase. From I•t = C•V, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_1 will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3-pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6dB to improve the detection accuracy. Note that the filter cut-off frequency is a function of R_{SET} through I_{OT} and is proportional to I_{OT}.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op amp A2 forces pin 6 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance R_{SET} will determine the value of the reference current I_{TR}. The internal resistance R_3 is only about 6kΩ, much less than R_{SET}. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync pulse with a threshold voltage V_{R2}, which is referenced at a

fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8µs to enable the actual sample of 2µs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divider R_1 and R_2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer vertical sync. pulse widths.

The internal timing circuits are referenced to I_{OT} and V_{R3}, the time-out period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by R_{SET}.

The odd/even circuit (O/E) comprises of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 7 is high during the odd field.

Loss of video signal can be detected by monitoring the C/S output. The 50% level of the previous video signal will remain held on the S/H capacitors after the input video signal has gone and the input on pin 2 has defaulted to the clamp voltage. Consequently, the C/S output will remain low longer than the normal vertical pulse period. An external timing circuit could be used to detect this condition.

Block Diagram

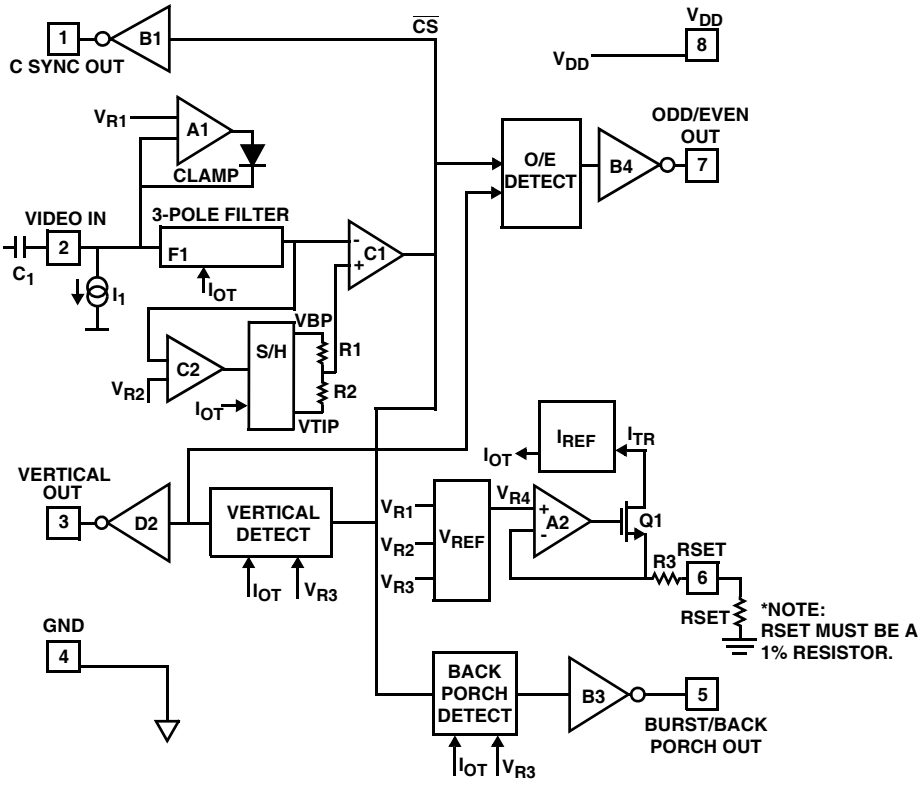
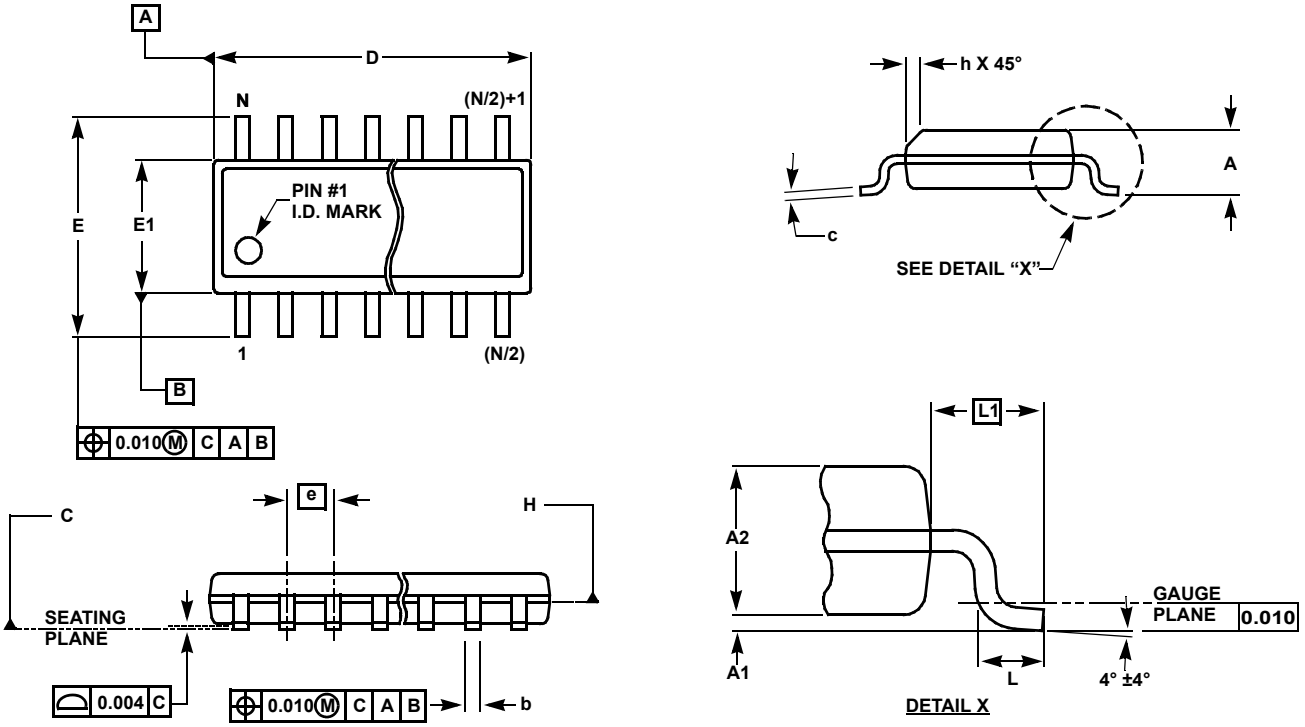


FIGURE 13. STANDARD (NTSC INPUT) H. SYNC DETAIL

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

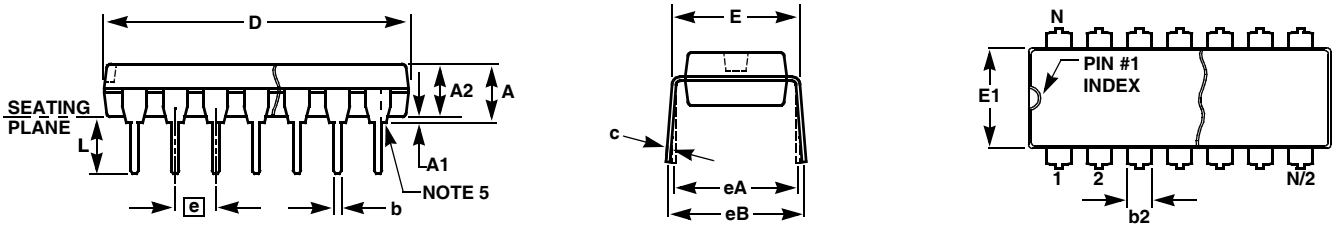
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.