User's Manual

8

78K0/Lx3-M

User's Manual: Hardware

8-Bit Single-Chip Microcontrollers

Renesas Electronics
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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers This manual is intended for user engineers who wish to understand the functions of the 78K0/Lx3-M microcontrollers and design and develop application systems and programs for these devices.
The target products are as follows.

- 78K0/LE3-M: μPD78F8052, 78F8053
- 78K0/LG3-M: μPD78F8054, 78F8055

Purpose This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization The manual for the 78K0/Lx3-M microcontrollers is separated into two parts: this manual and the instructions edition (common to the 78K0 microcontrollers).

78K0/Lx3-M User's Manual (This Manual)	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**.
  The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what: " field.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.
- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0/Lx3-M User's Manual	This manual
78K/0 Series Instructions User's Manual	U12326E
78K0 Microcontrollers Self Programming Library Type01 User's Manual	U18274E
78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual	U18275E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG to FP5 Flash Memory Programmer	U18865E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Products and Packages –	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (http://www2.renesas.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

CONTENTS

CHAPTER 1 OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.2 μs: @ 10 MHz operation with high-speed system clock) to ultra low-speed (122 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM (flash memory), RAM capacities

78K0/LE3-M	78K0/LG3-M	ROM[Note 2]	High-Speed RAM[Note 2]	Expansion RAM[Note 2]	LCD Display RAM
64 pins	100 pins				
–	μPD78F8055[Note 1]	60 KB	1 KB	1 KB	40 × 4 bits
–	μPD78F8054[Note 1]	48 KB	1 KB	1 KB	
μPD78F8053[Note 1]	–	32 KB	1 KB	–	24 × 4 bits
μPD78F8052[Note 1]	–	16 KB	768 B	–	

Notes 1. Under development

2. The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS). For IMS and IXS, see **30.1 Internal Memory Size Switching Register** and **30.2 Internal Expansion RAM Size Switching Register**.

- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function[Note]

Note The 78K0/Lx3-M microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with internal low-speed oscillation clock)
- On-chip LCD controller/driver (external resistance division and internal resistance division are switchable)

Part Number	Segment signals (SEG), Common signals (COM)			
	Static	1/2 bias	1/2, 1/3 bias	1/3 bias
78K0/LE3-M	SEG: 24 COM: 1	SEG: 24 COM: 2	SEG: 24 COM: 3	SEG: 24 COM: 4
78K0/LG3-M	SEG: 40 COM: 1	SEG: 40 COM: 2	SEG: 40 COM: 3	SEG: 40 COM: 4

- On-chip segment key scan function
- On-chip 10-bit successive approximation type A/D converter (AV_{REF} = 2.3 to 3.6 V)
- On-chip 24-bit ΔΣ-type A/D converter (AV_{DD} = 3.0 to 3.6 V)
- On-chip real-time counter
- On-chip remote controller transmitter
- On-chip power calculation circuit
- On-chip power quality measurement circuit
- On-chip digital frequency conversion circuit
- On-chip key interrupt function, buzzer output controller, I/O ports, timer, serial interface, and extended SFR interface
- Power supply voltage: V_{DD} = 1.8 to 3.6 V
- Operating ambient temperature: T_A = –40 to +85°C

Remark The functions mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

1.2 Applications

- Utility meters
  - Power meter

1.3 Ordering Information

- Flash memory version (Lead-free products)

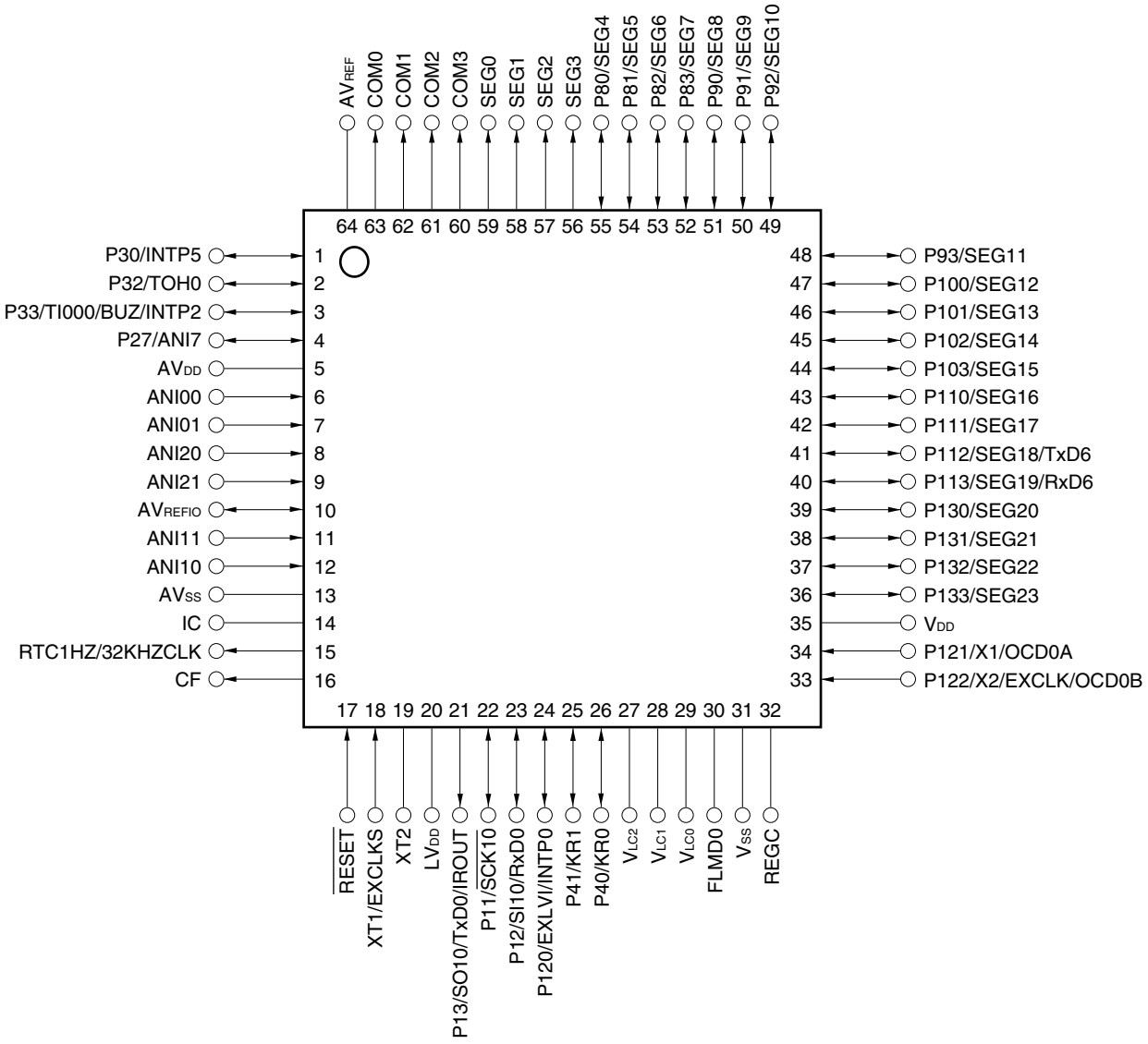
78K0/Lx3-M Microcontrollers	Package	Part Number
78K0/LE3-M	64-pin plastic LQFP (fine pitch) (10 x 10)	μPD78F8052GB-GAH-AX μPD78F8053GB-GAH-AX
78K0/LG3-M	100-pin plastic LQFP (fine pitch) (14 x 14)	μPD78F8054GC-UEU-AX μPD78F8055GC-UEU-AX

1.4 Pin Configuration (Top View)

1.4.1 78K0/LE3-M

(1) μPD78F8052, 78F8053

- 64-pin plastic LQFP (fine pitch) (10 × 10)



Cautions 1. Connect the AVSS to VSS.

2. Connect the REGC to VSS via a capacitor (0.47 to 1 μF: recommended).

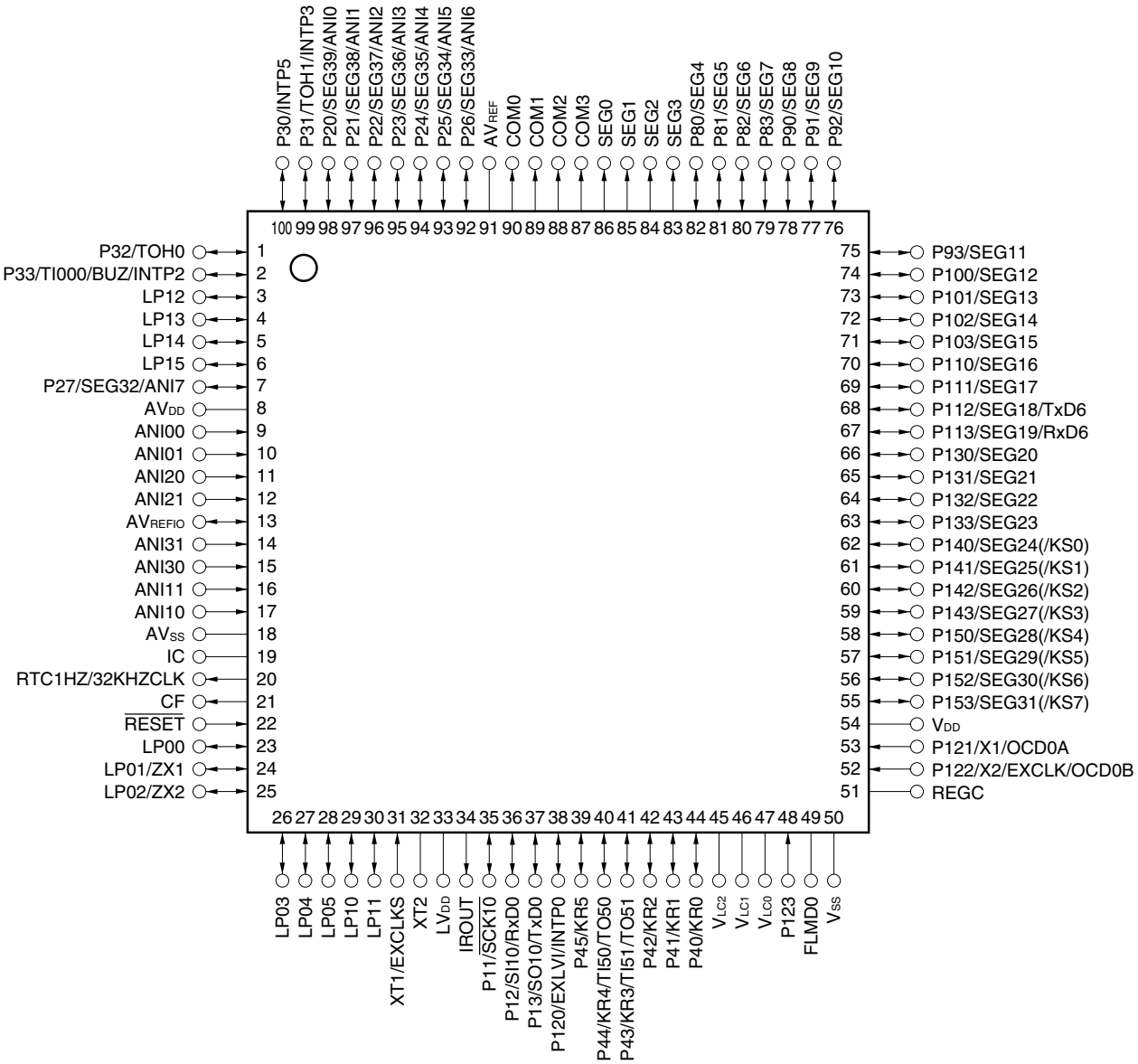
3. ANI7/P27 is set in the digital input mode after release of reset.

Remark For pin identification, see **1.5 Pin Identification**.

1.4.2 78K0/LG3-M

(1) μPD78F8054, 78F8055

- 100-pin plastic LQFP (fine pitch) (14 × 14)



Cautions 1. Connect the AVSS to VSS.

2. Connect the REGC to VSS via a capacitor (0.47 to 1 μF: recommended).

3. ANI7/P27 is set in the digital input mode after release of reset.

Remarks 1. The functions within parentheses can be used by setting the LCD mode register (LCDMD).

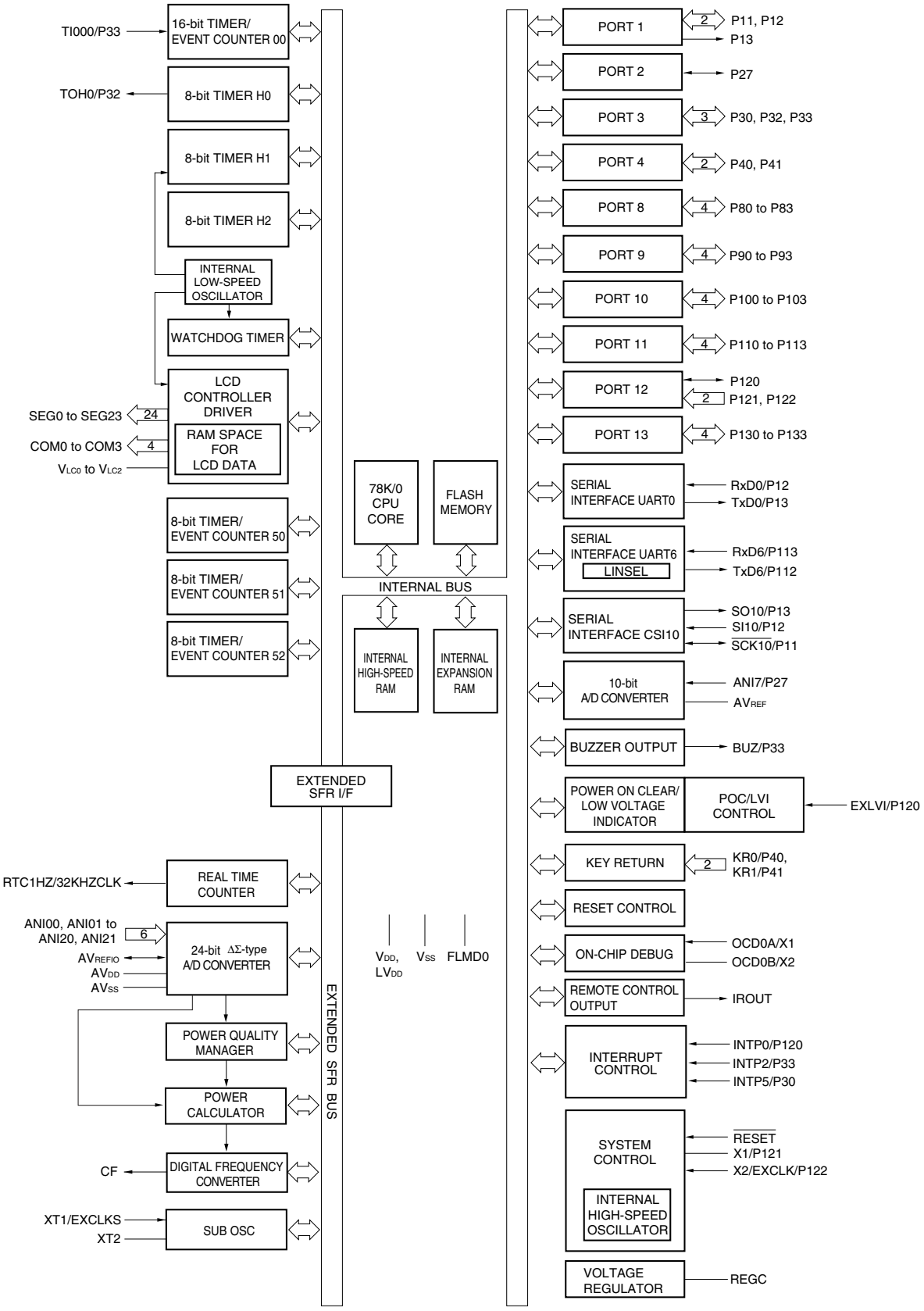
2. For pin identification, see **1.5 Pin Identification**.

1.5 Pin Identification

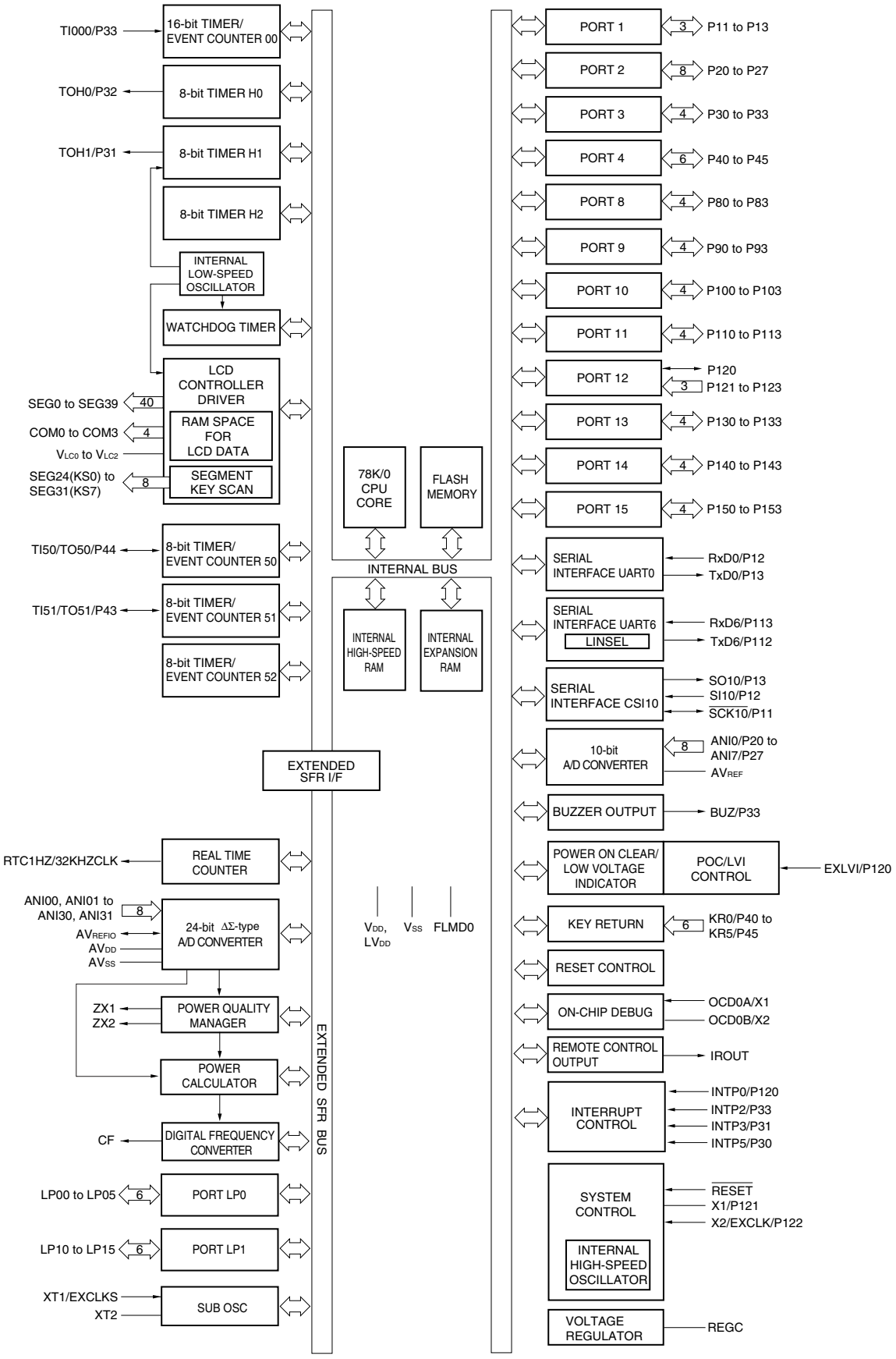
ANI0 to ANI7: Analog Input
ANI00, ANI01,
ANI10, ANI11,
ANI20, ANI21,
ANI30, ANI31: ΔΣ Analog Input
AV_{DD}: ΔΣ Analog Power Supply
AV_{REF}: Analog Reference Voltage
AV_{REFIO}: ΔΣ Analog Reference Voltage
AV_{SS}: ΔΣ Analog Ground
BUZ: Buzzer Output
CF: Calibration Frequency Output
COM0 to COM3: Common Output
EXCLK: External Clock Input
(Main System Clock)
EXCLKS: External Clock Input
(Subsystem Clock)
EXLVI: External potential Input
for Low-voltage Detector
FLMD0: Flash Programming Mode
IC: Internal Connection
INTP0, INTP2,
INTP3, INTP5: External Interrupt Input
IROUT: IR Output
KR0 to KR5: Key Return
LP00 to LP05: Port LP0
LP10 to LP15: Port LP1
LV_{DD}: Power Supply
OCD0A, OCD0B: On Chip Debug Input/Output
P11 to P13: Port 1
P20 to P27: Port 2
P30 to P33: Port 3
P40 to P45: Port 4
P80 to P83: Port 8
P90 to P93: Port 9
P100 to P103: Port 10
P110 to P113: Port 11
P120 to P123: Port 12
P130 to P133: Port 13
P140 to P143: Port 14
P150 to P153: Port 15
REGC: Regulator Capacitance
$\overline{\text{RESET}}$: Reset
RTC1HZ: Real-time Counter Correction Clock Output
RxD0, RxD6: Receive Data
SEG0 to SEG39: Segment Output
SEG24 (KS0)
to SEG31 (KS7): Segment Key Scan
$\overline{\text{SCK10}}$: Serial Clock Input/Output
SI10: Serial Data Input
SO10: Serial Data Output
TI000: Timer Input
TI50, TI51: Timer Input
TO50, TO51: Timer Output
TOH0, TOH1: Timer Output
TxD0, TxD6: Transmit Data
V_{DD}: Power Supply
V_{SS}: Ground
V_{LC0} to V_{LC2}: LCD Power Supply
X1, X2: Crystal Oscillator (Main System Clock)
XT1, XT2: Crystal Oscillator (Subsystem Clock)
ZX1, ZX2: Zero Cross Detection Signal Output
32KHZCLK: 32 kHz Clock Output

1.6 Block Diagram

1.6.1 78K0/LE3-M



1.6.2 78K0/LG3-M



1.7 Outline of Functions

Item \ 78K0/Lx3-M			78K0/LE3-M		78K0/LG3-M	
			μPD78F8052	μPD78F8053	μPD78F8054	μPD78F8055
			64 Pins		100 Pins	
Flash memory (KB)			16	32	48	60
High-speed RAM (KB)			0.75	1		
Expansion RAM (KB)			–		1	
LCD display RAM (bits)			24 × 4		40 × 4	
Memory space (KB)			64			
Power supply voltage			V_{DD} = 1.8 to 3.6 V			
Regulator			Provided			
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 3.6 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 3.6 V)			
Port (Total)			32		65	
Clock	Main	High-speed system	10 MHz: V_{DD} = 2.7 to 3.6 V/ 5 MHz: V_{DD} = 1.8 to 3.6 V			
		Internal high-speed oscillation	8 MHz (TYP.): V_{DD} = 1.8 to 3.6 V			
	Sub		32.768 kHz (TYP.): V_{DD} = 1.8 to 3.6 V			
	Internal low-speed oscillation		240 kHz (TYP.): V_{DD} = 1.8 to 3.6 V			
Timer	16 bits (TM0)		1 ch			
	8 bits (TM5)		3 ch			
	8 bits (TMH)		3 ch			
	Real-time counter (RTC)		1 ch			
	Watchdog (WDT)		1 ch			
Serial interface	3-wire CSI/UART[Note]		1 ch			
	UART supporting LIN-bus		1 ch			
LCD	Type		External resistance division and internal resistance division are switchable.			
	Segment signal		24		40	
	Common signal		4			
10-bit successive approximation type A/D			1 ch		8 ch	
24-bit ΔΣ-type A/D			3 ch		4 ch	
Interrupt	External		4		5	
	Internal		17			
Segment key source signal output			–		8 ch	
Key interrupt			2 ch		6 ch	
Reset	$\overline{\text{RESET}}$ pin		Provided			
	POC		1.59 V ±0.15 V			
	LVI		The detection level of the supply voltage is selectable in 10 steps.			
	WDT		Provided			
Buzzer output			Provided			
Remote controller transmitter			Provided			
Power calculation circuit			Provided			
Power quality measurement circuit			Provided			
Digital frequency conversion circuit			Provided			
On-chip debug function			Provided			
Operating ambient temperature			T_A = −40 to +85°C			
Package			64-pin plastic LQFP (fine pitch) (10 x 10)		100-pin plastic LQFP (fine pitch) (14 x 14)	

Note Select either of the functions of these alternate-function pins.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are five types of pin I/O buffer power supplies: AV_{DD}, AV_{REF}, LV_{DD}, V_{LC0}, and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{DD}	ANI00 to ANI31
AV_{REF}	P20 to P27
LV_{DD}	CF, EXCLKS, LP00 to LP05, LP10 to LP15, RTC1HZ, XT1, XT2, ZX1, ZX2, 32KHZCLK, IROUT, IC, $\overline{\text{RESET}}$
V_{LC0}	COM0 to COM3, SEG0 to SEG39, V_{LC0} to V_{LC2}
V_{DD}	Pins other than above

2.1.1 78K0/LE3-M

(1) Port functions : 78K0/LE3-M

Function Name	I/O	Function	After Reset	Alternate Function
P11	I/O	Port 1. 2-bit I/O port and 1-bit output port. Only P11 and P12, input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$
P12				SI10/RxD0
P13	Output		Output port	SO10/TxD0/IROUT
P27	I/O	Port 2. 1-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI7
P30	I/O	Port 3. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP5
P32				TOH0
P33				TI000/BUZ/INTP2
P40	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P41				KR1
P80 to P83	I/O	Port 8. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4 to SEG7
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG8 to SEG11
P100 to P103	I/O	Port 10. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG12 to SEG15
P110, P111	I/O	Port 11. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG16, SEG17
P112				SEG18/TxD6
P113				SEG19/RxD6
P120	I/O	Port 12. 1-bit I/O port and 2-bit Input port. Only P120, input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P130 to P133	I/O	Port 13. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG20 to SEG23

(2) Non-port functions (1/2): 78K0/LE3-M

Function Name	I/O	Function	After Reset	Alternate Function
ANI7	Input	10-bit successive approximation type A/D converter analog input.	Digital input port	P27
ANI00	Input	24-bit ΔΣ-type A/D converter analog input. ANIx0 is a negative input pin, and ANIx1 is a positive input pin. Note that the channel (voltage or current) that corresponds to each input pin varies according to whether the two-wire mode or three-wire mode is in use (See **CHAPTER 13 24-BIT ΔΣ-TYPE A/D CONVERTER**).	Input	–
ANI01				–
ANI10				–
ANI11				–
ANI20				–
ANI21				–
AV_{DD}	–	Positive power supply for 24-bit ΔΣ-type A/D converter	–	–
AV_{REF}	Input	10-bit successive approximation type A/D converter reference voltage input and positive power supply, positive power supply for port 2	–	–
AV_{REFIO}	I/O	24-bit ΔΣ-type A/D converter reference voltage	I/O	–
AV_{SS}	–	24-bit ΔΣ-type A/D converter ground potential. Make the same potential as V_{SS}.	–	–
BUZ	Output	Buzzer output	Input port	P33/TI000/INTP2
CF	Output	Calibration frequency output	Output	–
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B
EXCLKS	Input	External clock input for subsystem clock	Input port	XT1
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
FLMD0	–	Flash memory programming mode setting	–	–
IC	–	Internal connection pin. Connect to V_{SS}.	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP2				P33/TI000/BUZ
INTP5				P30
IROUT	Output	IR output	Output port	P13/SO10/TxD0
KR0	Input	Key interrupt input or segment key scan input	Input port	P40
KR1				P41
LV_{DD}	–	Real-time counter, power calculation circuit, subsystem clock oscillator, and positive power supply for port LP	–	–
OCD0A	Input	On-chip debug mode setting connection	Input port	P121/X1
OCD0B	–			P122/X2/EXCLK
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: recommended).	–	–
$\overline{RESET}$	Input	System reset input	–	–
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Output	32KHZCLK
RxD0	Input	Serial data input to UART0	Input port	P12/SI10
RxD6	Input	Serial data input to UART6	Input port	P113/SEG19

(2) Non-port functions (2/2): 78K0/LE3-M

Function Name	I/O	Function	After Reset	Alternate Function
$\overline{SCK10}$	I/O	Clock input/output for CSI10	Input port	P11
SEG0 to SEG3	Output	LCD controller/driver segment signal outputs	Output	–
SEG4 to SEG7			Input port	P80 to P83
SEG8 to SEG11				P90 to P93
SEG12 to SEG15				P100 to P103
SEG16, SEG17				P110, P111
SEG18				P112/TxD6
SEG19				P113/RxD6
SEG20 to SEG23				P130 to P133
SI10	Input	Serial data Input to CSI10	Input port	P12/RxD0
SO10	Output	Serial data output from CSI10	Output port	P13/TxD0/IROUT
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR010) of 16-bit timer/event counter 00	Input port	P33/BUZ/INTP2
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P44/TO50/KR4
TI51		External count clock input to 8-bit timer/event counter 51		P43/TO51/KR3
TOH0	Output	8-bit timer H0 output	Input port	P32
TxD0	Output	Serial data output from UART0	Output port	P13/SO10/IROUT
TxD6	Output	Serial data output from UART6	Input port	P112/SEG18
V_{DD}	–	Positive power supply	–	–
V_{LC0} to V_{LC2}	–	Voltage for driving the LCD	–	–
V_{SS}	–	Ground potential	–	–
X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A
X2	–			P122/EXCLK/OCD0B
XT1	–	Connecting resonator for subsystem clock	–	EXCLKS
XT2	–			–
32KHZCLK	Output	Real-time counter clock (32 kHz) output	Output	RTC1HZ

2.1.2 78K0/LG3-M

(1) Port functions (1/2): 78K0/LG3-M

Function Name	I/O	Function	After Reset	Alternate Function
P11	I/O	Port 1. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$
P12				SI10/RxD0
P13				SO10/TxD0
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG39/ANI0
P21				SEG38/ANI1
P22				SEG37/ANI2
P23				SEG36/ANI3
P24				SEG35/ANI4
P25				SEG34/ANI5
P26				SEG33/ANI6
P27				SEG32/ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP5
P31				TOH1/ INTP3
P32				TOH0
P33				TI000/BUZ/INTP2
P40	I/O	Port 4. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P41				KR1
P42				KR2
P43				TO51/TI51/KR3
P44				TO50/TI50/KR4
P45				KR5
P80 to P83	I/O	Port 8. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4 to SEG7
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG8 to SEG11
P100 to P103	I/O	Port 10. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG12 to SEG15
P110, P111	I/O	Port 11. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG16, SEG17
P112				SEG18/TxD6
P113				SEG19/RxD6

(1) Port functions (2/2): 78K0/LG3-M

Function Name	I/O	Function	After Reset	Alternate Function
P120	I/O	Port 12. 1-bit I/O port and 3-bit input port. Only for P120, input/output can be specified in 1-bit units and use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P123				–
P130 to P133	I/O	Port 13. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG20 to SEG23
P140	I/O	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG24 (KS0)
P141				SEG25 (KS1)
P142				SEG26 (KS2)
P143				SEG27 (KS3)
P150	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG28 (KS4)
P151				SEG29 (KS5)
P152				SEG30 (KS6)
P153				SEG31 (KS7)
LP00	I/O	Port LP0. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
LP01				ZX1
LP02				ZX2
LP03				–
LP04				–
LP05				–
LP10	I/O	Port LP1. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
LP11				–
LP12				–
LP13				–
LP14				–
LP15				–

(2) Non-port functions (1/3): 78K0/LG3-M

Function Name	I/O	Function	After Reset	Alternate Function
ANI0	Input	10-bit successive approximation type A/D converter analog input.	Digital input port	P20/SEG39
ANI1				P21/SEG38
ANI2				P22/SEG37
ANI3				P23/SEG36
ANI4				P24/SEG35
ANI5				P25/SEG34
ANI6				P26/SEG33
ANI7				P27/SEG32
ANI00	Input	24-bit ΔΣ-type A/D converter analog input. ANIx0 is a negative input pin, and ANIx1 is a positive input pin. Note that the channel (voltage or current) that corresponds to each input pin varies according to whether the two-wire mode or three-wire mode is in use (See **CHAPTER 13 24-BIT ΔΣ-TYPE A/D CONVERTER**).	Input	–
ANI01				–
ANI10				–
ANI11				–
ANI20				–
ANI21				–
ANI30				–
ANI31				–
AV_{DD}	–	Positive power supply for 24-bit ΔΣ-type A/D converter	–	–
AV_{REF}	Input	10-bit successive approximation type A/D converter reference voltage input and positive power supply, positive power supply for port 2	–	–
AV_{REFIO}	I/O	24-bit ΔΣ-type A/D converter reference voltage	I/O	–
AV_{SS}	–	24-bit ΔΣ-type A/D converter ground potential. Make the same potential as V_{SS}.	–	–
BUZ	Output	Buzzer output	Input port	P33/TI000/INTP2
CF	Output	Calibration frequency output	Output	–
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B
EXCLKS	Input	External clock input for subsystem clock	Input port	XT1
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
FLMD0	–	Flash memory programming mode setting	–	–
IC	–	Internal connection pin. Connect to V_{SS}.	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP2				P33/TI000/BUZ
INTP3				P30/TOH1
INTP5				P30
IROUT	Output	IR output	Input port	–
KR0	Input	Key interrupt input or segment key scan input	Input port	P40
KR1				P41
KR2				P42
KR3				P43/TO51/TI51
KR4				P44/TO50/TI50
KR5				P45

(2) Non-port functions (2/3): 78K0/LG3-M

Function Name	I/O	Function	After Reset	Alternate Function
LV_{DD}	–	Real-time counter, power calculation circuit, subsystem clock oscillator, and positive power supply for port LP	–	–
OCD0A	Input	On-chip debug mode setting connection	Input port	P121/X1
OCD0B	–			P122/X2/EXCLK
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: recommended).	–	–
$\overline{RESET}$	Input	System reset input	–	–
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Output	32KHZCLK
RxD0	Input	Serial data input to UART0	Input port	P12/SI10
RxD6	Input	Serial data input to UART6	Input port	P113/SEG19
$\overline{SCK10}$	I/O	Clock input/output for CSI10	Input port	P11
SEG0 to SEG3	Output	LCD controller/driver segment signal outputs	Output	–
SEG4 to SEG7			Input port	P80 to P83
SEG8 to SEG11				P90 to P93
SEG12 to SEG15				P100 to P103
SEG16, SEG17				P110, P111
SEG18				P112/TxD6
SEG19				P113/RxD6
SEG20 to SEG23				P130 to P133
SEG24 (KS0)		LCD controller/driver segment signal outputs. Segment key source signal can be simultaneously output.		P140
SEG25 (KS1)				P141
SEG26 (KS2)				P142
SEG27 (KS3)				P143
SEG28 (KS4)				P150
SEG29 (KS5)				P151
SEG30 (KS6)				P152
SEG31 (KS7)				P153
SEG32		LCD controller/driver segment signal outputs	Digital input port	P27/ANI7
SEG33				P26/ANI6
SEG34				P25/ANI5
SEG35				P24/ANI4
SEG36				P23/ANI3
SEG37				P22/ANI2
SEG38				P21/ANI1
SEG39				P20/ANI0
SI10	Input	Serial data Input to CSI10	Input port	P12/RxD0
SO10	Output	Serial data output from CSI10	Input port	P13/TxD0

(2) Non-port functions (3/3): 78K0/LG3-M

Function Name	I/O	Function	After Reset	Alternate Function
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR010) of 16-bit timer/event counter 00	Input port	P33/BUZ/INTP2
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P44/TO50/KR4
TI51		External count clock input to 8-bit timer/event counter 51		P43/TO51/KR3
TO50	Output	8-bit timer/event counter 50 output	Input port	P44/TI50/KR4
TO51		8-bit timer/event counter 51 output		P43/TI51/KR3
TOH0	Output	8-bit timer H0 output	Input port	P32
TOH1		8-bit timer H1 output		P31/INTP3
TxD0	Output	Serial data output from UART0	Input port	P13/SO10
TxD6	Output	Serial data output from UART6	Input port	P112/SEG18
V_{DD}	–	Positive power supply	–	–
V_{LC0} to V_{LC2}	–	Voltage for driving the LCD	–	–
V_{SS}	–	Ground potential	–	–
X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A
X2	–			P122/EXCLK/OCD0B
XT1	–	Connecting resonator for subsystem clock	–	EXCLKS
XT2	–			–
ZX1	Output	Zero-crossing detection signal output	Output port	LP01
ZX2				LP02
32KHZCLK	Output	Real-time counter clock (32 kHz) output	Output	RTC1HZ

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P11 to P13 (port 1)

P11 to P13 function as an I/O port. These pins also function as pins for serial interface data I/O, clock I/O, and IR output. P13 can be selected to function as pins, using port function register 1 (PF1) (see Figure 4-32).

78K0/LE3-M	78K0/LG3-M
P11/$\overline{\text{SCK10}}$	P11/$\overline{\text{SCK10}}$
P12/SI10/RxD0	P12/SI10/RxD0
P13/SO10/TxD0/IROUT	P13/SO10/TxD0

The following operation modes can be specified in 1-bit units.

(1) Port mode

P11 to P13 function as an I/O port[Note]. P11 to P13 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

Note In the 78K0/LE3-M, P13 is output port function only.

(2) Control mode

P11 to P13 function as serial interface data I/O and clock I/O, IR output.

(a) RxD0

This is the serial data input pin of serial interface UART0.

(b) TxD0

This is the serial data output pin of serial interface UART0.

(c) SI10

This is the serial data input pin of serial interface CSI10.

(d) SO10

This is the serial data output pin of serial interface CSI10.

(e) $\overline{\text{SCK10}}$

This is the serial clock I/O pin of serial interface CSI10.

(f) IROUT

This is the data output pin for IR.

2.2.2 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for segment signal output pins for the LCD controller/driver and 10-bit successive approximation type A/D converter analog input. Either I/O port function or segment signal output function can be selected using port function register 2 (PF2)[Note].

78K0/LE3-M	78K0/LG3-M
–	P20/SEG39/ANI0
–	P21/SEG38/ANI1
–	P22/SEG37/ANI2
–	P23/SEG36/ANI3
–	P24/SEG35/ANI4
–	P25/SEG34/ANI5
–	P26/SEG33/ANI6
P27/ANI7	P27/SEG32/ANI7

Note 78K0/LG3-M only.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as segment signal output for the LCD controller/driver and 10-bit successive approximation type A/D converter analog input.

(a) SEG32 to SEG39

These pins are the segment signal output pins for the LCD controller/driver.

(b) ANI0 to ANI7

These are 10-bit successive approximation type A/D converter analog input pins. When using these pins as analog input pins, see **(5)** in **12.6 Cautions for 10-bit successive approximation type A/D Converter**.

Caution P20 to P27 are set in the analog input mode after release of reset.

2.2.3 P30 to P33 (port 3)

P30 to P33 function as an I/O port. These pins also function as pins for external interrupt request input, timer I/O, and buzzer output.

78K0/LE3-M	78K0/LG3-M
P30/INTP5	P30/INTP5
–	P31/TOH1/INTP3
P32/TOH0	P32/TOH0
P33/TI000/BUZ/INTP2	P33/TI000/BUZ/INTP2

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as an I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input, timer I/O, and buzzer output.

(a) INTP2, INTP3, and INTP5

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TOH0, TOH1

These are 8-bit timer H0, H1 timer output pin.

(c) TI000

This is a pin for inputting an external count clock to 16-bit timer/event counters 00 and is also for inputting a capture trigger signal to the capture registers (CR000 or CR010) of 16-bit timer/event counters 00.

(d) BUZ

This is a buzzer output pin.

2.2.4 P40 to P45 (port 4)

P40 to P45 function as an I/O port. These pins also function as pins for key interrupt input, segment key scan input, and timer I/O.

78K0/LE3-M	78K0/LG3-M
P40/KR0	P40/KR0
P41/KR1	P41/KR1
–	P42/KR2
–	P43/TO51/TI51/KR3
–	P44/TO50/TI50/KR4
–	P45/KR5

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P45 function as an I/O port. P40 and P45 can be set to input port or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

(2) Control mode

P40 and P45 function as key interrupt input, segment key scan input, and timer I/O.

(a) KR0 to KR5

These are the key interrupt input or segment key scan input pins.

(b) TO50, TO51

These are the timer output pin from 8-bit timer/event counter 50 and 51.

(c) TI50, TI51

These are the pins for inputting an external count clock to 8-bit timer/event counter 50 and 51.

2.2.5 P80 to P83 (port 8)

P80 to P83 function as an I/O port. These pins also function as segment signal output pins for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
P80/SEG4	P80/SEG4
P81/SEG5	P81/SEG5
P82/SEG6	P82/SEG6
P83/SEG7	P83/SEG7

The following operation modes can be specified in 1-bit units.

(1) Port mode

P80 to P83 function as an I/O port. P80 to P83 can be set to input or output port in 1-bit units using port mode register 8 (PM8). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 8 (PU8).

(2) Control mode

P80 to P83 function as segment signal output for the LCD controller/driver.

(a) SEG4 to SEG7

These pins are the segment signal output pins for the LCD controller/driver.

2.2.6 P90 to P93 (port 9)

P90 to P93 function as an I/O port. These pins also function as segment signal output pins for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
P90/SEG8	P90/SEG8
P91/SEG9	P91/SEG9
P92/SEG10	P92/SEG10
P93/SEG11	P93/SEG11

The following operation modes can be specified in 1-bit units.

(1) Port mode

P90 to P93 function as an I/O port. P90 to P93 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

(2) Control mode

P90 to P93 function as segment signal output for the LCD controller/driver.

(a) SEG8 to SEG11

These pins are the segment signal output pins for the LCD controller/driver.

2.2.7 P100 to P103 (port 10)

P100 to P103 function as an I/O port. These pins also function as segment signal output pins for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
P100/SEG12	P100/SEG12
P101/SEG13	P101/SEG13
P102/SEG14	P102/SEG14
P103/SEG15	P103/SEG15

The following operation modes can be specified in 1-bit units.

(1) Port mode

P100 to P103 function as an I/O port. P100 to P103 can be set to input or output port in 1-bit units using port mode register 10 (PM10). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 10 (PU10).

(2) Control mode

P100 to P103 function as segment signal output for the LCD controller/driver.

(a) SEG12 to SEG15

These pins are the segment signal output pins for the LCD controller/driver.

2.2.8 P110 to P113 (port 11)

P110 to P113 function as an I/O port. These pins also function as pins for segment signal output for the LCD controller/driver and serial interface data I/O. Either I/O port function (other than segment signal output) or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
P110/SEG16	P110/SEG16
P111/SEG17	P111/SEG17
P112/SEG18/TxD6	P112/SEG18/TxD6
P113/SEG19/RxD6	P113/SEG19/RxD6

The following operation modes can be specified in 1-bit units.

(1) Port mode

P110 to P113 function as an I/O port. P110 to P113 can be set to input or output port in 1-bit units using port mode register 11 (PM11). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 11 (PU11).

(2) Control mode

P110 to P113 function as segment signal output for the LCD controller/driver and serial interface data I/O.

(a) SEG16 to SEG19

These pins are the segment signal output pins for the LCD controller/driver.

(b) RxD6

This is a serial data input pin of serial interface UART6.

(c) TxD6

This is a serial data output pin of serial interface UART6.

2.2.9 P120 to P123 (port 12)

P120 functions as an I/O port. P121 to P123 function as an input port. These pins also function as pins for external interrupt request input, potential input for external low-voltage detection, resonator for main system clock connection, and external clock input for main system clock.

78K0/LE3-M	78K0/LG3-M
P120/INTP0/EXLVI	P120/INTP0/EXLVI
P121/X1/OCD0A	P121/X1/OCD0A
P122/X2/EXCLK/OCD0B	P122/X2/EXCLK/OCD0B
–	P123

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as an I/O port. P120 can be set to input or output port using port mode register 12 (PM12). P120 use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P123 function as an input port

(2) Control mode

P120 to P123 function as an external interrupt request input, potential input for external low-voltage detection, resonator for main system clock connection, and external clock input for main system clock.

(a) INTP0

This functions as an external interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

Remark X1 and X2 can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION.**

2.2.10 P130 to P133 (port 13)

P130 to P133 function as an I/O port. These pins also function as pins for segment signal output pins for the LCD controller/driver and serial interface data I/O. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
P130/SEG20	P130/SEG20
P131/SEG21	P131/SEG21
P132/SEG22	P132/SEG22
P133/SEG23	P133/SEG23

The following operation modes can be specified in 1-bit units.

(1) Port mode

P130 to P133 function as an I/O port. P130 to P133 can be set to input or output port in 1-bit units using port mode register 13 (PM13). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 13 (PU13).

(2) Control mode

P130 to P133 function as segment signal output for the LCD controller/driver.

(a) SEG20 to SEG23

These pins are the segment signal output pins for the LCD controller/driver.

2.2.11 P140 to P143 (port 14)

P140 to P143 function as an I/O port. These pins also function as pins for segment signal output and simultaneous output of segment key source signal for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
–	P140/SEG24 (KS0)
–	P141/SEG25 (KS1)
–	P142/SEG26 (KS2)
–	P143/SEG27 (KS3)

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 to P143 function as an I/O port. P140 to P143 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 to P143 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

(a) SEG24 (KS0) to SEG27 (KS3)

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.12 P150 to P153 (port 15)

P150 to P153 function as an I/O port. These pins also function as pins for segment signal output and simultaneous output of segment key source signal for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LE3-M	78K0/LG3-M
–	P150/SEG28 (KS4)
–	P151/SEG29 (KS5)
–	P152/SEG30 (KS6)
–	P153/SEG31 (KS7)

The following operation modes can be specified in 1-bit units.

(1) Port mode

P150 to P153 function as an I/O port. P150 to P153 can be set to input or output port in 1-bit units using port mode register 15 (PM15). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 15 (PU15).

(2) Control mode

P150 to P153 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

(a) SEG28 (KS4) to SEG31 (KS7)

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.13 LP00 to LP05 (port LP0)

LP00 to LP05 function as an I/O port. These pins also function as pins for zero-crossing detection signal output of the power quality measurement circuit.

78K0/LE3-M	78K0/LG3-M
–	LP00
–	LP01/ZX1
–	LP02/ZX2
–	LP03
–	LP04
–	LP05

The following operation modes can be specified in 1-bit units.

(1) Port mode

LP00 to LP05 function as an I/O port. LP00 to LP05 can be set to input or output port in 1-bit units using port mode register LP0 (LPM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register LP0 (LPU0).

(2) Control mode

LP00 to LP05 function as zero-crossing detection signal output of the power quality measurement circuit.

(a) ZX1, ZX2

These are pins for zero-crossing detection signal output.

2.2.14 LP10 to LP15 (port LP1)

LP10 to LP15 function as an I/O port.

78K0/LE3-M	78K0/LG3-M
–	LP10
–	LP11
–	LP12
–	LP13
–	LP14
–	LP15

The following operation modes can be specified in 1-bit units.

(1) Port mode

LP10 to LP15 function as an I/O port. LP10 to LP15 can be set to input or output port in 1-bit units using port mode register LP1 (LPM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register LP1 (LPM1).

2.2.15 ANI00 to ANI31

78K0/LE3-M	78K0/LG3-M
ANI00	ANI00
ANI01	ANI01
ANI10	ANI10
ANI11	ANI11
ANI20	ANI20
ANI21	ANI21
–	ANI30
–	ANI31

(a) ANI00 to ANI31

These pins are the 24-bit ΔΣ-type A/D converter analog input.
ANIx0 is a negative input pin, and ANIx1 is a positive input pin.
Note that the channel (voltage or current) that corresponds to each input pin varies according to whether the two-wire mode or three-wire mode is in use (See **CHAPTER 13 24-BIT ΔΣ-TYPE A/D CONVERTER**).

2.2.16 AV_{DD}, AV_{REF}, AV_{REFIO}, AV_{SS}, LV_{DD}, V_{DD}, V_{LC0} to V_{LC2}, and V_{SS}

(a) AV_{DD}

This is the positive power supply pin of 24-bit ΔΣ-type A/D converter.

(b) AV_{REF}

This is the 10-bit successive approximation type A/D converter reference voltage input pin and the positive power supply pin of port 2.
When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note When one or more of the pins of port 2 is used as the digital port pins or for segment output, make AV_{REF} the same potential as V_{DD}.

(c) AV_{REFIO}

This is the reference voltage I/O pin of 24-bit ΔΣ-type A/D converter.

(d) AV_{SS}

This is the 24-bit ΔΣ-type A/D converter ground potential pin. Even when the 24-bit ΔΣ-type A/D converter is not used, always use this pin with the same potential as the V_{SS}.

(e) LV_{DD}

Real-time counter, power calculation circuit, subsystem clock oscillator, and positive power supply for port LP.

(f) V_{DD}

This is the positive power supply pin.

(g) V_{LC0} to V_{LC2}

These pins are the power supply voltage pins for driving the LCD.

(h) V_{SS}

This is the ground potential pin.

2.2.17 CF

This is the calibration frequency output pin of digital frequency conversion circuit.

2.2.18 COM0 to COM3

These pins are the common signal output pins for the LCD controller/driver.

2.2.19 EXCLKS

This is an external clock input pin for subsystem clock.

2.2.20 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to V_{SS} in the normal operation mode.

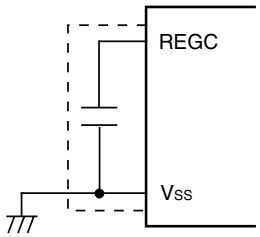
In flash memory programming mode, connect this pin to the flash memory programmer.

2.2.21 IC

This is an internal connection pin. Connect to V_{SS}.

2.2.22 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF: recommended).



Caution Keep the wiring length as short as possible in the area enclosed by the broken lines in the above figures.

2.2.23 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.2.24 RTC1HZ

This is the real-time counter correction clock (1 Hz) output pin.

2.2.25 SEGxx

These pins are the LCD controller/driver segment signal outputs.

2.2.26 XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

2.2.27 32KHZCLK

This is the real-time counter clock (32 kHz) output pin.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-2 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **2.1 Pin Function List**.

Table 2-2. Pin I/O Circuit Types (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P11/$\overline{\text{SCK10}}$	5-AH	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P12/SI10/RxD0			
P13/SO10/TxD0/IROUT			
P20/SEG39/ANI0 to P27/SEG32/ANI7[Note]	17-AA		<Analog setting> Connect to AV_{REF} or AV_{SS}. <Digital setting> Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P30/INTP5	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/TOH1/INTP3			
P32/TOH0	5-AG		
P33/TI000/BUZ/INTP2	5-AH		
P40/KR0			
P41/KR1			
P42/KR2			
P43/TO51/TI51/KR3			
P44/TO50/TI50/KR4			
P45/KR5			
P80/SEG4 to P83/SEG7	17-Y		<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P90/SEG8 to P93/SEG11			
P100/SEG12 to P103/SEG15			
P110/SEG16, P111/SEG17			
P112/SEG18/TxD6			
P113/SEG19/RxD6	17-Z		

Note P20/SEG39/ANI0 to P27/SEG32/ANI7 are set in the digital input mode after release of reset.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

Table 2-2. Pin I/O Circuit Types (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P120/INTP0/EXLVI	5-AH	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P121/X1/OCD0A[Note 1]	37-A	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK/OCD0B[Note 1]			
P123	2-B		
P130/SEG20 to P133/SEG23	17-Y	I/O	<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P140/SEG24 (KS0) to P143/SEG27 (KS3)			
P150/SEG28 (KS4) to P153/SEG31 (KS7)			
LP00	5-AG	I/O	Input: Independently connect to LV_{DD} or V_{SS} via a resistor. Output: Leave open.
LP01/ZX1			
LP02/ZX2			
LP03 to LP05, LP10 to LP15			
ANI00 to ANI31	35	Input	Independently connect to AV_{DD} or AV_{SS} via a resistor.
AV_{REF}	–	–	Connect directly to V_{DD}.[Note 2]
AV_{REFIO}	–	–	Connect to AV_{SS} via a capacitor.
AV_{SS}	–	–	Connect directly to V_{SS}.
CF	5-AG	Output	Leave open.
COM0 to COM3	18-B		
FLMD0	38	Input	Connect to V_{SS}.[Note 3]
LV_{DD}	–	–	Connect directly to V_{DD}.
$\overline{\text{RESET}}$	2	Input	Connect directly or via a resistor to V_{DD}.
RTC1HZ/32KHZCLK	5-AG	Output	Leave open.
SEGxx	17-D	Output	Leave open.
V_{LC0} to V_{LC2}	–	–	Leave open.
XT1/EXCLKS	–	–	<When the internal high-speed oscillation clock is used> Connect to V_{SS}.
<R> XT2	–	–	<When the internal high-speed oscillation clock or external clock is used> Leave open.

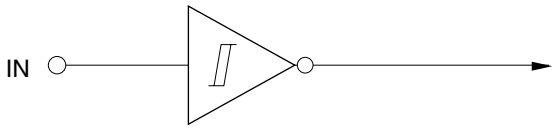
Notes 1. Use recommended connection above in I/O port mode (see **Figure 5-2 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

2. When using port 2 as a digital port or for segment output, set it to the same potential as that of V_{DD}.

3. FLMD0 is a pin used when writing data to flash memory. When rewriting flash memory data on-board or performing on-chip debugging, connect this pin to V_{SS} via a resistor (10 kΩ: recommended).

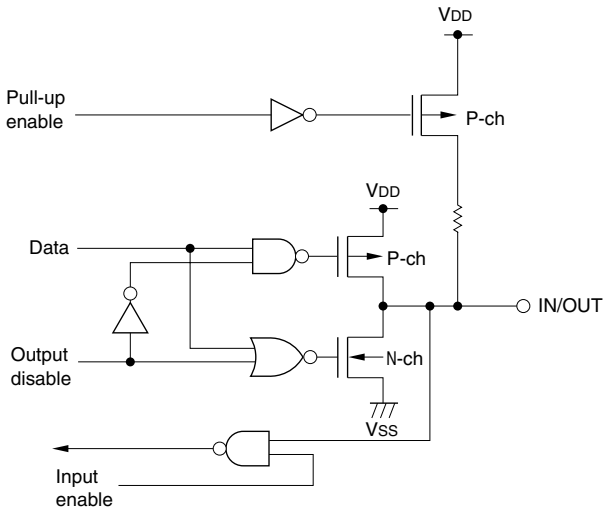
Figure 2-1. Pin I/O Circuit List (1/3)

Type 2

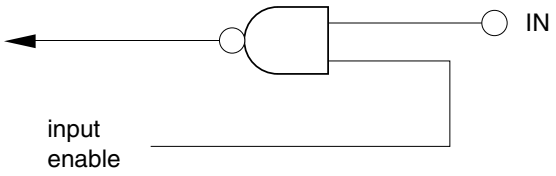


Schmitt-triggered input with hysteresis characteristics

Type 5-AG



Type 2-B



Type 5-AH

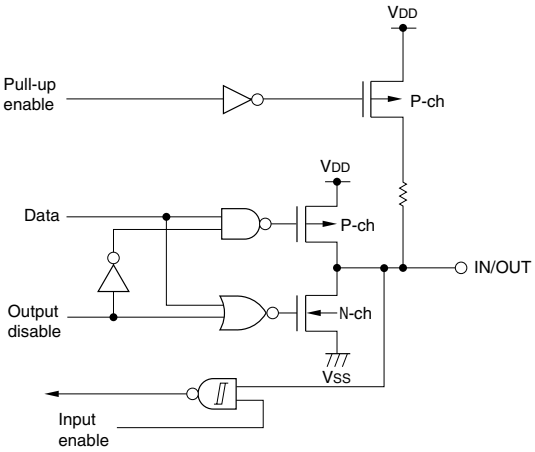
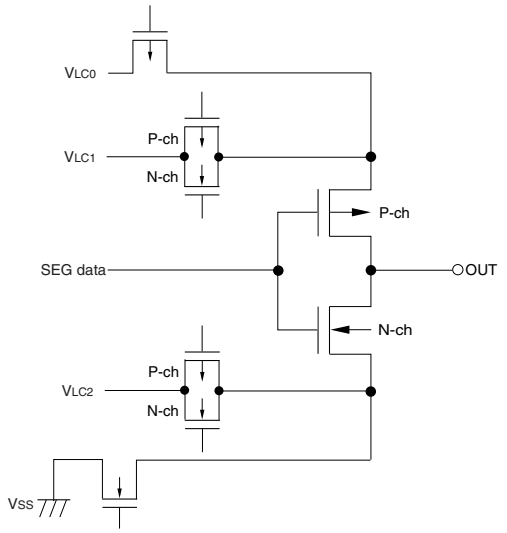
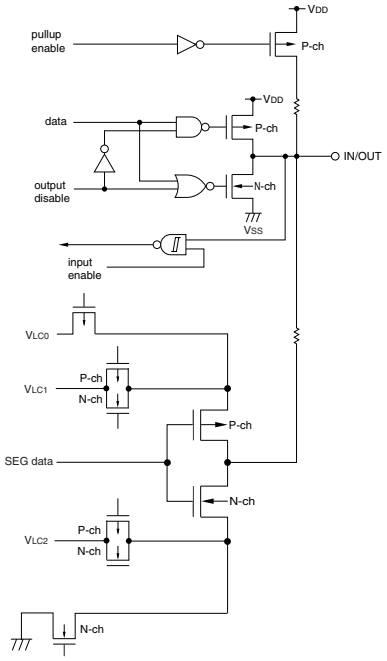


Figure 2-1. Pin I/O Circuit List (2/3)

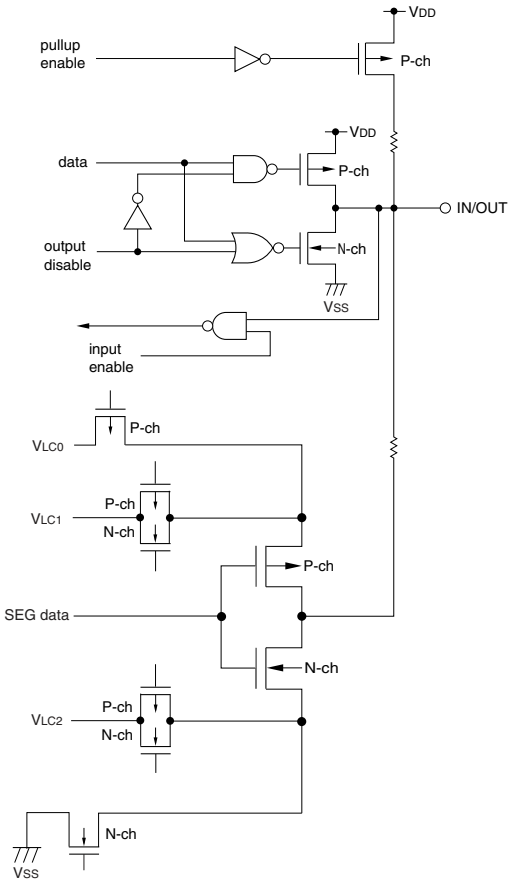
Type 17-D



Type 17-Z



Type 17-Y



Type 17-AA

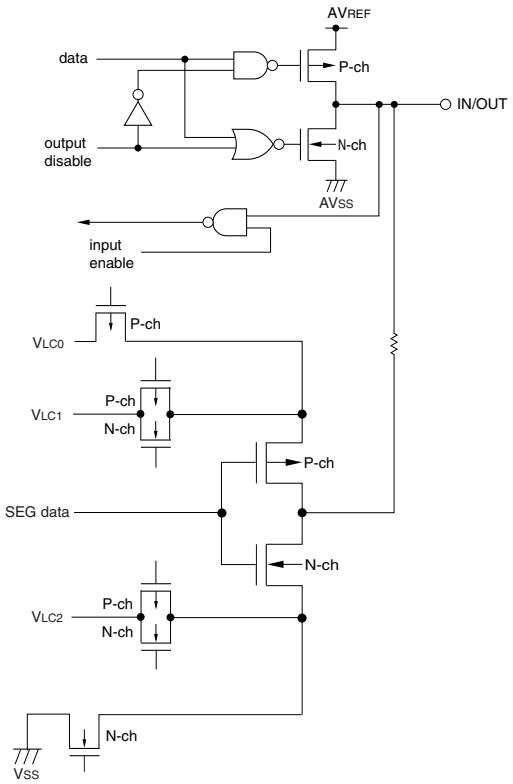
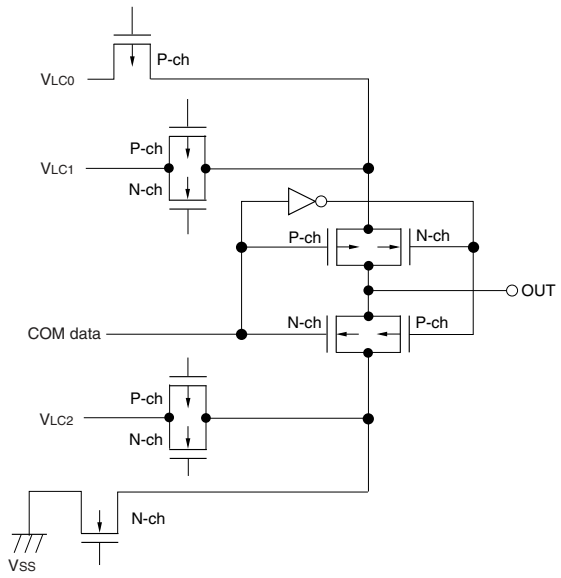
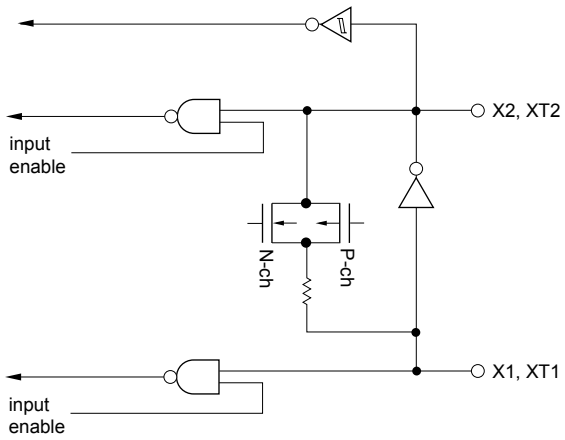


Figure 2-1. Pin I/O Circuit List (3/3)

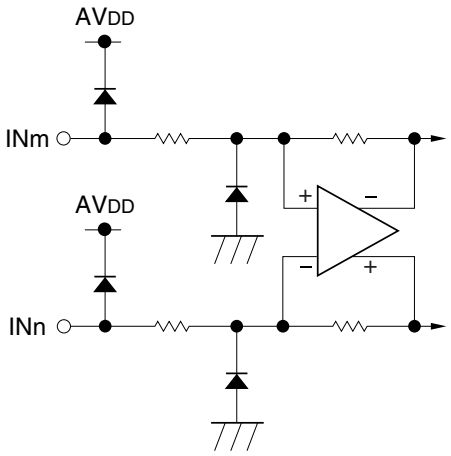
Type 18-B



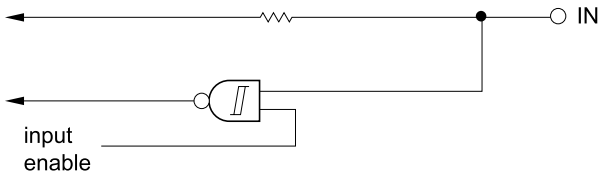
Type 37-A



Type 35



Type 38



CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

Each products in the 78K0/Lx3-M microcontrollers can access a 64 KB memory space.

In addition to special function registers (SFRs), each product has extended special function registers (extended SFRs).

The extended SFR interface is used to access the extended SFR space (See **CHAPTER 17 EXTENDED SFR INTERFACE**).

Figure 3-1 to Figure 3-4 show the memory maps.

Caution Regardless of the internal memory capacity, the initial values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) of all products in the 78K0/Lx3-M microcontrollers are fixed (IMS = CFH, IXS = 0CH). Therefore, set the value corresponding to each product as indicated below.

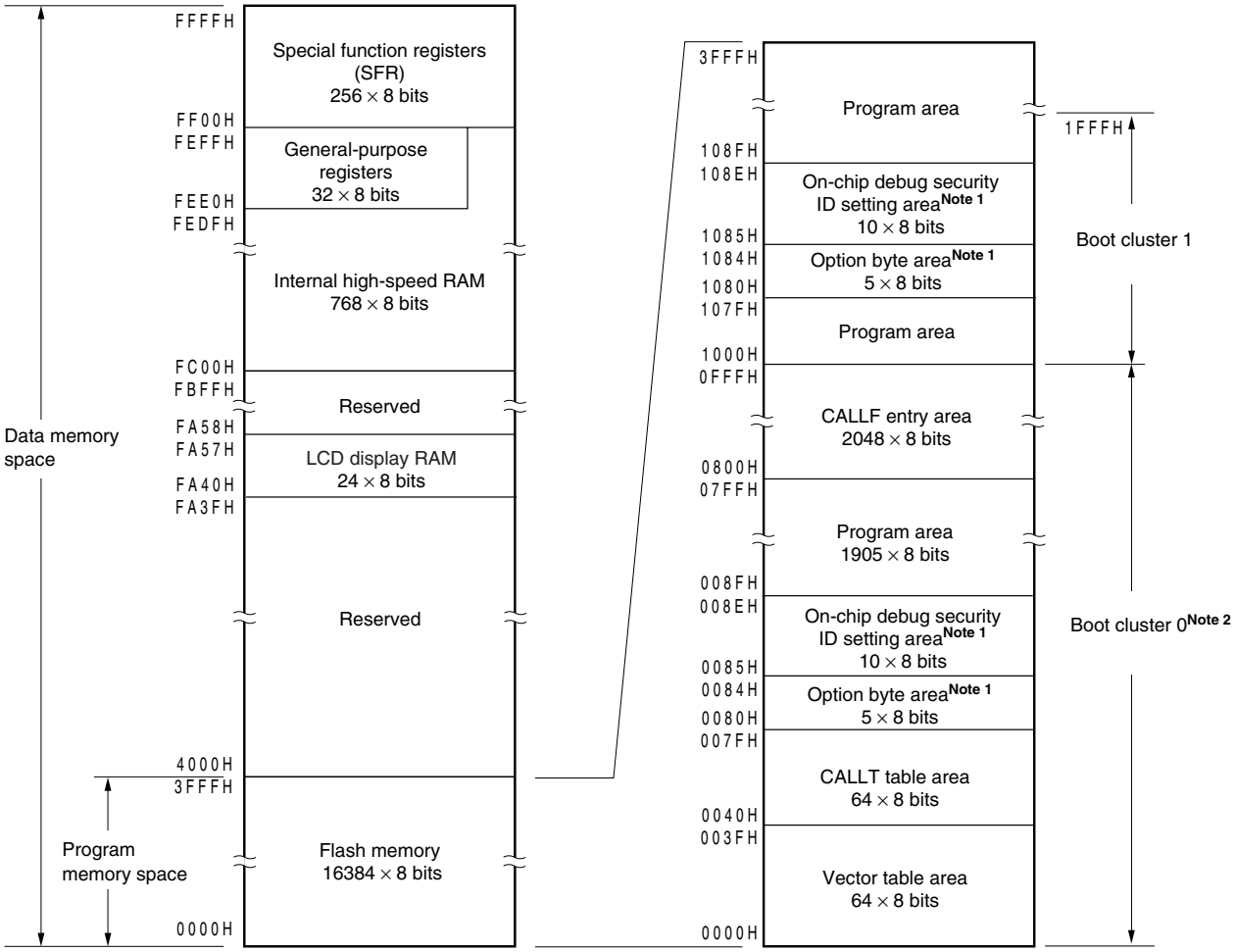
Table 3-1. Set Values of Internal Memory Size Switching Register (IMS) and Internal Expansion RAM Size Switching Register (IXS)

78K0/LE3-M	78K0/LG3-M	IMS	IXS	ROM Capacity	Internal High-Speed RAM Capacity	Internal Expansion RAM Capacity
μPD78F8052Note	–	04H	0CH	16 KB	768 bytes	–
μPD78F8053Note	–	C8H		32 KB		
–	μPD78F8054	CCH	0AH	48 KB		1 KB
–	μPD78F8055	CFH		60 KB	1 KB	

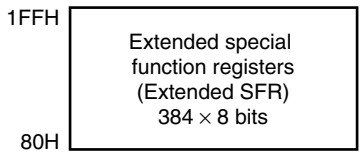
Note A product that does not have an internal expansion RAM is not provided with IXS.

Figure 3-1. Memory Map (μPD78F8052)

(a) SFR space



(b) Extended SFR space



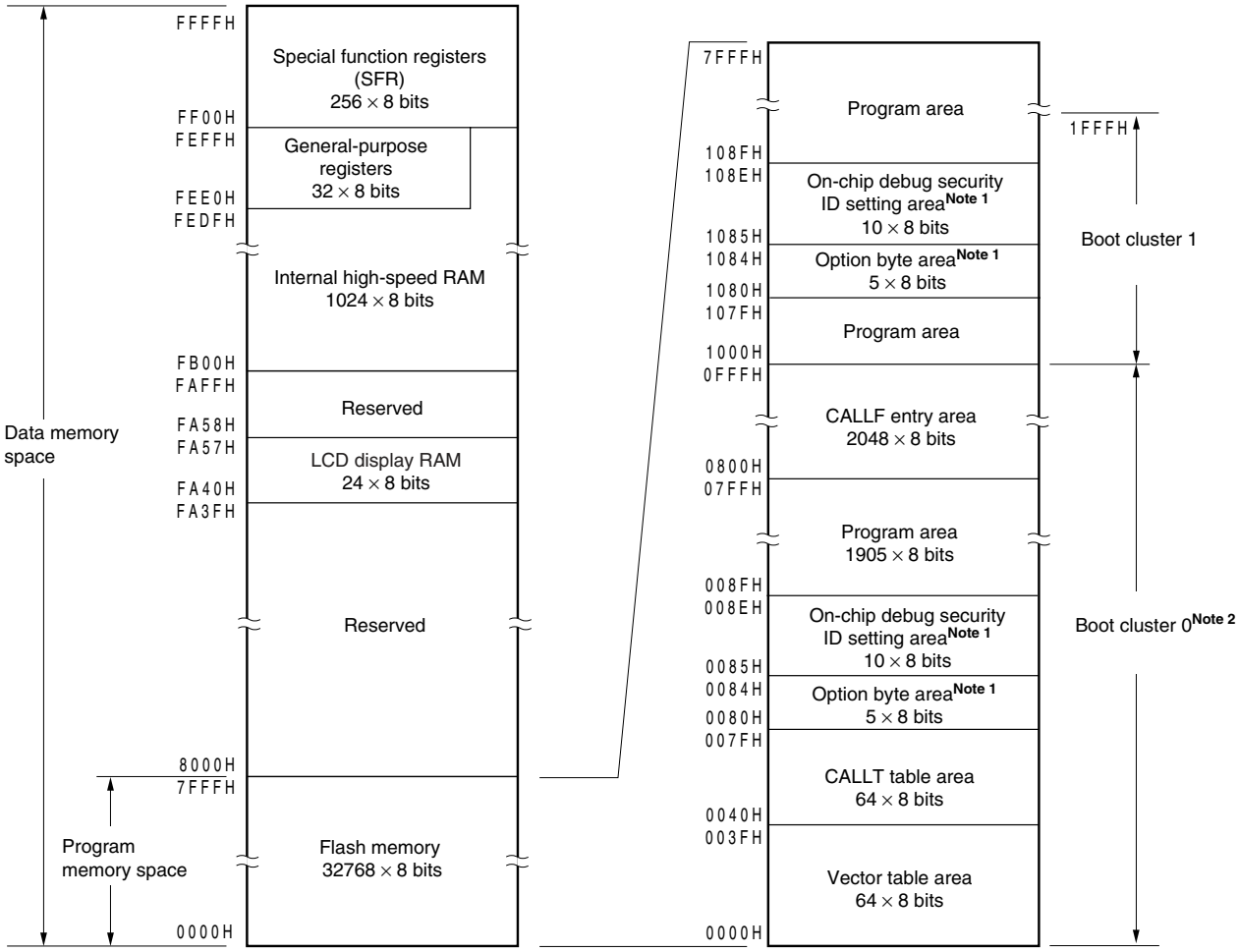
Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

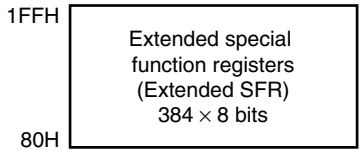
2. Writing boot cluster 0 can be prohibited depending on the setting of security.

Figure 3-2. Memory Map (μPD78F8053)

(a) SFR space



(b) Extended SFR space



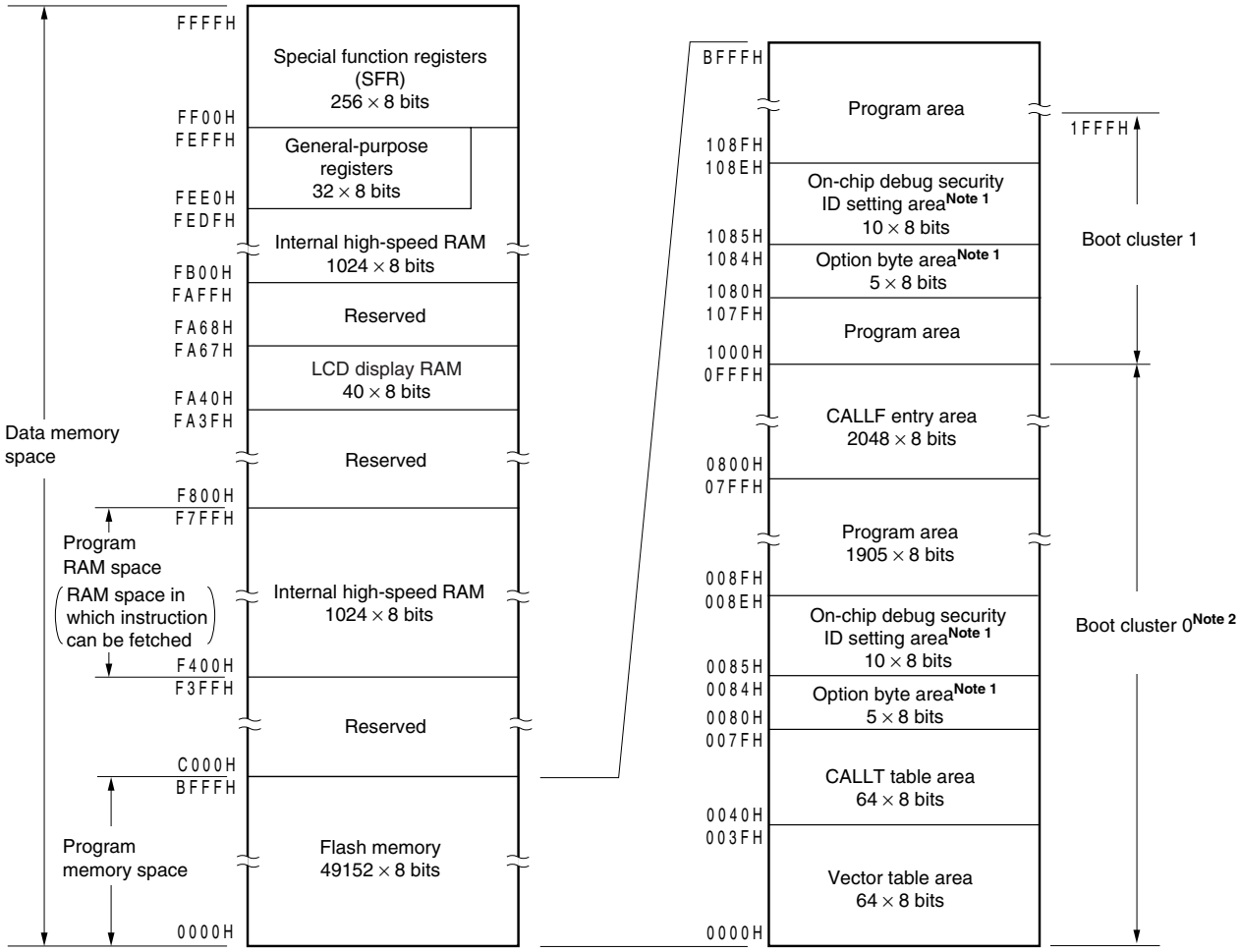
Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

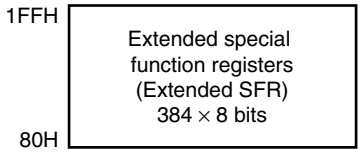
2. Writing boot cluster 0 can be prohibited depending on the setting of security.

Figure 3-3. Memory Map (μPD78F8054)

(a) SFR space



(b) Extended SFR space



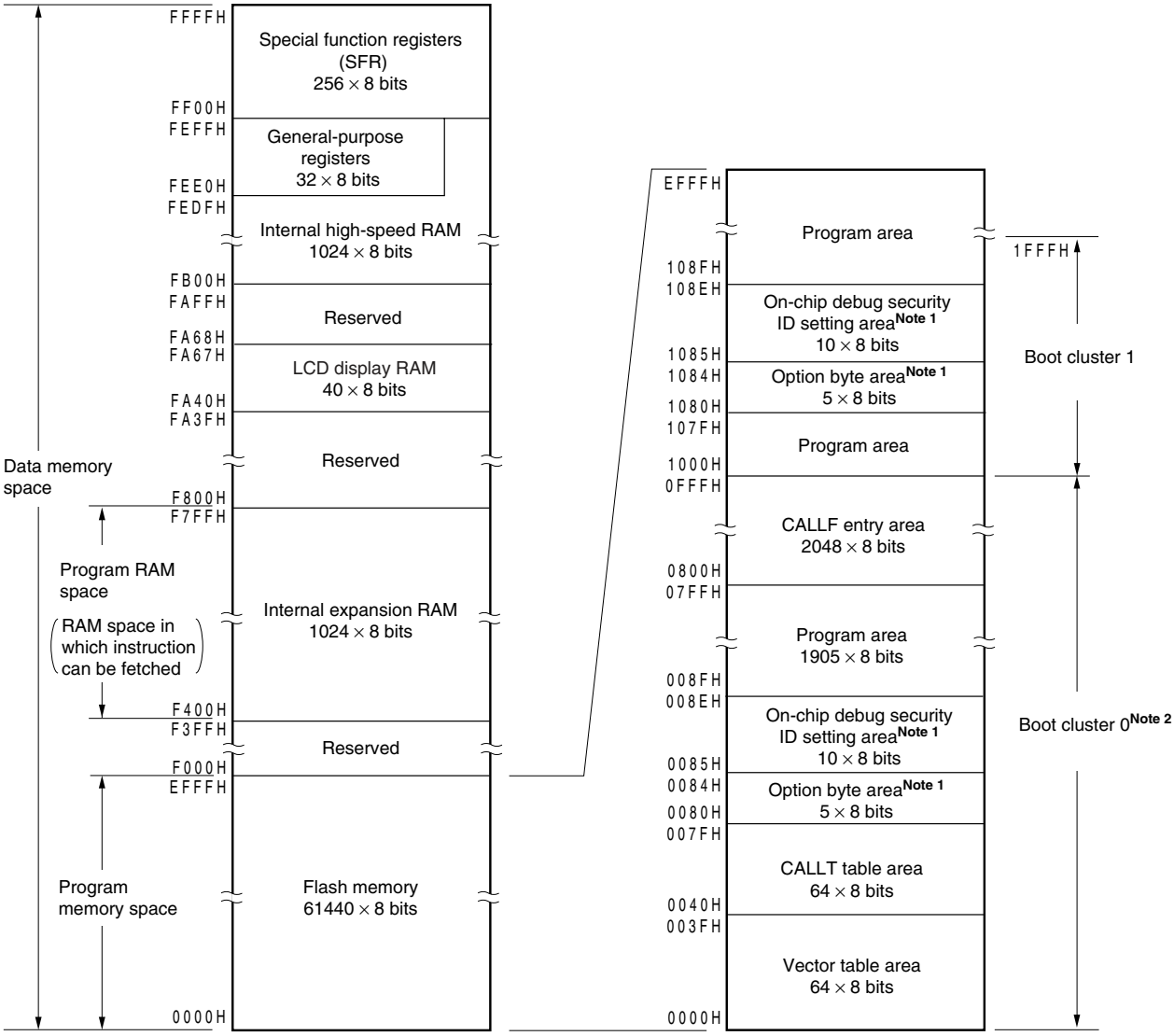
Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

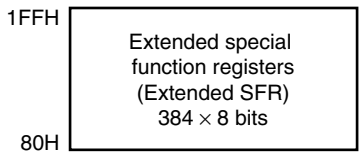
2. Writing boot cluster 0 can be prohibited depending on the setting of security.

Figure 3-4. Memory Map (μPD78F8055)

(a) SFR space



(b) Extended SFR space



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security.

The flash memory is divided into blocks (one block = 1 KB).

Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-2. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
0000H to 03FFH	00H	4000H to 43FFH	10H	8000H to 83FFH	20H	C000H to C3FFH	30H
0400H to 07FFH	01H	4400H to 47FFH	11H	8400H to 87FFH	21H	C400H to C7FFH	31H
0800H to 0BFFH	02H	4800H to 4BFFH	12H	8800H to 8BFFH	22H	C800H to CBFFH	32H
0C00H to 0FFFH	03H	4C00H to 4FFFH	13H	8C00H to 8FFFH	23H	CC00H to CFFFH	33H
1000H to 13FFH	04H	5000H to 53FFH	14H	9000H to 93FFH	24H	D000H to D3FFH	34H
1400H to 17FFH	05H	5400H to 57FFH	15H	9400H to 97FFH	25H	D400H to D7FFH	35H
1800H to 1BFFH	06H	5800H to 5BFFH	16H	9800H to 9BFFH	26H	D800H to DBFFH	36H
1C00H to 1FFFH	07H	5C00H to 5FFFH	17H	9C00H to 9FFFH	27H	DC00H to DFFFH	37H
2000H to 23FFH	08H	6000H to 63FFH	18H	A000H to A3FFH	28H	E000H to E3FFH	38H
2400H to 27FFH	09H	6400H to 67FFH	19H	A400H to A7FFH	29H	E400H to E7FFH	39H
2800H to 2BFFH	0AH	6800H to 6BFFH	1AH	A800H to ABFFH	2AH	E800H to EBFFH	3AH
2C00H to 2FFFH	0BH	6C00H to 6FFFH	1BH	AC00H to AFFFH	2BH	EC00H to EFFFH	3BH
3000H to 33FFH	0CH	7000H to 73FFH	1CH	B000H to B3FFH	2CH		
3400H to 37FFH	0DH	7400H to 77FFH	1DH	B400H to B7FFH	2DH		
3800H to 3BFFH	0EH	7800H to 7BFFH	1EH	B800H to BBFFH	2EH		
3C00H to 3FFFH	0FH	7C00H to 7FFFH	1FH	BC00H to BFFFH	2FH		

Remark μPD78F8052: Block numbers 00H to 0FH
μPD78F8053: Block numbers 00H to 1FH
μPD78F8054: Block numbers 00H to 2FH
μPD78F8055: Block numbers 00H to 3BH

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

78K0/Lx3-M microcontrollers incorporate internal ROM (flash memory), as shown below.

Table 3-3. Internal ROM Capacity

78K0/LE3-M	78K0/LG3-M	Internal ROM
64 pins	100 pins	(Flash memory)
μPD78F8052	−	16384 × 8 bits (0000H to 3FFFH)
μPD78F8053	−	32768 × 8 bits (0000H to 7FFFH)
−	μPD78F8054	49152 × 8 bits (0000H to BFFFH)
−	μPD78F8055	61440 × 8 bits (0000H to EFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 64-byte area 0000H to 003FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Table 3-4. Vector Table

Vector Table Address	Interrupt Source	78K0/LE3-M	78K0/LG3-M
0000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT	√	√
0004H	INTLVI	√	√
0006H	INTP0	√	√
0008H	INTP1	√	√
000AH	INTP2	√	√
000CH	INTP3	–	√
0010H	INTP5	√	√
0012H	INTSRE6	√	√
0014H	INTSR6	√	√
0016H	INTST6	√	√
0018H	INTCSI10/INTST0	√	√
001AH	INTTMH1	√	√
001CH	INTTMH0	√	√
001EH	INTTM50	√	√
0020H	INTTM000	√	√
0022H	INTTM010	√	√
0024H	INTAD	√	√
0026H	INTSR0	√	√
002AH	INTTM51	√	√
002CH	INTKR	√	√
0032H	INTTM52	√	√
0034H	INTTMH2	√	√
003CH	INTACSI	√	√
003EH	BRK	√	√

Remark √: Mounted, –: Not mounted

(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, see **CHAPTER 29 OPTION BYTE**.

(4) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

(5) On-chip debug security ID setting area

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION**.

3.1.2 Internal data memory space

78K0/Lx3-M microcontrollers incorporate the following RAMs.

(1) Internal high-speed RAM

The 32-byte area FEE0H to FEFFH is assigned to four general-purpose register banks consisting of eight 8-bit registers per bank.

This area cannot be used as a program area in which instructions are written and executed.

The internal high-speed RAM can also be used as a stack memory.

Table 3-5. Internal High-Speed RAM Capacity

78K0/LE3-M	78K0/LG3-M	Internal high-speed RAM
64 pins	100 pins	
μPD78F8052	–	768 × 8 bits (FC00H to FEFFH)
μPD78F8053	–	1024 × 8 bits (FB00H to FEFFH)
–	μPD78F8054	
–	μPD78F8055	

(2) Internal expansion RAM

The internal expansion RAM can also be used as a normal data area similar to the internal high-speed RAM, as well as a program area in which instructions can be written and executed.

The internal expansion RAM cannot be used as a stack memory.

Table 3-6. Internal Expansion RAM Capacity

78K0/LE3-M	78K0/LG3-M	Internal expansion RAM
64 pins	100 pins	
μPD78F8052	–	–
μPD78F8053	–	
–	μPD78F8054	1024 × 8 bits (FB00H to FEFFH)
–	μPD78F8055	

(3) LCD display RAM

LCD display RAM is incorporated in the LCD controller/driver (see **18.5 LCD Display Data Memory**).

Table 3-7. LCD Display RAM Capacity

78K0/LE3-M	78K0/LG3-M	LCD display RAM
64 pins	100 pins	
μPD78F8052	–	24 × 4 bits (FA40H to FA57H)
μPD78F8053	–	
–	μPD78F8054	40 × 4 bits (FA40H to FA67H)
–	μPD78F8055	

3.1.3 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FF00H to FFFFH (see **Table 3-8 Special Function Register List** in **3.2.3 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.1.4 Extended special function register (2nd SFR) area

On-chip peripheral hardware extended special function registers (2nd SFRs) are allocated in the area 80H to 1D8H (see **Table 3-9 Extended Special Function Register List** in **3.2.4 Extended special function registers (2nd SFRs)**).

The extended SFR interface is used to access the extended SFR space. (See **CHAPTER 17 EXTENDED SFR INTERFACE**).

Caution Do not access addresses to which extended SFRs are not assigned.

3.1.5 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the 78K0/Lx3-M microcontrollers, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of special function registers (SFRs) and general-purpose registers are available for use. Figure 3-5 to Figure 3-8 show correspondence between data memory and addressing. For details of each addressing mode, see **3.4 Operand Address Addressing**.

Figure 3-5. Correspondence Between Data Memory and Addressing (μPD78F8052)

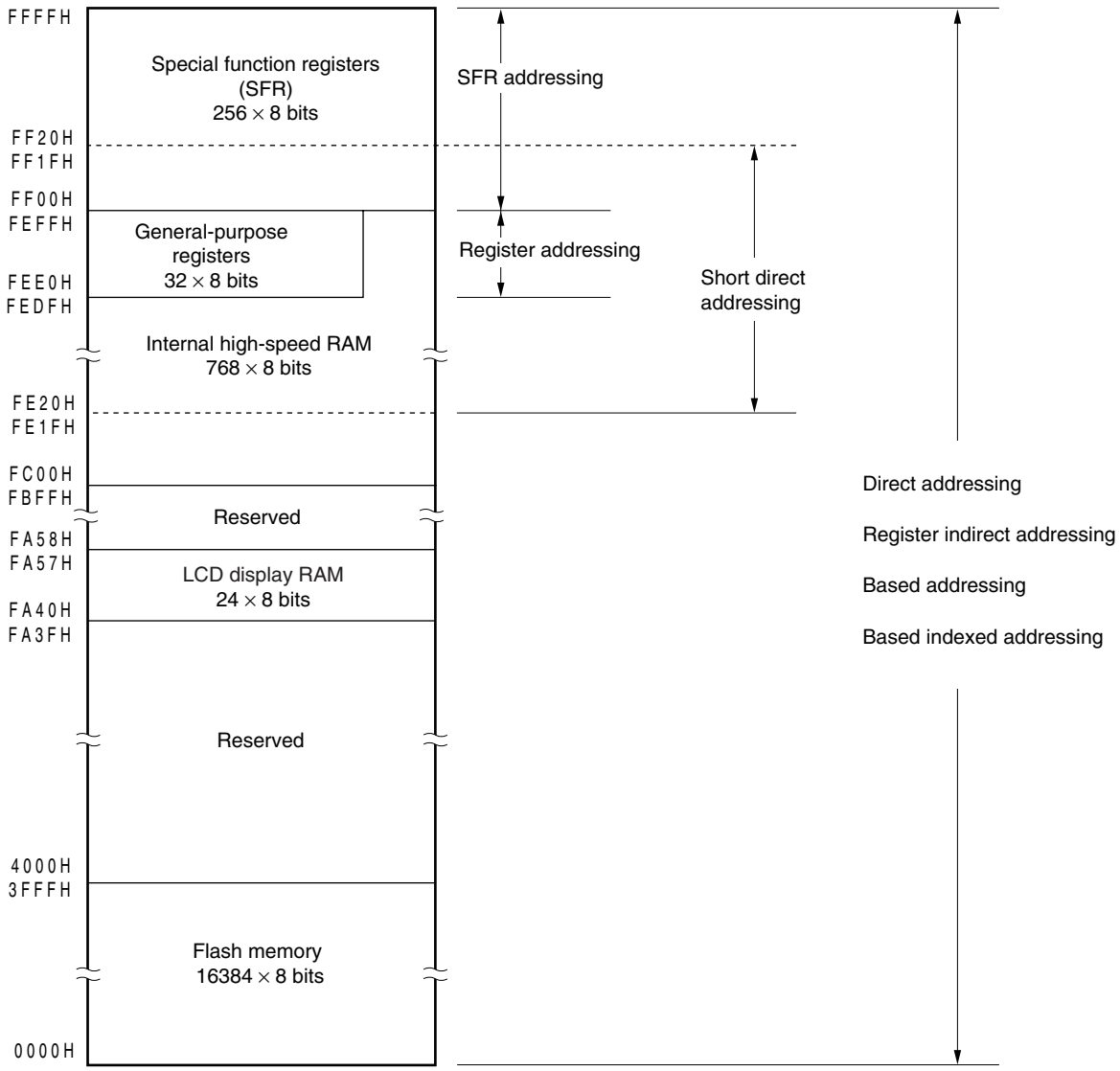


Figure 3-6. Correspondence Between Data Memory and Addressing (μPD78F8053)

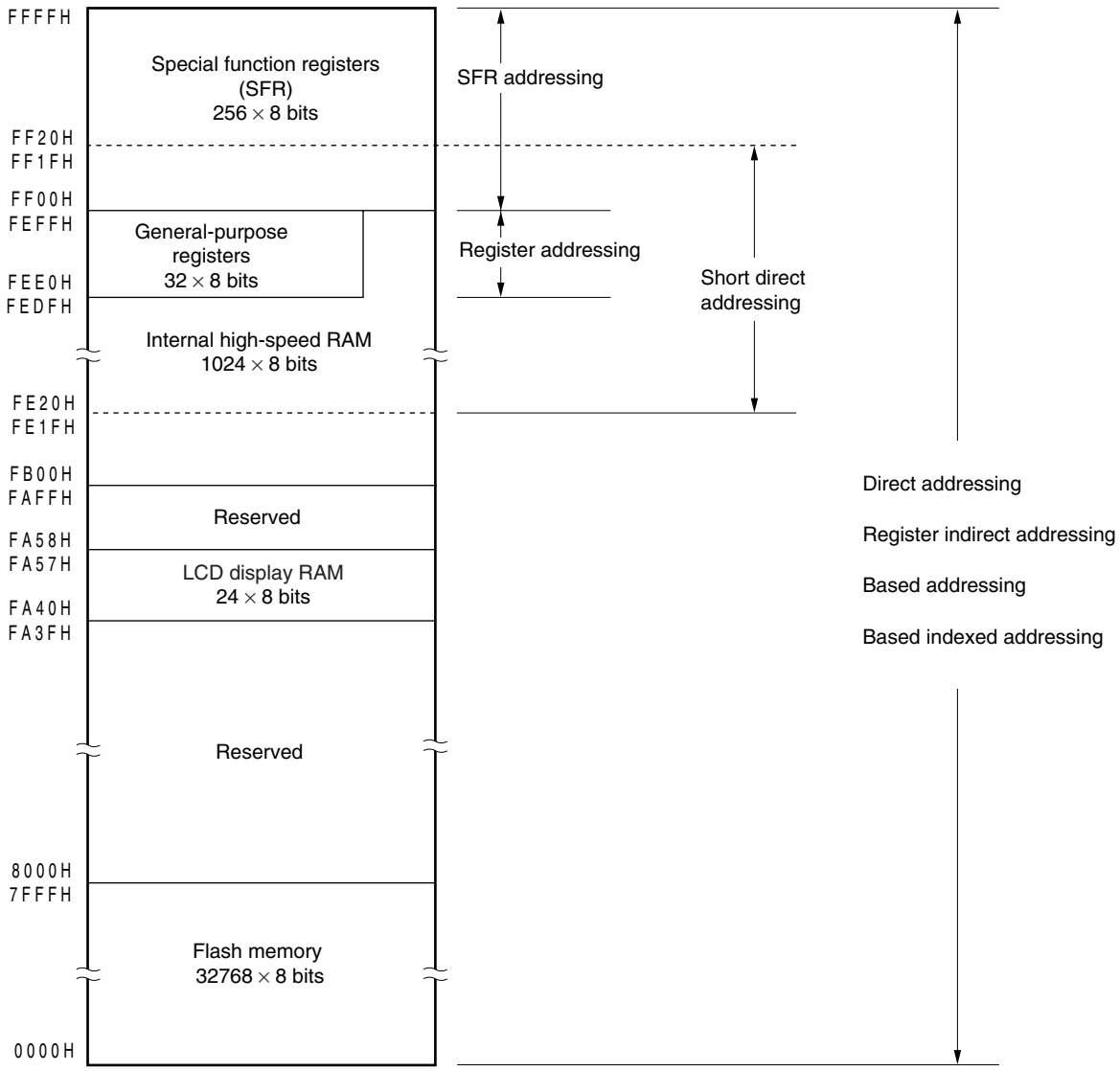


Figure 3-7. Correspondence Between Data Memory and Addressing (μPD78F8054)

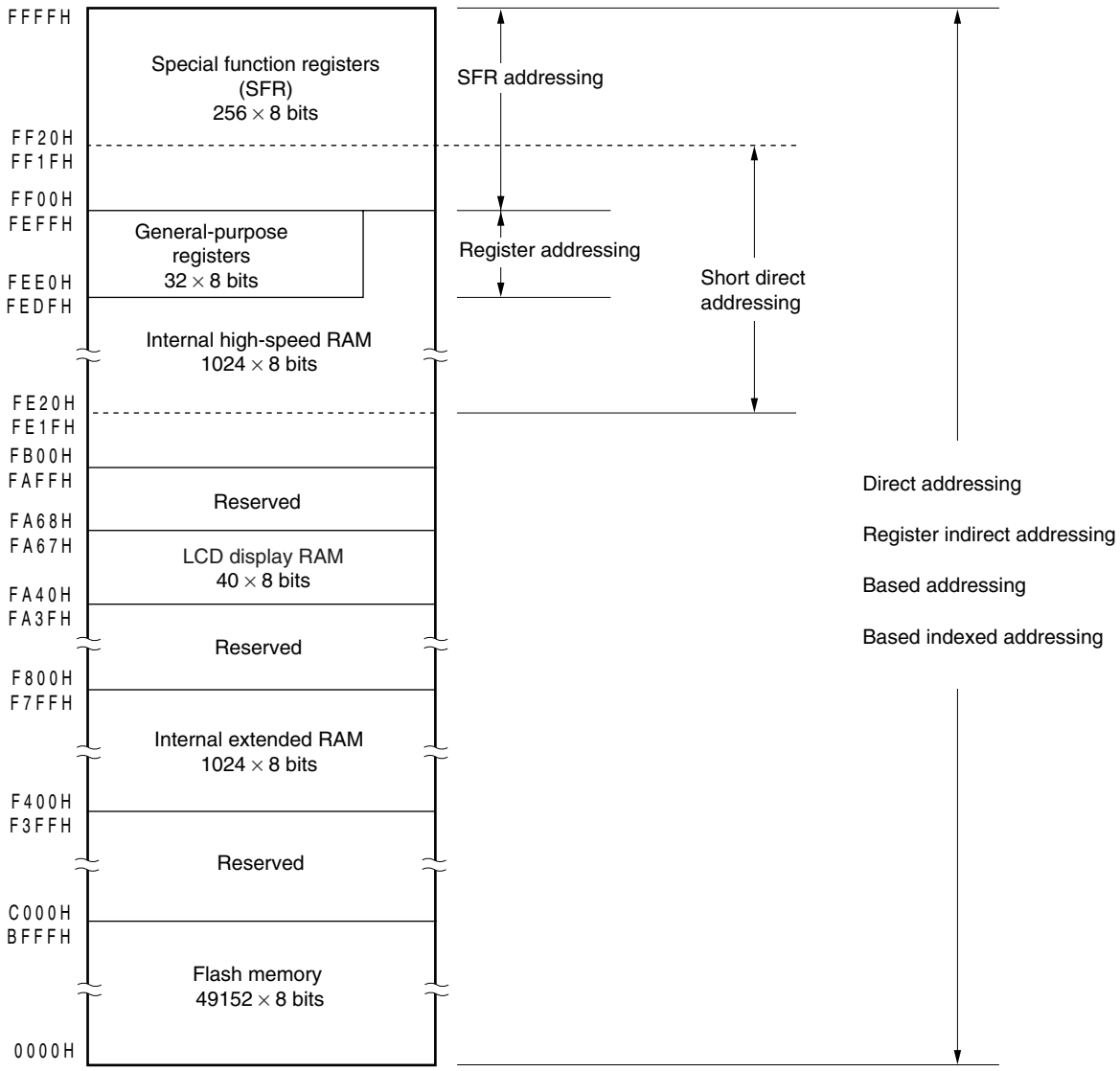
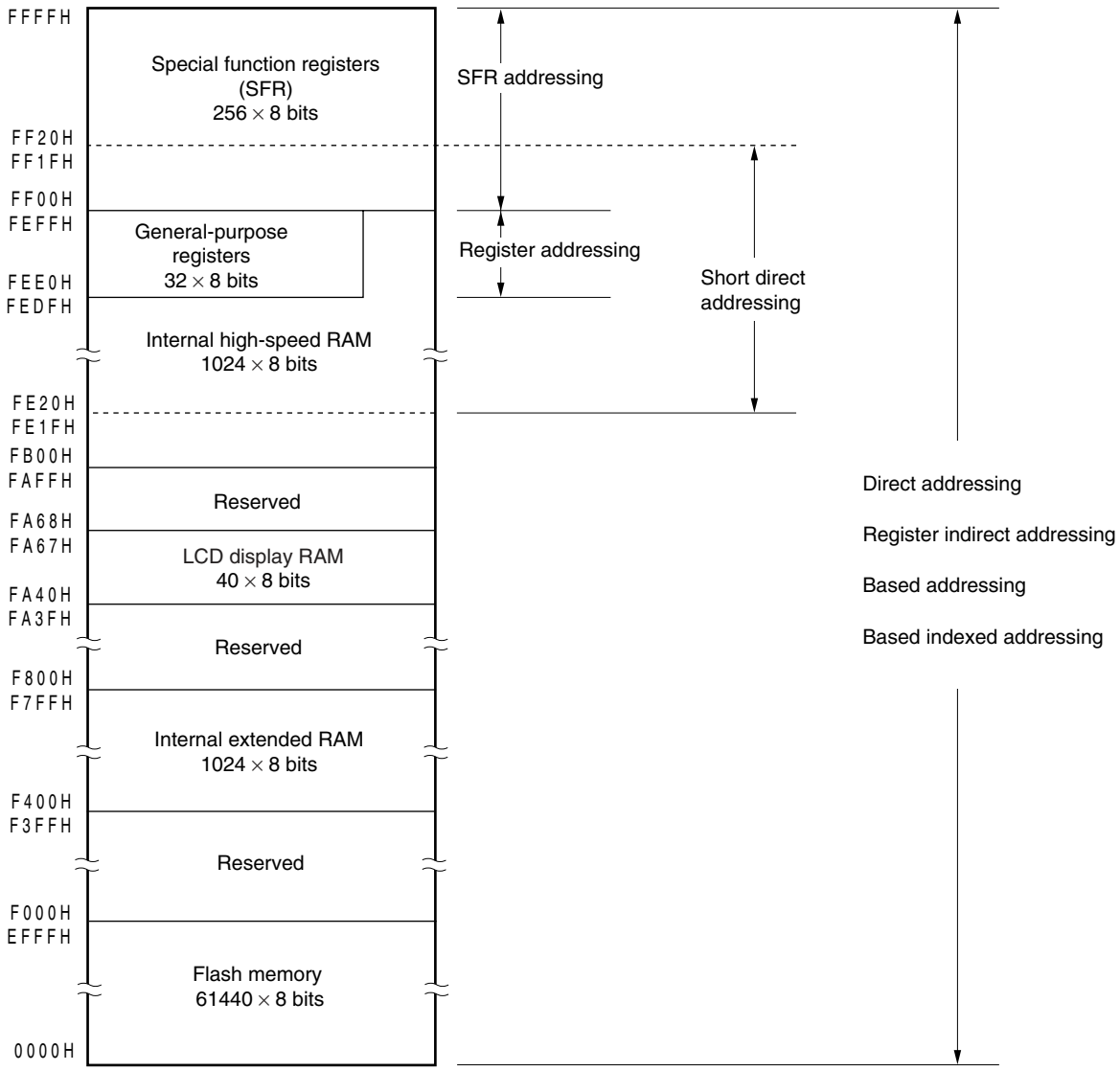


Figure 3-8. Correspondence Between Data Memory and Addressing (μPD78F8055)



3.2 Processor Registers

The 78K0/Lx3-M microcontrollers incorporate the following processor registers.

3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-9. Format of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vector interrupt request acknowledgment or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 3-10. Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0 and RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flag (ISP)

This flag manages the priority of acknowledgeable maskable vectored interrupts. When this flag is 0, low-level vectored interrupt requests specified by a priority specification flag register (PR0L, PR0H, PR1L, PR1H) (see **20.3 (5) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

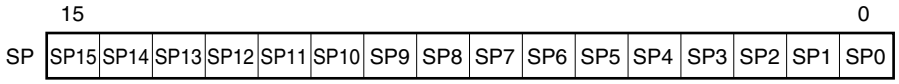
(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 3-11. Format of Stack Pointer



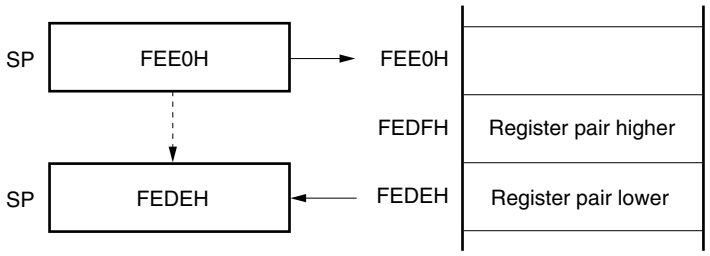
The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves/restores data as shown in Figure 3-12 and Figure 3-13.

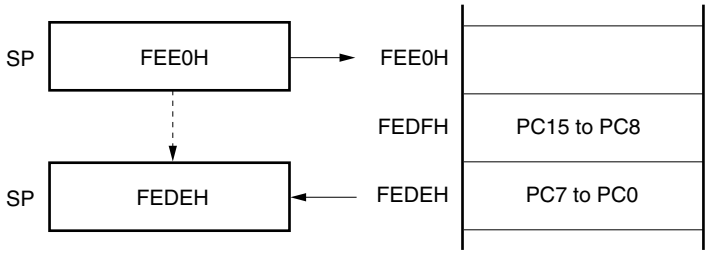
Caution Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

Figure 3-12. Data to Be Saved to Stack Memory

(a) PUSH rp instruction (when SP = FEE0H)



(b) CALL, CALLF, CALLT instructions (when SP = FEE0H)



(c) Interrupt, BRK instructions (when SP = FEE0H)

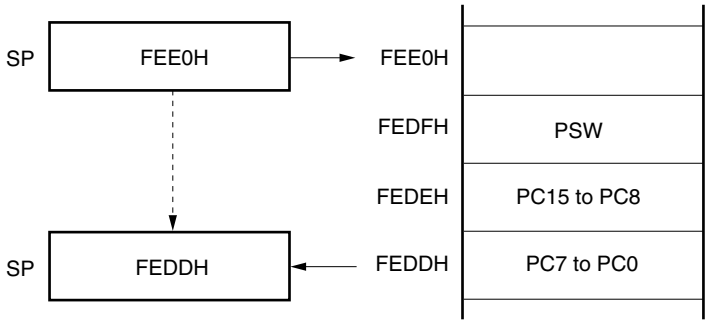
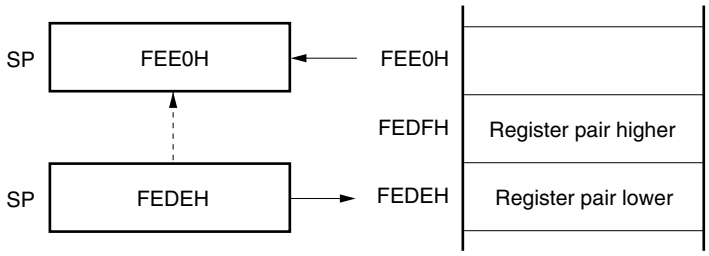
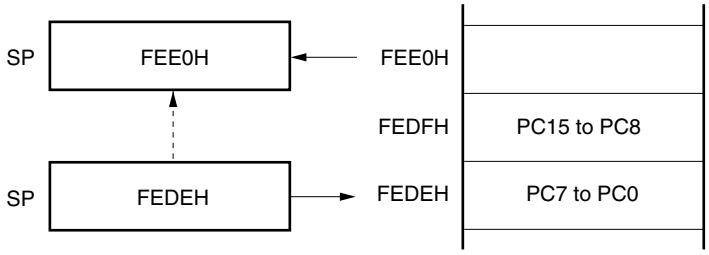


Figure 3-13. Data to Be Restored from Stack Memory

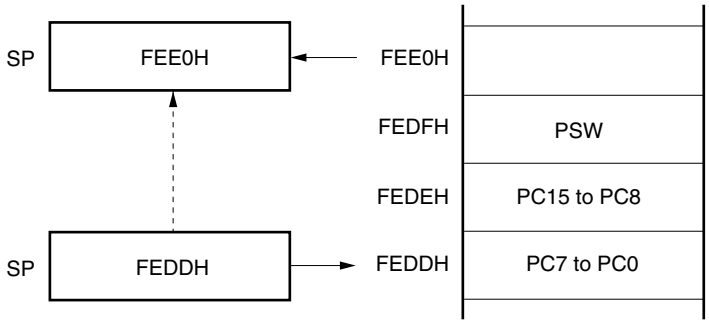
(a) POP rp instruction (when SP = FEDEH)



(b) RET instruction (when SP = FEDEH)



(c) RETI, RETB instructions (when SP = FEDDH)



3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FEE0H to FEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

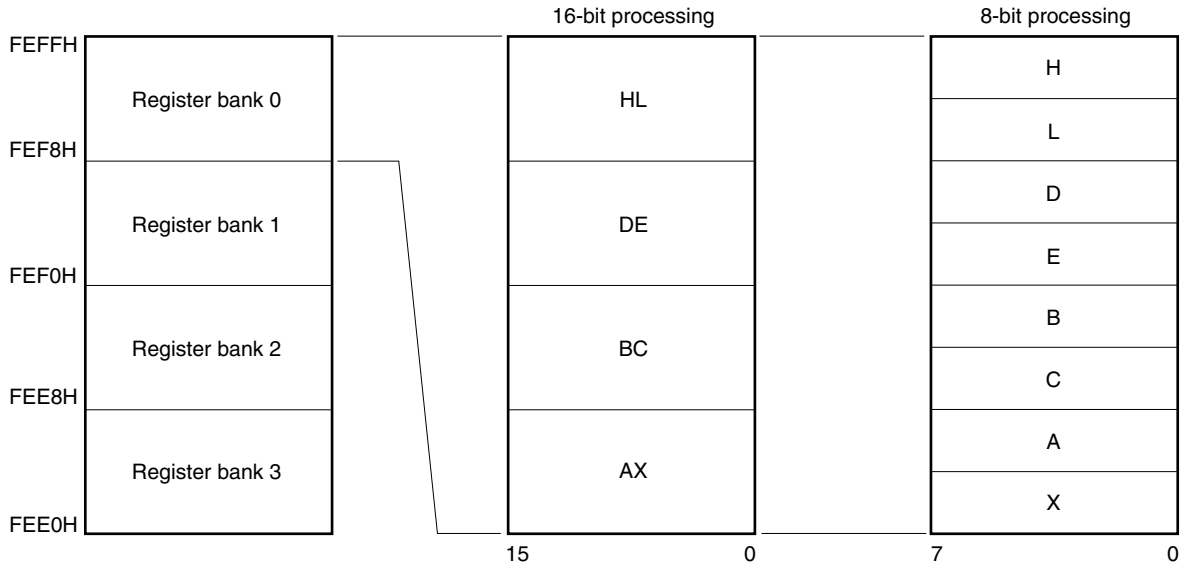
Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

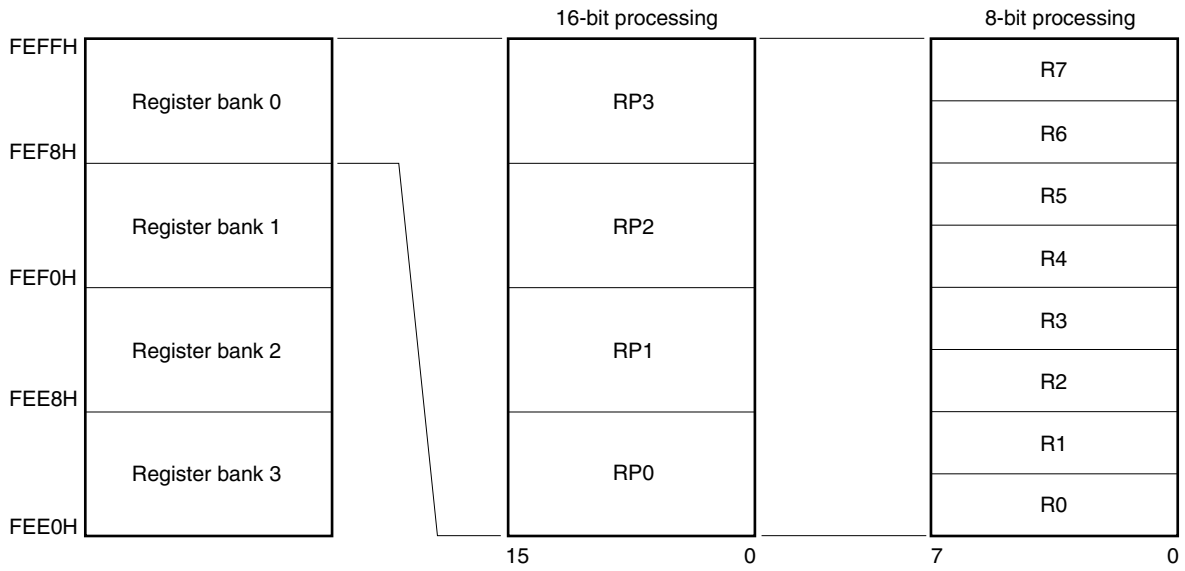
Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Figure 3-14. Configuration of General-Purpose Registers

(a) Function name



(b) Absolute name



3.2.3 Special function registers (SFRs)

Unlike a general-purpose register, each special function register has a special function.

SFRs are allocated to the FF00H to FFFFH areas.

Special function registers can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulatable bit units, 1, 8, and 16, depend on the special function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit).
  This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr).
  This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp).
  When specifying an address, describe an even address.

Table 3-8 gives a list of the special function registers. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a special function register. It is a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0. When using the RA78K0 and ID78K0-QB, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding special function register can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulatable bit units
  Indicates the manipulatable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which SFRs are not assigned.

Remark For the extended SFR (2nd SFR), see **3.2.4 Extended special function registers (2nd SFRs)**.

Table 3-8. Special Function Register List (1/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Receive buffer register 6	RXB6	R	–	√	–	FFH
FF01H	Port register 1	P1	R/W	√	√	–	00H
FF02H	Port register 2	P2	R/W	√	√	–	00H
FF03H	Port register 3	P3	R/W	√	√	–	00H
FF04H	Port register 4	P4	R/W	√	√	–	00H
FF05H	Transmit buffer register 6	TXB6	R/W	–	√	–	FFH
FF06H	10-bit A/D conversion result register	ADCR	R	–	–	√	0000H
FF07H	8-bit A/D conversion result register H	ADCRH	R	–	√	–	00H
FF08H	Port register 8	P8	R/W	√	√	–	00H
FF09H	Port register 9	P9	R/W	√	√	–	00H
FF0AH	Port register 10	P10	R/W	√	√	–	00H
FF0BH	Port register 11	P11	R/W	√	√	–	00H
FF0CH	Port register 12	P12	R/W	√	√	–	00H
FF0DH	Port register 13	P13	R/W	√	√	–	00H
FF0EH	Port register 14	P14	R/W	√	√	–	00H
FF0FH	Port register 15	P15	R/W	√	√	–	00H
FF10H	16-bit timer counter 00	TM00	R	–	–	√	0000H
FF11H							
FF12H	16-bit timer compare register 000	CR000	R/W	–	–	√	0000H
FF13H							
FF14H	16-bit timer capture/compare register 010	CR010	R/W	–	–	√	0000H
FF15H							
FF16H	8-bit timer counter 50	TM50	R	–	√	–	00H
FF17H	8-bit timer compare register 50	CR50	R/W	–	√	–	00H
FF18H	8-bit timer H compare register 00	CMP00	R/W	–	√	–	00H
FF19H	8-bit timer H compare register 10	CMP10	R/W	–	√	–	00H
FF1AH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	00H
FF1BH	8-bit timer H compare register 11	CMP11	R/W	–	√	–	00H
FF1FH	Serial I/O shift register 10	SIO10	R	–	√	–	00H
FF20H	Port function register 1	PF1	R/W	√	√	–	00H
FF21H	Port mode register 1	PM1	R/W	√	√	–	FFH
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FF23H	Port mode register 3	PM3	R/W	√	√	–	FFH
FF24H	Port mode register 4	PM4	R/W	√	√	–	FFH
FF28H	Port mode register 8	PM8	R/W	√	√	–	FFH
FF29H	Port mode register 9	PM9	R/W	√	√	–	FFH
FF2AH	Port mode register 10	PM10	R/W	√	√	–	FFH
FF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH
FF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH
FF2DH	Port mode register 13	PM13	R/W	√	√	–	FFH
FF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH
FF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH
FF30H	Internal high-speed oscillation trimming register	HIOTRM	R/W	–	√	–	10H

Table 3-8. Special Function Register List (2/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF31H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H
FF33H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H
FF34H	Pull-up resistor option register 4	PU4	R/W	√	√	–	00H
FF38H	Pull-up resistor option register 8	PU8	R/W	√	√	–	00H
FF39H	Pull-up resistor option register 9	PU9	R/W	√	√	–	00H
FF3AH	Pull-up resistor option register 10	PU10	R/W	√	√	–	00H
FF3BH	Pull-up resistor option register 11	PU11	R/W	√	√	–	00H
FF3CH	Pull-up resistor option register 12	PU12	R/W	√	√	–	00H
FF3DH	Pull-up resistor option register 13	PU13	R/W	√	√	–	00H
FF3EH	Pull-up resistor option register 14	PU14	R/W	√	√	–	00H
FF3FH	Pull-up resistor option register 15	PU15	R/W	√	√	–	00H
FF40H	Clock output selection register	CKS	R/W	√	√	–	00H
FF41H	8-bit timer compare register 51	CR51	R/W	–	√	–	00H
FF42H	8-bit timer H mode register 2	TMHMD2	R/W	√	√	–	00H
FF43H	8-bit timer mode control register 51	TMC51	R/W	√	√	–	00H
FF44H	8-bit timer H compare register 02	CMP02	R/W	–	√	–	00H
FF45H	8-bit timer H compare register 12	CMP12	R/W	–	√	–	00H
FF48H	External interrupt rising edge enable register	EGP	R/W	√	√	–	00H
FF49H	External interrupt falling edge enable register	EGN	R/W	√	√	–	00H
FF4FH	Input switch control register	ISC	R/W	√	√	–	00H
FF50H	Asynchronous serial interface operation mode register 6	ASIM6	R/W	√	√	–	01H
FF51H	8-bit timer counter 52	TM52	R	–	√	–	00H
FF53H	Asynchronous serial interface reception error status register 6	ASIS6	R	–	√	–	00H
FF55H	Asynchronous serial interface transmission status register 6	ASIF6	R	–	√	–	00H
FF56H	Clock selection register 6	CKSR6	R/W	–	√	–	00H
FF57H	Baud rate generator control register 6	BRGC6	R/W	–	√	–	FFH
FF58H	Asynchronous serial interface control register 6	ASICL6	R/W	√	√	–	16H
FF59H	8-bit timer compare register 52	CR52	R/W	–	√	–	00H
FF5BH	Timer clock selection register 52	TCL52	R/W	√	√	–	00H
FF5CH	8-bit timer mode control register 52	TMC52	R/W	√	√	–	00H
FF69H	8-bit timer H mode register 0	TMHMD0	R/W	√	√	–	00H
FF6AH	Timer clock selection register 50	TCL50	R/W	√	√	–	00H
FF6BH	8-bit timer mode control register 50	TMC50	R/W	√	√	–	00H
FF6CH	8-bit timer H mode register 1	TMHMD1	R/W	√	√	–	00H
FF6DH	8-bit timer H carrier control register 1	TMCYC1	R/W	√	√	–	00H

Table 3-8. Special Function Register List (3/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF6EH	Key return mode register	KRM	R/W	√	√	–	00H
FF6FH	8-bit timer counter 51	TM51	R	–	√	–	00H
FF70H	Asynchronous serial interface operation mode register 0	ASIM0	R/W	√	√	–	01H
FF71H	Baud rate generator control register 0	BRGC0	R/W	–	√	–	1FH
FF72H	Receive buffer register 0	RXB0	R	–	√	–	FFH
FF73H	Asynchronous serial interface reception error status register 0	ASIS0	R	–	√	–	00H
FF74H	Transmit shift register 0	TXS0	W	–	√	–	FFH
FF80H	Serial operation mode register 10	CSIM10	R/W	√	√	–	00H
FF81H	Serial clock selection register 10	CSIC10	R/W	√	√	–	00H
FF84H	Transmit buffer register 10	SOTB10	R/W	–	√	–	00H
FF8CH	Timer clock selection register 51	TCL51	R/W	√	√	–	00H
FF8DH	A/D converter mode register	ADM	R/W	√	√	–	00H
FF8EH	Analog input channel specification register	ADS	R/W	√	√	–	00H
FF8FH	A/D port configuration register 0	ADPC0	R/W	√	√	–	08H
FF90H	Serial operation mode specification register 0	CSIMA0	R/W	√	√	–	00H
FF91H	Serial status register 0	CSIS0	R/W	√	√	–	00H
FF93H	Division value selection register 0	BRGCA0	R/W	–	√	–	03H
FF96H	Serial I/O shift register 0	SIOA0	R/W	–	√	–	00H
FF99H	Watchdog timer enable register	WDTE	R/W	–	√	–	1AH/ 9AH[Note 1]
FF9FH	Clock operation mode select register	OSCCTL	R/W	√	√	–	00H
FFA0H	Internal oscillation mode register	RCM	R/W	√	√	–	80H[Note 2]
FFA1H	Main clock mode register	MCM	R/W	√	√	–	00H
FFA2H	Main OSC control register	MOC	R/W	√	√	–	80H
FFA3H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H
FFA4H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	05H
FFACH	Reset control flag register	RESF	R	–	√	–	00H[Note 3]
FFB0H	LCD mode register	LCDMD	R/W	√	√	–	00H
FFB1H	LCD display mode register	LCDM	R/W	√	√	–	00H
FFB2H	LCD clock control register 0	LCDC0	R/W	√	√	–	00H

Notes 1. The reset value of WDTE is determined by the setting of the option byte.

2. The value of this register is 00H immediately after a reset release but automatically changes to 80H after oscillation accuracy stabilization of high-speed internal oscillator has been waited.

3. The reset value of RESF varies depending on the reset source.

Table 3-8. Special Function Register List (4/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FFB5H	Port function register 2	PF2		R/W	√	√	–	00H
FFB6H	Port function register ALL	PFALL		R/W	√	√	–	00H
FFBAH	16-bit timer mode control register 00	TMC00		R/W	√	√	–	00H
FFBBH	Prescaler mode register 00	PRM00		R/W	√	√	–	00H
FFBCH	Capture/compare control register 00	CRC00		R/W	√	√	–	00H
FFBEH	Low-voltage detection register	LVIM		R/W	√	√	–	00H[Note 1]
FFBFH	Low-voltage detection level selection register	LVIS		R/W	√	√	–	00H[Note 1]
FFE0H	Interrupt request flag register 0L	IF0	IF0L	R/W	√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H	R/W	√	√		00H
FFE2H	Interrupt request flag register 1L	IF1	IF1L	R/W	√	√	√	00H
FFE3H	Interrupt request flag register 1H		IF1H	R/W	√	√		00H
FFE4H	Interrupt mask flag register 0L	MK0	MK0L	R/W	√	√	√	FFH
FFE5H	Interrupt mask flag register 0H		MK0H	R/W	√	√		FFH
FFE6H	Interrupt mask flag register 1L	MK1	MK1L	R/W	√	√	√	FFH
FFE7H	Interrupt mask flag register 1H		MK1H	R/W	√	√		FFH
FFE8H	Priority specification flag register 0L	PR0	PR0L	R/W	√	√	√	FFH
FFE9H	Priority specification flag register 0H		PR0H	R/W	√	√		FFH
FFEAH	Priority specification flag register 1L	PR1	PR1L	R/W	√	√	√	FFH
FFEBH	Priority specification flag register 1H		PR1H	R/W	√	√		FFH
FFF0H	Internal memory size switching register[Note 2]	IMS		R/W	–	√	–	CFH
FFF4H	Internal expansion RAM size switching register[Note 2]	IXS		R/W	–	√	–	0CH
FFFBH	Processor clock control register	PCC		R/W	√	√	–	01H

Notes 1. The reset values of LVIM and LVIS vary depending on the reset source.

2. Regardless of the internal memory capacity, the initial values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) of all products in the 78K0/Lx3-M microcontrollers are fixed (IMS = CFH, IXS = 0CH). Therefore, set the value corresponding to each product as indicated below.

78K0/LE3-M	78K0/LG3-M	IMS	IXS	ROM Capacity	Internal High-Speed RAM Capacity	Internal Expansion RAM Capacity
μPD78F8052	–	04H	0CH	16 KB	768 bytes	–
μPD78F8053	–	C8H		32 KB		
–	μPD78F8054	CCH	0AH	48 KB		1 KB
–	μPD78F8055	CFH		60 KB	1 KB	

3.2.4 Extended special function registers (2nd SFRs)

Unlike a general-purpose register, each extended SFRs (2nd SFRs) has a special function.

2nd SFRs are allocated to the 80H to 1D8H areas.

The extended SFR interface is used to access the extended SFR space (See **CHAPTER 17 EXTENDED SFR INTERFACE**).

Table 3-9 gives a list of the extended SFR. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of an extended SFR.
- R/W
  Indicates whether the corresponding extended special function register can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulatable bit units
  Indicates the manipulatable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For the SFRs, see **3.2.3 Special function registers (SFRs)**.

Table 3-9. Extended SFR (2nd SFR) List (1/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
80H	Extended SFR interrupt request flag register 20	IF20		R/W	–	–	–	00H
81H	Extended SFR interrupt request flag register 21	IF21		R/W	–	–	–	00H
82H	Extended SFR interrupt request flag register 22	IF22		R/W	–	–	–	00H
83H	Extended SFR interrupt request flag register 23	IF23		R/W	–	–	–	00H
84H	Extended SFR interrupt mask flag register 20	MK20		R/W	–	–	–	FFH
85H	Extended SFR interrupt mask flag register 21	MK21		R/W	–	–	–	FFH
86H	Extended SFR interrupt mask flag register 22	MK22		R/W	–	–	–	FFH
87H	Extended SFR interrupt mask flag register 23	MK23		R/W	–	–	–	FFH
88H	Pull-down status control register	PUTCTL		R/W	–	–	–	00H
8BH	Port register LP0	LP0		R/W	–	–	–	00H
8CH	Port mode register LP0	LPM0		R/W	–	–	–	FFH
8DH	Pull-up resistor option register LP0	LPU0		R/W	–	–	–	00H
8EH	Port register LP1	LP1		R/W	–	–	–	00H
8FH	Port mode register LP1	LPM1		R/W	–	–	–	FFH
90H	Pull-up resistor option register LP1	LPU1		R/W	–	–	–	00H
91H	Port function control register	PORTCTL		R/W	–	–	–	00H
92H	Real-time counter control register 2	RTCC2		R/W	–	–	–	00H
93H	Alarm minute register	ALARMWM		R/W	–	–	–	00H
94H	Alarm hour register	ALARMWH		R/W	–	–	–	12H
95H	Alarm week register	ALARMWW		R/W	–	–	–	00H
96H	Real-time counter control register 0	RTCC0		R/W	–	–	–	00H
97H	Real-time counter control register 1	RTCC1		R/W	–	–	–	00H
98H	Sub-count register	RSUBC	RSUBCL	R	–	–	–	00H
99H			RSUBCH	R	–	–	–	00H
9AH	Second count register	SEC		R/W	–	–	–	00H
9BH	Minute count register	MIN		R/W	–	–	–	00H
9CH	Hour count register	HOUR		R/W	–	–	–	12H
9DH	Week count register	WEEK		R/W	–	–	–	00H
9EH	Day count register	DAY		R/W	–	–	–	01H
9FH	Month count register	MONTH		R/W	–	–	–	01H
A0H	Year count register	YEAR		R/W	–	–	–	00H
A1H	Watch error correction register	SUBCUD		R/W	–	–	–	00H
A3H	24-bit ΔΣ-type A/D converter mode register	ADM2		R/W	–	–	–	00H
A4H	A/D clock delay setting register	ADLY		R/W	–	–	–	00H
A5H	HPF control register 0	HPFC0		R/W	–	–	–	00H
A6H	HPF control register 1	HPFC1		R/W	–	–	–	00H
A7H	24-bit ΔΣ-type A/D conversion result register 0	ADCR0	ADCR0L	R	–	–	–	00H
A8H			ADCR0M	R	–	–	–	00H
A9H			ADCR0H	R	–	–	–	00H
AAH	24-bit ΔΣ-type A/D conversion result register 1	ADCR1	ADCR1L	R	–	–	–	00H
ABH			ADCR1M	R	–	–	–	00H
ACH			ADCR1H	R	–	–	–	00H

Remark The 80H to 1D8H registers are accessed by using the extended SFR interface.

Table 3-9. Extended SFR (2nd SFR) List (2/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
ADH	24-bit ΔΣ-type A/D conversion result register 2	ADCR2	ADCR2L	R	–	–	–	00H
AEH			ADCR2M	R	–	–	–	00H
AFH			ADCR2H	R	–	–	–	00H
B0H	24-bit ΔΣ-type A/D conversion result register 3	ADCR3	ADCR3L	R	–	–	–	00H
B1H			ADCR3M	R	–	–	–	00H
B2H			ADCR3H	R	–	–	–	00H
B3H	Phase control registers 0	PHC0	PHC0L	R/W	–	–	–	00H
B4H			PHC0H	R/W	–	–	–	00H
B5H	Phase control registers 1	PHC1	PHC1L	R/W	–	–	–	00H
B6H			PHC1H	R/W	–	–	–	00H
CBH	Real-time counter mode register	RTCMD		R/W	–	–	–	00H
100H	Period and frequency measurement result register	PFVAL	PFVALL	R	–	–	–	00H
101H			PFVALH	R	–	–	–	00H
102H	Zero-crossing timeout specification register for voltage channel 1	ZXTOUT1	ZXTOUT1L	R/W	–	–	–	FFH
103H			ZXTOUT1H	R/W	–	–	–	03H
104H	Zero-crossing timeout specification register for voltage channel 2	ZXTOUT2	ZXTOUT2L	R/W	–	–	–	FFH
105H			ZXTOUT2H	R/W	–	–	–	03H
106H	SAG line cycle number specification register for voltage channel 1	SAGNUM1		R/W	–	–	–	FFH
107H	SAG level specification register for voltage channel 1	SAGVAL1	SAGVAL1L	R/W	–	–	–	00H
108H			SAGVAL1M	R/W	–	–	–	00H
109H			SAGVAL1H	R/W	–	–	–	00H
10AH	SAG line cycle number specification register for voltage channel 2	SAGNUM2		R/W	–	–	–	FFH
10BH	SAG level specification register for voltage channel 2	SAGVAL2	SAGVAL2L	R/W	–	–	–	00H
10CH			SAGVAL2M	R/W	–	–	–	00H
10DH			SAGVAL2H	R/W	–	–	–	00H
10EH	Peak current level specification register	IPKLMT	IPKLMTL	R/W	–	–	–	FFH
10FH			IPKLMTM	R/W	–	–	–	FFH
110H	Peak voltage level specification register	VPKLMT	VPKLMTL	R/W	–	–	–	FFH
111H			VPKLMTM	R/W	–	–	–	FFH
112H	Peak current value register	IMAX	IMAXL	R	–	–	–	00H
113H			IMAXM	R	–	–	–	00H
114H			IMAXH	R	–	–	–	00H
116H	Peak current value clearing register	RSTIMAX	RSTIMAXL	R	–	–	–	00H
117H			RSTIMAXM	R	–	–	–	00H
118H			RSTIMAXH	R	–	–	–	00H
119H	Peak voltage value register	VMAX	VMAXL	R	–	–	–	00H
11AH			VMAXM	R	–	–	–	00H
11BH			VMAXH	R	–	–	–	00H
11DH	Peak voltage value clearing register	RSTVMAX	RSTVMAXL	R	–	–	–	00H
11EH			RSTVMAXM	R	–	–	–	00H
11FH			RSTVMAXH	R	–	–	–	00H

Remark The 80H to 1D8H registers are accessed by using the extended SFR interface.

Table 3-9. Extended SFR (2nd SFR) List (3/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
120H	Gain specification register	IMATGAIN	IMATGAINL	R/W	–	–	–	00H
121H			IMATGAINH	R/W	–	–	–	00H
122H	Fault detection control register	PQMCTL		R/W	–	–	–	00H
123H	Fault detection threshold value specification register	IST		R/W	–	–	–	8BH
124H	Fault control register	ICHK		R/W	–	–	–	84H
150H	Frequency conversion control register	CFCTL		R/W	–	–	–	02H
151H	Frequency scaling specification register	CFMUL	CFMULL	R/W	–	–	–	FFH
152H			CFMULH	R/W	–	–	–	FFH
153H	Pulse width specification register	PULCTL		R/W	–	–	–	00H
180H	Power calculation mode control register 1	PWCTL1		R/W	–	–	–	00H
181H	Power calculation mode control register 2	PWCTL2		R/W	–	–	–	00H
182H	No-load level control register	NLCTL		R/W	–	–	–	00H
183H	Active power scaling specification register	ACTDIV		R/W	–	–	–	00H
184H	Reactive power scaling specification register	READIV		R/W	–	–	–	00H
185H	Apparent power scaling specification register	APPDIV		R/W	–	–	–	00H
186H	RMS register for voltage channel 1	V1RMS	V1RMSL	R	–	–	–	00H
187H			V1RMSM	R	–	–	–	00H
188H			V1RMSH	R	–	–	–	00H
189H	RMS register for voltage channel 2	V2RMS	V2RMSL	R	–	–	–	00H
18AH			V2RMSM	R	–	–	–	00H
18BH			V2RMSH	R	–	–	–	00H
18CH	RMS register for current channel 1	I1RMS	I1RMSL	R	–	–	–	00H
18DH			I1RMSM	R	–	–	–	00H
18EH			I1RMSH	R	–	–	–	00H
18FH	RMS register for current channel 2	I2RMS	I2RMSL	R	–	–	–	00H
190H			I2RMSM	R	–	–	–	00H
191H			I2RMSH	R	–	–	–	00H
192H	Active power accumulation reading register	ACTHR	ACTHRL	R	–	–	–	00H
193H			ACTHRM	R	–	–	–	00H
194H			ACTHRH	R	–	–	–	00H
196H	Active power accumulation reading and resetting register	RACTHR	RACTHRL	R	–	–	–	00H
197H			RACTHRM	R	–	–	–	00H
198H			RACTHRH	R	–	–	–	00H
199H	Active power accumulation synchronous reading register	LACTHR	LACTHRL	R	–	–	–	00H
19AH			LACTHRM	R	–	–	–	00H
19BH			LACTHRH	R	–	–	–	00H
19CH	Reactive power accumulation reading register	REAHR	REAHRL	R	–	–	–	00H
19DH			REAHRM	R	–	–	–	00H
19EH			REAHRH	R	–	–	–	00H

Remark The 80H to 1D8H registers are accessed by using the extended SFR interface.

Table 3-9. Extended SFR (2nd SFR) List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
1A0H	Reactive power accumulation reading and resetting register	RREAHR	RREAHRL	R	–	–	–	00H
1A1H			RREAHRM	R	–	–	–	00H
1A2H			RREAHRH	R	–	–	–	00H
1A3H	Reactive power accumulation synchronous reading register	LREAHR	LREAHRL	R	–	–	–	00H
1A4H			LREAHRM	R	–	–	–	00H
1A5H			LREAHRH	R	–	–	–	00H
1A6H	Apparent power accumulation reading register	APPHR	APPHRL	R	–	–	–	00H
1A7H			APPHRM	R	–	–	–	00H
1A8H			APPHRH	R	–	–	–	00H
1AAH	Apparent power accumulation reading and resetting register	RAPPHR	RAPPHRL	R	–	–	–	00H
1ABH			RAPPHRM	R	–	–	–	00H
1ACH			RAPPHRH	R	–	–	–	00H
1ADH	Apparent power accumulation synchronous reading register	LAPPHR	LAPPHRL	R	–	–	–	00H
1AEH			LAPPHRM	R	–	–	–	00H
1AFH			LAPPHRH	R	–	–	–	00H
1B0H	Line cycle number specification register	LINNUM	LINNUML	R/W	–	–	–	FFH
1B1H			LINNUMH	R	–	–	–	FFH
1B2H	Active power gain specification register 1	ACT1GAIN	ACT1GAINL	R/W	–	–	–	00H
1B3H			ACT1GAINH	R/W	–	–	–	00H
1B4H	Active power gain specification register 2	ACT2GAIN	ACT2GAINL	R/W	–	–	–	00H
1B5H			ACT2GAINH	R/W	–	–	–	00H
1B6H	Reactive power gain specification register 1	REA1GAIN	REA1GAINL	R/W	–	–	–	00H
1B7H			REA1GAINH	R/W	–	–	–	00H
1B8H	Reactive power gain specification register 2	REA2GAIN	REA2GAINL	R/W	–	–	–	00H
1B9H			REA2GAINH	R/W	–	–	–	00H
1BAH	Apparent power gain specification register 1	APP1GAIN	APP1GAINL	R/W	–	–	–	00H
1BBH			APP1GAINH	R/W	–	–	–	00H
1BCH	Apparent power gain specification register 2	APP2GAIN	APP2GAINL	R/W	–	–	–	00H
1BDH			APP2GAINH	R/W	–	–	–	00H
1BEH	RMS gain specification register for current channel 1	IRMS1GAIN	IRMS1GAINL	R/W	–	–	–	00H
1BFH			IRMS1GAINH	R/W	–	–	–	00H
1C0H	RMS gain specification register for current channel 2	IRMS2GAIN	IRMS2GAINL	R/W	–	–	–	00H
1C1H			IRMS2GAINH	R/W	–	–	–	00H
1C2H	Active power offset specification register 1	ACT1OS	ACT1OSL	R/W	–	–	–	00H
1C3H			ACT1OSH	R	–	–	–	00H
1C4H	Active power offset specification register 2	ACT2OS	ACT2OSL	R/W	–	–	–	00H
1C5H			ACT2OSH	R	–	–	–	00H
1C6H	Reactive power offset specification register 1	REA1OS	REA1OSL	R/W	–	–	–	00H
1C7H			REA1OSH	R	–	–	–	00H
1C8H	Reactive power offset specification register 2	REA2OS	REA2OSL	R/W	–	–	–	00H
1C9H			REA2OSH	R	–	–	–	00H

Remark The 80H to 1D8H registers are accessed by using the extended SFR interface.

Table 3-9. Extended SFR (2nd SFR) List (5/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
1CAH	RMS offset specification register for current channel 1	I1RMSOS	I1RMSOSL	R/W	–	–	–	00H
1CBH			I1RMSOSH	R/W	–	–	–	00H
1CCH	RMS offset specification register for voltage channel 1	V1RMSOS	V1RMSOSL	R/W	–	–	–	00H
1CDH			V1RMSOSH	R/W	–	–	–	00H
1CEH	RMS offset specification register for current channel 2	I2RMSOS	I2RMSOSL	R/W	–	–	–	00H
1CFH			I2RMSOSH	R/W	–	–	–	00H
1D0H	RMS offset specification register for voltage channel 2	V2RMSOS	V2RMSOSL	R/W	–	–	–	00H
1D1H			V2RMSOSH	R/W	–	–	–	00H
1D2H	Sampling mode selection register	SAMPMODE		R/W	–	–	–	00H
1D3H	Sampling result register 1	SAMP1	SAMP1L	R	–	–	–	00H
1D4H			SAMP1M	R	–	–	–	00H
1D5H			SAMP1H	R	–	–	–	00H
1D6H	Sampling result register 2	SAMP2	SAMP2L	R	–	–	–	00H
1D7H			SAMP2M	R	–	–	–	00H
1D8H			SAMP2H	R	–	–	–	00H

Remark The 80H to 1D8H registers are accessed by using the extended SFR interface.

3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC), and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

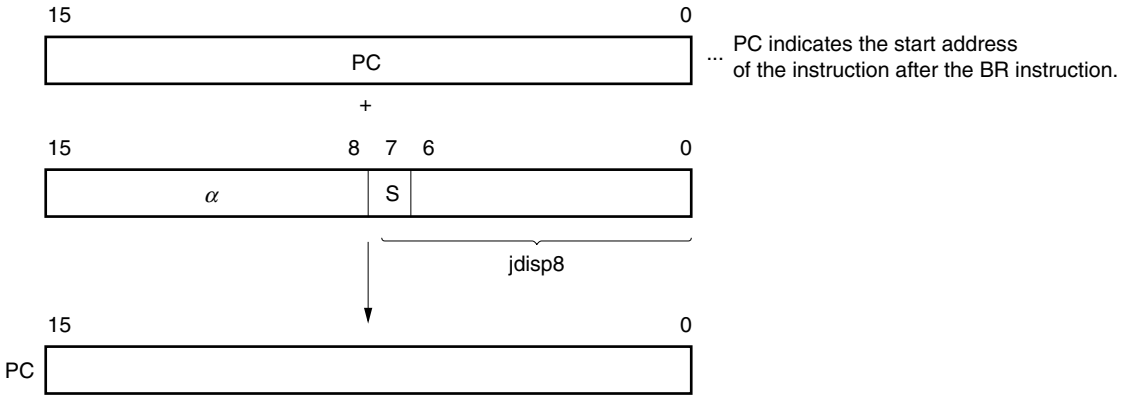
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

3.3.2 Immediate addressing

[Function]

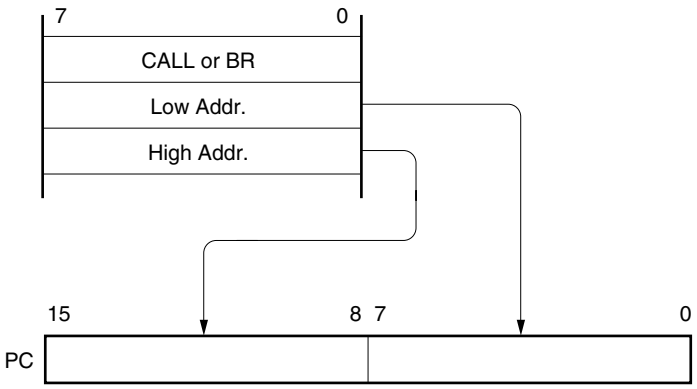
Immediate data in the instruction word is transferred to the program counter (PC) and branched.

This function is carried out when the CALL !addr16 or BR !addr16 or CALLF !addr11 instruction is executed.

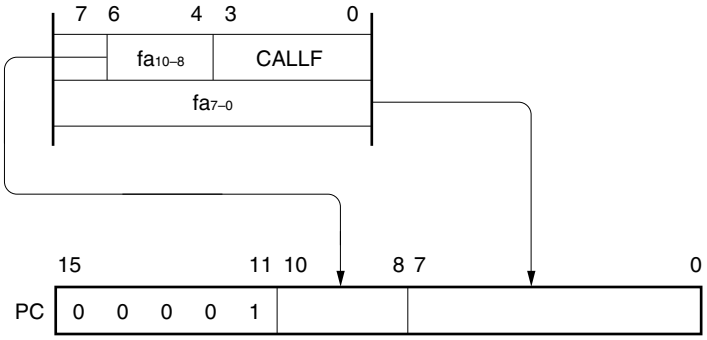
CALL !addr16 and BR !addr16 instructions can be branched to the entire memory space. The CALLF !addr11 instruction is branched to the 0800H to 0FFFH area.

[Illustration]

In the case of CALL !addr16 and BR !addr16 instructions



In the case of CALLF !addr11 instruction



3.3.3 Table indirect addressing

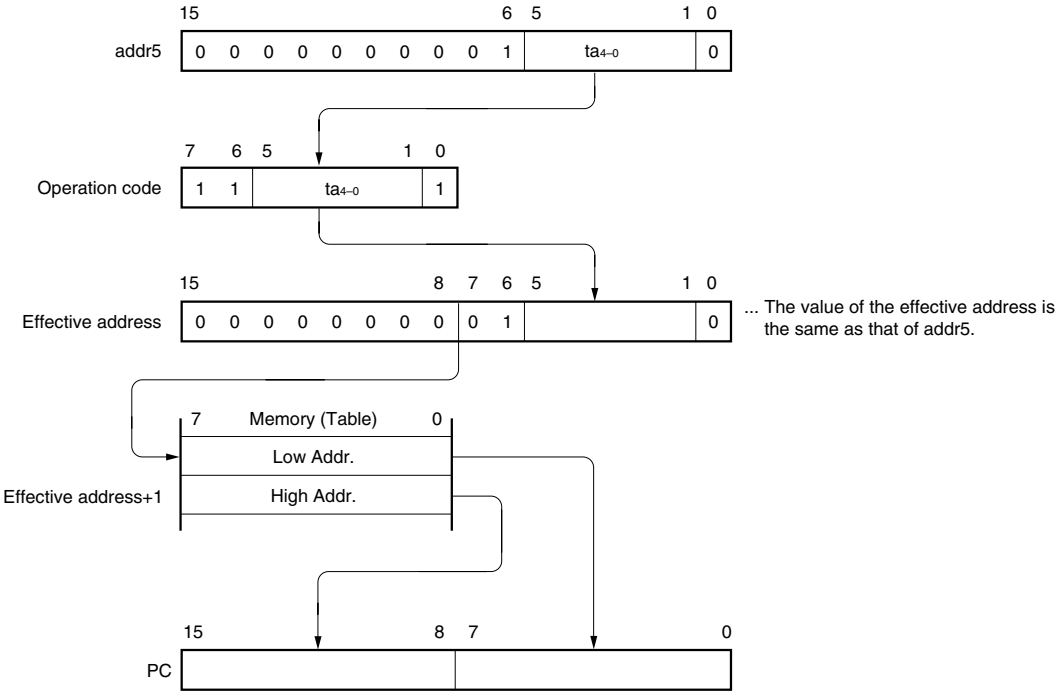
[Function]

Table contents (branch destination address) of the particular location to be addressed by bits 1 to 5 of the immediate data of an operation code are transferred to the program counter (PC) and branched.

This function is carried out when the CALLT [addr5] instruction is executed.

This instruction references the address stored in the memory table from 40H to 7FH, and allows branching to the entire memory space.

[Illustration]



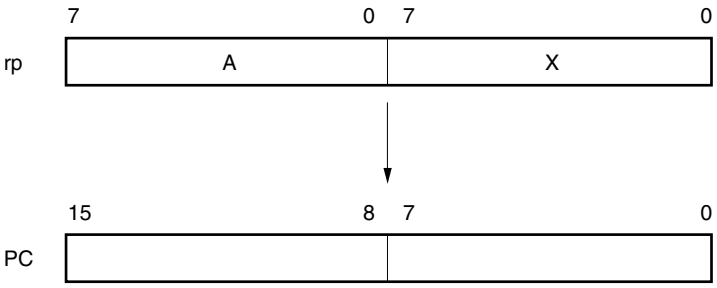
3.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



3.4 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) to undergo manipulation during instruction execution.

3.4.1 Implied addressing

[Function]

The register that functions as an accumulator (A and AX) among the general-purpose registers is automatically (implicitly) addressed.

Of the 78K0/Lx3-M microcontroller instruction words, the following instructions employ implied addressing.

Instruction	Register to Be Specified by Implied Addressing
MULU	A register for multiplicand and AX register for product storage
DIVUW	AX register for dividend and quotient storage
ADJBA/ADJBS	A register for storage of numeric values that become decimal correction targets
ROR4/ROL4	A register for storage of digit data that undergoes digit rotation

[Operand format]

Because implied addressing can be automatically determined with an instruction, no particular operand format is necessary.

[Description example]

In the case of MULU X

With an 8-bit × 8-bit multiply instruction, the product of the A register and X register is stored in AX. In this example, the A and AX registers are specified by implied addressing.

3.4.2 Register addressing

[Function]

The general-purpose register to be specified is accessed as an operand with the register bank select flags (RBS0 to RBS1) and the register specify codes of an operation code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

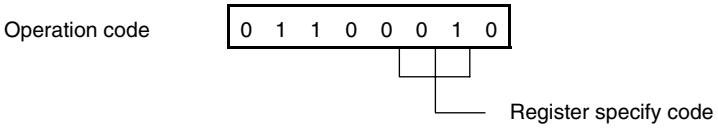
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

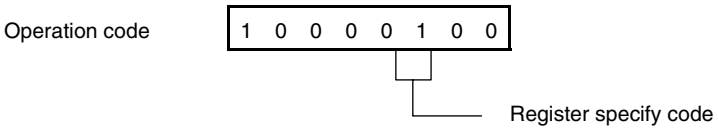
'r' and 'rp' can be described by absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp



3.4.3 Direct addressing

[Function]

The memory to be manipulated is directly addressed with immediate data in an instruction word becoming an operand address.

[Operand format]

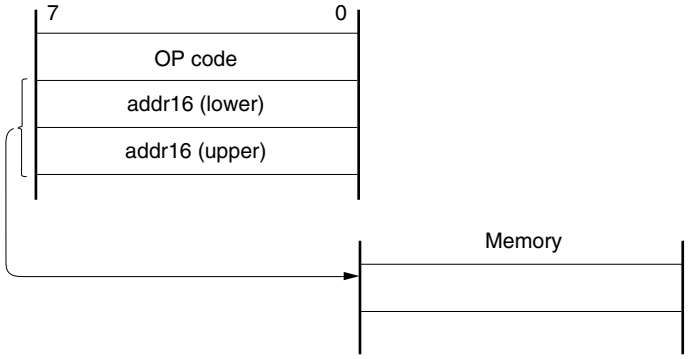
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !0FE00H; when setting !addr16 to FE00H

Operation code	1 0 0 0 1 1 1 0	OP code
	0 0 0 0 0 0 0 0	00H
	1 1 1 1 1 1 1 0	FEH

[Illustration]



3.4.4 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

This addressing is applied to the 256-byte space FE20H to FF1FH. Internal high-speed RAM and special function registers (SFRs) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the overall SFR area. Ports that are frequently accessed in a program and compare and capture registers of the timer/event counter are mapped in this area, allowing SFRs to be manipulated with a small number of bytes and clocks.

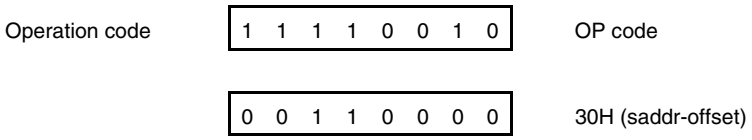
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. See the **[Illustration]** shown below.

[Operand format]

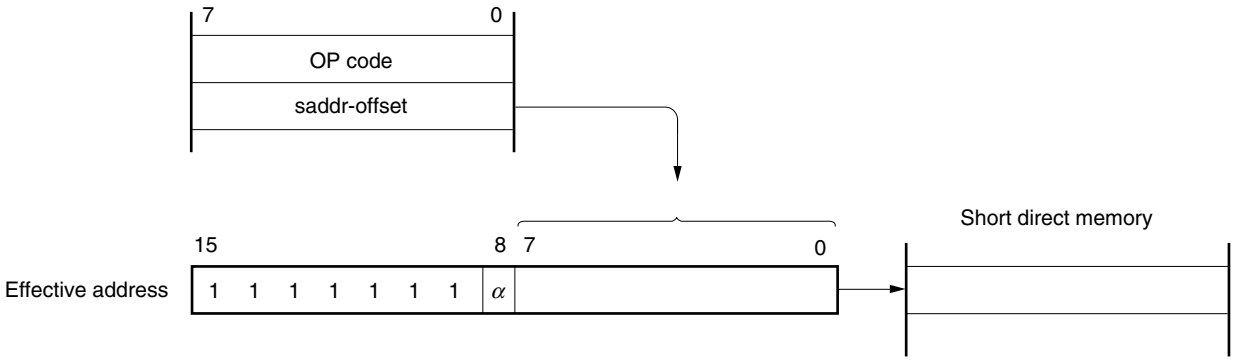
Identifier	Description
saddr	Immediate data that indicate label or FE20H to FF1FH
saddrp	Immediate data that indicate label or FE20H to FF1FH (even address only)

[Description example]

MOV 0FE30H, A ; When transferring the value of A register to the saddr (FE30H)



[Illustration]



When 8-bit immediate data is 20H to FFH, $\alpha = 0$

When 8-bit immediate data is 00H to 1FH, $\alpha = 1$

3.4.5 Special function register (SFR) addressing

[Function]

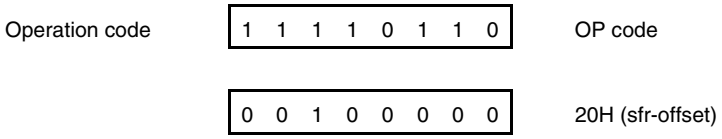
A memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word. This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

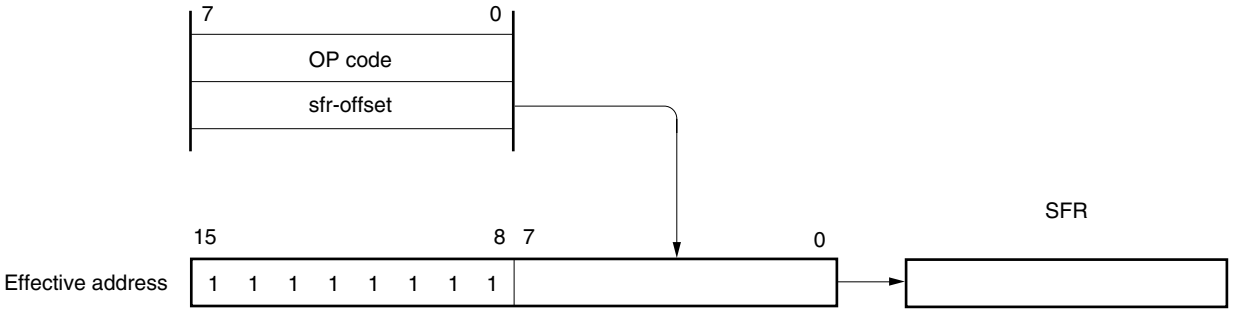
Identifier	Description
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

[Description example]

MOV PM0, A; when selecting PM0 (FF20H) as sfr



[Illustration]



3.4.6 Register indirect addressing

[Function]

Register pair contents specified by a register pair specify code in an instruction word and by a register bank select flag (RBS0 and RBS1) serve as an operand address for addressing the memory. This addressing can be carried out for all of the memory spaces.

[Operand format]

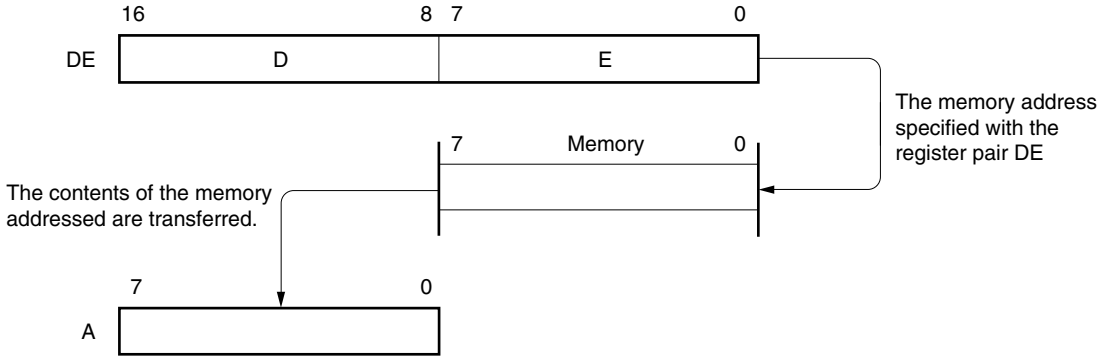
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; when selecting [DE] as register pair

Operation code	1	0	0	0	0	1	0	1

[Illustration]



3.4.7 Based addressing

[Function]

8-bit immediate data is added as offset data to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all of the memory spaces.

[Operand format]

Identifier	Description
–	[HL + byte]

[Description example]

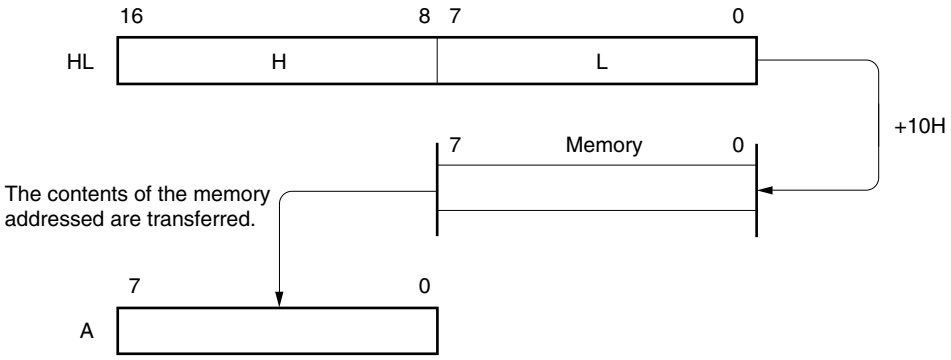
MOV A, [HL + 10H]; when setting byte to 10H

Operation code

1	0	1	0	1	1	1	0

0	0	0	1	0	0	0	0

[Illustration]



3.4.8 Based indexed addressing

[Function]

The B or C register contents specified in an instruction word are added to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the B or C register contents as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all of the memory spaces.

[Operand format]

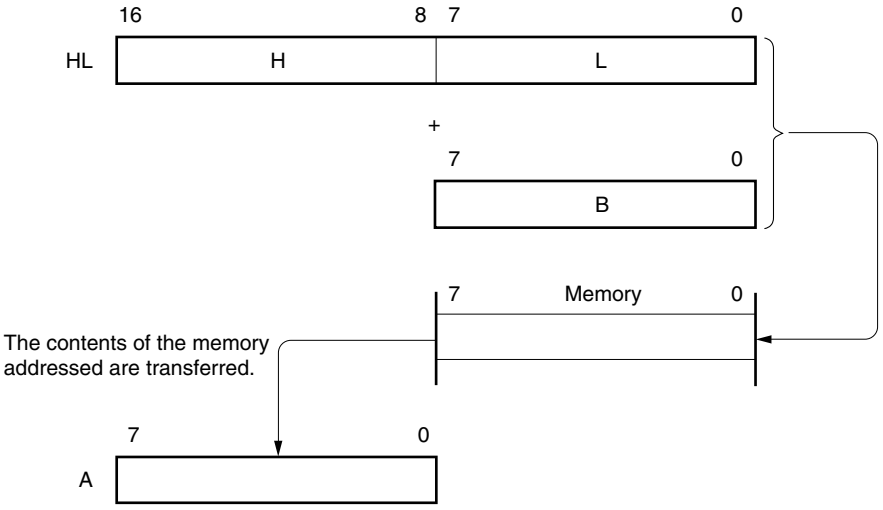
Identifier	Description
–	[HL + B], [HL + C]

[Description example]

MOV A, [HL +B]; when selecting B register

Operation code	1	0	1	0	1	0	1	1

[Illustration]



3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and return instructions are executed or the register is saved/reset upon generation of an interrupt request.

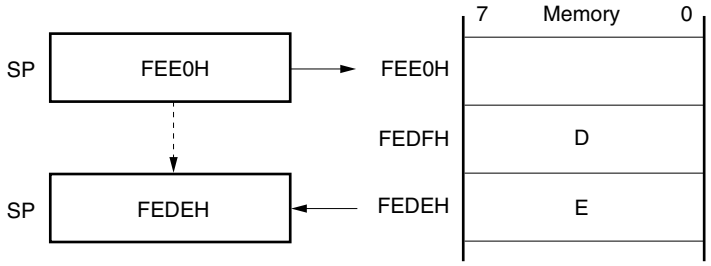
With stack addressing, only the internal high-speed RAM area can be accessed.

[Description example]

PUSH DE; when saving DE register

Operation code	1	0	1	1	0	1	0	1

[Illustration]



CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are three types of pin I/O buffer power supplies: AV_{REF}, LV_{DD}, and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 4-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
LV_{DD}	LP00 to LP05, LP10 to LP15
V_{DD}	Port pins other than above

78K0/Lx3-M microcontroller products are provided with the digital I/O ports, which enable variety of control operations. The functions of each port are shown in Table 4-2 and Table 4-3.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

4.1.1 78K0/LE3-M

Table 4-2. Port Functions (78K0/LE3-M)

Function Name	I/O	Function	After Reset	Alternate Function
P11	I/O	Port 1. 2-bit I/O port and 1 bit output port. Only for P11 and P12, Input/output can be specified in 1-bit units and Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$
P12				SI10/RxD0
P13	Output		Output port	SO10/TxD0/IROUT
P27	I/O	Port 2. 1-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI7
P30	I/O	Port 3. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP5
P32				TOH0
P33				TI000/BUZ/INTP2
P40	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P41				KR1
P80 to P83	I/O	Port 8. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4 to SEG7
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG8 to SEG11
P100 to P103	I/O	Port 10. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG12 to SEG15
P110, P111	I/O	Port 11. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG16, SEG17
P112				SEG18/TxD6
P113				SEG19/RxD6
P120	I/O	Port 12. 1-bit I/O port and 2-bit input port. Only for P120, Input/output can be specified in 1-bit units and use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P130 to P133	I/O	Port 13. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG20 to SEG23

4.1.2 78K0/LG3-M

Table 4-3. Port Functions (78K0/LG3-M) (1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P11	I/O	Port 1. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$
P12				SI10/RxD0
P13				SO10/TxD0
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG39/ANI0
P21				SEG38/ANI1
P22				SEG37/ANI2
P23				SEG36/ANI3
P24				SEG35/ANI4
P25				SEG34/ANI5
P26				SEG33/ANI6
P27				SEG32/ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP5
P31				TOH1/INTP3
P32				TOH0
P33				TI000/BUZ/INTP2
P40	I/O	Port 4. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P41				KR1
P42				KR2
P43				TO51/TI51/KR3
P44				TO50/TI50/KR4
P45				KR5
P80 to P83	I/O	Port 8. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4 to SEG7
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG8 to SEG11
P100 to P103	I/O	Port 10. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG12 to SEG15
P110, P111	I/O	Port 11. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG16, SEG17
P112				SEG18/TxD6
P113				SEG19/RxD6

Table 4-3. Port Functions (78K0/LG3-M) (2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P120	I/O	Port 12. 1-bit I/O port and 3-bit input port. Only for P120, Input/output can be specified in 1-bit units and use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P123				–
P130 to P133	I/O	Port 13. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG20 to SEG23
P140	I/O	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG24 (KS0)
P141				SEG25 (KS1)
P142				SEG26 (KS2)
P143				SEG27 (KS3)
P150	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG28 (KS4)
P151				SEG29 (KS5)
P152				SEG30 (KS6)
P153				SEG31 (KS7)
LP00	I/O	Port LP0. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Output port	–
LP01				ZX1
LP02				ZX2
LP03				–
LP04				–
LP05				–
LP10	I/O	Port LP1. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Output port	–
LP11				–
LP12				–
LP13				–
LP14				–
LP15				–

4.2 Port Configuration

Ports include the following hardware.

Table 4-4. Port Configuration

Item	Configuration
Control registers	• 78K0/LE3-M Port mode register (PMxx): PM1 to PM4, PM8 to PM13 Port register (Pxx): P1 to P4, P8 to P13 Pull-up resistor option register (PUxx): PU1, PU3, PU4, PU8 to PU13 Port function register 1 (PF1) Port function register ALL (PFALL) A/D port configuration register 0 (ADPC0) • 78K0/LG3-M Port mode register (PMxx, LPMx): PM1 to PM4, PM8 to PM15, LPM0, LPM1 Port register (Pxx, LPx): P1 to P4, P8 to P15, LP0, LP1 Pull-up resistor option register (PUxx, LPUx): PU1, PU3, PU4, PU8 to PU15, LPU0, LPU1 Port function register 1 (PF1) Port function register 2 (PF2) Port function register ALL (PFALL) A/D port configuration register 0 (ADPC0)
Port	• 78K0/LE3-M: Total: 32 (CMOS I/O: 29, CMOS input: 2, CMOS output: 1) • 78K0/LG3-M: Total: 65 (CMOS I/O: 62, CMOS input: 3)
Pull-up resistor	• 78K0/LE3-M: Total: 29 • 78K0/LG3-M: Total: 54

4.2.1 Port 1

78K0/LE3-M	78K0/LG3-M
P11/$\overline{\text{SCK10}}$	P11/$\overline{\text{SCK10}}$
P12/SI10/RxD0	P12/SI10/RxD0
P13/SO10/TxD0/IROUT	P13/SO10/TxD0

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P11 to P13 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

This port can also be used for serial interface data I/O, clock I/O, and IR output.

P13 can be selected to function as pin, using port function register 1 (PF1) (see Figure 4-32).

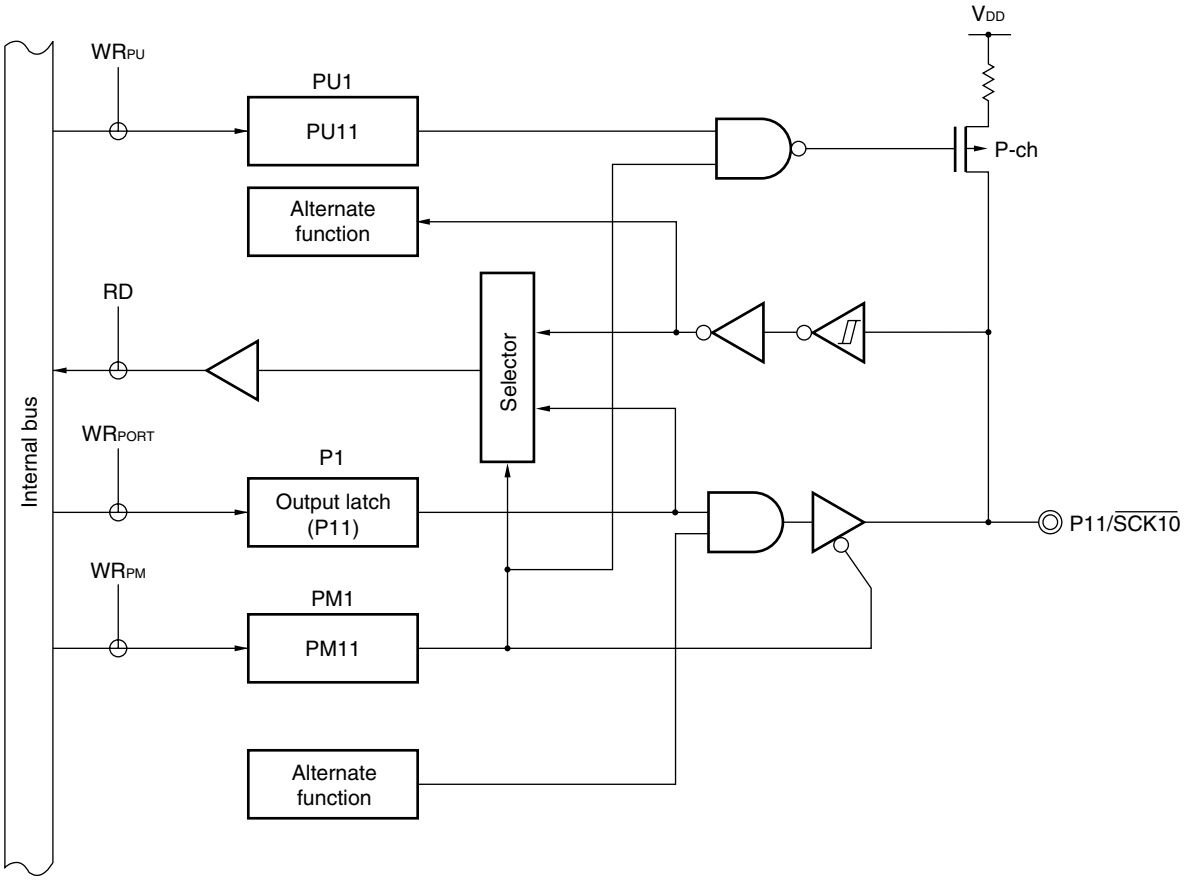
Reset signal generation sets port 1 to input mode[Note].

Figure 4-1 to Figure 4-3 show block diagrams of port 1.

Note Only P13/SO10/TxD0/IROUT pin of 78K0/LE3-M is set to output mode.

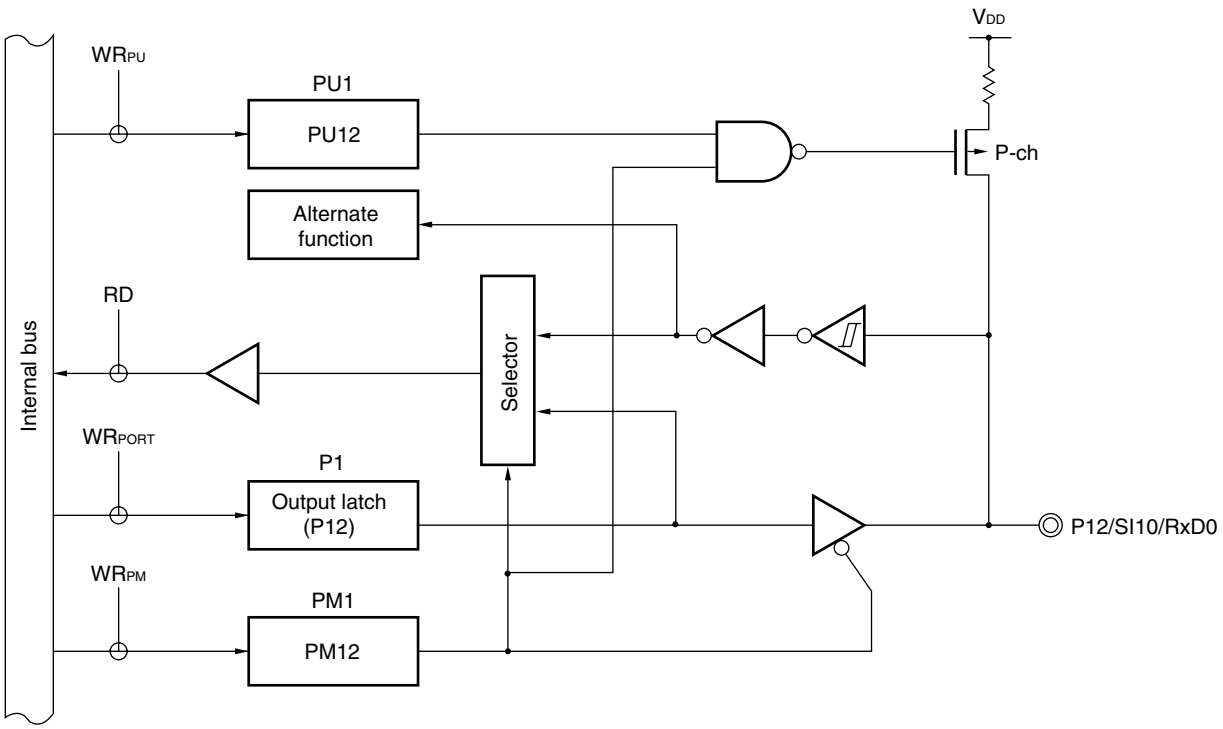
Caution To use P11/$\overline{\text{SCK10}}$, P12/SI10, and P13/SO10 as general-purpose ports, set serial operation mode register 10 (CSIM10) and serial clock selection register 10 (CSIC10) to the default status (00H).

Figure 4-1. Block Diagram of P11



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

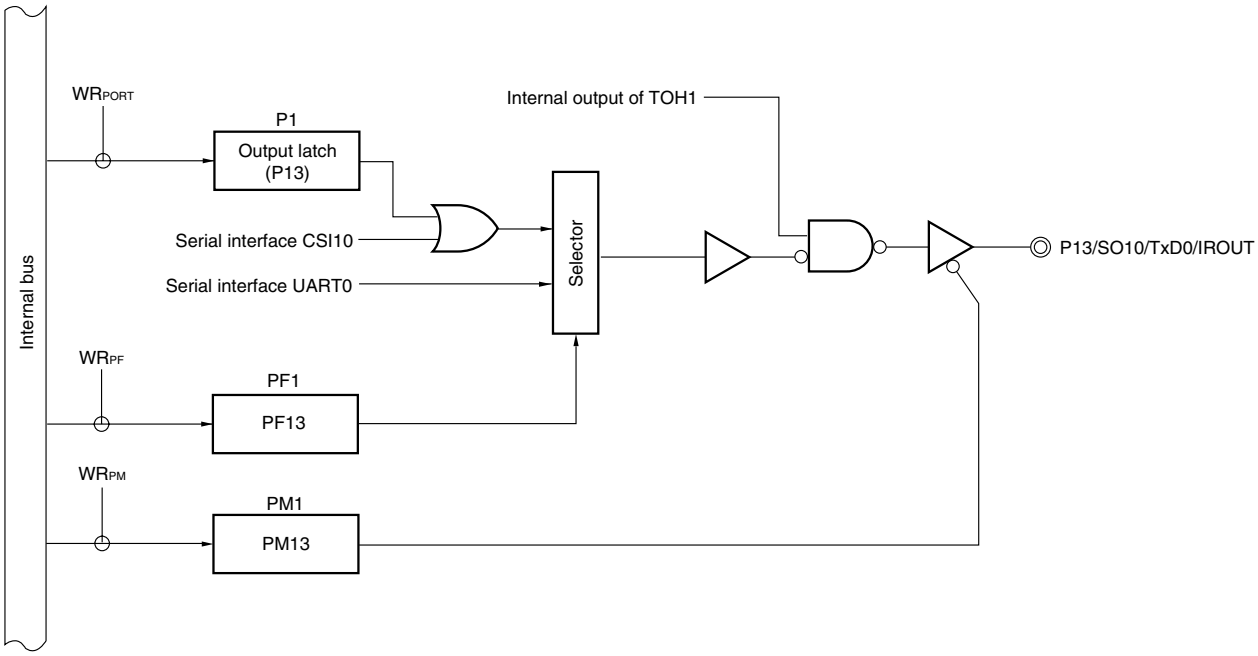
Figure 4-2. Block Diagram of P12



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 4-3. Block Diagram of P13 (1/2)

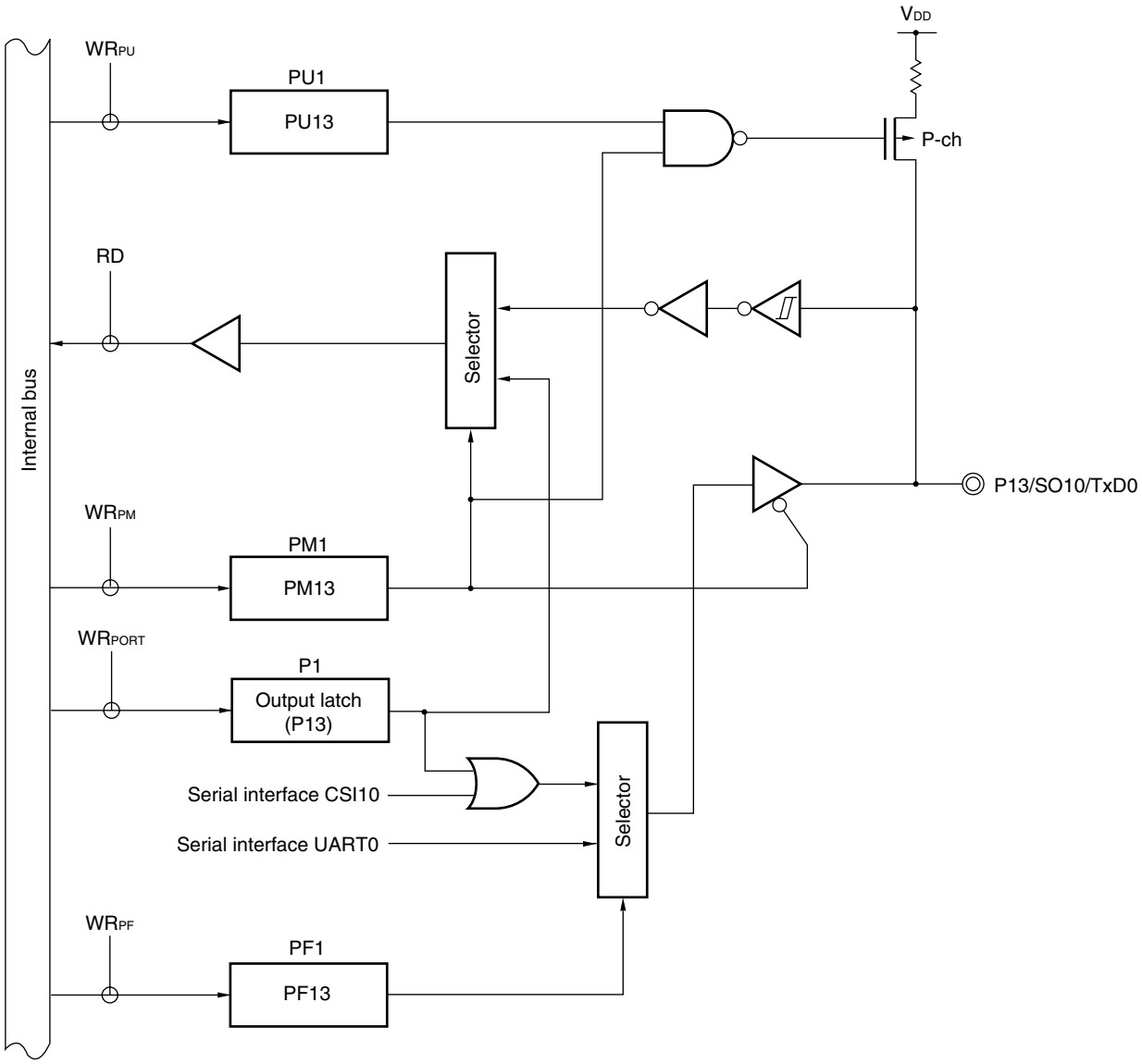
(1) 78K0/LE3-M



P1: Port register 1
PM1: Port mode register 1
PF1: Port function register 1
RD: Read signal
WR××: Write signal

Figure 4-3. Block Diagram of P13 (2/2)

(2) 78K0/LG3-M



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
PF1: Port function register 1
RD: Read signal
WR××: Write signal

4.2.2 Port 2

78K0/LE3-M	78K0/LG3-M
–	P20/SEG39/ANI0
–	P21/SEG38/ANI1
–	P22/SEG37/ANI2
–	P23/SEG36/ANI3
–	P24/SEG35/ANI4
–	P25/SEG34/ANI5
–	P26/SEG33/ANI6
P27/ANI7	P27/SEG32/ANI7

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for segment signal output of the LCD controller/driver and 10-bit successive approximation type A/D converter analog input.

In the 78K0/LG3-M, either I/O port function or segment signal output function can be selected using port function register 2 (PF2).

To use P20 to P27 as digital input pins, set them to port function (other than segment output) by using the port function register 2 (PF2), to digital I/O by using ADPC0, and to input mode by using PM2. Use these pins starting from the lower bit.

P20 to P27 as digital output pins, set them to port function (other than segment output) by using the port function register 2 (PF2), to digital I/O by using ADPC0, and to output mode by using PM2. Use these pins starting from the lower bit.

Reset signal generation sets port 1 to input mode.

Figure 4-4 and Figure 4-5 show block diagrams of port 2.

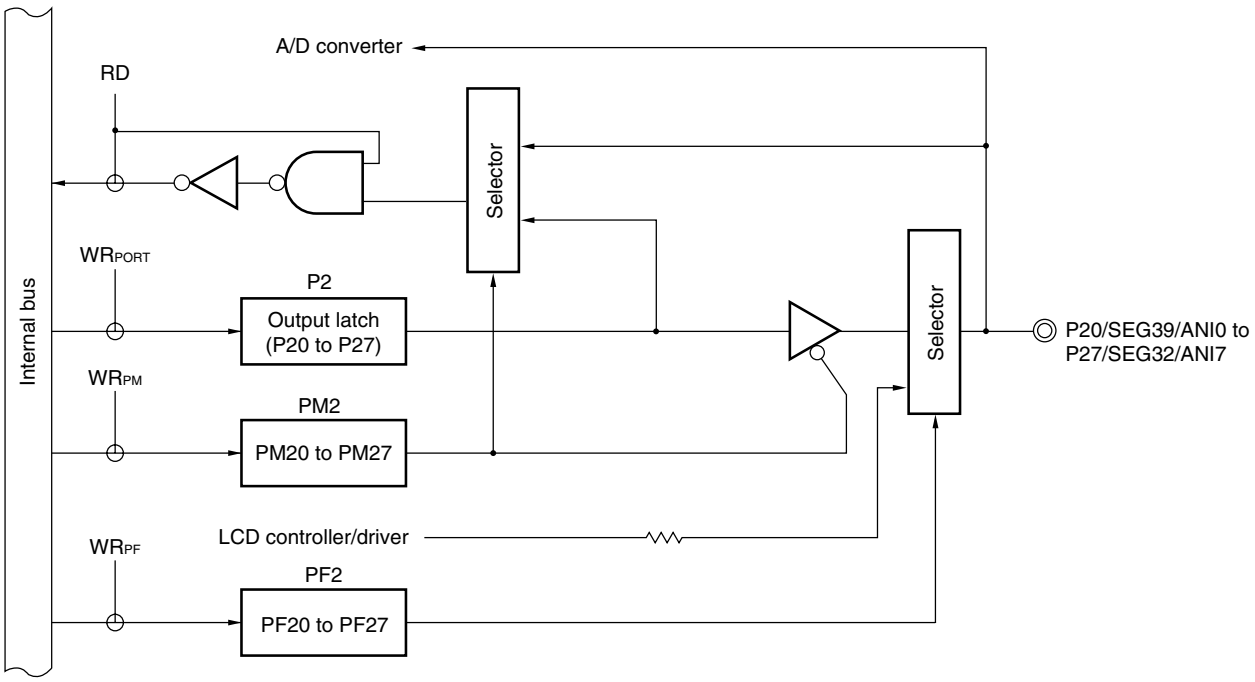
Caution Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

Table 4-5. Setting Functions of P20/SEG39/ANI0 to P27/SEG32/ANI7 Pins

PF2 Note	ADPC0	PM2	ADS	P20/SEG39/ANI0 to P27/SEG32/ANI7 Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output selection Note	–	–	–	Segment output Note

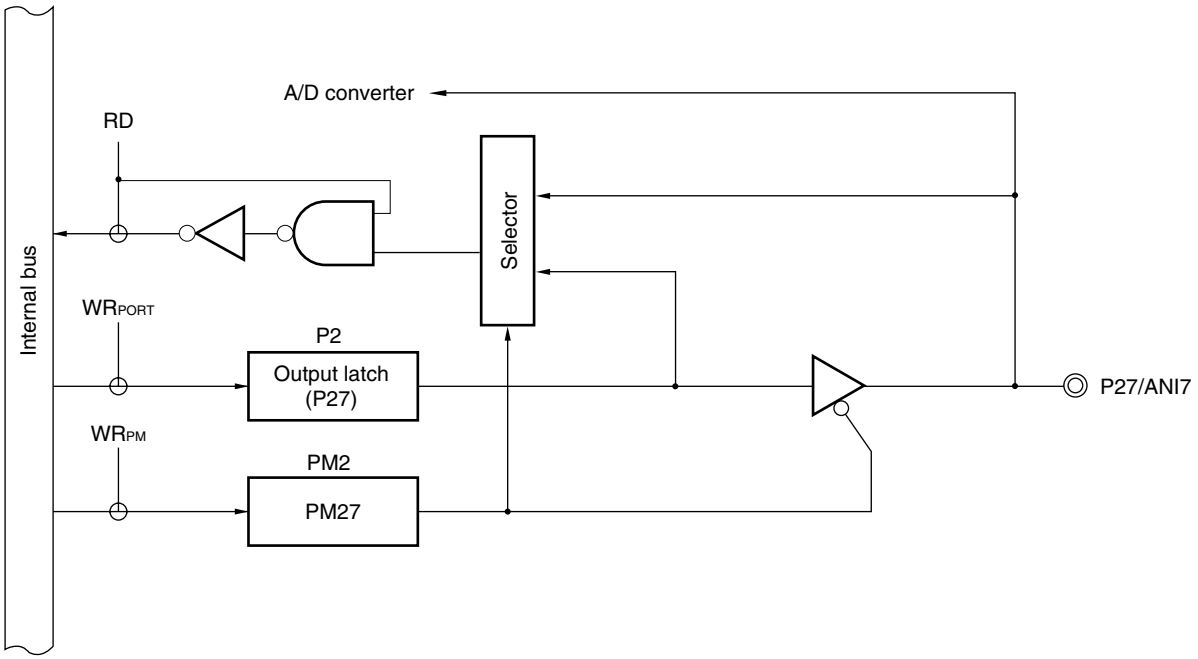
Note 78K0/LG3-M only.

Figure 4-4. Block Diagram of P20 to P27 (78K0/LG3-M)



P2: Port register 2
PM2: Port mode register 2
PF2: Port function register 2
RD: Read signal
WR××: Write signal

Figure 4-5. Block Diagram of P27 (78K0/LE3-M)



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

4.2.3 Port 3

78K0/LE3-M	78K0/LG3-M
P30/INTP5	P30/INTP5
–	P31/TOH1/INTP3
P32/TOH0	P32/TOH0
P33/TI000/BUZ/INTP2	P33/TI000/BUZ/INTP2

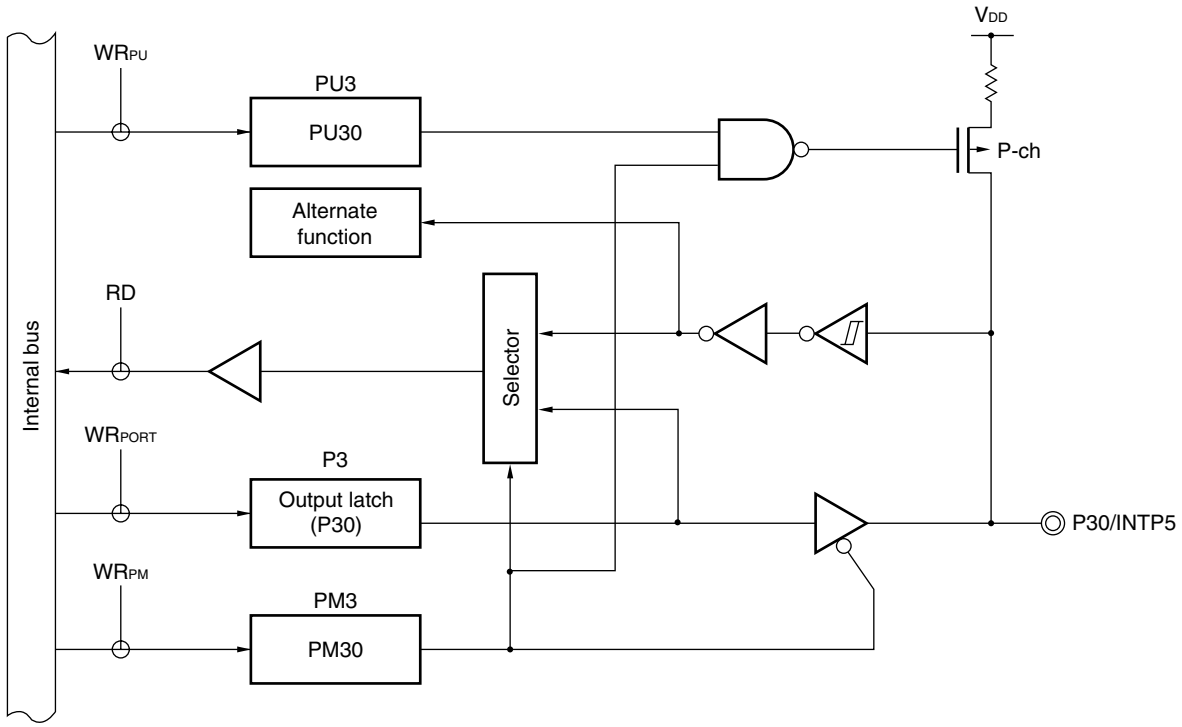
Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P33 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

This port can also be used for external interrupt request input, timer I/O, and buzzer output.

Reset signal generation sets port 3 to input mode.

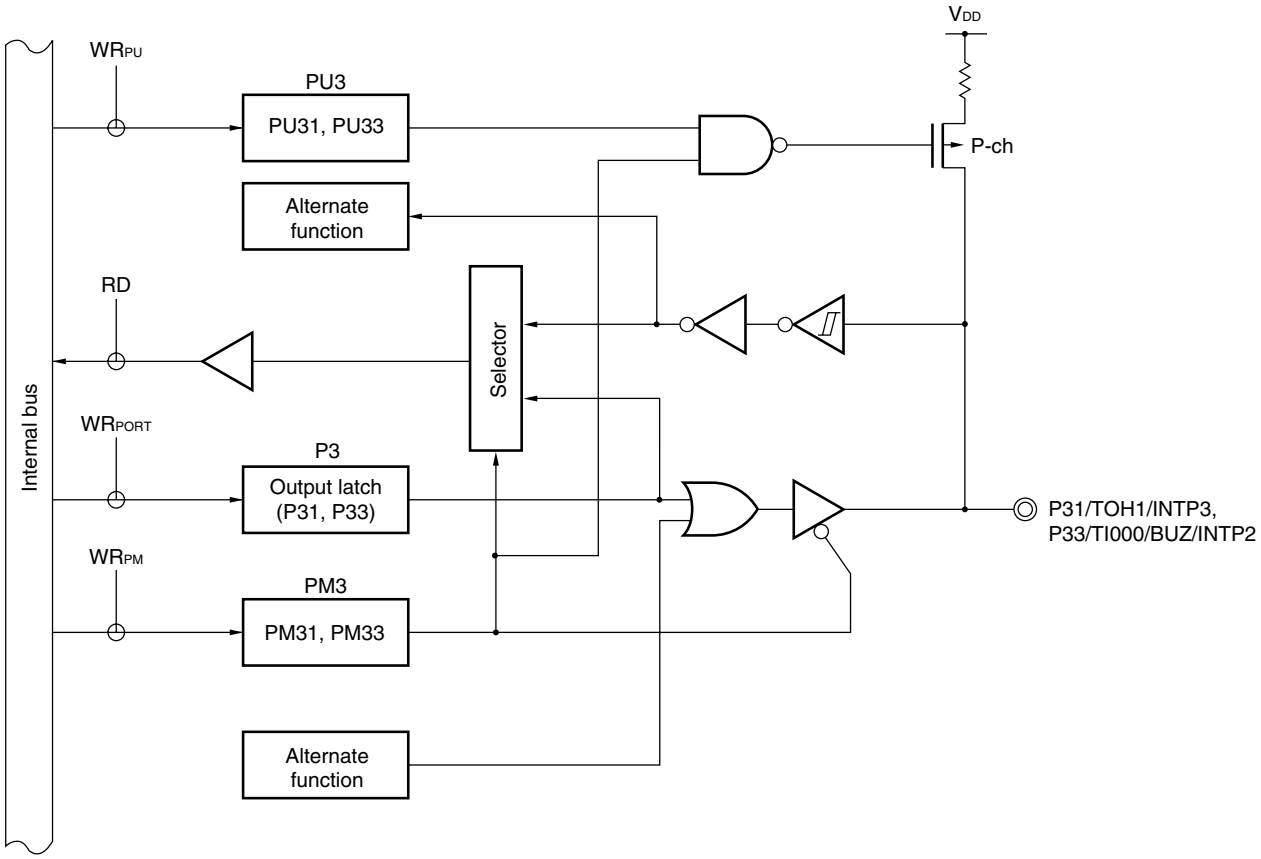
Figure 4-6 to Figure 4-8 show block diagrams of port 3.

Figure 4-6. Block Diagram of P30



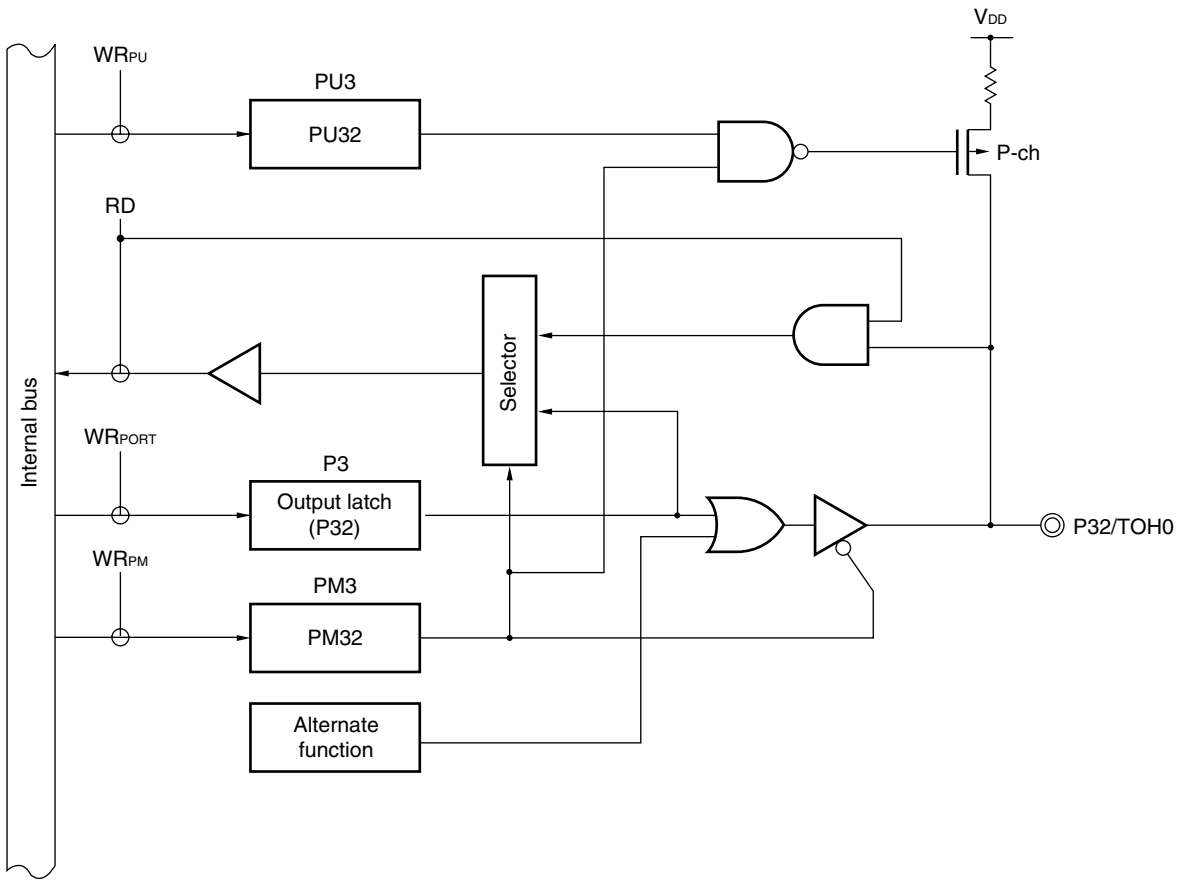
P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-7. Block Diagram of P31, P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-8. Block Diagram of P32



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

4.2.4 Port 4

78K0/LE3-M	78K0/LG3-M
P40/KR0	P40/KR0
P41/KR1	P41/KR1
–	P42/KR2
–	P43/TO51/TI51/KR3
–	P44/TO50/TI50/KR4
–	P45/KR5

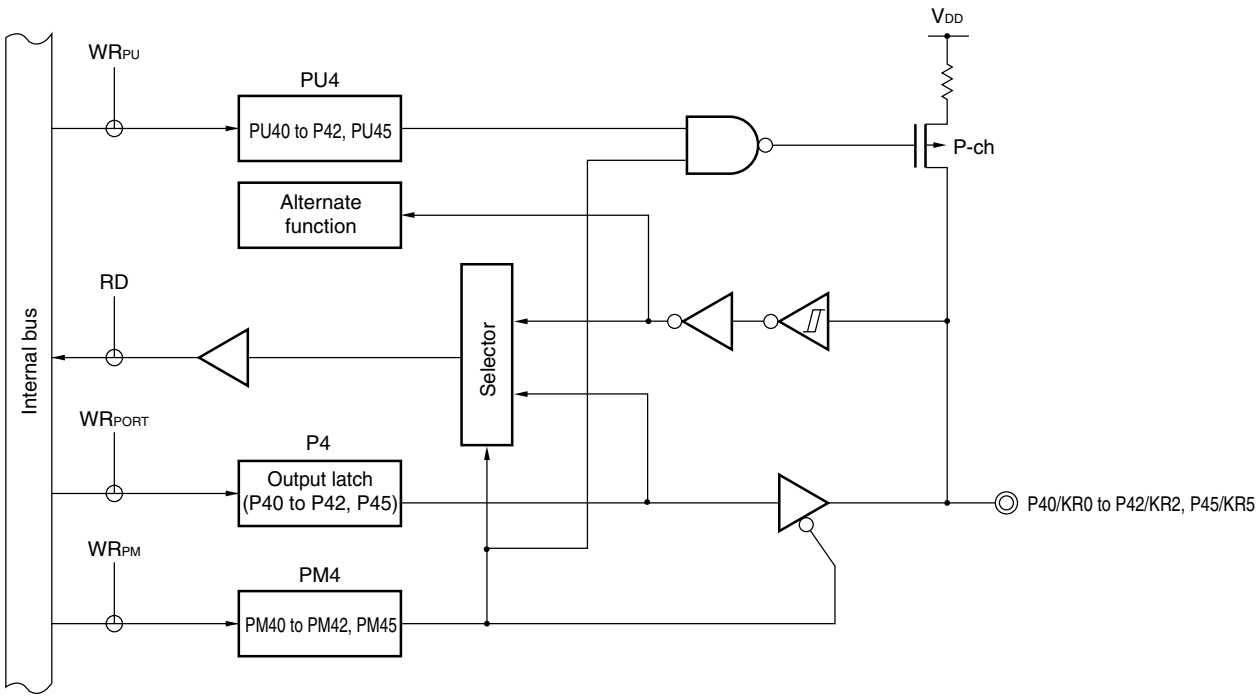
Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P45 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

This port can also be used for key interrupt input, segment key scan input, and timer I/O.

Reset signal generation sets port 4 to input mode.

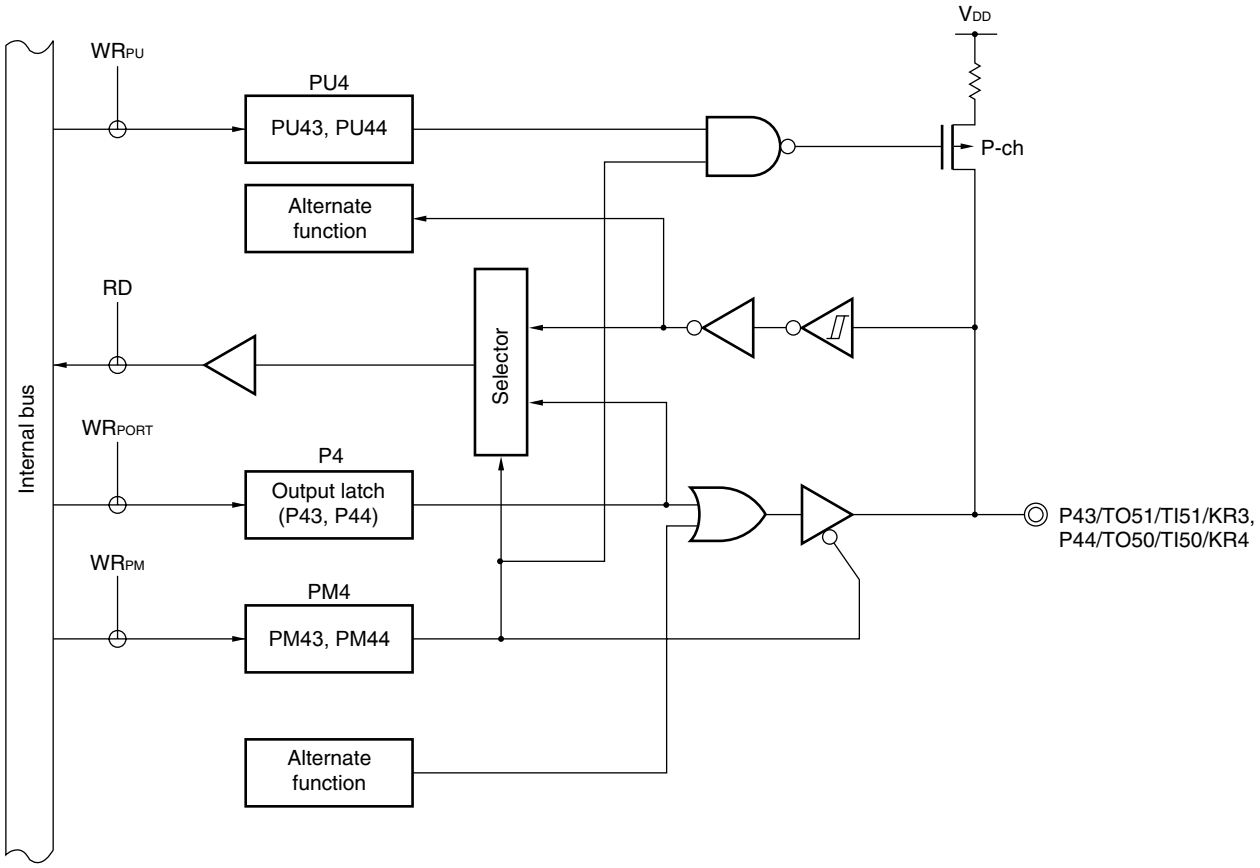
Figure 4-9 and Figure 4-10 show block diagrams of port 4.

Figure 4-9. Block Diagram of P40 to P42, P45



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 4-10. Block Diagram of P43 and P44



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

4.2.5 Port 8

78K0/LE3-M	78K0/LG3-M
P80/SEG4	P80/SEG4
P81/SEG5	P81/SEG5
P82/SEG6	P82/SEG6
P83/SEG7	P83/SEG7

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8). When the P80 to P83 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 8 (PU8).

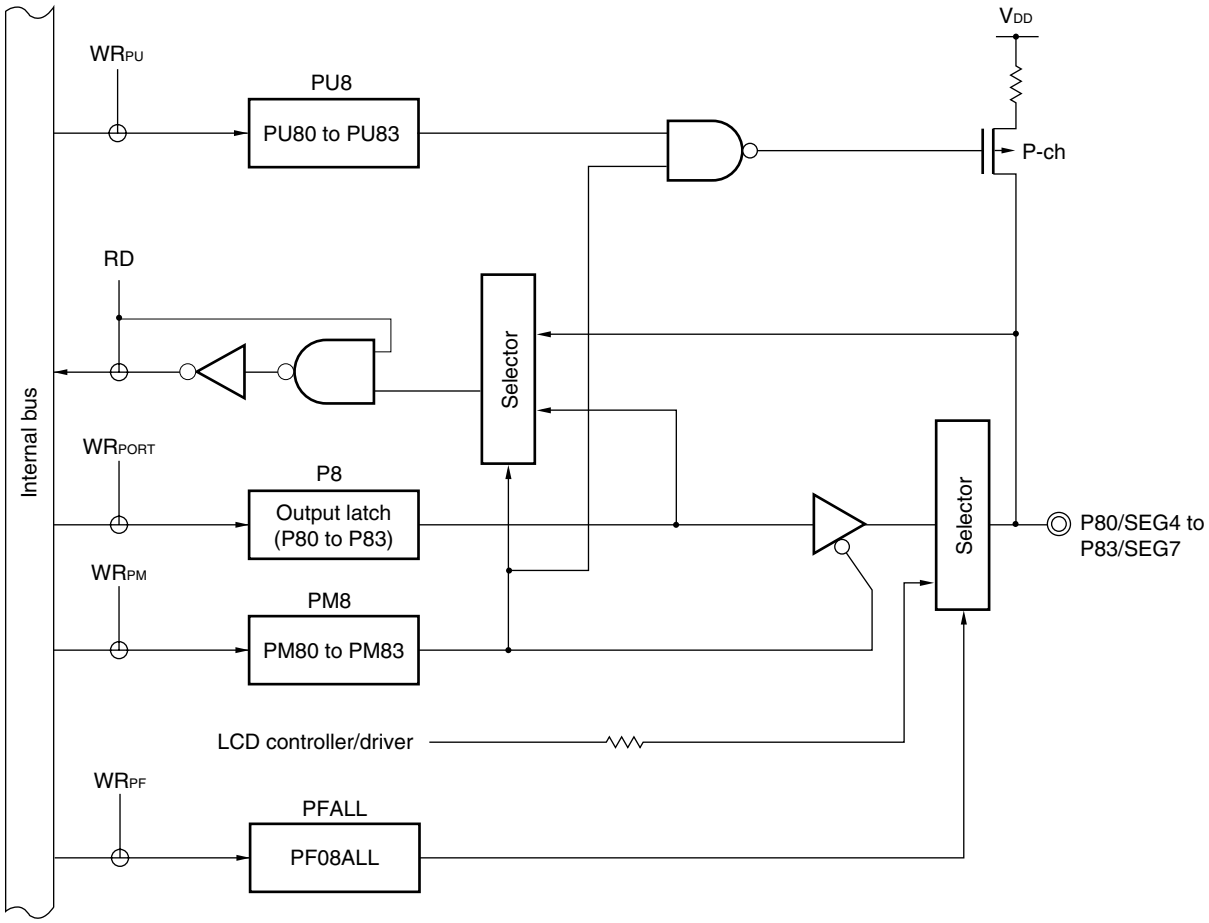
This port can also be used for segment signal output of the LCD controller/driver.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 8 to input mode.

Figure 4-11 shows a block diagram of port 8.

Figure 4-11. Block Diagram of P80 to P83



P8: Port register 8
PU8: Pull-up resistor option register 8
PM8: Port mode register 8
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.6 Port 9

78K0/LE3-M	78K0/LG3-M
P90/SEG8	P90/SEG8
P91/SEG9	P91/SEG9
P92/SEG10	P92/SEG10
P93/SEG11	P93/SEG11

Port 9 is an I/O port with an output latch. Port 9 can be set to the input mode or output mode in 1-bit units using port mode register 9 (PM9). When the P90 to P93 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 9 (PU9).

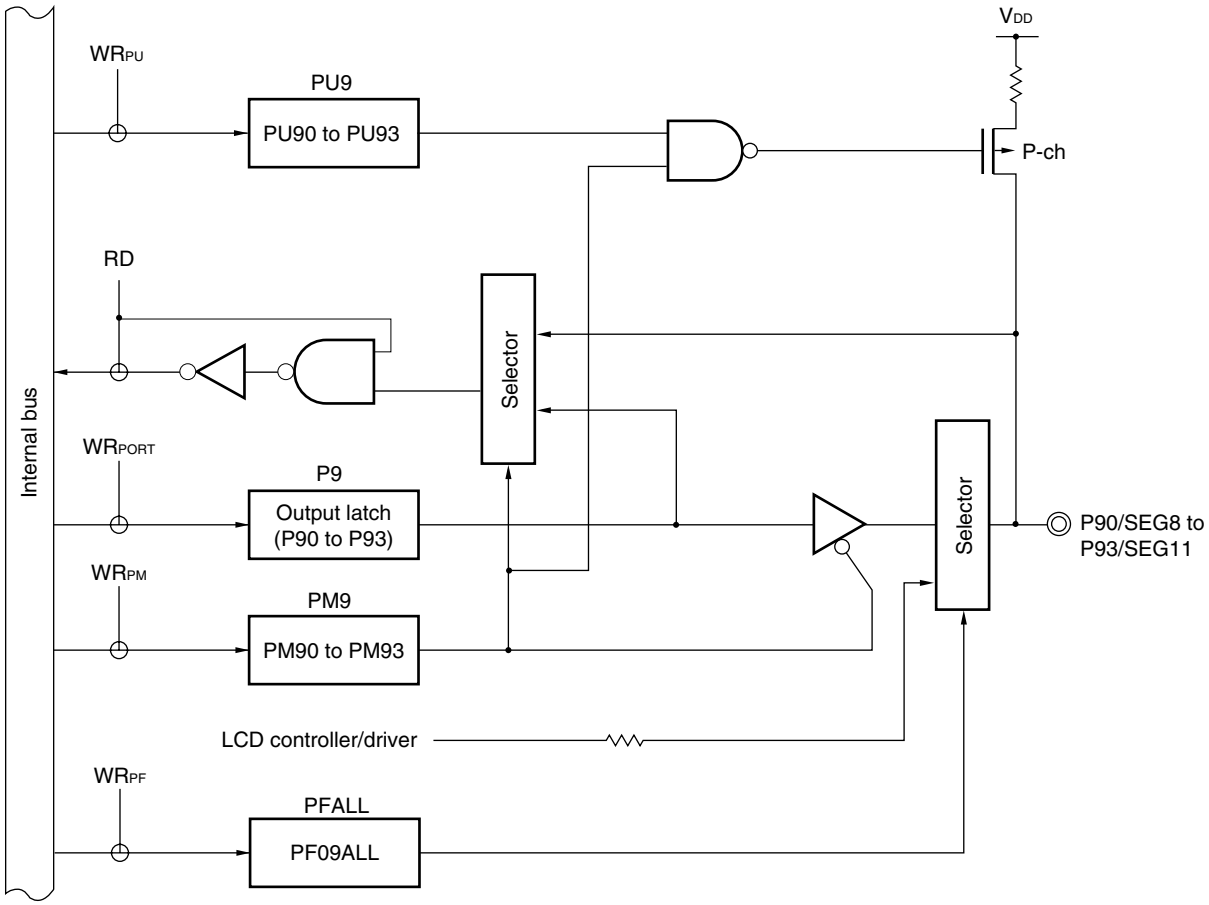
This port can also be used for segment signal output of the LCD controller/driver.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 9 to input mode.

Figure 4-12 shows a block diagram of port 9.

Figure 4-12. Block Diagram of P90 to P93



P9: Port register 9
PU9: Pull-up resistor option register 9
PM9: Port mode register 9
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.7 Port 10

78K0/LE3-M	78K0/LG3-M
P100/SEG12	P100/SEG12
P101/SEG13	P101/SEG13
P102/SEG14	P102/SEG14
P103/SEG15	P103/SEG15

Port 10 is an I/O port with an output latch. Port 10 can be set to the input mode or output mode in 1-bit units using port mode register 10 (PM10). When the P100 to P103 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 10 (PU10).

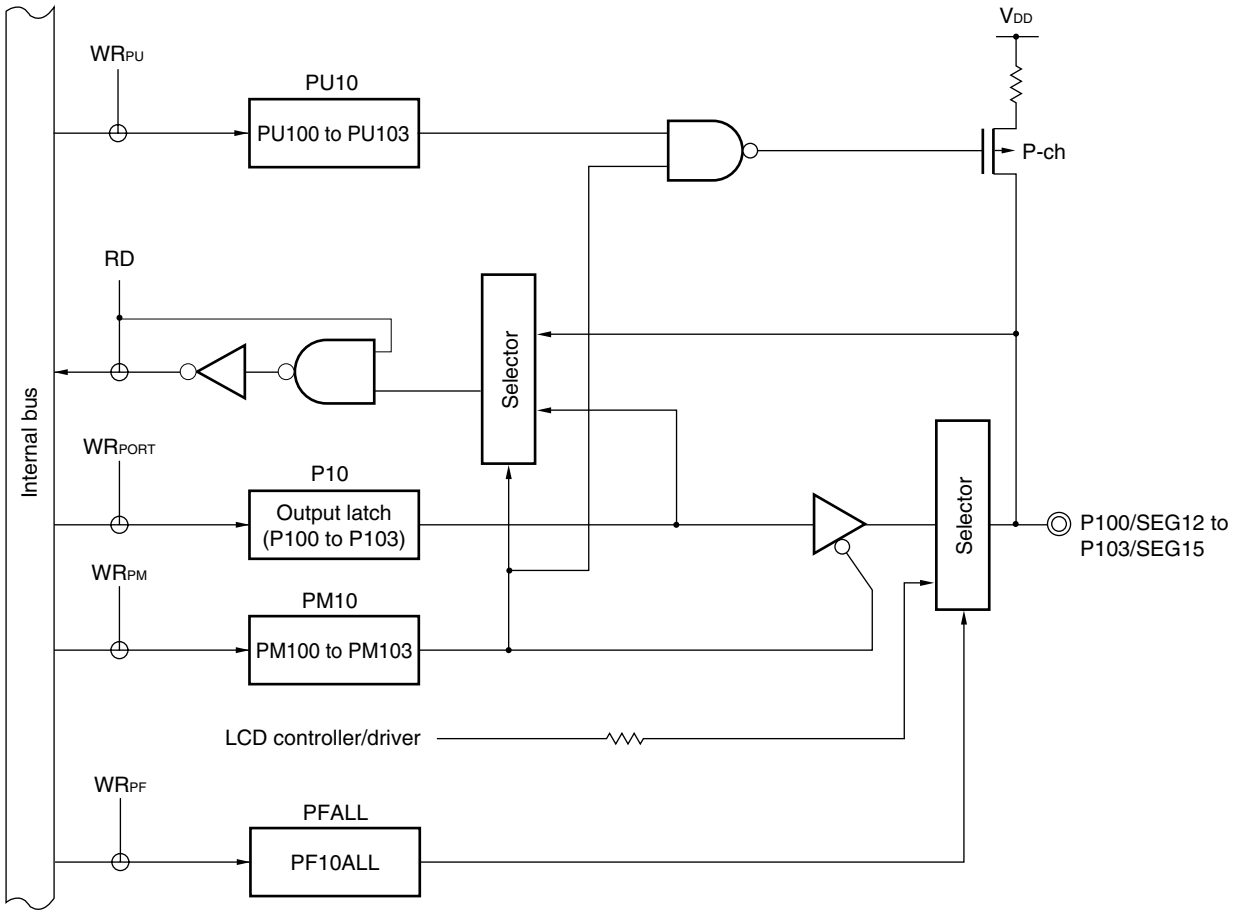
This port can also be used for segment signal output of the LCD controller/driver.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 10 to input mode.

Figure 4-13 shows a block diagram of port 10.

Figure 4-13. Block Diagram of P100 to P103



P10: Port register 10
PU10: Pull-up resistor option register 10
PM10: Port mode register 10
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.8 Port 11

78K0/LE3-M	78K0/LG3-M
P110/SEG16	P110/SEG16
P111/SEG17	P111/SEG17
P112/SEG18/TxD6	P112/SEG18/TxD6
P113/SEG19/RxD6	P113/SEG19/RxD6

Port 11 is a 4-bit I/O port with an output latch. Port 11 can be set to the input mode or output mode in 1-bit units using port mode register 11 (PM11). When the P110 to P113 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 11 (PU11).

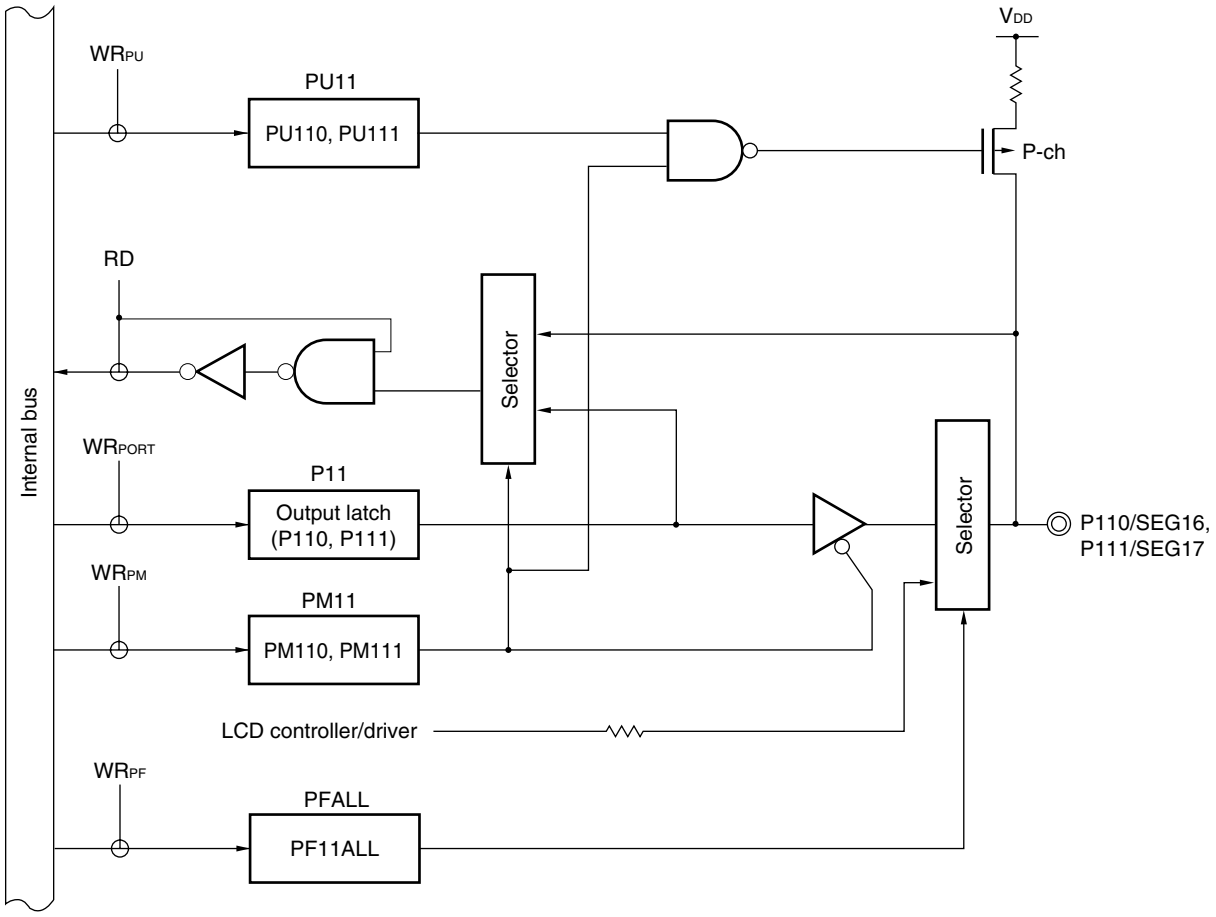
This port can also be used for segment signal output of LCD controller/driver and serial interface data I/O,

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 11 to input mode.

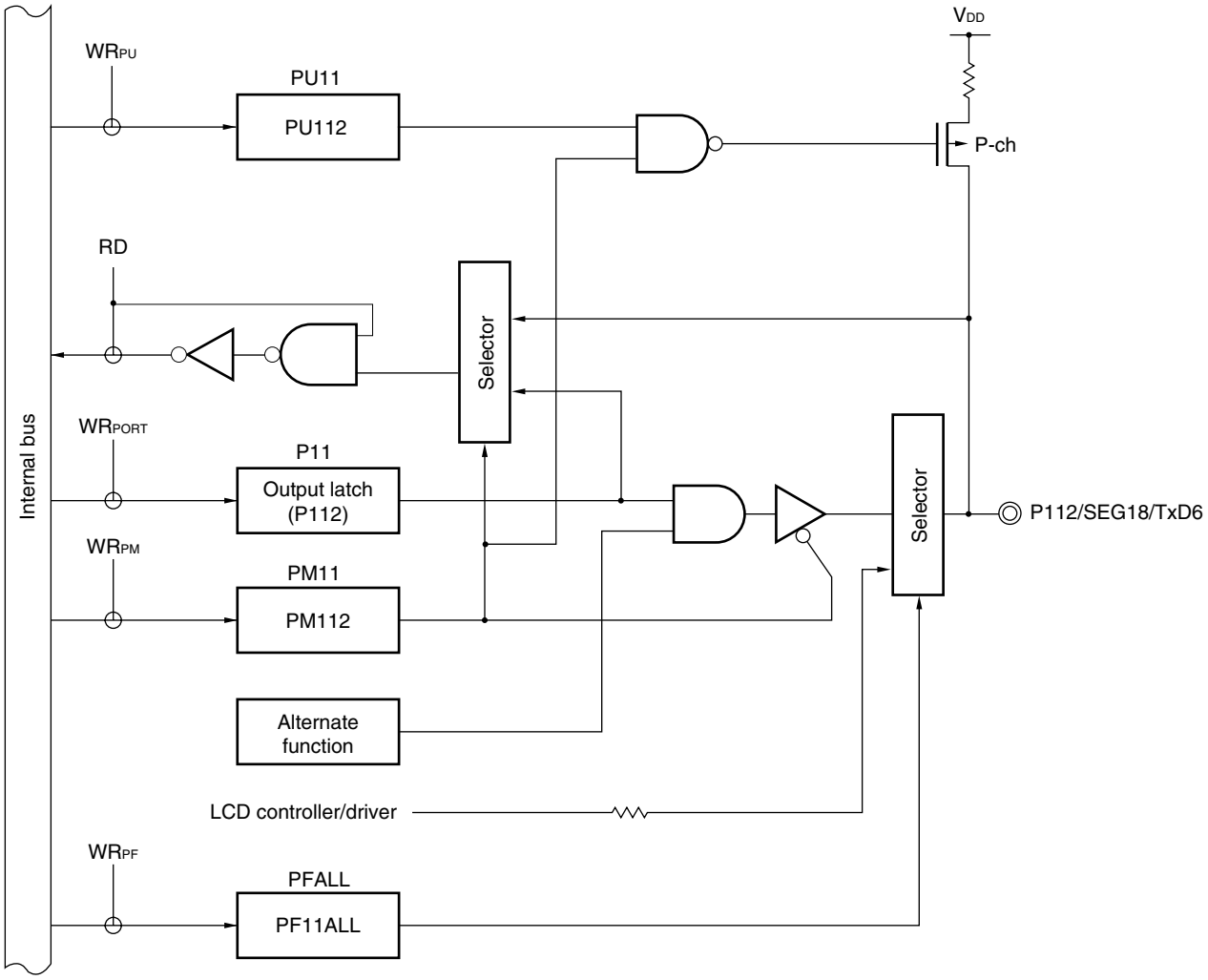
Figure 4-14 to Figure 4-16 show block diagrams of port 11.

Figure 4-14. Block Diagram of P110 and P111



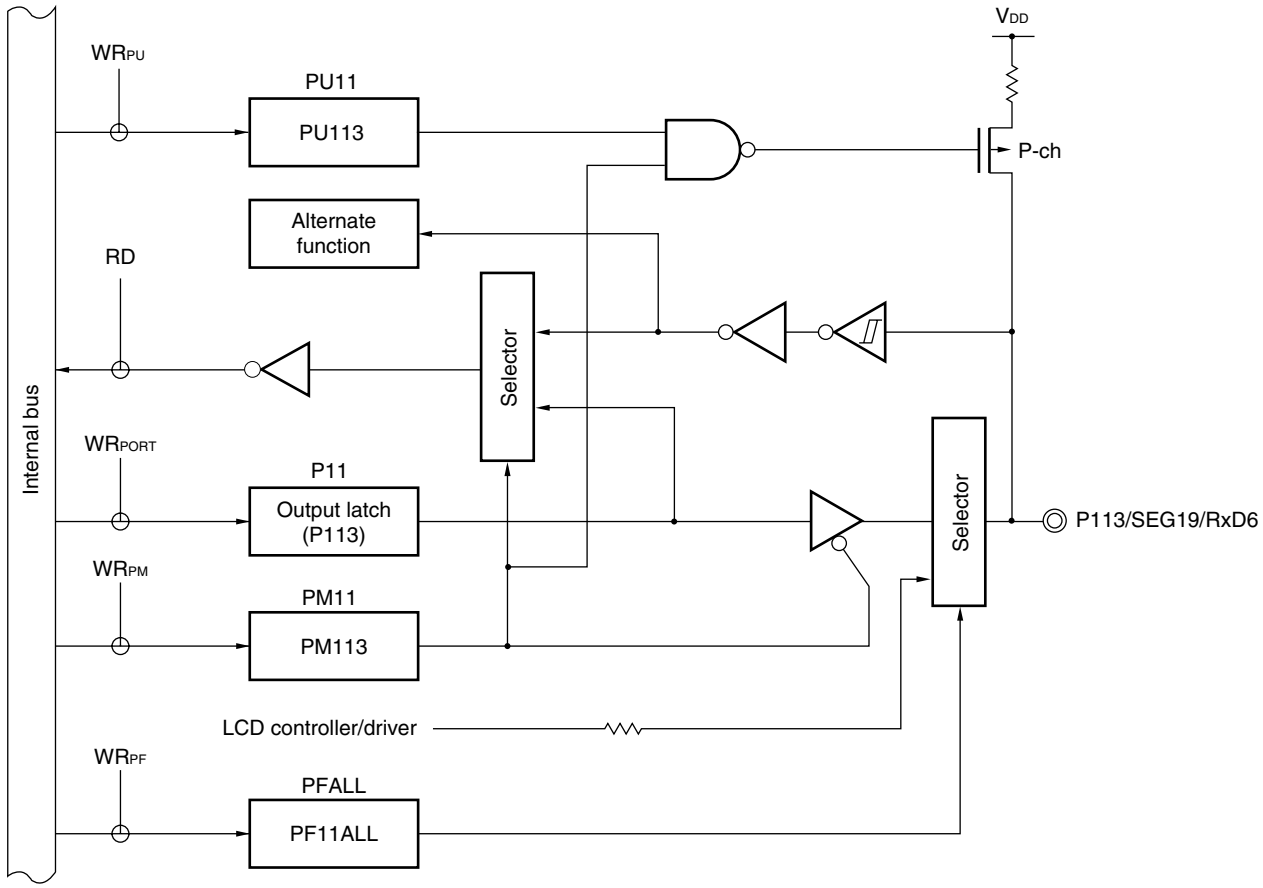
P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

Figure 4-15. Block Diagram of P112



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

Figure 4-16. Block Diagram of P113



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.9 Port 12

78K0/LE3-M	78K0/LG3-M
P120/INTP0/EXLVI	P120/INTP0/EXLVI
P121/X1/OCD0A	P121/X1/OCD0A
P122/X2/EXCLK/OCD0B	P122/X2/EXCLK/OCD0B
–	P123

P120 is a 1-bit I/O port with an output latch. P120 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P123 are a 3-bit input-only registers.

This port can also be used as pins for the external interrupt request input, potential input for external low-voltage detection, connecting resonator for the main system clock, and external clock input for the main system clock.

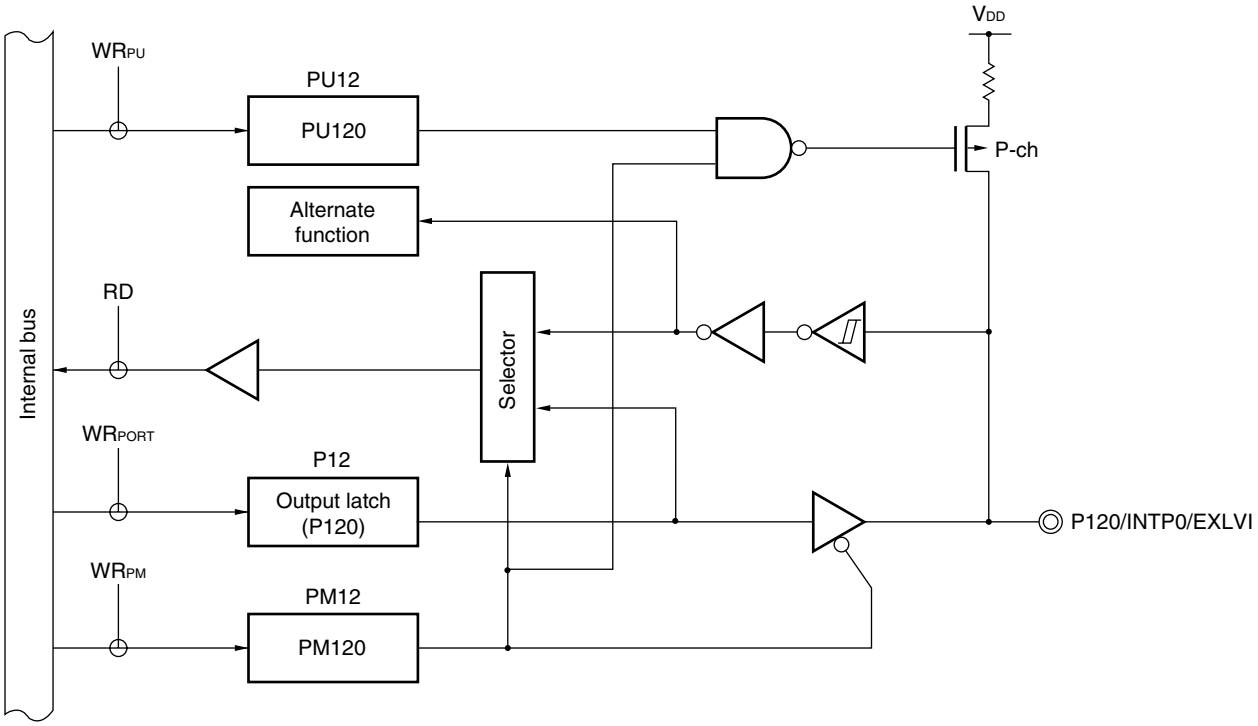
Reset signal generation sets port 12 to input mode.

Figure 4-17 to Figure 4-19 show block diagrams of port 12.

Caution When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see 5.3 (1) Clock operation mode select register (OSCCTL) and (4) Setting of operation mode for subsystem clock pin). The reset value of OSCCTL is 00H (both the P121 and P122 pins are input port pins).

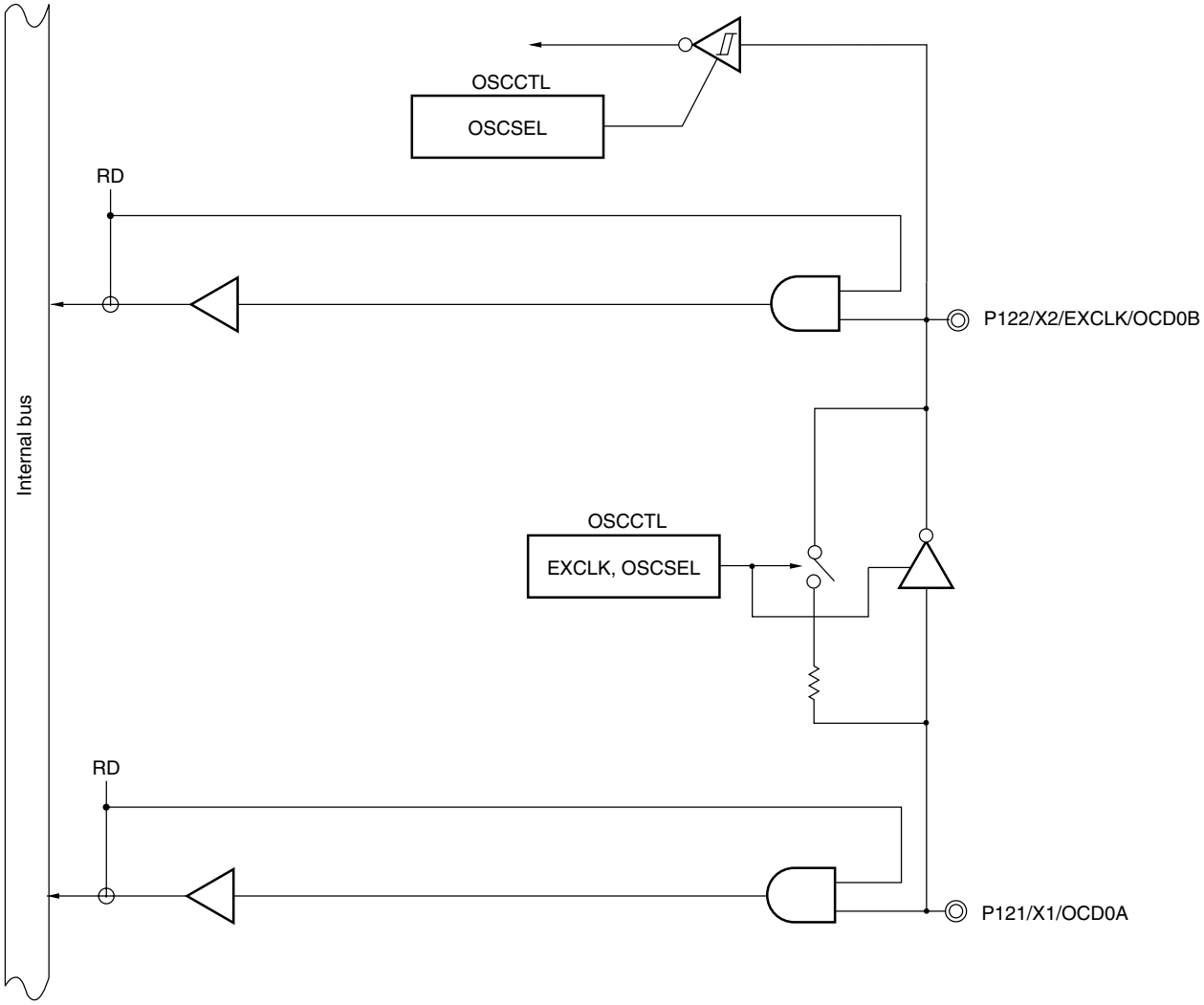
Remark P121 and P122 can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION.**

Figure 4-17. Block Diagram of P120



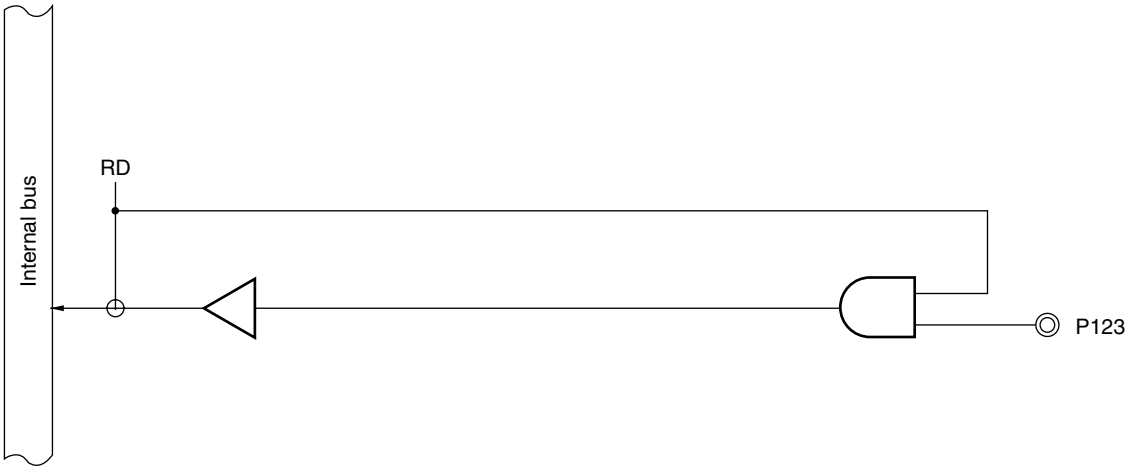
P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Figure 4-18. Block Diagram of P121 and P122



OSCCTL: Clock operation mode select register
RD: Read signal

Figure 4-19. Block Diagram of P123



RD: Read signal

4.2.10 Port 13

78K0/LE3-M	78K0/LG3-M
P130/SEG20	P130/SEG20
P131/SEG21	P131/SEG21
P132/SEG22	P132/SEG22
P133/SEG23	P133/SEG23

Port 13 is an I/O port with an output latch. Port 13 can be set to the input mode or output mode in 1-bit units using port mode register 13 (PM13). When the P130 to P133 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 13 (PU13).

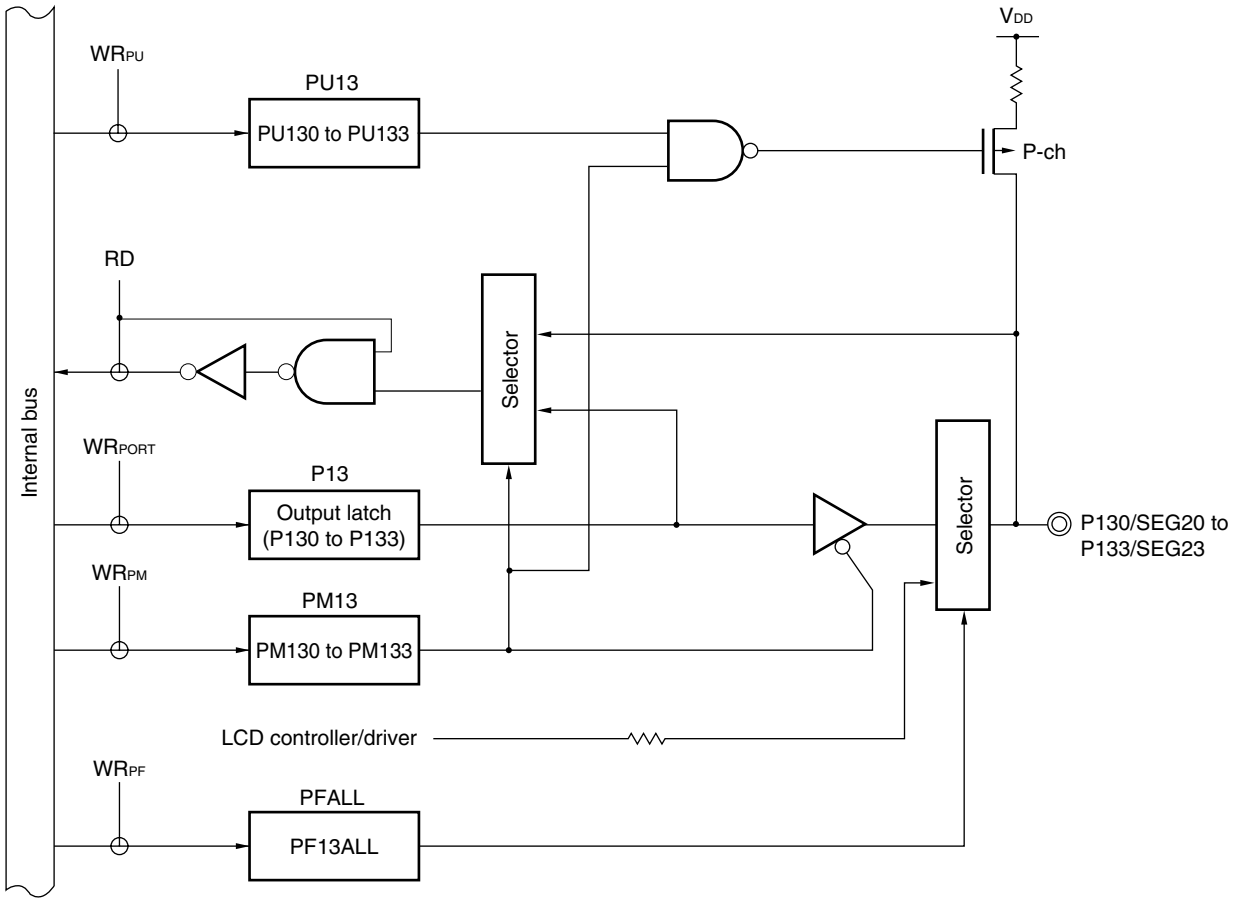
This port can also be used for segment signal output of the LCD controller/driver.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 13 to input mode.

Figure 4-20 shows a block diagram of port 13.

Figure 4-20. Block Diagram of P130 to P133



P13: Port register 13
PU13: Pull-up resistor option register 13
PM13: Port mode register 13
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.11 Port 14

78K0/LE3-M	78K0/LG3-M
–	P140/SEG24 (KS0)
–	P141/SEG25 (KS1)
–	P142/SEG26 (KS2)
–	P143/SEG27 (KS3)

Port 14 is an I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 to P143 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

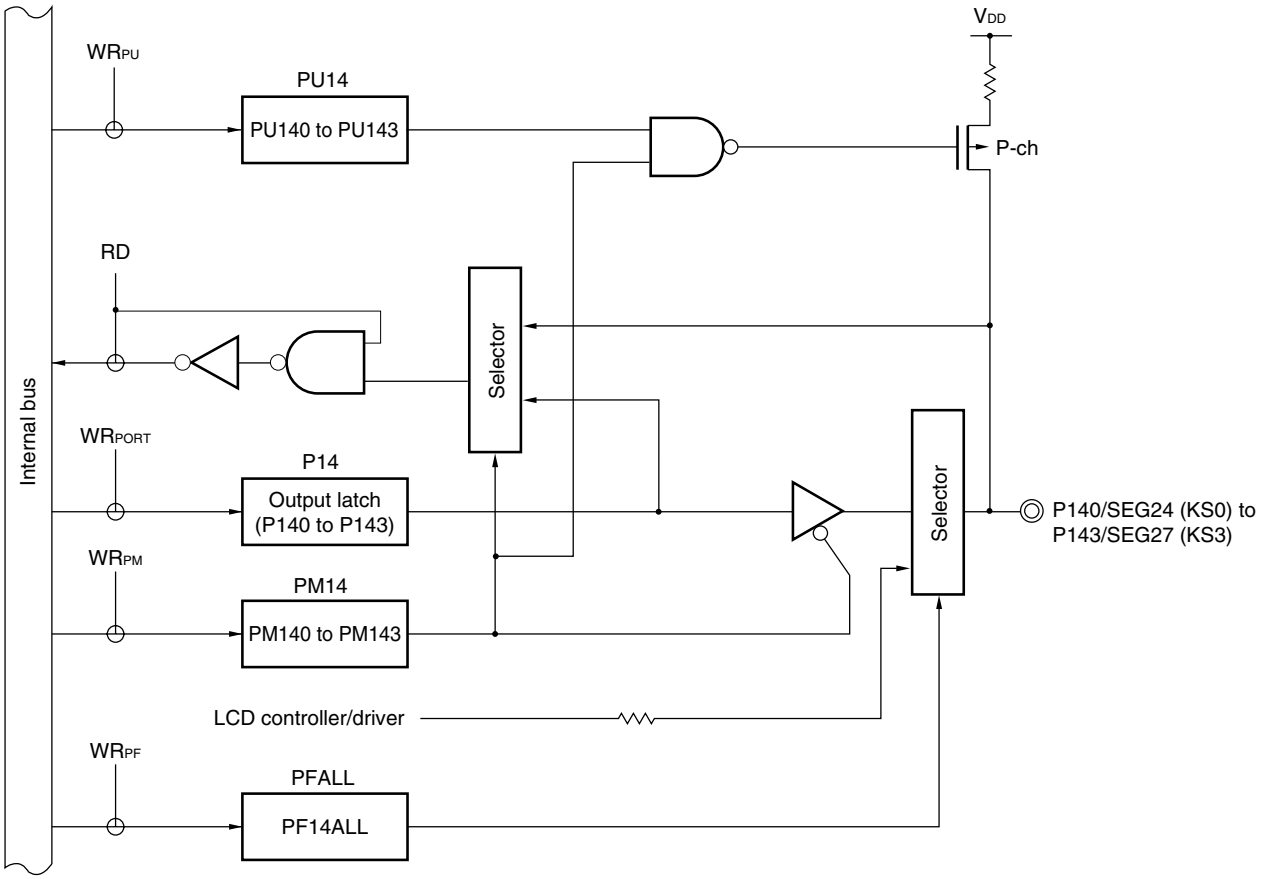
This port can also be used for segment signal output of the LCD controller/driver and simultaneous output of segment key source signal.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 14 to input mode.

Figure 4-21 shows a block diagram of port 14.

Figure 4-21. Block Diagram of P140 to P143



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.12 Port 15

78K0/LE3-M	78K0/LG3-M
–	P150/SEG28 (KS4)
–	P151/SEG29 (KS5)
–	P152/SEG30 (KS6)
–	P153/SEG31 (KS7)

Port 15 is an I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15). When the P150 to P153 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 15 (PU15).

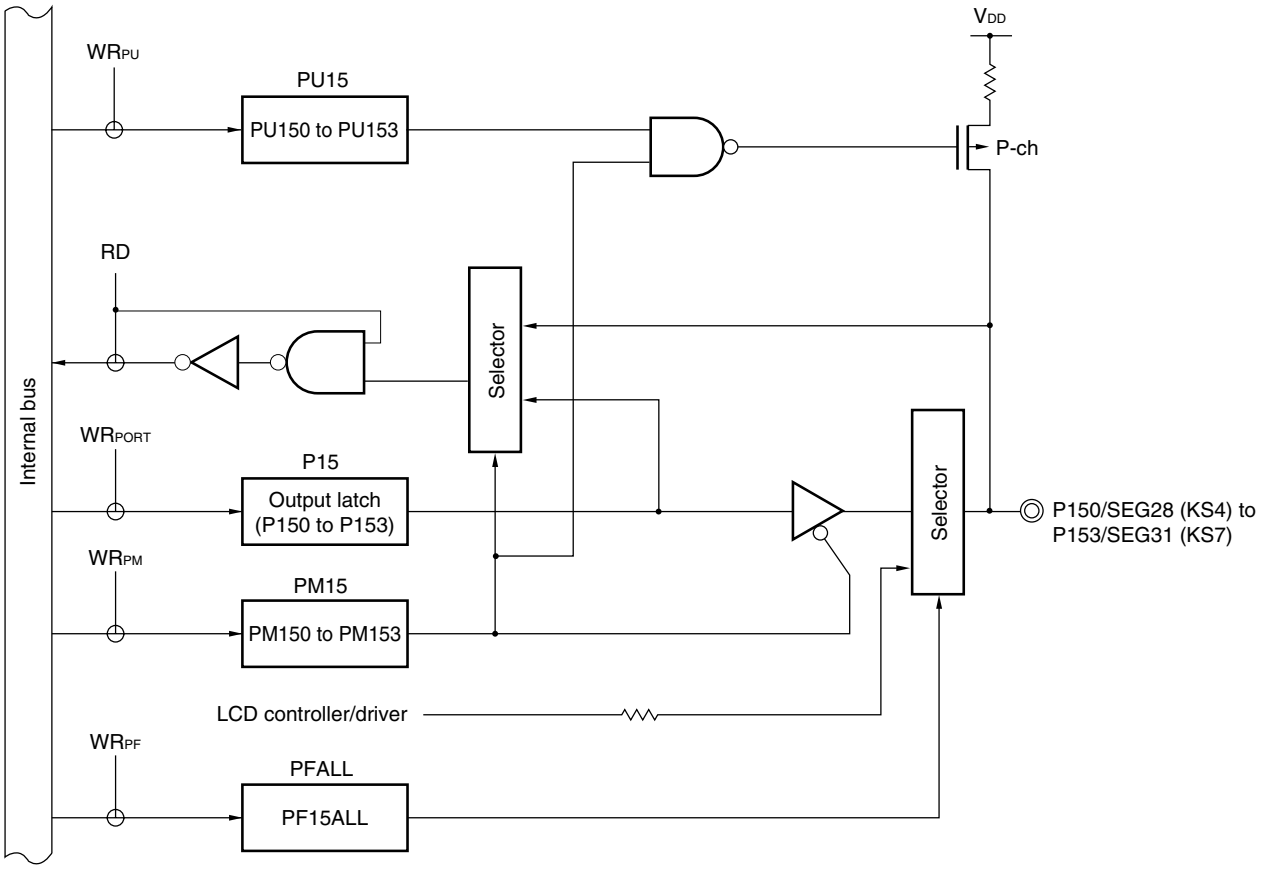
This port can also be used for segment signal output for the LCD controller/driver and simultaneous output of segment key source signal.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 15 to input mode.

Figure 4-22 shows a block diagram of port 15.

Figure 4-22. Block Diagram of P150 to P153



P15: Port register 15
PU15: Pull-up resistor option register 15
PM15: Port mode register 15
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

4.2.13 Port LP0

78K0/LE3-M	78K0/LG3-M
–	LP00
–	LP01/ZX1
–	LP02/ZX2
–	LP03
–	LP04
–	LP05

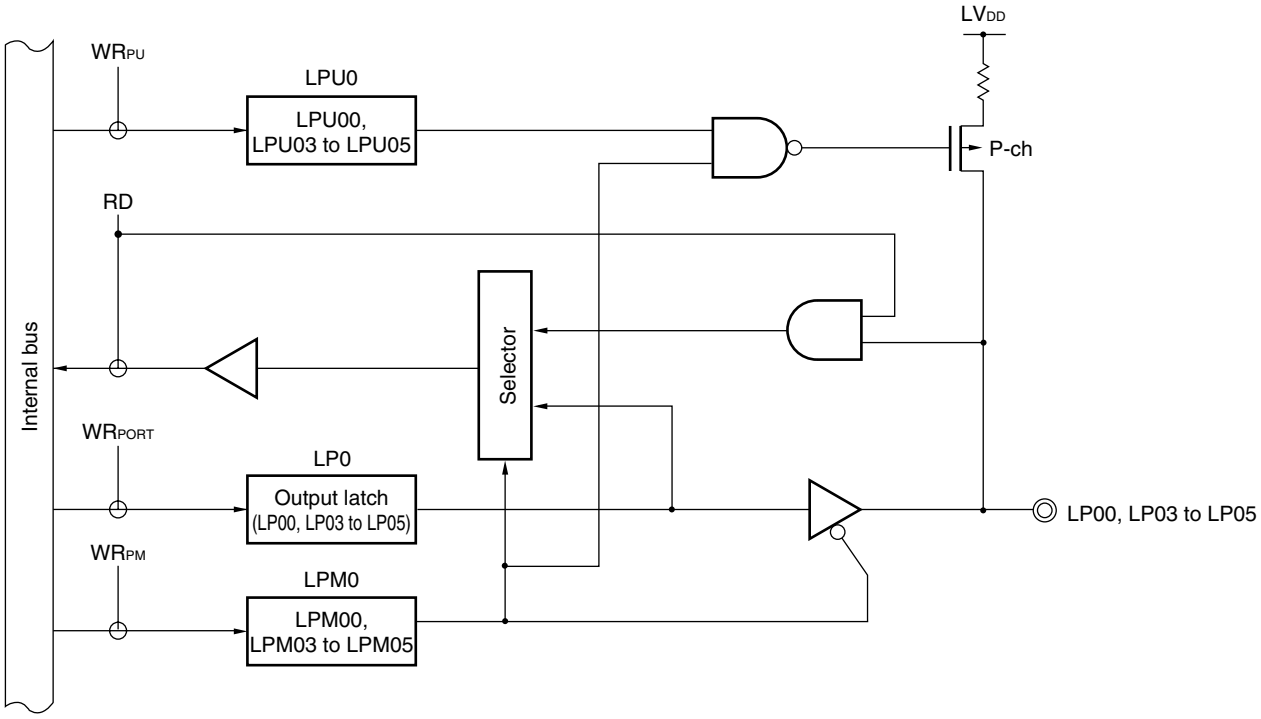
Port LP0 is a I/O port with an output latch. Port LP0 can be set to the input mode or output mode in 1-bit units using port mode register LP0 (LPM0). When the LP00 to LP05 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register LP0 (LPU0).

This port can also be used for zero-crossing detection signal output of power quality measurement circuit.

Reset signal generation sets port LP0 to input mode.

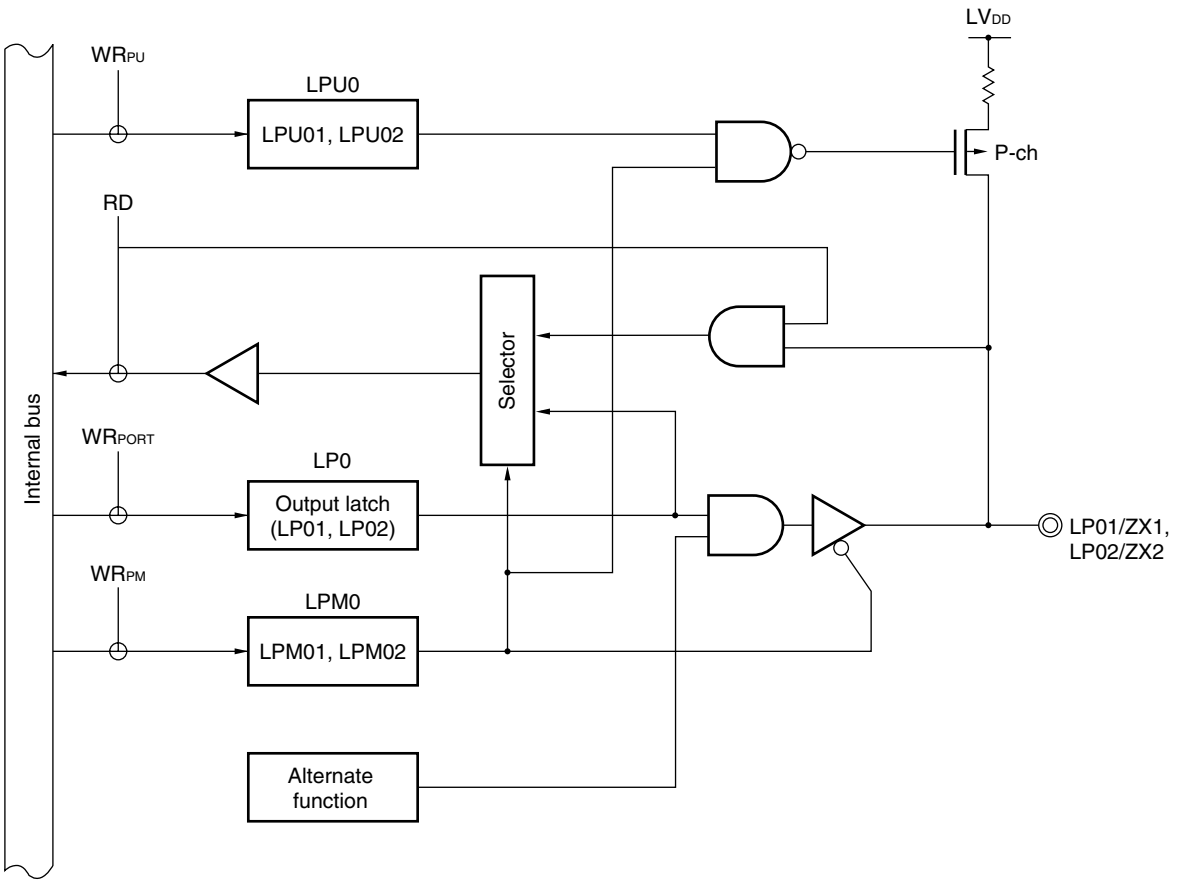
Figure 4-23 and Figure 4-24 show block diagrams of port LP0.

Figure 4-23. Block Diagram of LP00, LP03 to LP05



LP0: Port register LP0
LPU0: Pull-up resistor option register LP0
LPM0: Port mode register LP0
RD: Read signal
WR××: Write signal

Figure 4-24. Block Diagram of LP01 and LP02



LP0: Port register LP0
LPU0: Pull-up resistor option register LP0
LPM0: Port mode register LP0
RD: Read signal
WR××: Write signal

4.2.14 Port LP1

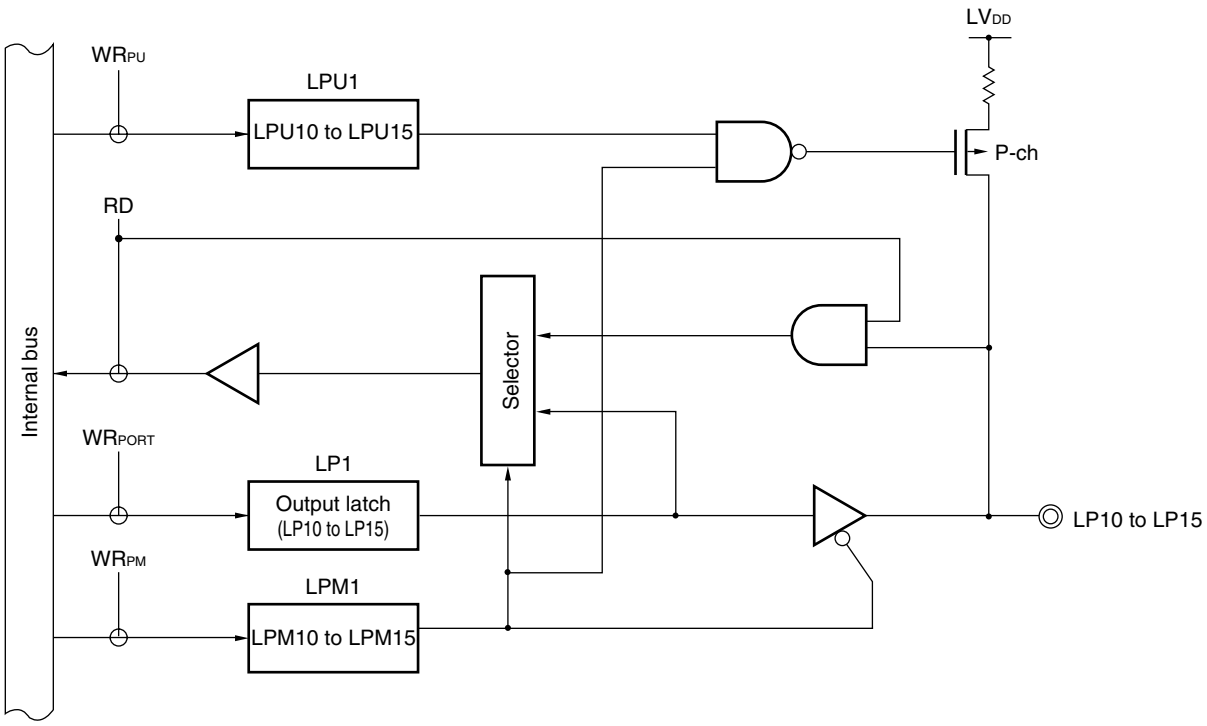
78K0/LE3-M	78K0/LG3-M
–	LP10
–	LP11
–	LP12
–	LP13
–	LP14
–	LP15

Port LP1 is a I/O port with an output latch. Port LP1 can be set to the input mode or output mode in 1-bit units using port mode register LP1 (LPM1). When the LP10 to LP15 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register LP1 (LPU1).

Reset signal generation sets port LP1 to input mode.

Figure 4-25 shows a block diagram of port LP1.

Figure 4-25. Block Diagram of LP10 to LP15



LP1: Port register LP1
LPU1: Pull-up resistor option register LP1
LPM1: Port mode register LP1
RD: Read signal
WR××: Write signal

4.3 Registers Controlling Port Function

Port functions are controlled by the following seven types of registers.

- Port mode registers (PMxx, LPMx)
- Port registers (Pxx, LPx)
- Pull-up resistor option registers (PUxx, LPUx)
- Port function register 1 (PF1)
- Port function register 2 (PF2) Note
- Port function register ALL (PFALL)
- A/D port configuration register 0 (ADPC0)

Note 78K0/LG3-M only.

(1) Port mode registers (PMxx, LPMx)

These registers specify input or output mode for the port in 1-bit units.

Port mode register PMxx can be set by a 1-bit or 8-bit memory manipulation instruction.

Port mode register LPMx can be set by using the extended SFR interface.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function**.

Figure 4-26. Format of Port Mode Register (78K0/LE3-M)

	Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
	PM1	PM17	PM16	1	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
<R>	PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
	PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
	PM4	PM47	PM46	1	1	1	1	PM41	PM40	FF24H	FFH	R/W
	PM8	1	1	1	1	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
	PM9	1	1	1	1	PM93	PM92	PM91	PM90	FF29H	FFH	R/W
	PM10	1	1	1	1	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
	PM11	1	1	1	1	PM113	PM112	PM111	PM110	FF2BH	FFH	R/W
	PM12	1	1	1	1	1	1	1	PM120	FF2CH	FFH	R/W
	PM13	1	1	1	1	PM133	PM132	PM131	PM130	FF2DH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 1 to 4, 8 to 13; n = 0 to 4, 6, 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

<R> **Cautions 1. Be sure to set bit 5 of PM1, bits 4 to 7 of PM3, bits 2 to 5 of PM4, bits 4 to 7 of PM8, bits 4 to 7 of PM9, bits 4 to 7 of PM10, bits 4 to 7 of PM11, bits 1 to 7 of PM12, and bits 4 to 7 of PM13 to "1".**

<R> **2. After reset release, be sure to clear PM10, PM14, PM16, PM17, PM20 to PM26, PM31, PM46, and PM47 to "0".**

Figure 4-27. Format of Port Mode Register (78K0/LG3-M)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM1	PM17	PM16	1	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM8	1	1	1	1	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
PM9	1	1	1	1	PM93	PM92	PM91	PM90	FF29H	FFH	R/W
PM10	1	1	1	1	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
PM11	1	1	1	1	PM113	PM112	PM111	PM110	FF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FF2CH	FFH	R/W
PM13	1	1	1	1	PM133	PM132	PM131	PM130	FF2DH	FFH	R/W
PM14	1	1	1	1	PM143	PM142	PM141	PM140	FF2EH	FFH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FF2FH	FFH	R/W
LPM0	1	1	LPM05	LPM04	LPM03	LPM02	LPM01	LPM00	8CH	FFH	R/W
LPM1	1	1	LPM15	LPM14	LPM13	LPM12	LPM11	LPM10	8FH	FFH	R/W

PMmn, LPMxy	Pmn and LPxy pins I/O mode selection (m = 1 to 4, 8 to 15; n = 0 to 7; x = 0, 1; y = 0 to 5)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Cautions 1. Be sure to set bit 5 of PM1, bits 4 to 7 of PM3, bits 4 to 7 of PM8, bits 4 to 7 of PM9, bits 4 to 7 of PM10, bits 4 to 7 of PM11, bits 1 to 7 of PM12, bits 4 to 7 of PM13, bits 4 to 7 of PM14, bits 4 to 7 of PM15, bits 6 and 7 of LPM0, and bits 6 and 7 of LPM1 to "1".

2. After reset release, be sure to clear PM10, PM14, PM16, PM17, PM46, and PM47 to "0".

(2) Port registers (Pxx, LPx)

These registers write the data that is output from the chip when data is output from a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read.

Port register Pxx can be set by a 1-bit or 8-bit memory manipulation instruction.

Port register LPx can be set by using the extended SFR interface.

Reset signal generation clears these registers to 00H.

Figure 4-28. Format of Port Register (78K0/LE3-M)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P1	P17	0	0	P14	P13	P12	P11	0	FF01H	00H (output latch)	R/W
P2	P27	0	0	0	0	0	0	0	FF02H	00H (output latch)	R/W
P3	0	0	0	0	P33	P32	P31	P30	FF03H	00H (output latch)	R/W
P4	P47	P46	0	0	0	0	P41	P40	FF04H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FF08H	00H (output latch)	R/W
P9	0	0	0	0	P93	P92	P91	P90	FF09H	00H (output latch)	R/W
P10	0	0	0	0	P103	P102	P101	P100	FF0AH	00H (output latch)	R/W
P11	0	0	0	0	P113	P112	P111	P110	FF0BH	00H (output latch)	R/W
P12	0	0	0	0	0	P122 Note 2	P121 Note 2	P120	FF0CH	00H Note 1 (output latch)	R/W Note 1
P13	0	0	0	0	P133	P132	P131	P130	FF0DH	00H (output latch)	R/W

Pmn	m = 1 to 4, 8 to 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. P121 and P122 are read-only. These become undefined at reset.

2. When the operation mode of the pin is the clock input mode, 0 is always read.

Caution After reset release, be sure to set P14, P46, and P47 to "1".

Figure 4-29. Format of Port Register (78K0/LG3-M)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P1	P17	0	0	P14	P13	P12	P11	0	FF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P3	0	0	0	0	P33	P32	P31	P30	FF03H	00H (output latch)	R/W
P4	P47	P46	P45	P44	P43	P42	P41	P40	FF04H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FF08H	00H (output latch)	R/W
P9	0	0	0	0	P93	P92	P91	P90	FF09H	00H (output latch)	R/W
P10	0	0	0	0	P103	P102	P101	P100	FF0AH	00H (output latch)	R/W
P11	0	0	0	0	P113	P112	P111	P110	FF0BH	00H (output latch)	R/W
P12	0	0	0	0	P123 Note 2	P122 Note 2	P121 Note 2	P120	FF0CH	00H Note 1 (output latch)	R/W Note 1
P13	0	0	0	0	P133	P132	P131	P130	FF0DH	00H (output latch)	R/W
P14	PK143 Note 3	PK142 Note 3	PK141 Note 3	PK140 Note 3	P143	P142	P141	P140	FF0EH	00H (output latch)	R/W
P15	PK153 Note 3	PK152 Note 3	PK151 Note 3	PK150 Note 3	P153	P152	P151	P150	FF0FH	00H (output latch)	R/W
LP0	0	0	LP05	LP04	LP03	LP02	LP01	LP00	8BH	00H (output latch)	R/W
LP1	0	0	LP15	LP14	LP13	LP12	LP11	LP10	8EH	00H (output latch)	R/W

Pmn, LPxy	m = 1 to 4, 8 to 15; n = 0 to 7; x = 0, 1; y = 0 to 5	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. P121 to P123 are read-only. These become undefined at reset.

2. When the operation mode of the pin is the clock input mode, 0 is always read.

3. This bit is used for the segment key scan function. For details, see **18.3 Registers Controlling LCD Controller/Driver.**

Caution After reset release, be sure to set P14, P46, and P47 to "1".

(3) Pull-up resistor option registers (PUxx, LPUx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in pull-up resistor option registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of pull-up resistor option registers.

Pull-up resistor option register PUxx can be set by a 1-bit or 8-bit memory manipulation instruction.

Pull-up resistor option register LPUx can be set by using the extended SFR interface.

Reset signal generation clears these registers to 00H.

Figure 4-30. Format of Pull-up Resistor Option Register (78K0/LE3-M)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU1	0	0	0	0	0	PU12	PU11	0	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	0	PU30	FF33H	00H	R/W
PU4	0	0	PU45	PU44	PU43	PU42	PU41	PU40	FF34H	00H	R/W
PU8	0	0	0	0	PU83	PU82	PU81	PU80	FF38H	00H	R/W
PU9	0	0	0	0	PU93	PU92	PU91	PU90	FF39H	00H	R/W
PU10	0	0	0	0	PU103	PU102	PU101	PU100	FF3AH	00H	R/W
PU11	0	0	0	0	PU113	PU112	PU111	PU110	FF3BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU13	0	0	0	0	PU133	PU132	PU131	PU130	FF3DH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 1, 3, 4, 8 to 13; n = 0 to 3)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Caution After reset release, be sure to set PU42 to PU45 to "1".

Figure 4-31. Format of Pull-up Resistor Option Register (78K0/LG3-M)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU1	0	0	0	0	PU13	PU12	PU11	0	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4	0	0	PU45 Note	PU44 Note	PU43 Note	PU42 Note	PU41 Note	PU40 Note	FF34H	00H	R/W
PU8	0	0	0	0	PU83	PU82	PU81	PU80	FF38H	00H	R/W
PU9	0	0	0	0	PU93	PU92	PU91	PU90	FF39H	00H	R/W
PU10	0	0	0	0	PU103	PU102	PU101	PU100	FF3AH	00H	R/W
PU11	0	0	0	0	PU113	PU112	PU111	PU110	FF3BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU13	0	0	0	0	PU133	PU132	PU131	PU130	FF3DH	00H	R/W
PU14	0	0	0	0	PU143	PU142	PU141	PU140	FF3EH	00H	R/W
PU15	0	0	0	0	PU153	PU152	PU151	PU150	FF3FH	00H	R/W
LPU0	0	0	LPU05	LPU04	LPU03	LPU02	LPU01	LPU00	8DH	00H	R/W
LPU1	0	0	LPU15	LPU14	LPU13	LPU12	LPU11	LPU10	90H	00H	R/W

PUmn, LPUxy	Pmn, LPxy on-chip pull-up resistor selection (m = 1, 3, 4, 8 to 15; n = 0 to 5; x = 0, 1; y = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Note For setting when using the segment key scan function, see **18.3 Registers Controlling LCD Controller/Driver**.

(4) Port function register 1 (PF1)

This register sets the pin functions of P13 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 4-32. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	0	0	0	PF13	0	0	0

PF13	Port (P13), CSI10, UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

(5) Port function register 2 (PF2) (78K0/LG3-M only)

This register sets whether to use pins P20 to P27 as port pins (other than segment output pins) or segment output pins.

PF2 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF2 to 00H.

Figure 4-33. Format of Port Function Register 2 (PF2)

Address: FFB5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF2	PF27	PF26	PF25	PF24	PF23	PF22	PF21	PF20

PF2n	Port/segment output specification (n = 0 to 7)
0	Used as port (other than segment output)
1	Used as segment output

(6) Port function register ALL (PFALL)

This register sets whether to use pins P8 to P11 and P13 to P15 as port pins (other than segment output pins) or segment output pins.

PFALL is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PFALL to 00H.

Figure 4-34. Format of Port Function Register ALL (PFALL)

(a) 78K0/LE3-M

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	0	0	PF13ALL	PF11ALL	PF10ALL	PF09ALL	PF08ALL

(b) 78K0/LG3-M

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	PF13ALL	PF11ALL	PF10ALL	PF09ALL	PF08ALL

PFnALL	Port/segment output specification (n = 08 to 11, 13 to 15)
0	Used as port (other than segment output)
1	Used as segment output

(7) A/D port configuration register 0 (ADPC0)

This register switches the P20/ANI0 to P27/ANI7 pins to analog input of A/D converter or digital I/O of port.

ADPC0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 08H.

Figure 4-35. Format of A/D Port Configuration Register 0 (ADPC0)

(a) 78K0/LE3-M

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPC03	0	0	0

ADPC03	Digital I/O (D)/analog input (A) switching
	P27/ANI7
0	A
1	D

(b) 78K0/LG3-M

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPC03	ADPC02	ADPC01	ADPC00

ADPC03	ADPC02	ADPC01	ADPC00	Digital I/O (D)/analog input (A) switching							
				P27 /ANI7	P26 /ANI6	P25 /ANI5	P24 /ANI4	P23 /ANI3	P22 /AN2	P21 /ANI1	P20 /ANI0
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

2. The pin to be set as a digital I/O via ADPC, must not be set via ADS.

3. If data is written to ADPC0, a wait cycle is generated. Do not write data to ADPC0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

4. If pins ANIx/P2x/SEGxx are set to segment output via the PF2 register, output is set to segment output, regardless of the ADPC0 setting (78K0/LG3-M only).

4.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

Caution In the case of 1-bit memory manipulation instruction, although a single bit is manipulated, the port is accessed as an 8-bit unit. Therefore, on a port with a mixture of input and output pins, the output latch contents for pins specified as input are undefined, even for bits other than the manipulated bit.

4.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.
Once data is written to the output latch, it is retained until data is written to the output latch again.

4.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

4.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change.

4.5 Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the PFALL, PF2, PF1, ISC, port mode register, and output latch as shown in Table 4-6 and Table 4-7.

Table 4-6. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (78K0/LE3-M)

Pin Name	Alternate Function		PFALL Note 1	PF1	ISC	PM××	P××
	Function Name	I/O					
P11	$\overline{SCK10}$	Input	–			1	×
		Output	–			0	1
P12	SI10	Input	–			1	×
	RxD0	Input	–			1	×
P13 Note 2	SO10	Output	–	PF13 = 0		0	0
	TxD0	Output	–	PF13 = 1		0	×
	IROUT Note 4	Output	–	PF13 = 1		0	×
P27 Note 3	ANI7	Input	0			1	×
P30	INTP5	Input	–			1	×
P32	TOH0	Output	–			0	0
P33	TI000	Input	–		ISC1 = 0	1	×
	BUZ	Output	–			0	0
	INTP2	Input	–			1	×
P40	KR0	Input	–			1	×
P41	KR1	Input	–			1	×
P80 to P83	SEG4 to SEG7	Output	1			×	×
P90 to P93	SEG8 to SEG11	Output	1			×	×
P100 to P103	SEG12 to SEG15	Output	1			×	×
P110	SEG16	Output	1		ISC3 = 0	×	×
P111	SEG17	Output	1		ISC3 = 0	×	×
P112	SEG18	Output	1		ISC3 = 0	×	×
	TxD6	Output	0		ISC3 = 1	0	1
P113	SEG19	Output	1		ISC3 = 0	×	×
	RxD6	Input	0		ISC3 = 1 Notes 5, 6	1	×
P120	EXLVI	Input	–			1	×
	INTP0	Input	–		ISC0 = 0	1	×
P121	X1 Note 7	–	–			×	×
	OCD0A	–	–			×	×
P122	X2 Note 7	–	–			×	×
	EXCLK Note 7	Input	–			×	×
	OCD0B	–	–			×	×
P130 to P133	SEG20 to SEG23	Output	1			×	×

(**Note** and **Remark** are listed on the next page.)

Notes 1. Targeted at registers corresponding to each port.

2. Set PF13 = 0 when using as port function.

3. The functions of the P27/ANI7 pin is determined according to the settings of A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), and analog input channel specification register (ADS). For details, see Table 4-5.

4. The IROUT function is controlled with the carrier signal (internal signal) generated by TOH1 of 8 bit timer H1.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

7. When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)**. The reset value of OSCCTL is 00H (all of the P121 and P122 are Input port pins).

Remarks 1. ×: Don't care
–: Does not apply.
PM××: Port mode register
P××: Port output latch

2. X1 and X2 pins can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION.**

Table 4-7. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (78K0/LG3-M) (1/2)

Pin Name	Alternate Function		PFALL, PF2[Note 1]	PF1	ISC	PM××	P××
	Function Name	I/O					
P11	$\overline{SCK10}$	Input	–			1	×
		Output	–			0	1
P12	SI10	Input	–			1	×
	RxD0	Input	–			1	×
P13[Note 2]	SO10	Output	–	PF13 = 0		0	0
	TxD0	Output	–	PF13 = 1		0	×
P20 to P27[Note 3]	SEG39 to SEG32	Output	1			×	×
	ANI0 to ANI7	Input	0			1	×
P30	INTP5	Input	–			1	×
P31	TOH1	Output	–			0	0
	INTP3	Input	–			1	×
P32	TOH0	Output	–			0	0
P33	TI000	Input	–		ISC1 = 0	1	×
	BUZ	Output	–			0	0
	INTP2	Input	–			1	×
P40	KR0	Input	–			1	×
P41	KR1	Input	–			1	×
P42	KR2	Input	–			1	×
P43	KR3	Input	–			1	×
	TI51	Input	–			1	×
	TO51	Output	–			0	0
P44	KR4	Input	–			1	×
	TI50	Input	–			1	×
	TO50	Output	–			0	0
P45	KR5	Input	–			1	×
P80 to P83	SEG4 to SEG7	Output	1			×	×
P90 to P93	SEG8 to SEG11	Output	1			×	×
P100 to P103	SEG12 to SEG15	Output	1			×	×
P110	SEG16	Output	1		ISC3 = 0	×	×
P111	SEG17	Output	1		ISC3 = 0	×	×
P112	SEG18	Output	1		ISC3 = 0	×	×
	TxD6	Output	0		ISC3 = 1	0	1
P113	SEG19	Output	1		ISC3 = 0	×	×
	RxD6	Input	0		ISC3 = 1[Notes 4, 5]	1	×

(**Note** and **Remark** are listed on the next page.)

Table 4-7. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (78K0/LG3-M) (2/2)

Pin Name	Alternate Function		PFALL, PF2[Note 1]	PF1	ISC	PM××	P××
	Function Name	I/O					
P120	EXLVI	Input	–			1	×
	INTP0	Input	–		ISC0 = 0	1	×
P121	X1[Note 6]	–	–			×	×
	OCD0A	–	–			×	×
P122	X2[Note 6]	–	–			×	×
	EXCLK[Note 6]	Input	–			×	×
	OCD0B	–	–			×	×
P130 to P133	SEG20 to SEG23	Output	1			×	×
P140 to P143	SEG24 (KS0) to SEG27(KS3)	Output	1			×	×
P150 to P153	SEG28 (KS4) to SEG31 (KS7)	Output	1			×	×
LP01	ZX1[Note 7]	Output	–			0	0
LP02	ZX2[Note 7]	Output	–			0	0

Notes 1. Targeted at registers corresponding to each port.

2. Set PF13 = 0 when using as port function.

3. The functions of the P20/SEG39/ANI0 to P27/SEG32/ANI7 pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), and analog input channel specification register (ADS). For details, see Table 4-5.

4. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

5. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

6. When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)**. The reset value of OSCCTL is 00H (P121 and P122 are Input ports).

7. When using the LP01 and LP02 pins as the zero-crossing signal ZX1 and ZX2 outputs, set the zero-crossing output control bit (ZX1EN and ZX2EN) of the fault detection control register (PQMCTL) to 1.

Remarks 1. ×: Don't care
–: Does not apply.
PM××: Port mode register
P××: Port output latch

2. X1, X2 pins can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION.**

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P20 is an output port, P21 to P27 are input ports (all pin statuses are high level), and the output latch value of port 2 is 00H, if the output of output port P20 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 2 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0/Lx3-M.

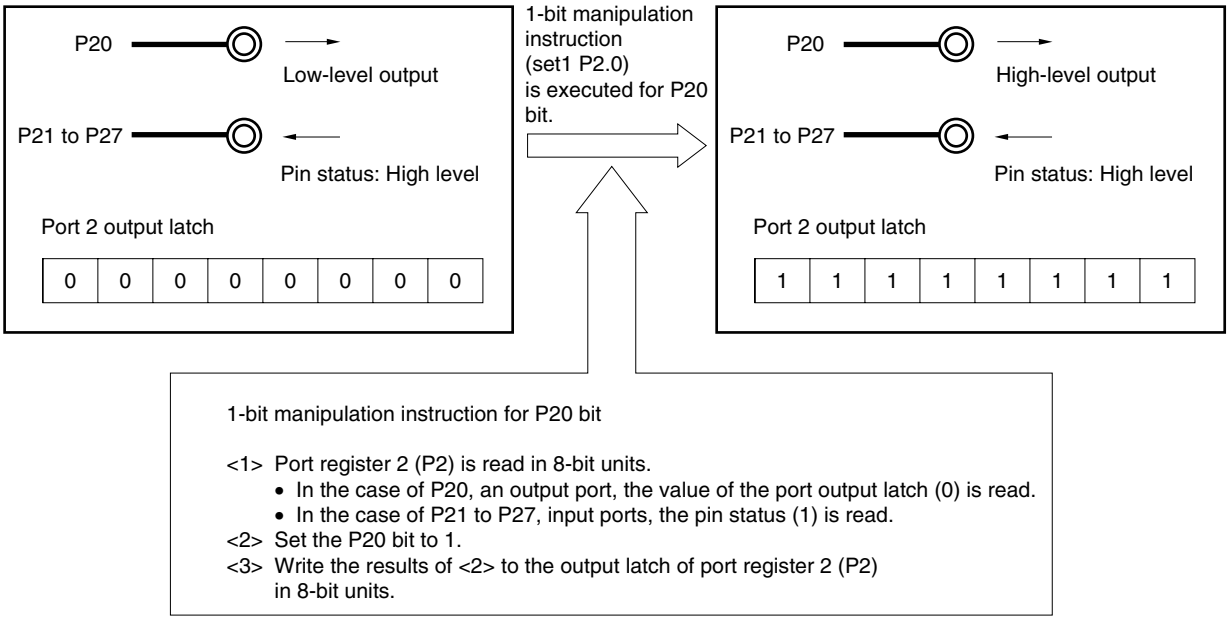
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P20, which is an output port, is read, while the pin statuses of P21 to P27, which are input ports, are read. If the pin statuses of P21 to P27 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-36. Bit Manipulation Instruction (P20)



CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 2 to 10 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or using the main OSC control register (MOC).

<2> Internal high-speed oscillator

This circuit oscillates a clock of f_{RH} = 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or using the internal oscillation mode register (RCM).

An external main system clock (f_{EXCLK} = 2 to 10 MHz) can also be supplied from the OCD0B/EXCLK/X2/P122 pin.
An external main system clock input can be disabled by executing the STOP instruction or using RCM.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by using the main clock mode register (MCM).

Caution A 10 MHz clock is necessary to operate the power calculation circuit and ΔΣ-type A/D converter. Supply a 10 MHz resonator or external clock to the X1 and X2 pins.

<R> **(2) Subsystem clock**

- **Subsystem clock oscillator**

  This circuit oscillates at a frequency of f_{XT} = 32.768 kHz by connecting a 32.768 kHz resonator across XT1 and XT2.

An external subsystem clock (f_{EXCLKS} = 32.768 kHz) can also be supplied from the EXCLKS/XT1 pin.

Remark f_X: X1 clock oscillation frequency
f_{RH}: Internal high-speed oscillation clock frequency
f_{EXCLK}: External main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXCLKS}: External subsystem clock frequency

(3) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

  This circuit oscillates a clock of f_{RL} = 240 kHz (TYP.). After a reset release, the internal low-speed oscillation clock always starts operating.

  Oscillation can be stopped by using the internal oscillation mode register (RCM) when “internal low-speed oscillator can be stopped by software” is set by option byte.

  The internal low-speed oscillation clock cannot be used as the CPU clock. The following hardware operates with the internal low-speed oscillation clock.

  - Watchdog timer
  - 8-bit timer H1 (if f_{RL}, $f_{RL}/2^7$ or $f_{RL}/2^9$ is selected as the count clock)
  - LCD controller/driver (if $f_{RL}/2^3$ is selected as the LCD source clock)

Remark f_{RL}: Internal low-speed oscillation clock frequency

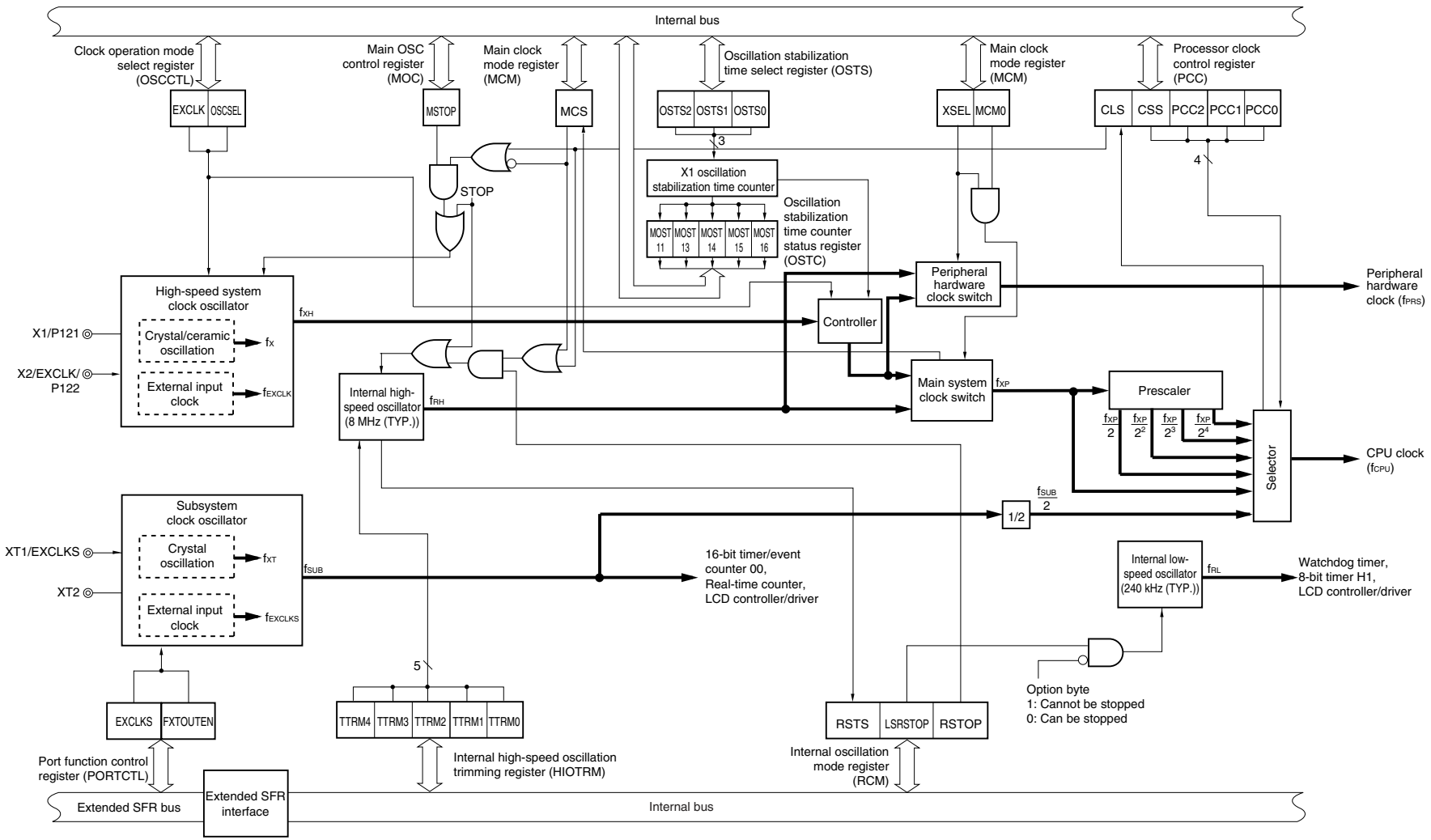
5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode select register (OSCCTL) Port function control register (PORTCTL) Processor clock control register (PCC) Internal oscillation mode register (RCM) Main OSC control register (MOC) Main clock mode register (MCM) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Internal high-speed oscillation trimming register (HIOTRM)
Oscillators	X1 oscillator XT1 oscillator Internal high-speed oscillator Internal low-speed oscillator

Figure 5-1. Block Diagram of Clock Generator



Remark f_X: X1 clock oscillation frequency
f_{RH}: Internal high-speed oscillation clock frequency
f_{EXCLK}: External main system clock frequency
f_{XH}: High-speed system clock frequency
f_{XP}: Main system clock frequency
f_{PRS}: Peripheral hardware clock frequency
f_{CPU}: CPU clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXCLKS}: External subsystem clock frequency
f_{SUB}: Subsystem clock frequency
f_{RL}: Internal low-speed oscillation clock frequency

5.3 Registers Controlling Clock Generator

The following nine registers are used to control the clock generator.

- Clock operation mode select register (OSCCTL)
- Port function control register (PORTCTL)
- Processor clock control register (PCC)
- Internal oscillation mode register (RCM)
- Main OSC control register (MOC)
- Main clock mode register (MCM)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- Internal high-speed oscillation trimming register (HIOTRM)

(1) Clock operation mode select register (OSCCTL)

This register selects the operation modes of the high-speed system and subsystem clocks, and the gain of the on-chip oscillator.

OSCCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-2. Format of Clock Operation Mode Select Register (OSCCTL)

Address: FF9FH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
OSCCTL	EXCLK	OSCSEL	EXCLKS[Note]	OSCSELS[Note]	0	0	0	0

EXCLK	OSCSEL	High-speed system clock pin operation mode	P121/X1 pin	P122/X2/EXCLK pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Note For the setting of EXCLKS and OSCSELS, see **(4) Setting of operation mode for subsystem clock pin**.

Cautions 1. To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).

2. Be sure to clear bits 3 to 0 to "0".

Remark f_{XH}: High-speed system clock oscillation frequency

(2) Port function control register (PORTCTL)

This register controls the operation mode of subsystem clock.

PORTCTL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 5-3. Format of Port Function Control Register (PORTCTL)

Address: 91H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PORTCTL	SUBSTAT	0	0	0	0	0	EXCLKS2	FXTOUTEN

SUBSTAT	Oscillation stabilization status flag for subsystem clock
0	Pin reset status
1	After a pin reset release, this flag is set after the oscillation stabilization time for the subsystem clock (2^{16} (2 sec at 32.768 kHz)) elapses.

EXCLKS2	Set up subsystem clock
0	Connects a resonator.
1	Inputs an external clock signal.

FXTOUTEN	Specify whether to enable or disable output from subsystem clock oscillator
0	Disables output from subsystem clock oscillator.
1	Enables output from subsystem clock oscillator.

Cautions 1. Only rewrite the value of EXCLKS2 after clearing the RTCE bit of the FXTOUTEN and RTCC0 registers to 0 (FXTOUTEN = 0, RTCE = 0).

2. After a reset release, the resonator connection mode (EXCLKS2 = 0) cannot be specified after specifying the external clock input mode (EXCLKS2 = 1).

3. If the resonator connection mode is selected, be sure to set FXTOUTEN to 1 (to enable sub-clock oscillation) and RTCE to 1 (to enable RTC operation) after the oscillation stabilization time for the subsystem clock has elapsed (SUBSTAT = 1).

(3) Processor clock control register (PCC)

This register is used to select the CPU clock, the division ratio, and operation mode for subsystem clock.

PCC is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PCC to 01H.

Figure 5-4. Format of Processor Clock Control Register (PCC)

Address: FFFBH After reset: 01H R/W[Note]

Symbol	7	6	<5>	<4>	3	2	1	0
PCC	0	0	CLS	CSS	0	PCC2	PCC1	PCC0

CLS	CPU clock status
0	Main system clock
1	Subsystem clock

CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection
0	0	0	0	f_{XP}
	0	0	1	$f_{XP}/2$ (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
1	0	0	0	$f_{SUB}/2$
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Other than above				Setting prohibited

Note Bit 5 is read-only.

Cautions 1. Be sure to clear bits 3, 6, and 7 to "0".

2. The peripheral hardware clock (f_{PRS}) is not divided when the division ratio of the PCC is set.

Remarks 1. f_{XP}: Main system clock oscillation frequency

2. f_{SUB}: Subsystem clock oscillation frequency

The fastest instruction can be executed in 2 clocks of the CPU clock in the 78K0/Lx3-M microcontrollers. Therefore, the relationship between the CPU clock (f_{CPU}) and the minimum instruction execution time is as shown in Table 5-2.

Table 5-2. Relationship Between CPU Clock and Minimum Instruction Execution Time

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$		
	Main System Clock		Subsystem Clock
	High-Speed System Clock[Note]	Internal High-Speed Oscillation Clock[Note]	
	At 10 MHz Operation	At 8 MHz (TYP.) Operation	At 32.768 kHz Operation
f_{XP}	0.2 μs	0.25 μs (TYP.)	–
$f_{XP}/2$	0.4 μs	0.5 μs (TYP.)	–
$f_{XP}/2^2$	0.8 μs	1.0 μs (TYP.)	–
$f_{XP}/2^3$	1.6 μs	2.0 μs (TYP.)	–
$f_{XP}/2^4$	3.2 μs	4.0 μs (TYP.)	–
$f_{SUB}/2$	–	–	122.1 μs

Note The main clock mode register (MCM) is used to set the main system clock supplied to CPU clock (high-speed system clock/internal high-speed oscillation clock) (see **Figure 5-7**).

(4) Setting of operation mode for subsystem clock pin

The operation mode for the subsystem clock pin can be set by using bits 5 and 4 (EXCLKS and OSCSELS) of the clock operation mode select register (OSCCTL) and bits 1 and 0 (EXCLKS2 and FXTOUTEN) of the port function control register (PORTCTL) in combination.

<R> **Table 5-3. Whether Subsystem Clock Can Be Used**

OSCCTL		Subsystem Clock
Bit 5	Bit 4	
EXCLKS	OSCSELS	
0	0	Using disabled[Note]
0	1	Setting prohibited
1	0	
1	1	Using enabled

Note Only the real-time counter can be used.

Caution Confirm that bit 5 (CLS) of the processor clock control register (PCC) is 0 (CPU is operating with main system clock) when changing the current values of EXCLKS and OSCSELS.

Table 5-4. Whether Subsystem Clock Can Be Used and Setting of Operation Mode for Subsystem Clock Pin

PORTCTL		Subsystem Clock	Subsystem Clock Pin Operation Mode	XT1/EXCLKS Pin	XT2 Pin
Bit 1	Bit 0				
EXCLKS2	FXTOUTEN				
0	0	Using disabled[Note 1]	XT1 oscillation mode	Crystal resonator connection	
0	1	Using enabled			
1	0	Using disabled[Note 1]	External clock input mode	External clock input	**Note 2**
1	1	Using enabled			

Notes 1. Only the real-time counter can be used.

2. Leave the XT2 pin open when the XT1/EXCLKS pin is used as external system clock input.

Cautions 1. To use the subsystem clock, sets EXCLKS and OSCSELS bits of OSCCTL register and EXCLKS2 and FXTOUTEN bits of PORTCTL register.

2. Do not rewrite EXCLKS bit of OSCCTL register and EXCLKS2 and FXTOUTEN bits of PORTCTL register when the CPU clock operates with the subsystem clock.

(5) Internal oscillation mode register (RCM)

This register sets the operation mode of internal oscillator.

RCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H[Note 1].

Figure 5-5. Format of Internal Oscillation Mode Register (RCM)

Address: FFA0H After reset: 80H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
RCM	RSTS	0	0	0	0	0	LSRSTOP	RSTOP

RSTS	Status of internal high-speed oscillator
0	Waiting for accuracy stabilization of internal high-speed oscillator
1	Stability operating of internal high-speed oscillator

LSRSTOP	Internal low-speed oscillator oscillating/stopped
0	Internal low-speed oscillator oscillating
1	Internal low-speed oscillator stopped

RSTOP	Internal high-speed oscillator oscillating/stopped
0	Internal high-speed oscillator oscillating
1	Internal high-speed oscillator stopped

Notes 1. The value of this register is 00H immediately after a reset release but automatically changes to 80H after internal high-speed oscillator has been stabilized.

2. Bit 7 is read-only.

Caution When setting RSTOP to 1, be sure to confirm that the CPU operates with a clock other than the internal high-speed oscillation clock. Specifically, set under either of the following conditions.

- **When MCS = 1 (when CPU operates with the high-speed system clock)**
- **When CLS = 1 (when CPU operates with the subsystem clock)**

In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock before setting RSTOP to 1.

(6) Main OSC control register (MOC)

This register selects the operation mode of the high-speed system clock.

This register is used to stop the X1 oscillator or to disable an external clock input from the EXCLK pin when the CPU operates with a clock other than the high-speed system clock.

MOC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H.

Figure 5-6. Format of Main OSC Control Register (MOC)

Address: FFA2H After reset: 80H R/W

Symbol	<7>	6	5	4	3	2	1	0
MOC	MSTOP	0	0	0	0	0	0	0

MSTOP	Control of high-speed system clock operation	
	X1 oscillation mode	External clock input mode
0	X1 oscillator operating	External clock from EXCLK pin is enabled
1	X1 oscillator stopped	External clock from EXCLK pin is disabled

Cautions 1. When setting MSTOP to 1, be sure to confirm that the CPU operates with a clock other than the high-speed system clock. Specifically, set under either of the following conditions.

- **When MCS = 0 (when CPU operates with the internal high-speed oscillation clock)**
- **When CLS = 1 (when CPU operates with the subsystem clock)**

In addition, stop peripheral hardware that is operating on the high-speed system clock before setting MSTOP to 1.

2. Do not clear MSTOP to 0 while bit 6 (OSCSEL) of the clock operation mode select register (OSCCTL) is 0 (I/O port mode).

3. The peripheral hardware cannot operate when the peripheral hardware clock is stopped. To resume the operation of the peripheral hardware after the peripheral hardware clock has been stopped, initialize the peripheral hardware.

(7) Main clock mode register (MCM)

This register selects the main system clock supplied to CPU clock and clock supplied to peripheral hardware clock.

MCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-7. Format of Main Clock Mode Register (MCM)

Address: FFA1H After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	<2>	<1>	<0>
MCM	0	0	0	0	0	XSEL	MCS	MCM0

XSEL	MCM0	Selection of clock supplied to main system clock and peripheral hardware	
		Main system clock (f_{XP})	Peripheral hardware clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})
1	1	High-speed system clock (f_{XH})	

MCS	Main system clock status
0	Operates with internal high-speed oscillation clock
1	Operates with high-speed system clock

Note Bit 1 is read-only.

Cautions 1. XSEL can be changed only once after a reset release.

2. Do not rewrite MCM0 when the CPU clock operates with the subsystem clock.

3. A clock other than f_{PRS} is supplied to the following peripheral functions regardless of the setting of XSEL and MCM0.

- **Watchdog timer (operates with internal low-speed oscillation clock)**
- **When "f_{RL}", "$f_{RL}/2^7$", or "$f_{RL}/2^9$" is selected as the count clock for 8-bit timer H1 (operates with internal low-speed oscillation clock)**
- **When "$f_{RL}/2^3$" is selected as the LCD source clock for LCD controller/driver (operates with internal low-speed oscillation clock)**
- **Peripheral hardware selects the external clock as the clock source (Except when the external count clock of TM00 is selected (TI000 pin valid edge))**

(8) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock or subsystem clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

Figure 5-8. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFA3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16

MOST 11	MOST 13	MOST 14	MOST 15	MOST 16	Oscillation stabilization time status			
						f_X = 2 MHz	f_X = 5 MHz	f_X = 10 MHz
1	0	0	0	0	$2^{11}/f_X$ min.	1.02 ms min.	409.6 μs min.	204.8 μs min.
1	1	0	0	0	$2^{13}/f_X$ min.	4.10 ms min.	1.64 ms min.	819.2 μs min.
1	1	1	0	0	$2^{14}/f_X$ min.	8.19 ms min.	3.27 ms min.	1.64 ms min.
1	1	1	1	0	$2^{15}/f_X$ min.	16.38 ms min.	6.55 ms min.	3.27 ms min.
1	1	1	1	1	$2^{16}/f_X$ min.	32.77 ms min.	13.11 ms min.	6.55 ms min.

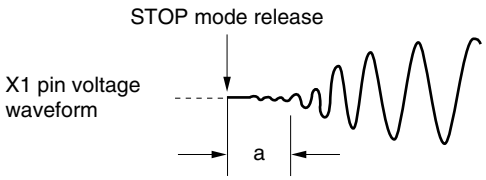
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

• Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

(9) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 5-9. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection			
				fx = 2 MHz	fx = 5 MHz	fx = 10 MHz
0	0	1	2^{11}/fx	1.02 ms	409.6 μs	204.8 μs
0	1	0	2^{13}/fx	4.10 ms	1.64 ms	819.2 μs
0	1	1	2^{14}/fx	8.19 ms	3.27 ms	1.64 ms
1	0	0	2^{15}/fx	16.38 ms	6.55 ms	3.27 ms
1	0	1	2^{16}/fx	32.77 ms	13.11 ms	6.55 ms
Other than above			Setting prohibited			

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

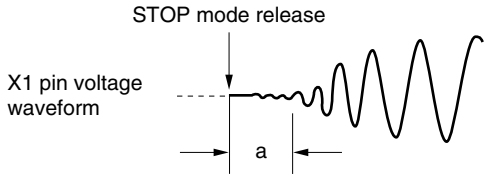
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

• Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

(10) Internal high-speed oscillation trimming register (HIOTRM)

This register corrects the accuracy of the internal high-speed oscillator. The accuracy can be corrected by self-measuring the frequency of the internal high-speed oscillator, using a subsystem clock using a crystal resonator or using a timer with high-accuracy external clock input, such as a real-time counter.

HIOTRM can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets HIOTRM to 10H.

Caution If the temperature or V_{DD} pin voltage is changed after accuracy correction, the frequency will fluctuate. Also, if a value other than the initial value (10H) is set to the HIOTRM register, the oscillation accuracy of the internal high-speed oscillation clock may exceed the MIN. and MAX. values described in CHAPTER 33 ELECTRICAL SPECIFICATIONS due to the subsequent fluctuation in the temperature or V_{DD} voltage, or HIOTRM register setting value. If the temperature or V_{DD} voltage fluctuates, accuracy correction must be executed either before frequency accuracy will be required or regularly.

Figure 5-10. Format of Internal High-speed Oscillation Trimming Register (HIOTRM)

Address: FF30H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	0	TTRM4	TTRM3	TTRM2	TTRM1	TTRM0

TTRM4	TTRM3	TTRM2	TTRM1	TTRM0	Clock correction value (2.5 V ≤ VDD ≤ 3.6 V)		
					MIN.	TYP.	MAX.
0	0	0	0	0	–5.54%	–4.88%	–4.02%
0	0	0	0	1	–5.28%	–4.62%	–3.76%
0	0	0	1	0	–4.99%	–4.33%	–3.47%
0	0	0	1	1	–4.69%	–4.03%	–3.17%
0	0	1	0	0	–4.39%	–3.73%	–2.87%
0	0	1	0	1	–4.09%	–3.43%	–2.57%
0	0	1	1	0	–3.79%	–3.13%	–2.27%
0	0	1	1	1	–3.49%	–2.83%	–1.97%
0	1	0	0	0	–3.19%	–2.53%	–1.67%
0	1	0	0	1	–2.88%	–2.22%	–1.36%
0	1	0	1	0	–2.23%	–1.91%	–1.31%
0	1	0	1	1	–1.92%	–1.60%	–1.28%
0	1	1	0	0	–1.60%	–1.28%	–0.96%
0	1	1	0	1	–1.28%	–0.96%	–0.64%
0	1	1	1	0	–0.96%	–0.64%	–0.32%
0	1	1	1	1	–0.64%	–0.32%	±0%
1	0	0	0	0	±0% (default)		
1	0	0	0	1	±0%	+0.32%	+0.64%
1	0	0	1	0	+0.33%	+0.65%	+0.97%
1	0	0	1	1	+0.66%	+0.98%	+1.30%
1	0	1	0	0	+0.99%	+1.31%	+1.63%
1	0	1	0	1	+1.32%	+1.64%	+1.96%
1	0	1	1	0	+1.38%	+1.98%	+2.30%
1	0	1	1	1	+1.46%	+2.32%	+2.98%
1	1	0	0	0	+1.80%	+2.66%	+3.32%
1	1	0	0	1	+2.14%	+3.00%	+3.66%
1	1	0	1	0	+2.48%	+3.34%	+4.00%
1	1	0	1	1	+2.83%	+3.69%	+4.35%
1	1	1	0	0	+3.18%	+4.04%	+4.70%
1	1	1	0	1	+3.53%	+4.39%	+5.05%
1	1	1	1	0	+3.88%	+4.74%	+5.40%
1	1	1	1	1	+4.24%	+5.10%	+5.76%

Caution The internal high-speed oscillation frequency will increase in speed if the HIOTRM register value is incremented above a specific value, and will decrease in speed if decremented below that specific value. A reversal, such that the frequency decreases in speed by incrementing the value, or increases in speed by decrementing the value, will not occur.

5.4 System Clock Oscillator

5.4.1 X1 oscillator

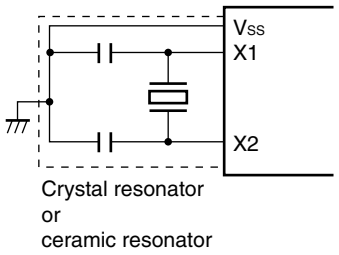
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (2 to 10 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

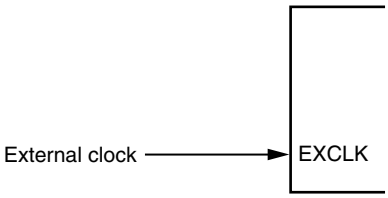
Figure 5-11 shows an example of the external circuit of the X1 oscillator.

Figure 5-11. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



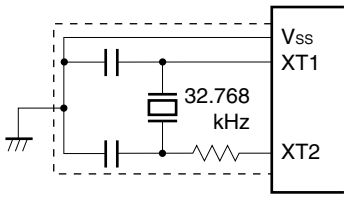
5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

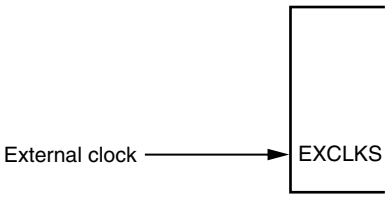
Figure 5-12 shows an example of the external circuit of the XT1 oscillator.

Figure 5-12. Example of External Circuit of XT1 Oscillator

(a) Crystal oscillation



(b) External clock



Cautions 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figure 5-11 and Figure 5-12 to avoid an adverse effect from wiring capacitance.

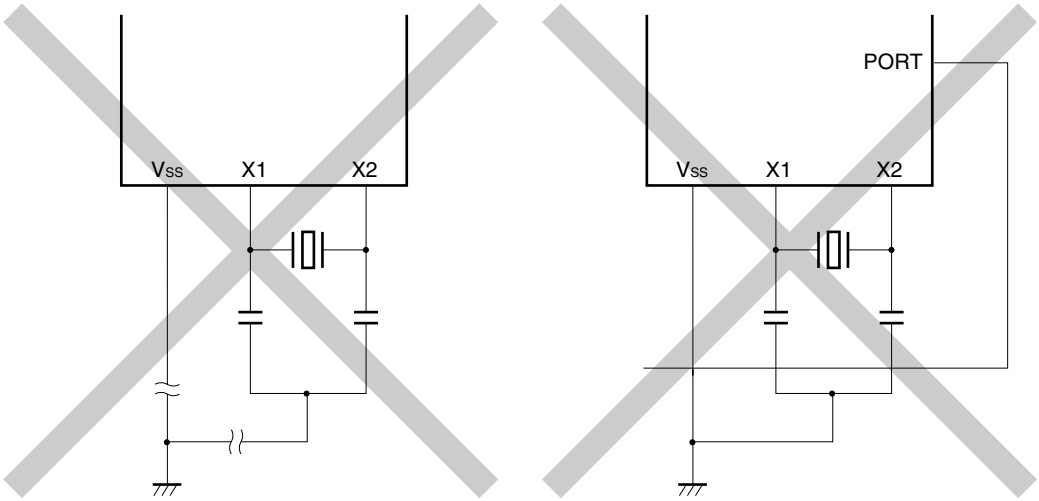
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as VSS. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Note that the XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption.

Figure 5-13 shows examples of incorrect resonator connection.

Figure 5-13. Examples of Incorrect Resonator Connection (1/2)

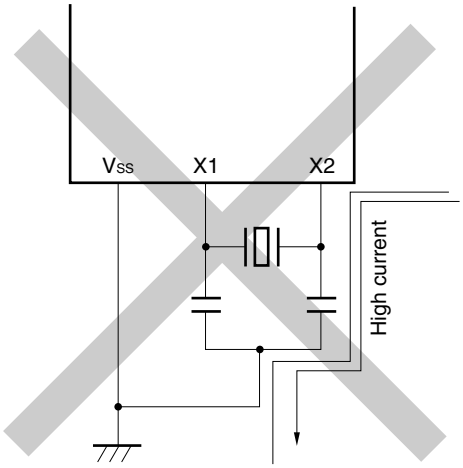
(a) Too long wiring **(b) Crossed signal line**



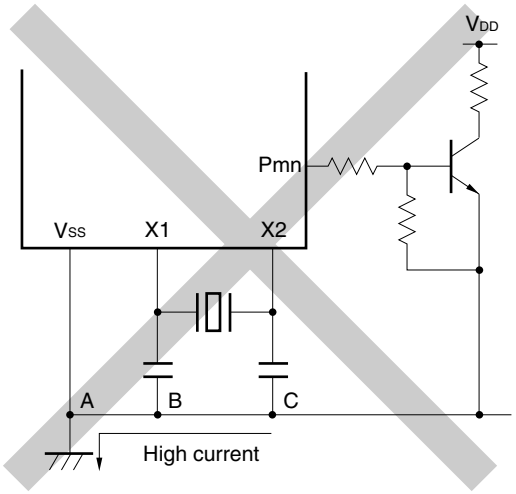
Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Figure 5-13. Examples of Incorrect Resonator Connection (2/2)

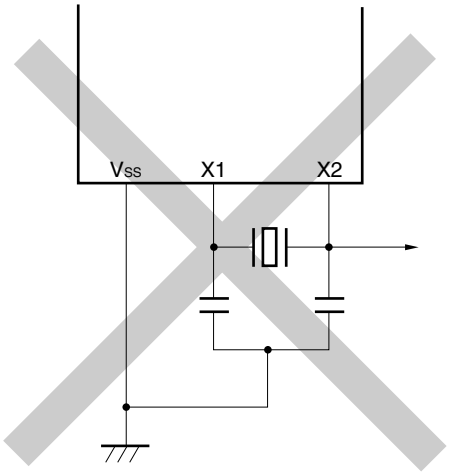
(c) Wiring near high alternating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(e) Signals are fetched



Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Cautions 2. When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

5.4.3 When subsystem clock is not used

<R> If it is not necessary to use the subsystem clock for low power consumption or timer operations, connect the XT1 pin to V_{DD} or V_{SS} via a resistor, and leave the XT2 pin open.

5.4.4 Internal high-speed oscillator

The internal high-speed oscillator is incorporated in the 78K0/Lx3-M microcontrollers. Oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal high-speed oscillator automatically starts oscillation (8 MHz (TYP.)).

5.4.5 Internal low-speed oscillator

The internal low-speed oscillator is incorporated in the 78K0/Lx3-M microcontrollers.

The internal low-speed oscillation clock is only used as the clock of the watchdog timer, 8-bit timer H1, and LCD controller/driver. The internal low-speed oscillation clock cannot be used as the CPU clock.

“Can be stopped by software” or “Cannot be stopped” can be selected by the option byte. When “Can be stopped by software” is set, oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal low-speed oscillator automatically starts oscillation, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation is enabled using the option byte.

5.4.6 Prescaler

The prescaler generates various clocks by dividing the main system clock when the main system clock is selected as the clock to be supplied to the CPU.

5.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5-1**).

- Main system clock f_{XP}
  - High-speed system clock f_{XH}
    X1 clock f_X
    External main system clock f_{EXCLK}
  - Internal high-speed oscillation clock f_{RH}
- Subsystem clock f_{SUB}
  - XT1 clock f_{XT}
  - External subsystem clock f_{EXCLKS}
- Internal low-speed oscillation clock f_{RL}
- CPU clock f_{CPU}
- Peripheral hardware clock f_{PRS}

The CPU starts operation when the internal high-speed oscillator starts outputting after a reset release in the 78K0/Lx3-M microcontrollers, thus enabling the following.

(1) Enhancement of security function

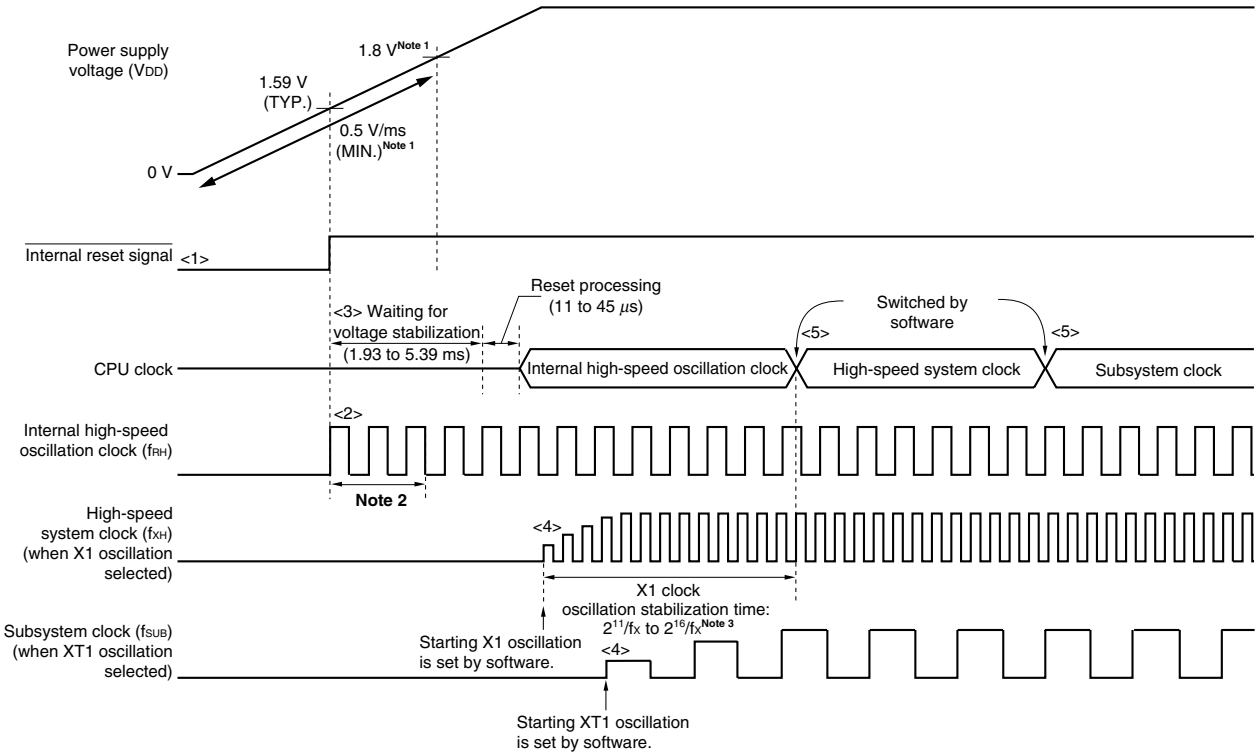
When the X1 clock is set as the CPU clock by the default setting, the device cannot operate if the X1 clock is damaged or badly connected and therefore does not operate after reset is released. However, the start clock of the CPU is the internal high-speed oscillation clock, so the device can be started by the internal high-speed oscillation clock after a reset release. Consequently, the system can be safely shut down by performing a minimum operation, such as acknowledging a reset source by software or performing safety processing when there is a malfunction.

(2) Improvement of performance

Because the CPU can be started without waiting for the X1 clock oscillation stabilization time, the total performance can be improved.

When the power supply voltage is turned on, the clock generator operation is shown in Figure 5-14.

Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.59 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> When the power supply voltage rises with a slope of 0.5 V/ms (MIN.), the CPU starts operation on the internal high-speed oscillation clock after the reset is released and after the stabilization times for the voltage of the power supply and regulator have elapsed, and then reset processing is performed.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Notes 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using the option byte (POCMODE = 1) (see **Figure 5-15**). When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 1.8 V, the CPU operates with the same timing as <2> and thereafter in Figure 5-14, after the reset has been released by the $\overline{\text{RESET}}$ pin.

2. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

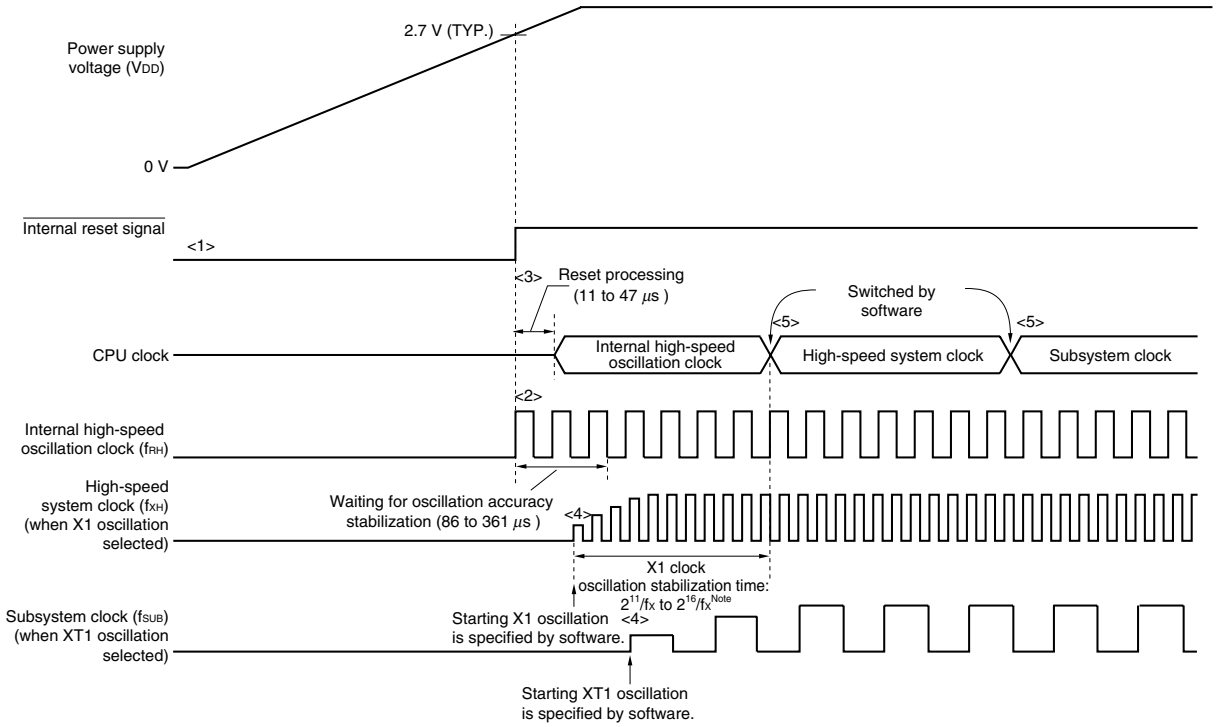
3. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Caution It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing

the STOP instruction (see **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**, and **(4)** in **5.6.3 Example of controlling subsystem clock**).

Figure 5-15. Clock Generator Operation When Power Supply Voltage Is Turned On (When 2.7 V/1.59 V POC Mode Is Set (Option Byte: POCMODE = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 2.7 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Note When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Cautions 1. A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the time the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) is within 1.93 to 5.39 ms, a power supply stabilization wait time of 0 to 5.39 ms occurs automatically before reset processing, and the reset processing time becomes 19 to 80 μs.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (see **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2**

Example of controlling internal high-speed oscillation clock, and **(4)** in **5.6.3 Example of controlling subsystem clock**).

5.5.1 Notes on supplying power supply voltage

Note the following when supplying power supply voltage to the 78K0/Lx3-M microcontroller:

<1> Be sure to supply power in the following order: LV_{DD}, V_{DD}/AV_{DD}, and then AV_{REF}.

<2> After V_{DD} reaches the operating voltage, input a high-level signal to the $\overline{RESET}$ pin.

5.5.2 Notes on settings after reset release

After a reset release, be sure to specify the following settings:

<1> Enable output (PM10 = 0) for PM10 (bit 0 of the PM1 register), and then use the clock output selection register (CKS) to select the output clock.

<2> Enable output for PM47, PM46, PM17, PM16, and PM14 (PM47, PM46, PM17, PM16, PM14 = 0).

<3> Cancel the pull-down status (by setting the PUTCTL register to 01H).

Caution If an internal reset is triggered while using the extended SFR interface to transmit data, the data might not be correctly transmitted to an extended SFR.

5.5.3 Note when V_{DD} is detected to be 0 V

If V_{DD} is detected to be 0 V (SAG detection or EXLVI detection), be sure to specify 59H for the real-time counter mode register (RTCMD).

5.6 Controlling Clock

5.6.1 Example of controlling high-speed system clock

The following two types of high-speed system clocks are available.

- X1 clock: Crystal/ceramic resonator is connected across the X1 and X2 pins.
- External main system clock: External clock is input to the EXCLK pin.

When the high-speed system clock is not used, the OCD0A/X1/P121 and OCD0B/X2/EXCLK/P122 pins can be used as I/O port pins.

Caution The OCD0A/X1/P121 and OCD0B/X2/EXCLK/P122 pins are in the I/O port mode after a reset release.

The following describes examples of setting procedures for the following cases.

(1) When oscillating X1 clock
(2) When using external main system clock
(3) When using high-speed system clock as CPU clock and peripheral hardware clock
(4) When stopping high-speed system clock

(1) Example of setting procedure when oscillating the X1 clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting X1 clock or external clock (OSCCTL register)
When EXCLK is cleared to 0 and OSCSEL is set to 1, the mode is switched from port mode to X1 oscillation mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	

<2> Controlling oscillation of X1 clock (MOC register)
If MSTOP is cleared to 0, the X1 oscillator starts oscillating.

<3> Waiting for the stabilization of the oscillation of X1 clock
Check the OSTC register and wait for the necessary time.
During the wait time, other software processing can be executed with the internal high-speed oscillation clock.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 33 ELECTRICAL SPECIFICATIONS).

(2) Example of setting procedure when using the external main system clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting operation mode (OSCCTL register)
When EXCLK and OSCSEL are set to 1, the mode is switched from port mode to external clock input mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
1	1	External clock input mode	I/O port	External clock input

<2> Controlling external main system clock input (MOC register)
When MSTOP is cleared to 0, the input of the external main system clock is enabled.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the external main system clock is operating.
2. Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 33 ELECTRICAL SPECIFICATIONS).

(3) Example of setting procedure when using high-speed system clock as CPU clock and peripheral hardware clock

<1> Setting high-speed system clock oscillation[Note]
(See **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when high-speed system clock is already operating.

<2> Setting the high-speed system clock as the main system clock (MCM register)
When XSEL and MCM0 are set to 1, the high-speed system clock is supplied as the main system clock and peripheral hardware clock.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
1	1	High-speed system clock (f_{XH})	High-speed system clock (f_{XH})

Caution If the high-speed system clock is selected as the main system clock, a clock other than the high-speed system clock cannot be set as the peripheral hardware clock.

<3> Setting the main system clock as the CPU clock and selecting the division ratio (PCC register)
When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	$f_{XP}/2$ (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

(4) Example of setting procedure when stopping the high-speed system clock

The high-speed system clock can be stopped in the following two ways.

- Executing the STOP instruction and stopping the X1 oscillation (disabling clock input if the external clock is used)
- Setting MSTOP to 1 and stopping the X1 oscillation (disabling clock input if the external clock is used)

(a) To execute a STOP instruction

<1> Setting to stop peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, see **CHAPTER 25 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and X1 oscillation is stopped (the input of the external clock is disabled).

(b) To stop X1 oscillation (disabling external clock input) by setting MSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the high-speed system clock. When CLS = 0 and MCS = 1, the high-speed system clock is supplied to the CPU, so change the CPU clock to the subsystem clock or internal high-speed oscillation clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the high-speed system clock (MOC register)

When MSTOP is set to 1, X1 oscillation is stopped (the input of the external clock is disabled).

Caution Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.

5.6.2 Example of controlling internal high-speed oscillation clock

The following describes examples of clock setting procedures for the following cases.

(1) When restarting oscillation of the internal high-speed oscillation clock
(2) When using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock
(3) When stopping the internal high-speed oscillation clock

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)
When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)
Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

(2) Example of setting procedure when using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock

<1>
- Restarting oscillation of the internal high-speed oscillation clock[Note]
(See **5.6.2 (1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock**).
- Oscillating the high-speed system clock[Note]
(This setting is required when using the high-speed system clock as the peripheral hardware clock. See **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when the internal high-speed oscillation clock or high-speed system clock is already operating.

<2> Selecting the clock supplied as the main system clock and peripheral hardware clock (MCM register)
Set the main system clock and peripheral hardware clock using XSEL and MCM0.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})

<3> Selecting the CPU clock division ratio (PCC register)
When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	f_{XP}/2 (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

(3) Example of setting procedure when stopping the internal high-speed oscillation clock

The internal high-speed oscillation clock can be stopped in the following two ways.

- Executing the STOP instruction to set the STOP mode
- Setting RSTOP to 1 and stopping the internal high-speed oscillation clock

(a) To execute a STOP instruction

<1> Setting of peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, see **CHAPTER 25 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed. To operate the CPU immediately after the STOP mode has been released, cleared MCM0 to 0, switch the CPU clock to the internal high-speed oscillation clock, and check that RSTS is 1.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and internal high-speed oscillation clock is stopped.

(b) To stop internal high-speed oscillation clock by setting RSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the internal high-speed oscillation clock.

When CLS = 0 and MCS = 0, the internal high-speed oscillation clock is supplied to the CPU, so change the CPU clock to the high-speed system clock or subsystem clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the internal high-speed oscillation clock (RCM register)

When RSTOP is set to 1, internal high-speed oscillation clock is stopped.

Caution Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.

5.6.3 Example of controlling subsystem clock

The following two types of subsystem clocks are available.

- XT1 clock: Crystal/ceramic resonator is connected across the XT1 and XT2 pins.
- External subsystem clock: External clock is input to the EXCLKS pin.

Caution Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

The following describes examples of setting procedures for the following cases.

(1) When oscillating XT1 clock
(2) When using external subsystem clock
(3) When using subsystem clock as CPU clock
(4) When stopping subsystem clock

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PORTCTL register)
When EXCLKS2 and FXTOUTEN are set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

EXCLKS2	FXTOUTEN	Operation Mode of Subsystem Clock Pin	XT1/EXCLKS Pins	XT2 Pin
0	0	XT1 oscillation mode	Crystal/ceramic resonator connection	
0	1			

<2> Waiting for the stabilization of the subsystem clock oscillation
Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the values of EXCLKS2 and FXOUTEN while the subsystem clock is operating.

(2) Example of setting procedure when using the external subsystem clock

<1> Setting XT1 and XT2 pins, selecting XT1 clock/external clock and controlling oscillation (PORTCTL registers)
When EXCLKS2 and FXTOUTEN are set as any of the following, the mode is switched from port mode to external clock input mode. In this case, input the external clock to the EXCLKS/XT1 pins.

EXCLKS2	FXTOUTEN	Operation Mode of Subsystem Clock Pin	XT1/EXCLKS Pins	XT2 Pin
1	0	External clock input mode	External clock input mode	**Note**
1	1			

Note Leave the XT2 pin open when the XT1/EXCLKS pin is used as external system clock input.

Caution Do not change the values of EXCLKS2 and FXOUTEN while the subsystem clock is operating.

(3) Example of setting procedure when using the subsystem clock as the CPU clock

<1> Setting subsystem clock oscillation[Note]

(See **5.6.3 (1) Example of setting procedure when oscillating the XT1 clock** and **(2) Example of setting procedure when using the external subsystem clock**)

Note The setting of <1> is not necessary when while the subsystem clock is operating.

<2> Setting operation mode (OSCCTL register)

Set EXCLKS and OSCSELS bits of the OSCCTL register to 1.

<3> Switching the CPU clock (PCC register)

When CSS is set to 1, the subsystem clock is supplied to the CPU.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
1	0	0	0	f_{SUB}/2
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
	Other than above			Setting prohibited

(4) Example of setting procedure when stopping the subsystem clock

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the subsystem clock.

When CLS = 1, the subsystem clock is supplied to the CPU, so change the CPU clock to the internal high-speed oscillation clock or high-speed system clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the subsystem clock (OSCCTL register)

<R> When OSCSELS and EXCLKS are cleared to 0, the subsystem clock can no longer be used, but the real-time counter can be. Note that XT1 oscillation does not stop.

Cautions 1. Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the peripheral hardware if it is operating on the subsystem clock.

2. The subsystem clock oscillation cannot be stopped using the STOP instruction.

5.6.4 Example of controlling internal low-speed oscillation clock

The internal low-speed oscillation clock cannot be used as the CPU clock.

Only the following peripheral hardware can operate with this clock.

- Watchdog timer
- 8-bit timer H1 (if f_{RL}, $f_{RL}/2^7$ or $f_{RL}/2^9$ is selected as the count clock)
- LCD controller/driver (if $f_{RL}/2^3$ is selected as the LCD source clock)

In addition, the following operation modes can be selected by the option byte.

- Internal low-speed oscillator cannot be stopped
- Internal low-speed oscillator can be stopped by software

The internal low-speed oscillator automatically starts oscillation after a reset release, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation has been enabled by the option byte.

(1) Example of setting procedure when stopping the internal low-speed oscillation clock

<1> Setting LSRSTOP to 1 (RCM register)

When LSRSTOP is set to 1, the internal low-speed oscillation clock is stopped.

(2) Example of setting procedure when restarting oscillation of the internal low-speed oscillation clock

<1> Clearing LSRSTOP to 0 (RCM register)

When LSRSTOP is cleared to 0, the internal low-speed oscillation clock is restarted.

Caution If "Internal low-speed oscillator cannot be stopped" is selected by the option byte, oscillation of the internal low-speed oscillation clock cannot be controlled.

5.6.5 Clocks supplied to CPU and peripheral hardware

The following table shows the relation among the clocks supplied to the CPU and peripheral hardware, and setting of registers.

Table 5-5. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting

Supplied Clock		XSEL	CSS	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware				
Internal high-speed oscillation clock		0	0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0	0
	External main system clock	1	0	0	1
X1 clock		1	0	1	0
External main system clock		1	0	1	1
Subsystem clock	Internal high-speed oscillation clock	0	1	×	×
	X1 clock	1	1	0	0
		1	1	1	0
	External main system clock	1	1	0	1
		1	1	1	1

Remarks 1. XSEL: Bit 2 of the main clock mode register (MCM)

2. CSS: Bit 4 of the processor clock control register (PCC)

3. MCM0: Bit 0 of MCM

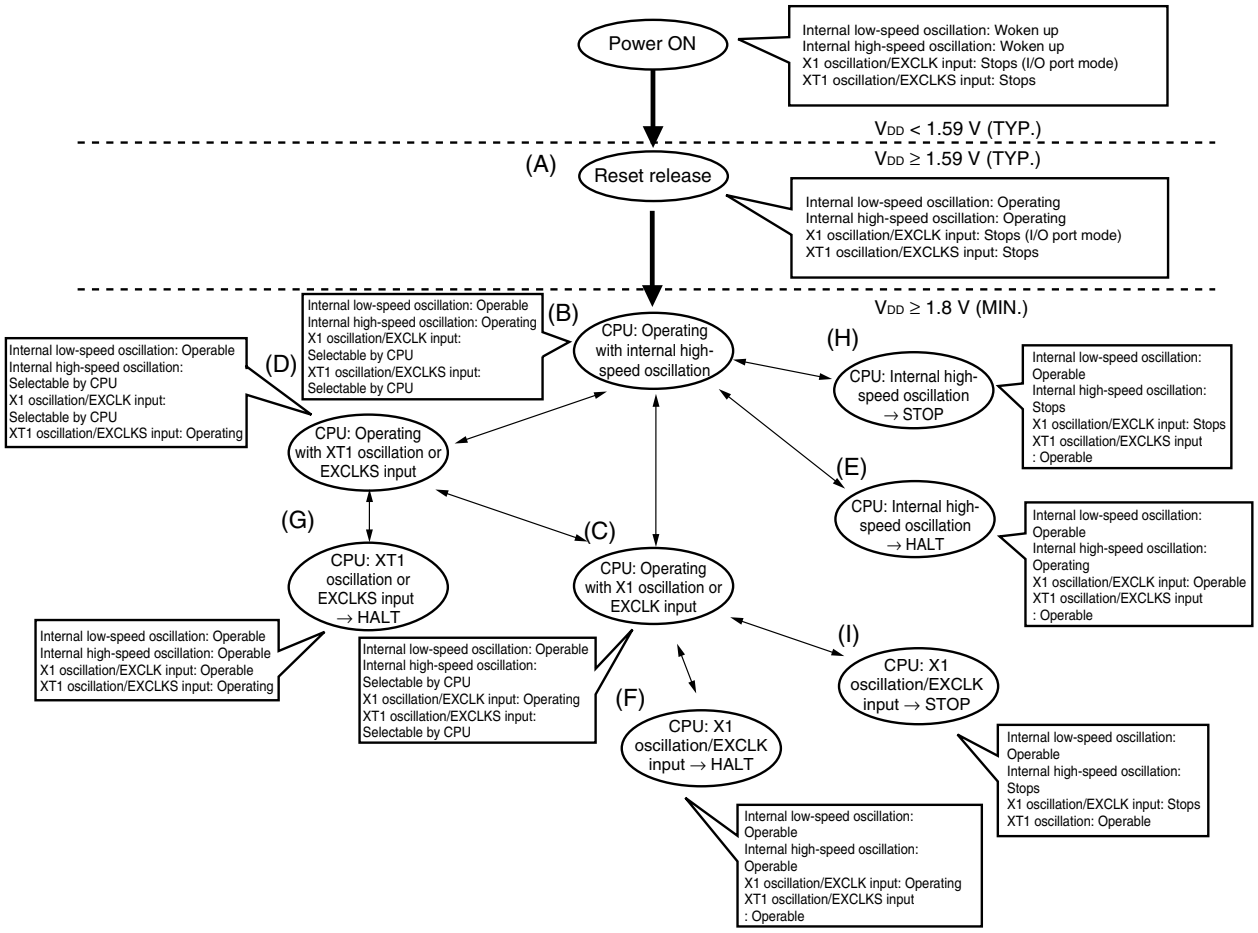
4. EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)

5. ×: don't care

5.6.6 CPU clock status transition diagram

Figure 5-16 shows the CPU clock status transition diagram of this product.

Figure 5-16. CPU Clock Status Transition Diagram
(When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))



Remark In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 2.7 V (TYP.), and to (B) after reset processing (11 to 47 μs (TYP.)).

Table 5-6 shows transition of the CPU clock and examples of setting the SFR registers.

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (1/4)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL	MCM0
(A) → (B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(A) → (B) → (C) (external main clock)	1	1	0	Must not be checked	1	1

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 33 ELECTRICAL SPECIFICATIONS).

(3) CPU operating with subsystem clock (D) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLKS2	FXTOUTEN	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(A) → (B) → (D) (XT1 clock)	0	1	1	1	Necessary	1
(A) → (B) → (D) (external subsystem clock)	1	1	1	1	Unnecessary	1

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-16.

2. EXCLK, OSCSEL, EXCLKS, OSCSELS:
Bits 7 to 4 of the clock operation mode select register (OSCCTL)

MSTOP: Bit 7 of the main OSC control register (MOC)

XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)

CSS: Bit 4 of the processor clock control register (PCC)

EXCLKS2, FXTOUTEN:
Bits 1 and 0 of port function control register (PORTCTL)

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (2/4)

(4) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(B) → (C) (external main clock)	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 33 ELECTRICAL SPECIFICATIONS).

(5) CPU clock changing from internal high-speed oscillation clock (B) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLKS2	FXTOUTEN	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(B) → (D) (XT1 clock)	0	1	1	1	Necessary	1
(B) → (D) (external subsystem clock)	1	1	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-16.

2. EXCLK, OSCSEL, EXCLKS, OSCSELS:
Bits 7 to 4 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)
EXCLKS2, FXTOUTEN:
Bits 1 and 0 of port function control register (PORTCTL)

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (3/4)

(6) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers)

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLKS2	FXTOUTEN	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(C) → (D) (XT1 clock)	0	1	1	1	Necessary	1
(C) → (D) (external subsystem clock)	1	1	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0	CSS
(D) → (B)	0	Confirm this flag is 1.	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

↑

Unnecessary if XSEL is 0

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-16.

2. MCM0: Bit 0 of the main clock mode register (MCM)
EXCLKS, OSCSELS: Bits 5 and 4 of the clock operation mode select register (OSCCTL)
RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)
CSS: Bit 4 of the processor clock control register (PCC)
EXCLKS2, FXTOUTEN: Bits 1 and 0 of port function control register (PORTCTL)

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (4/4)

(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0	CSS
(D) → (C) (X1 clock)	0	1	0	Must be checked	1	1	0
(D) → (C) (external main clock)	1	1	0	Must not be checked	1	1	0

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 33 ELECTRICAL SPECIFICATIONS).

(10) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
• HALT mode (F) set while CPU is operating with high-speed system clock (C)
• HALT mode (G) set while CPU is operating with subsystem clock (D)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G)	Executing HALT instruction

(11) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

Status Transition	Setting	
(B) → (H) (C) → (I)	Stopping peripheral functions that cannot operate in STOP mode	Executing STOP instruction

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-16.

2. EXCLK, OSCSEL: Bits 7 and 6 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)

5.6.7 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5-7. Changing CPU Clock

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time	• Internal high-speed oscillator can be stopped (RSTOP = 1).
	External main system clock	Enabling input of external clock from EXCLK pin • MSTOP = 0, OSCSEL = 1, EXCLK = 1	
X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • RSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
Internal high-speed oscillation clock	XT1 clock	Stabilization of XT1 oscillation (SUBSTAT = 1) • EXCLKS2 = 0, FXTOUTEN = 1 • EXCLKS = 1, OSCSELS = 1	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
X1 clock			X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
Internal high-speed oscillation clock	External subsystem clock	Enabling input of external clock from EXCLKS pin • EXCLKS2 =1, FXTOUTEN = 1 • EXCLKS = 1, OSCSELS = 1	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
X1 clock			X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
XT1 clock, external subsystem clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • RSTOP = 0, MCS = 0	XT1 oscillation can be stopped or external subsystem clock input can be disabled (OSCSELS = 0).
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 1 • MCS = 1	

5.6.8 Time required for switchover of CPU clock and main system clock

By setting bits 0 to 2 (PCC0 to PCC2) and bit 4 (CSS) of the processor clock control register (PCC), the CPU clock can be switched (between the main system clock and the subsystem clock) and the division ratio of the main system clock can be changed.

The actual switchover operation is not performed immediately after rewriting to PCC; operation continues on the pre-switchover clock for several clocks (see **Table 5-8**).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 5 (CLS) of the PCC register.

Table 5-8. Time Required for Switchover of CPU Clock and Main System Clock Cycle Division Factor

Set Value Before Switchover				Set Value After Switchover																							
CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0
				0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	×	×	×
0	0	0	0					16 clocks				16 clocks				16 clocks				16 clocks				$2f_{XP}/f_{SUB}$ clocks			
	0	0	1	8 clocks								8 clocks				8 clocks				8 clocks				f_{XP}/f_{SUB} clocks			
	0	1	0	4 clocks				4 clocks								4 clocks				4 clocks				$f_{XP}/2f_{SUB}$ clocks			
	0	1	1	2 clocks				2 clocks				2 clocks								2 clocks				$f_{XP}/4f_{SUB}$ clocks			
	1	0	0	1 clock				1 clock				1 clock				1 clock								$f_{XP}/8f_{SUB}$ clocks			
1	×	×	×	2 clocks				2 clocks				2 clocks				2 clocks				2 clocks							

Caution Selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the main system clock to the subsystem clock (changing CSS from 0 to 1) should not be set simultaneously.

Simultaneous setting is possible, however, for selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the subsystem clock to the main system clock (changing CSS from 1 to 0).

Remarks 1. The number of clocks listed in Table 5-8 is the number of CPU clocks before switchover.

2. When switching the CPU clock from the main system clock to the subsystem clock, calculate the number of clocks by rounding up to the next clock and discarding the decimal portion, as shown below.

Example When switching CPU clock from $f_{XP}/2$ to $f_{SUB}/2$ (@ oscillation with f_{XP} = 10 MHz, f_{SUB} = 32.768 kHz)

f_{XP}/f_{SUB} = 10000/32.768 ≅ 305.1 → 306 clocks

By setting bit 0 (MCM0) of the main clock mode register (MCM), the main system clock can be switched (between the internal high-speed oscillation clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to MCM0; operation continues on the pre-switchover clock for several clocks (see **Table 5-9**).

Whether the CPU is operating on the internal high-speed oscillation clock or the high-speed system clock can be ascertained using bit 1 (MCS) of MCM.

Table 5-9. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		1 + 2f_{RH}/f_{XH} clock
1	1 + 2f_{XH}/f_{RH} clock	

Caution 1. When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

2. Do not rewrite MCM0 when the CPU clock operates with the subsystem clock.

Remarks 1. The number of clocks listed in Table 5-9 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-9 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{RH} = 8 MHz, f_{XH} = 10 MHz)

$1 + 2f_{RH}/f_{XH} = 1 + 2 \times 8/10 = 1 + 2 \times 0.8 = 1 + 1.6 = 2.6 \rightarrow 2$ clocks

5.6.9 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-10. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	RSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
XT1 clock External subsystem clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	OSCSELS = 0

5.6.10 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/Lx3-M microcontrollers.

Remark The peripheral hardware depends on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

Table 5-11. Peripheral Hardware and Source Clocks

Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Subsystem Clock (f_{SUB})	Internal Low-Speed Oscillation Clock (f_{RL})	TM50 Output	TM52 Output	TMH1 Output	External Clock from Peripheral Hardware Pins
16-bit timer/ event counter	00	Y	Y	N	N	Y	N	Y (TI000 pin)[Note]
8-bit timer/ event counter	50	Y	N	N	N	N	N	Y (TI50 pin)[Note]
	51	Y	N	N	N	N	Y	Y (TI51 pin)[Note]
	52	Y	N	N	N	N	N	N
8-bit timer	H0	Y	N	N	Y	N	N	N
	H1	Y	N	Y	N	N	N	N
	H2	Y	N	N	N	N	N	N
Real-time counter		N	Y	N	N	N	N	N
Watchdog timer		N	N	Y	N	N	N	N
Buzzer output		Y	N	N	N	N	N	N
Successive approximation type A/D converter		Y	N	N	N	N	N	N
ΔΣ-type A/D converter		Y	N	N	N	N	N	N
Serial interface	UART0	Y	N	N	Y	N	N	N
	UART6	Y	N	N	Y	N	N	N
	CSI10	Y	N	N	N	N	N	Y ($\overline{SCK10}$ pin)[Note]
Extended SFR interface		Y	N	N	N	N	N	N
LCD controller/driver		Y	Y	Y	N	N	N	N
Power calculation circuit		Y	N	N	N	N	N	N
Power quality measurement circuit		Y	N	N	N	N	N	N
Digital frequency conversion circuit		Y	N	N	N	N	N	N

Note Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Remark Y: Can be selected, N: Cannot be selected

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 is mounted onto all 78K0/Lx3-M microcontroller products.

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates an interrupt request at the preset time interval.

(2) External event counter

16-bit timer/event counter 00 can measure the number of pulses of an externally input signal.

(3) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

6.2 Configuration of 16-Bit Timer/Event Counter 00

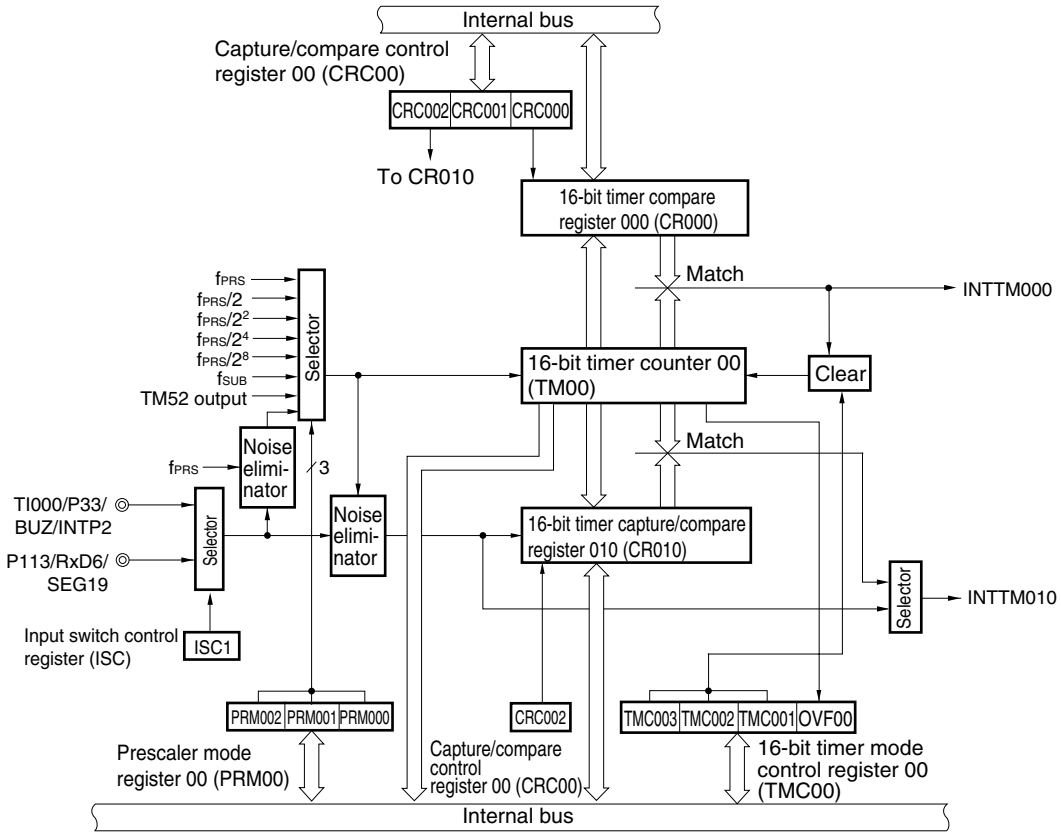
16-bit timer/event counter 00 includes the following hardware.

Table 6-1. Configuration of 16-Bit Timer/Event Counter 00

Item	Configuration
Time/counter	16-bit timer counter 00 (TM00)
Register	16-bit timer compare register 000 (CR000) 16-bit timer capture/compare register 010 (CR010)
Timer input	TI000 pin
Timer output	Output controller
Control registers	16-bit timer mode control register 00 (TMC00) Capture/compare control register 00 (CRC00) Prescaler mode register 00 (PRM00) Input switch control register (ISC) Port mode register 3 (PM3) Port register 3 (P3)

Figure 6-1 shows the block diagram.

Figure 6-1. Block Diagram of 16-Bit Timer/Event Counter 00



Cautions 1. If clearing of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) to 00 and input of the capture trigger conflict, then the captured data is undefined.

2. To change the mode from the capture mode to the comparison mode, first clear the TMC003 and TMC002 bits to 00, and then change the setting.

A value that has been once captured remains stored in CR000 unless the device is reset. If the mode has been changed to the comparison mode, be sure to set a comparison value.

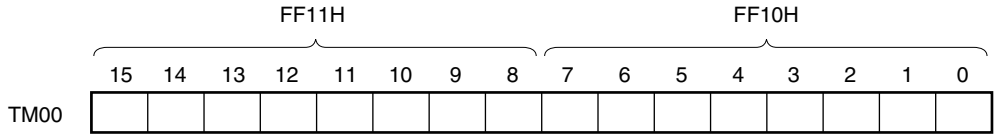
(1) 16-bit timer counter 00 (TM00)

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 6-2. Format of 16-Bit Timer Counter 00 (TM00)

Address: FF10H, FF11H After reset: 0000H R



The count value of TM00 can be read by reading TM00 when the value of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) is other than 00. The value of TM00 is 0000H if it is read when TMC003 and TMC002 = 00.

The count value is reset to 0000H in the following cases.

- At reset signal generation
- If TMC003 and TMC002 are cleared to 00
- If the valid edge of the TI000 pin is input in the mode in which the clear & start occurs when inputting the valid edge to the TI000 pin
- If TM00 and CR000 match in the mode in which the clear & start occurs when TM00 and CR000 match

Caution Even if TM00 is read, the value is not captured by CR010.

(2) 16-bit timer compare register 000 (CR000), 16-bit timer capture/compare register 010 (CR010)

CR000 is 16-bit registers that is only used with a compare function.

CR010 is 16-bit registers that is used with a capture function or comparison function selected by using CRC00.

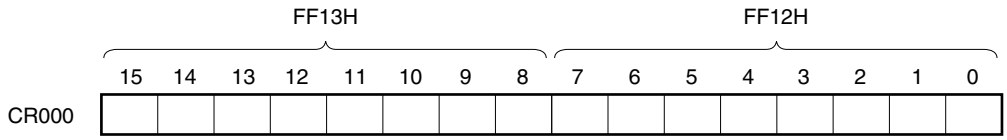
Change the value of CR000 while the timer is stopped (TMC003 and TMC002 = 00).

These registers can be read or written in 16-bit units.

Reset signal generation sets these registers to 0000H.

Figure 6-3. Format of 16-Bit Timer Compare Register 000 (CR000)

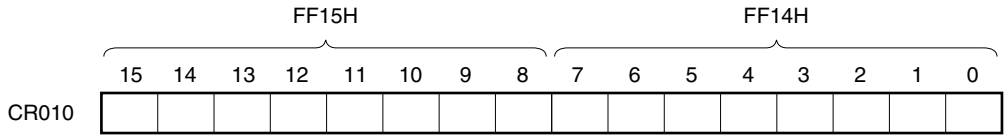
Address: FF12H, FF13H After reset: 0000H R/W



The value set in CR000 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM000) is generated if they match. The value is held until CR000 is rewritten.

Figure 6-4. Format of 16-Bit Timer Capture/Compare Register 010 (CR010)

Address: FF14H, FF15H After reset: 0000H R/W



(i) When CR010 is used as a compare register

The value set in CR010 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM010) is generated if they match.

Caution CR010 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR010 is used as a capture register

The count value of TM00 is captured to CR010 when a capture trigger is input.

It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 pin valid edge is set by PRM00.

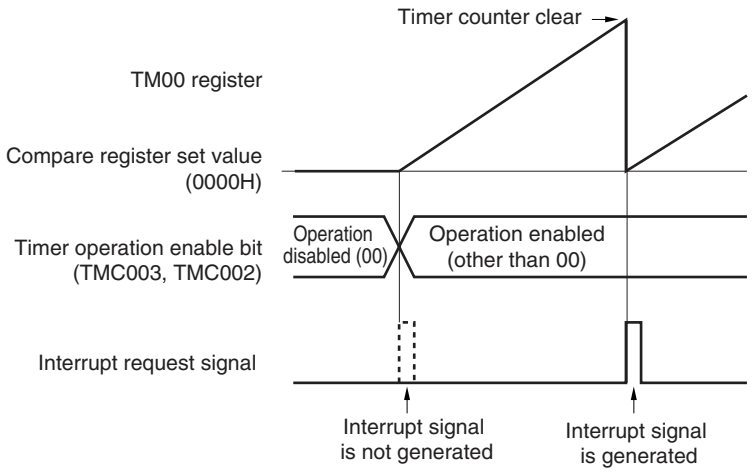
(iii) Setting range when CR000 or CR010 is used as a compare register

When CR000 or CR010 is used as a compare register, set it as shown below.

Operation	CR000 Register Setting Range	CR010 Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM010).
Operation as external event counter		
Operation in the clear & start mode entered by TI000 pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM00 register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI000 pin valid edge (when clear & start mode is entered by TI000 pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM00 and CR000 (CR000 = other than 0000H, CR010 = 0000H))



Remarks 1. N: CR000 register set value, M: CR010 register set value

2. For details of TMC003 and TMC002, see **6.3 (1) 16-bit timer mode control register 00 (TMC00)**.

Table 6-2. Capture Operation of CR010

External Input Signal / Capture Operation	TI000 Pin Input	
Capture operation of CR010	TI000 pin input[Note]	Set values of ES001 and ES000 Position of edge to be captured
		01: Rising
		00: Falling
		11: Both edges
	Interrupt signal	INTTM010 signal is generated each time value is captured.

Note The capture operation of CR010 is not affected by the setting of the CRC001 bit.

Caution To capture the count value of the TM00 register to the CR000 register by using the phase reverse to that input to the TI000 pin, the interrupt request signal (INTTM000) is not generated after the value has been captured.

Remark CRC001: See **6.3 (2) Capture/compare control register 00 (CRC00)**.
ES101, ES100, ES001, ES000: See **6.3 (3) Prescaler mode register 00 (PRM00)**.

6.3 Registers Controlling 16-Bit Timer/Event Counter 00

Registers used to control 16-bit timer/event counter 00 are shown below.

- 16-bit timer mode control register 00 (TMC00)
- Capture/compare control register 00 (CRC00)
- Prescaler mode register 00 (PRM00)
- Input switch control register (ISC)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) 16-bit timer mode control register 00 (TMC00)

TMC00 is an 8-bit register that sets the 16-bit timer/event counter 00 operation mode, TM00 clear mode, and output timing, and detects an overflow.

Rewriting TMC00 is prohibited during operation (when TMC003 and TMC002 = other than 00). However, it can be changed when TMC003 and TMC002 are cleared to 00 (stopping operation) and when OVF00 is cleared to 0.

TMC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets TMC00 to 00H.

Caution 16-bit timer/event counter 00 starts operation at the moment TMC002 and TMC003 are set to values other than 00 (operation stop mode), respectively. Set TMC002 and TMC003 to 00 to stop the operation.

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FFBAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	0	OVF00

TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

Note The TI000 pin valid edge is set by bits 5 and 4 (ES001, ES000) of prescaler mode register 00 (PRM00).

(2) Capture/compare control register 00 (CRC00)

CRC00 is the register that controls the operation of CR000 and CR010.

Changing the value of CRC00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

CRC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

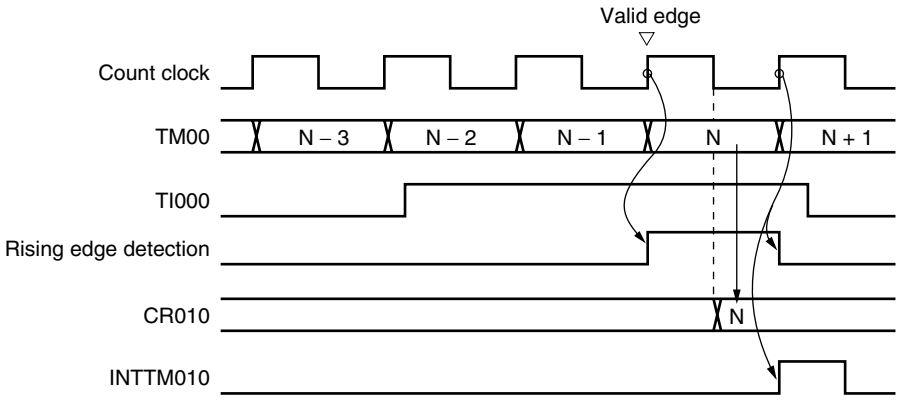
Address: FFBCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	0	0

CRC002	CR010 operating mode selection
0	Operates as compare register
1	Operates as capture register

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by prescaler mode register 00 (PRM00).

Figure 6-7. Example of CR010 Capture Operation (When Rising Edge Is Specified)



(3) Prescaler mode register 00 (PRM00)

PRM00 is the register that sets the TM00 count clock and TI000 pin input valid edges.

Rewriting PRM00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

PRM00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PRM00 to 00H.

Cautions 1. Do not apply the following setting when setting the PRM001 and PRM000 bits to 11 (to specify the valid edge of the TI000 pin as a count clock).

- **Clear & start mode entered by the TI000 pin valid edge**
- **Setting the TI000 pin as a capture trigger**

2. If the operation of the 16-bit timer/event counter 00 is enabled when the TI000 pin is at high level and when the valid edge of the TI000 pin is specified to be the rising edge or both edges, the high level of the TI000 pin is detected as a rising edge. Note this when the TI000 pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.

Figure 6-8. Format of Prescaler Mode Register 00 (PRM00)

Address: FFBBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	0	0	ES001	ES000	0	PRM002	PRM001	PRM000

ES001	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM002	PRM001	PRM000	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^4$	1.25 MHz	2.5 MHz	625 kHz
1	0	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	0	1	f_{SUB}	32.768 kHz		
1	1	0	TI000 valid edge[Notes 3, 4]			
1	1	1	TM52 output			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of PRM002 = PRM001 = PRM000 = 0 (count clock: f_{PRS}) is prohibited.

3. The external clock from the TI000 pin requires a pulse longer than twice the cycle of the peripheral hardware clock (f_{PRS}).

4. Do not start timer operation with the external clock from the TI000 pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Caution Do not select the valid edge of TI000 as the count clock during the pulse width measurement.

Remarks 1. 8-bit timer/event counter 52 (TM52) output can be selected as the TM00 count clock by setting PRM002, PRM001, PRM000 = 1, 1, 1. Any frequency can be set as the 16-bit timer (TM00) count clock, depending on the TM52 count clock and compare register setting values.

2. f_{PRS}: Peripheral hardware clock frequency
f_{SUB}: Subsystem clock frequency

(4) Input switch control register (ISC)

The input source to TI000 becomes the input signal from the P33/TI000 pin, by setting ISC1 to 0.

ISC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISC to 00H.

Figure 6-9. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	ICS3	0	ICS1	ICS0

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P113)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P113)

(5) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P33/TI000/BUZ/INTP2 pin for timer input, set PM33 to 1. At this time, the output latch of P33 may be 0 or 1.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 6-10. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

If bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register (TMC00) are set to 11 (clear & start mode entered upon a match between TM00 and CR000), the count operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H and a match interrupt signal (INTTM000) is generated. This INTTM000 signal enables TM00 to operate as an interval timer.

Remarks 1. For the setting of I/O pins, see **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 6-11. Block Diagram of Interval Timer Operation

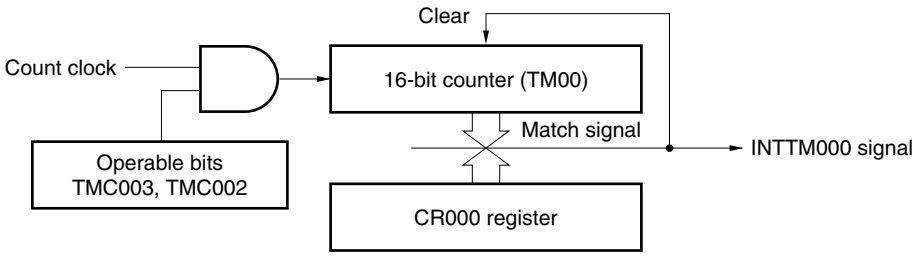


Figure 6-12. Basic Timing Example of Interval Timer Operation

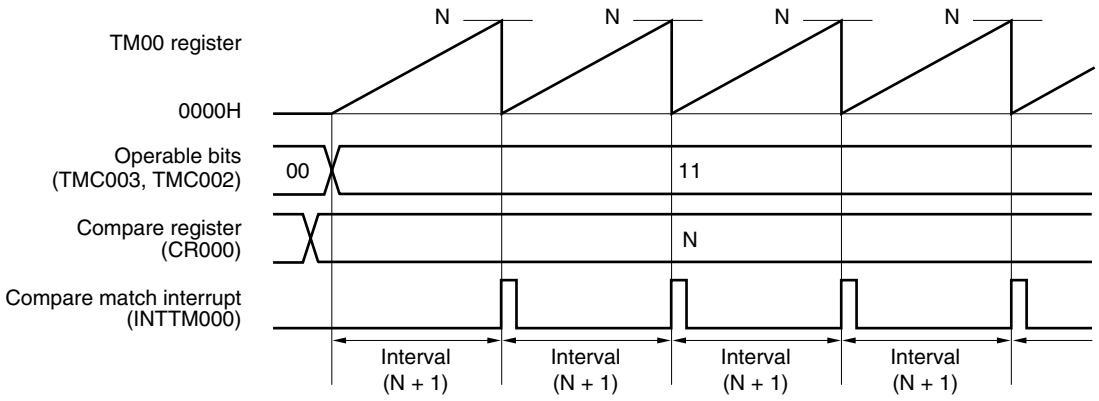
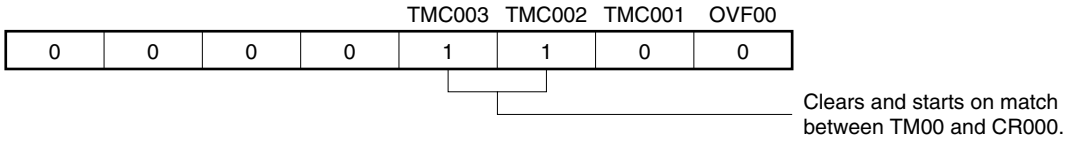
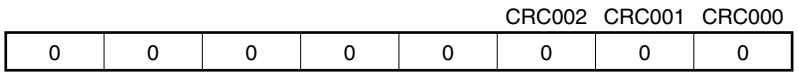


Figure 6-13. Example of Register Settings for Interval Timer Operation

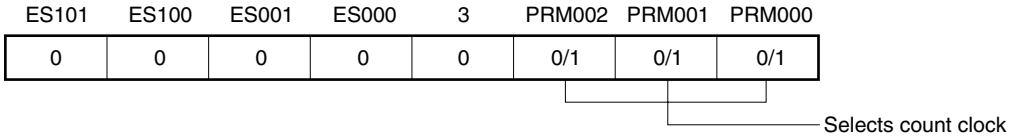
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(e) 16-bit compare register 000 (CR000)

If M is set to CR000, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

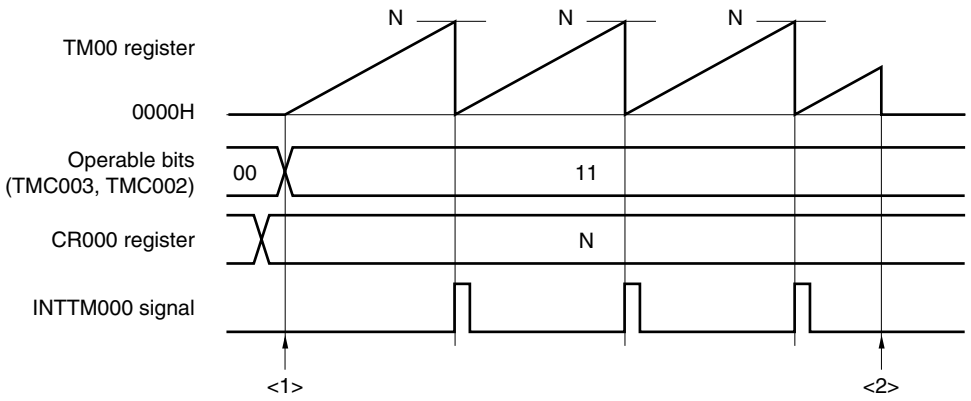
Setting CR000 to 0000H is prohibited.

(f) 16-bit capture/compare register 010 (CR010)

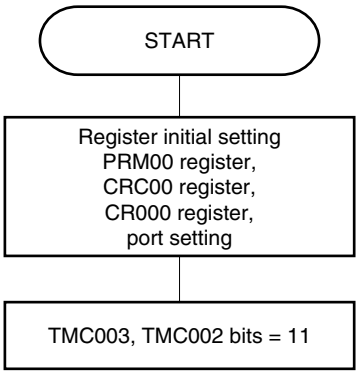
Usually, CR010 is not used for the interval timer function. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-14. Example of Software Processing for Interval Timer Function



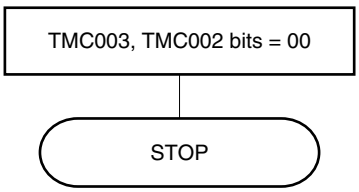
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

6.4.2 External event counter operation

When bits 1 and 0 (PRM001 and PRM000) of the prescaler mode register 00 (PRM00) are set to 11 (for counting up with the valid edge of the TI000 pin) and bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11, the valid edge of an external event input is counted, and a match interrupt signal indicating matching between TM00 and CR000 (INTTM000) is generated.

To input the external event, the TI000 pin is used. Therefore, the timer/event counter cannot be used as an external event counter in the clear & start mode entered by the TI000 pin valid edge input (when TMC003 and TMC002 = 10).

The INTTM000 signal is generated with the following timing.

- Timing of generation of INTTM000 signal (second time or later)
  = Number of times of detection of valid edge of external event × (Set value of CR000 + 1)

However, the first match interrupt immediately after the timer/event counter has started operating is generated with the following timing.

- Timing of generation of INTTM000 signal (first time only)
  = Number of times of detection of valid edge of external event input × (Set value of CR000 + 2)

To detect the valid edge, the signal input to the TI000 pin is sampled during the clock cycle of f_{PRS}. The valid edge is not detected until it is detected two times in a row. Therefore, a noise with a short pulse width can be eliminated.

Remarks 1. For the setting of I/O pins, see **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 6-15. Block Diagram of External Event Counter Operation

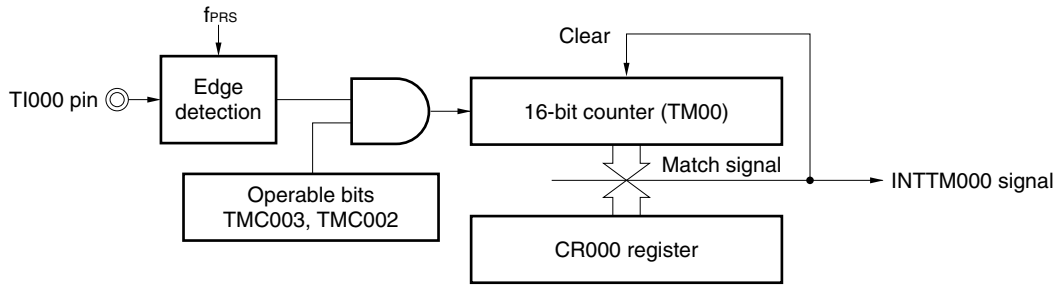
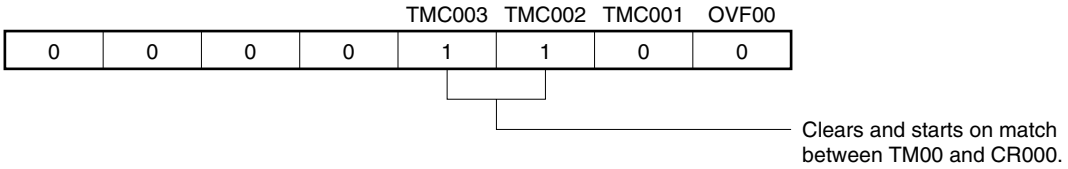
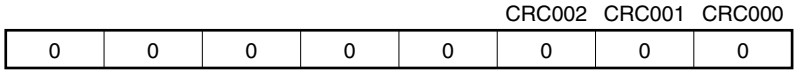


Figure 6-16. Example of Register Settings in External Event Counter Mode

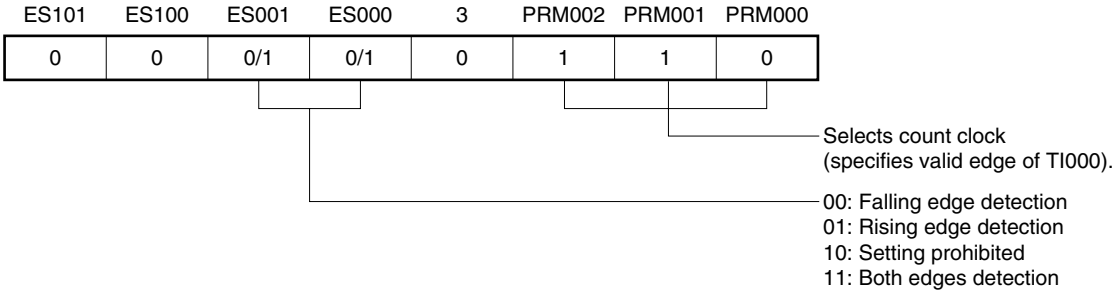
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(e) 16-bit compare register 000 (CR000)

If M is set to CR000, the interrupt signal (INTTM000) is generated when the number of external events reaches (M + 1).

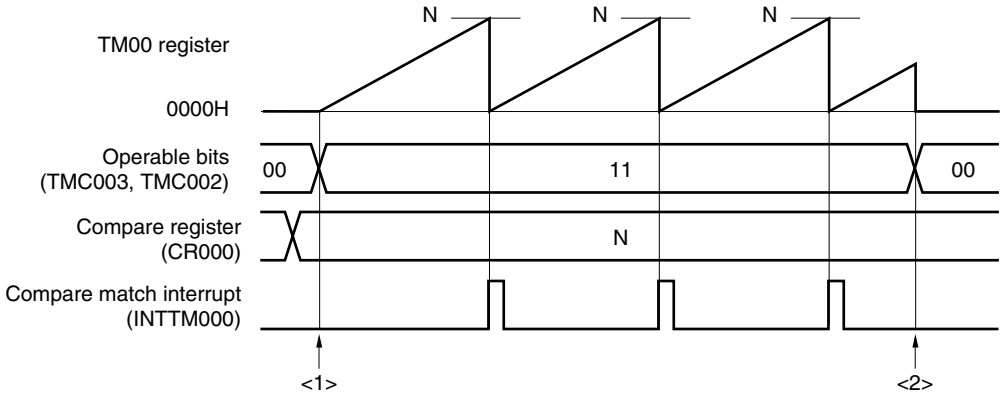
Setting CR000 to 0000H is prohibited.

(f) 16-bit capture/compare register 010 (CR010)

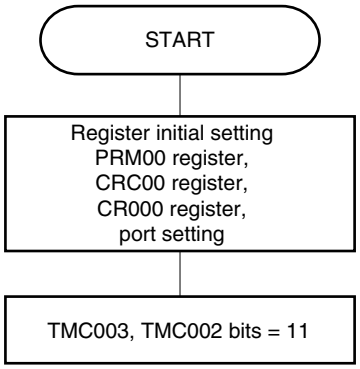
Usually, CR010 is not used in the external event counter mode. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-17. Example of Software Processing in External Event Counter Mode



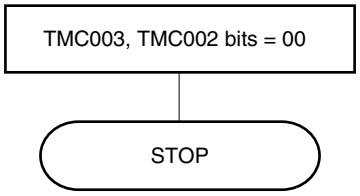
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

6.4.3 Operation in clear & start mode entered by TI000 pin valid edge input

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 10 (clear & start mode entered by the TI000 pin valid edge input) and the count clock (set by PRM00) is supplied to the timer/event counter, TM00 starts counting up. When the valid edge of the TI000 pin is detected during the counting operation, TM00 is cleared to 0000H and starts counting up again. If the valid edge of the TI000 pin is not detected, TM00 overflows and continues counting.

The valid edge of the TI000 pin is a cause to clear TM00. Starting the counter is not controlled immediately after the start of the operation.

CR000 is only used as compare register.

CR010 is used as compare register and capture register.

- **When CR000 and CR010 are used as compare registers**

  Signals INTTM000 and INTTM010 are generated when the value of TM00 matches the values of CR000 and CR010.

Caution Do not set the count clock as the valid edge of the TI000 pin (PRM002, PRM001, and PRM000 = 110). When PRM002, PRM001, and PRM000 = 110, TM00 is cleared.

Remarks 1. For the setting of the I/O pins, see **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

(1) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: compare register, CR010: compare register)

Figure 6-18. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Compare Register)

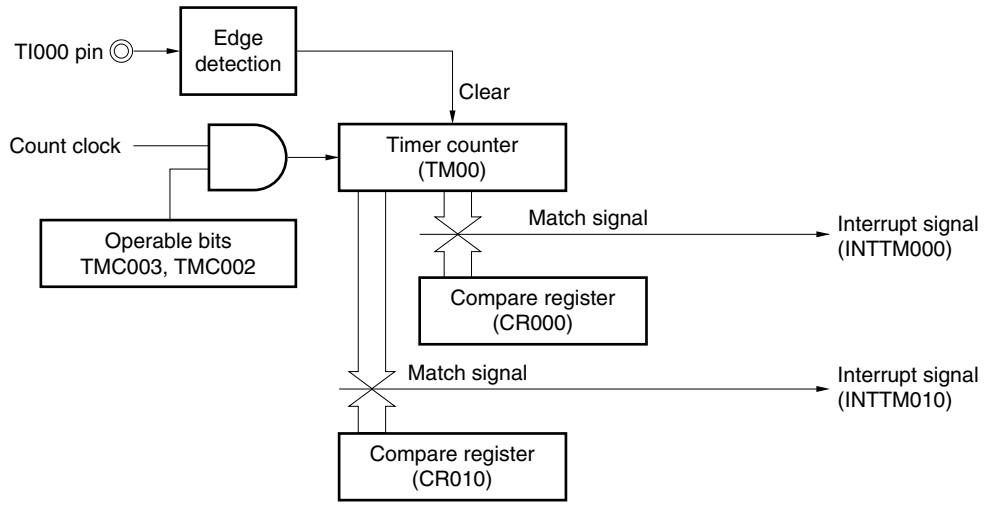
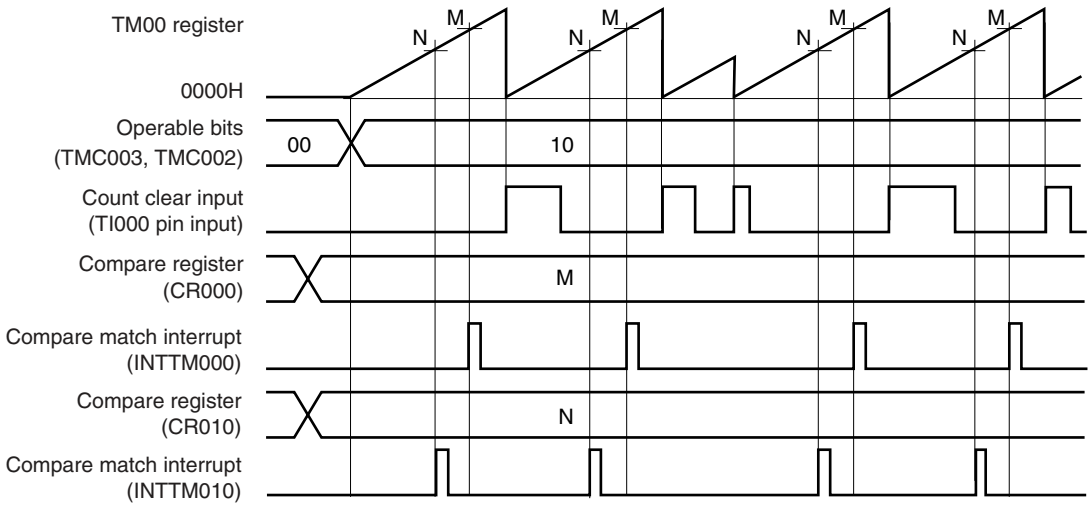


Figure 6-19. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Compare Register)

• PRM00 = 10H, CRC00, = 00H, TMC00 = 08H



(2) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: compare register, CR010: capture register)

Figure 6-20. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)

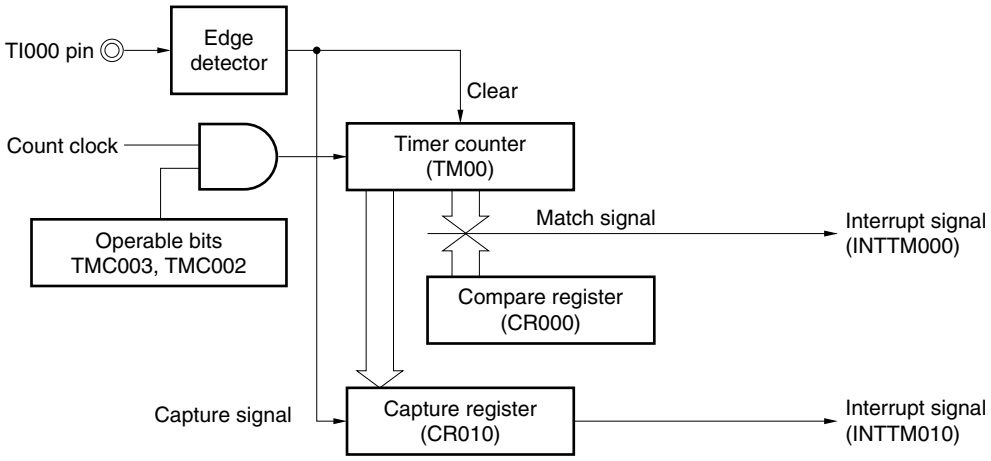


Figure 6-21. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)

- **PRM00 = 10H, CRC00, = 04H, TMC00 = 08H, CR000 = 0001H**

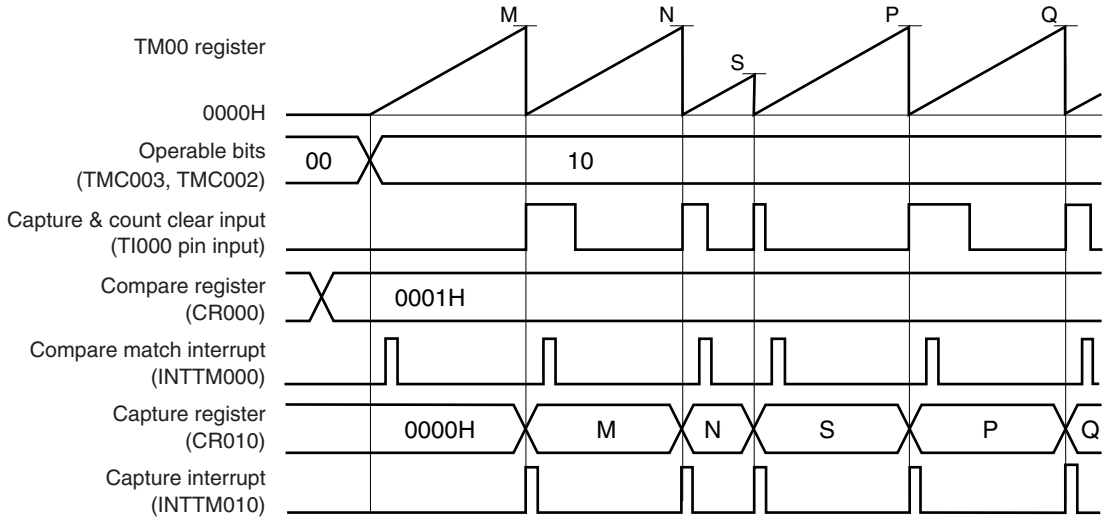
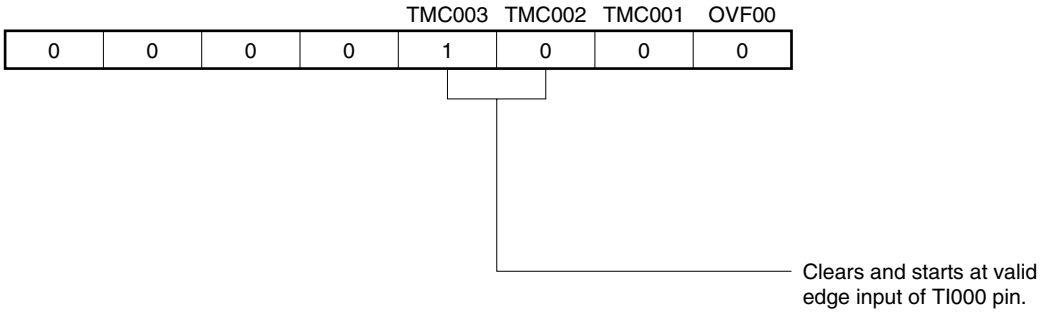
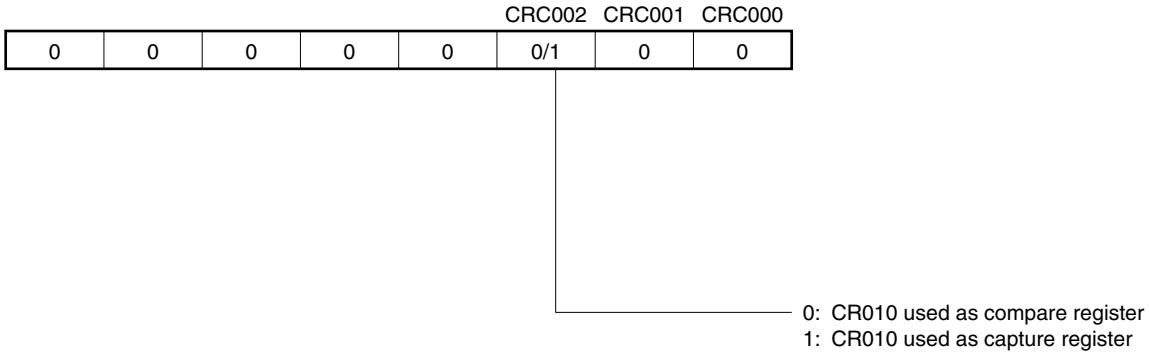


Figure 6-22. Example of Register Settings in Clear & Start Mode Entered by TI000 Pin Valid Edge Input

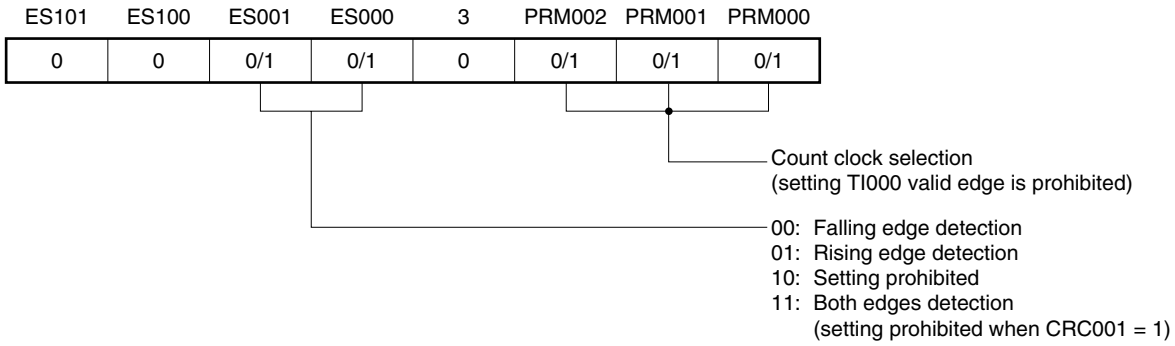
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(e) 16-bit compare register 000 (CR000)

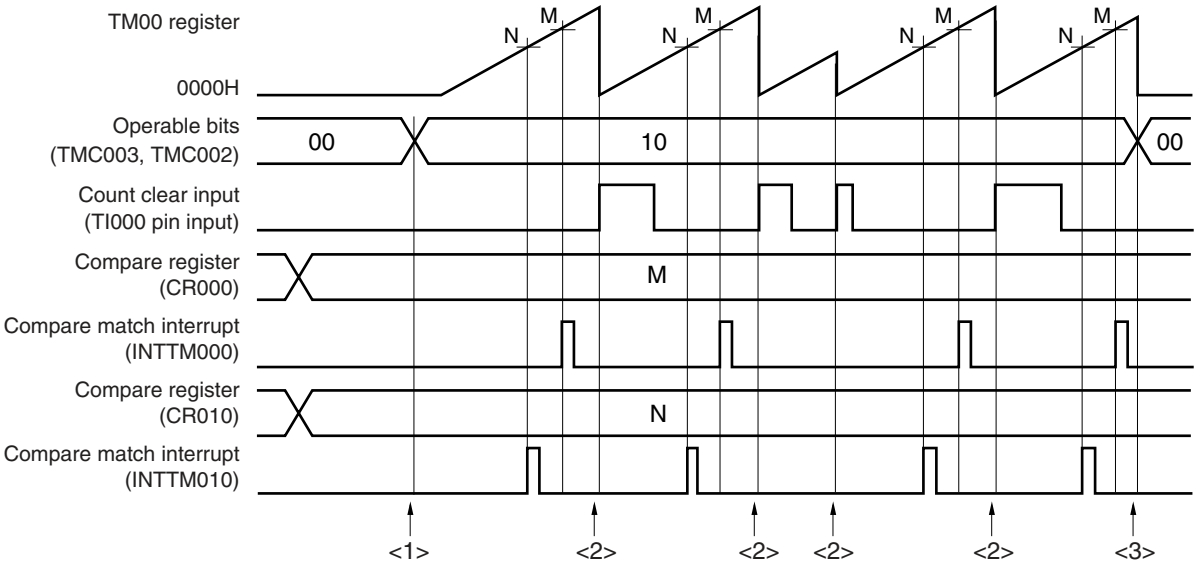
When its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

(f) 16-bit capture/compare register 010 (CR010)

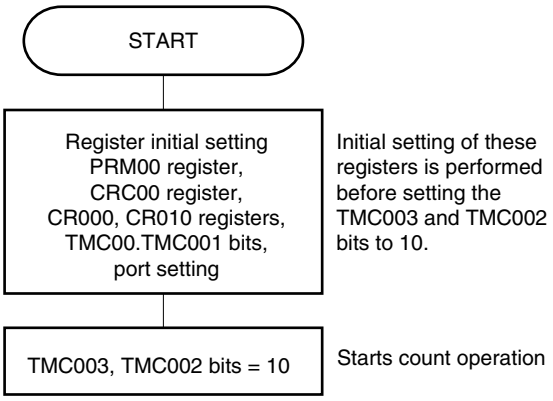
When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

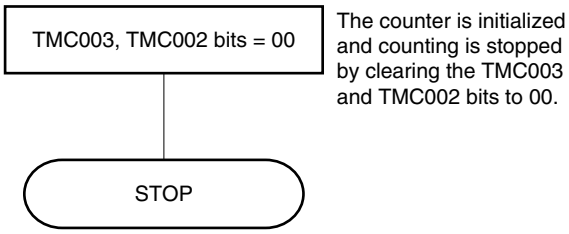
Figure 6-23. Example of Software Processing in Clear & Start Mode Entered by TI000 Pin Valid Edge Input



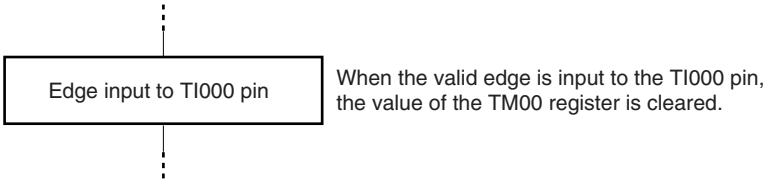
<1> Count operation start flow



<3> Count operation stop flow



<2> TM00 register clear & start flow



6.4.4 Free-running timer operation

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 01 (free-running timer mode), 16-bit timer/event counter 00 continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF00) is set to 1 at the next clock, and TM00 is cleared (to 0000H) and continues counting. Clear OVF00 to 0 by executing the CLR instruction via software.

The following two types of free-running timer operations are available.

- Both CR000 and CR010 are used as compare registers.
- One of CR000 or CR010 is used as a compare register and the other is used as a capture register.

Remarks 1. For the setting of the I/O pins, see **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation (CR000: compare register, CR010: compare register)

Figure 6-24. Block Diagram of Free-Running Timer Mode (CR000: Compare Register, CR010: Compare Register)

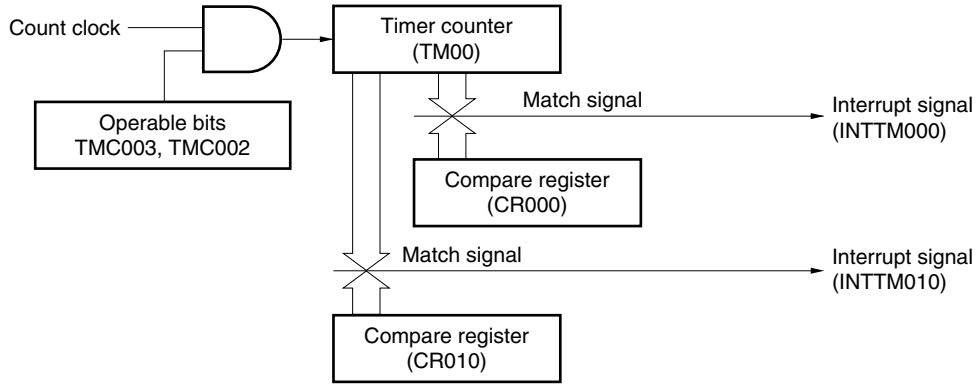
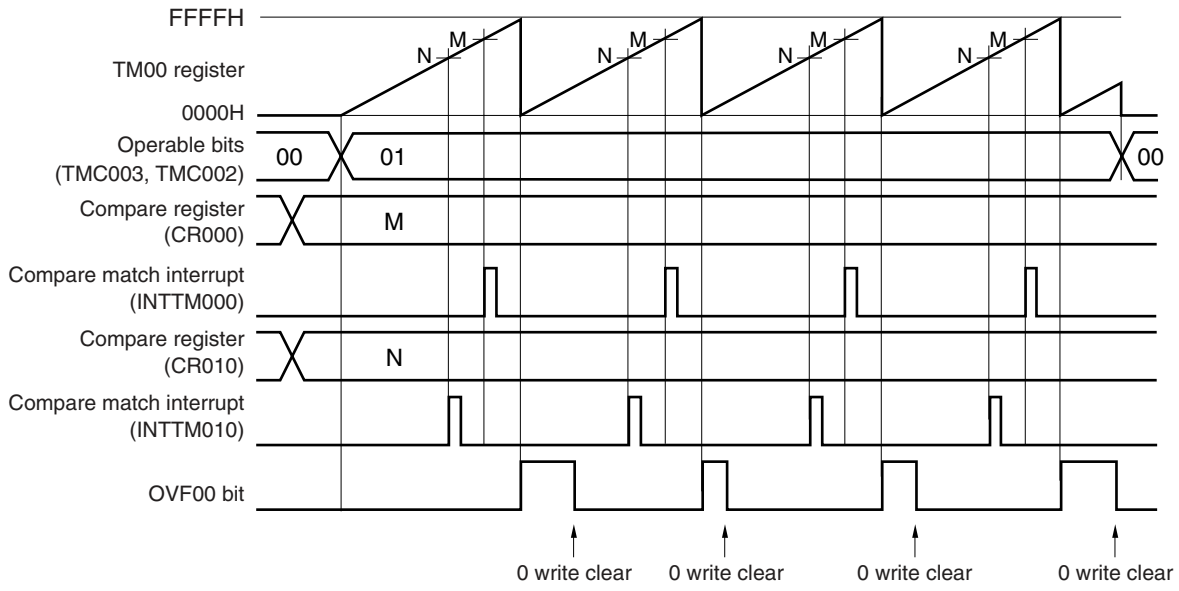


Figure 6-25. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

• PRM00 = 00H, CRC00 = 00H, TMC00 = 04H



This is an application example where two compare registers are used in the free-running timer mode.

(2) Free-running timer mode operation
(CR000: compare register, CR010: capture register)

Figure 6-26. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)

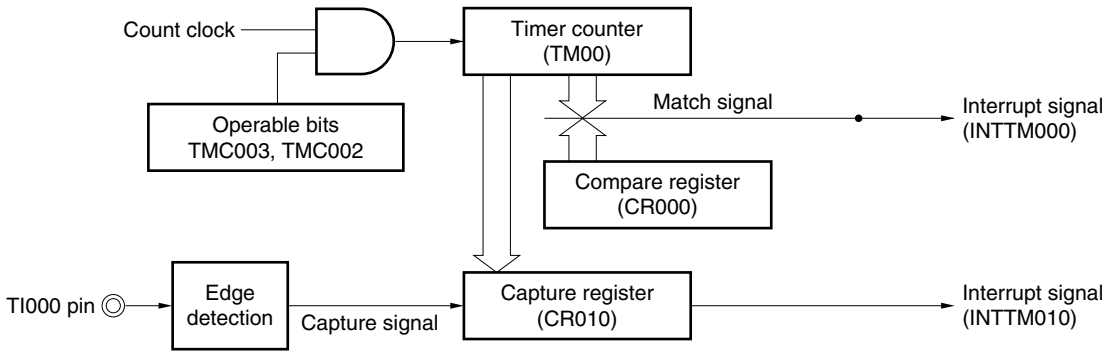
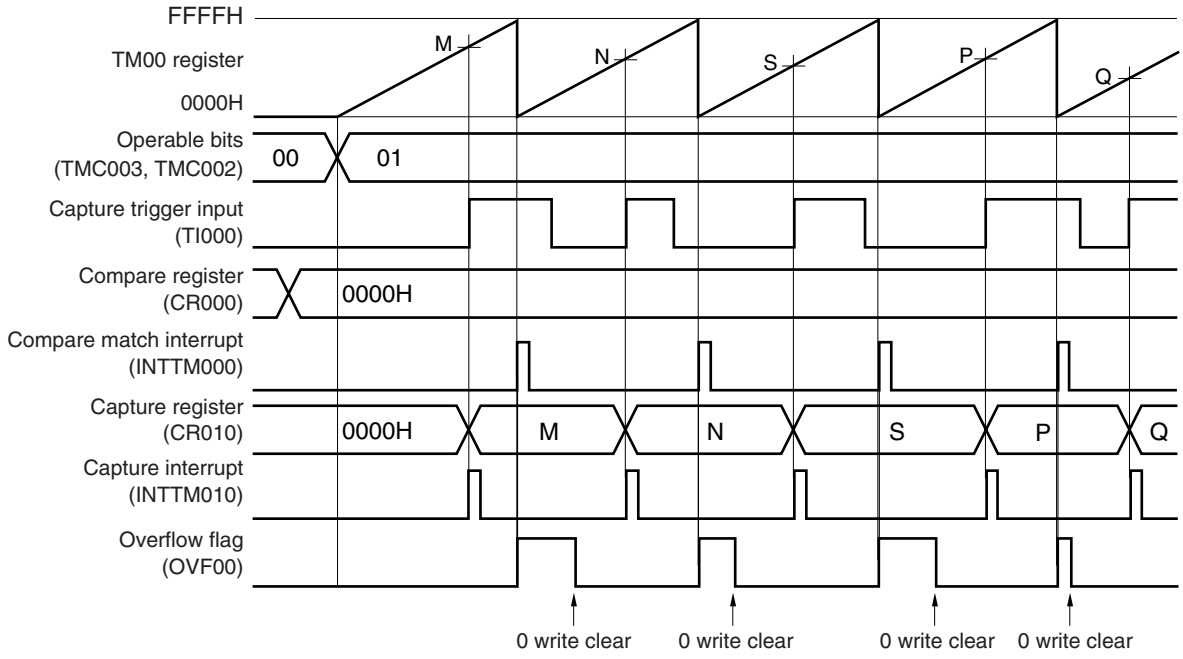


Figure 6-27. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)

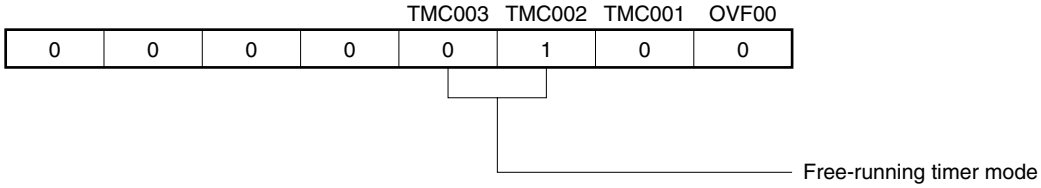
• PRM00 = 10H, CRC00 = 04H, TMC00 = 04H



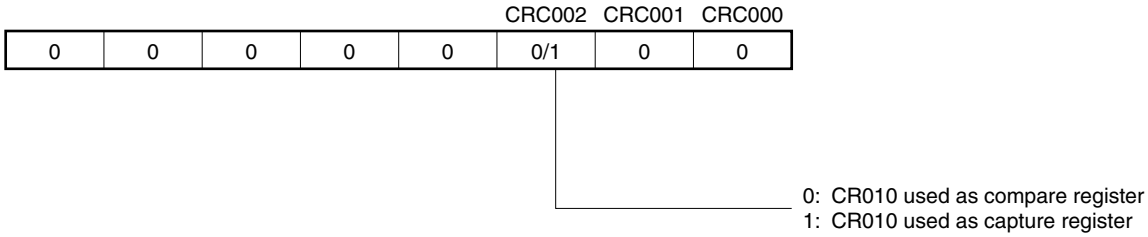
This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

Figure 6-28. Example of Register Settings in Free-Running Timer Mode

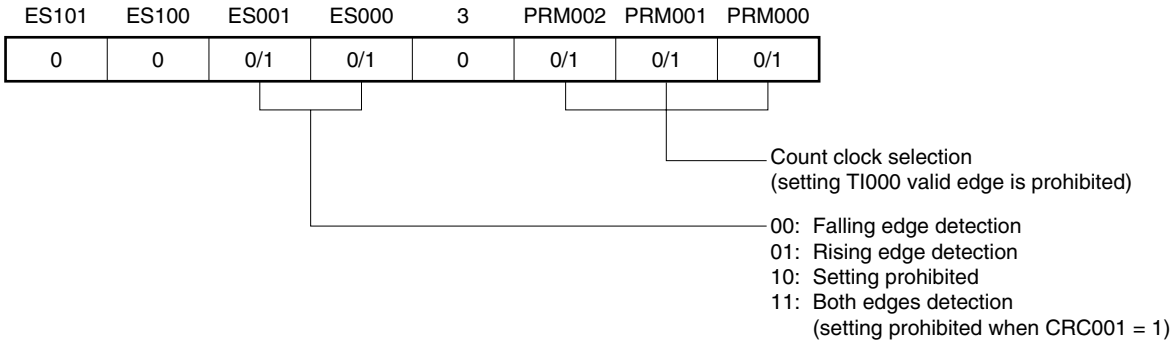
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(e) 16-bit compare register 000 (CR000)

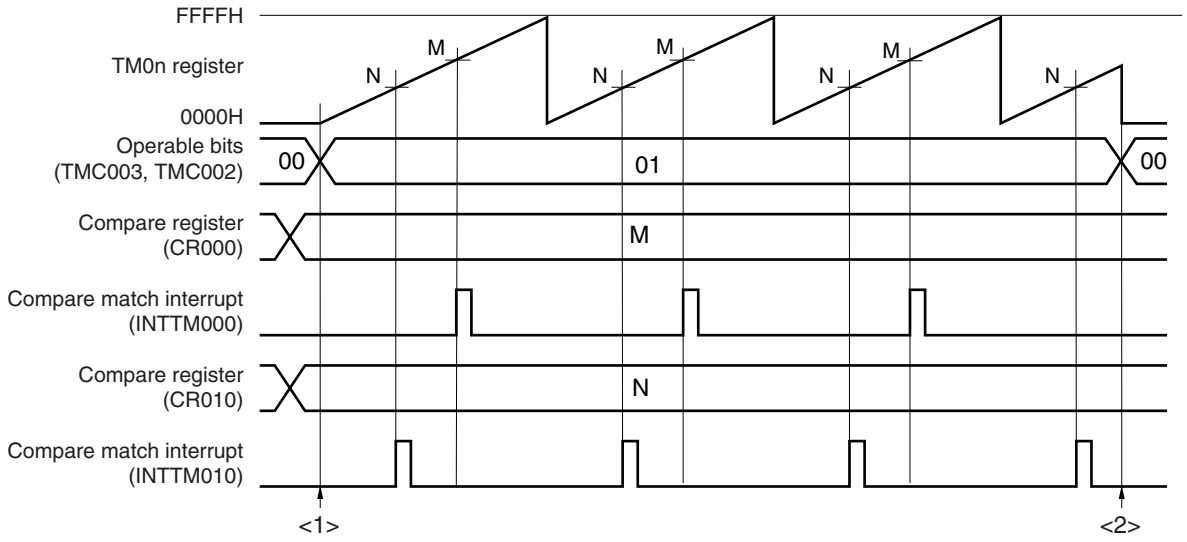
When its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

(f) 16-bit capture/compare register 010 (CR010)

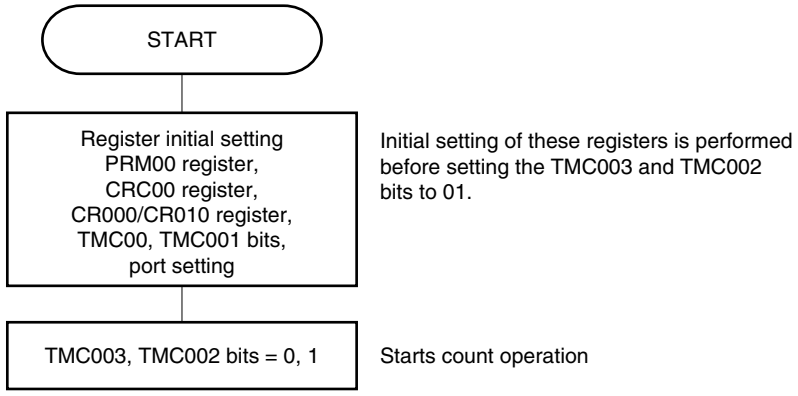
When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 6-29. Example of Software Processing in Free-Running Timer Mode



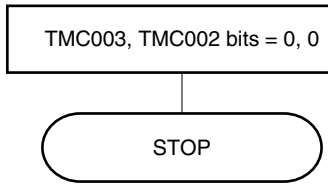
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 01.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

6.4.5 Pulse width measurement operation

TM00 can be used to measure the pulse width of the signal input to the TI000 pin.

Measurement can be accomplished by operating the 16-bit timer/event counter 00 in the free-running timer mode or by restarting the timer in synchronization with the signal input to the TI000 pin.

When an interrupt is generated, read the value of the valid capture register and measure the pulse width. Check bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00). If it is set (to 1), clear it to 0 by software.

Figure 6-30. Block Diagram of Pulse Width Measurement (Free-Running Timer Mode)

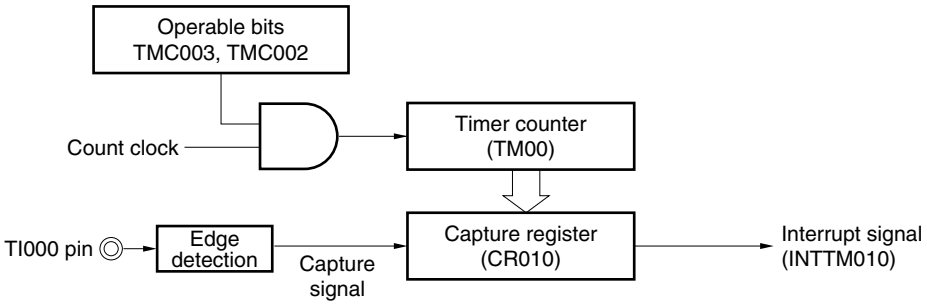
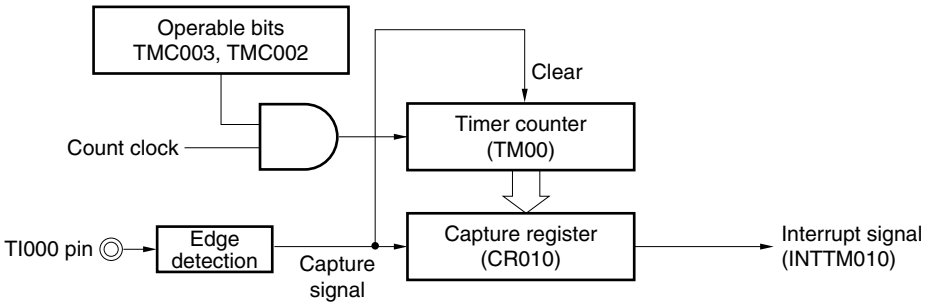


Figure 6-31. Block Diagram of Pulse Width Measurement (Clear & Start Mode Entered by TI000 Pin Valid Edge Input)



A pulse width can be measured in the following two ways.

- Measuring the pulse width by using input signal of the TI000 pin (free-running timer mode)
- Measuring the pulse width by using input signal of the TI000 pin (clear & start mode entered by the TI000 pin valid edge input)

Caution Do not select the TI000 valid edge as the count clock when measuring the pulse width.

Remark For the setting of the I/O pins, see **6.3 (5) Port mode register 3 (PM3)**.

(1) Measuring the pulse width by using input signal of the TI000 pin (free-running timer mode)

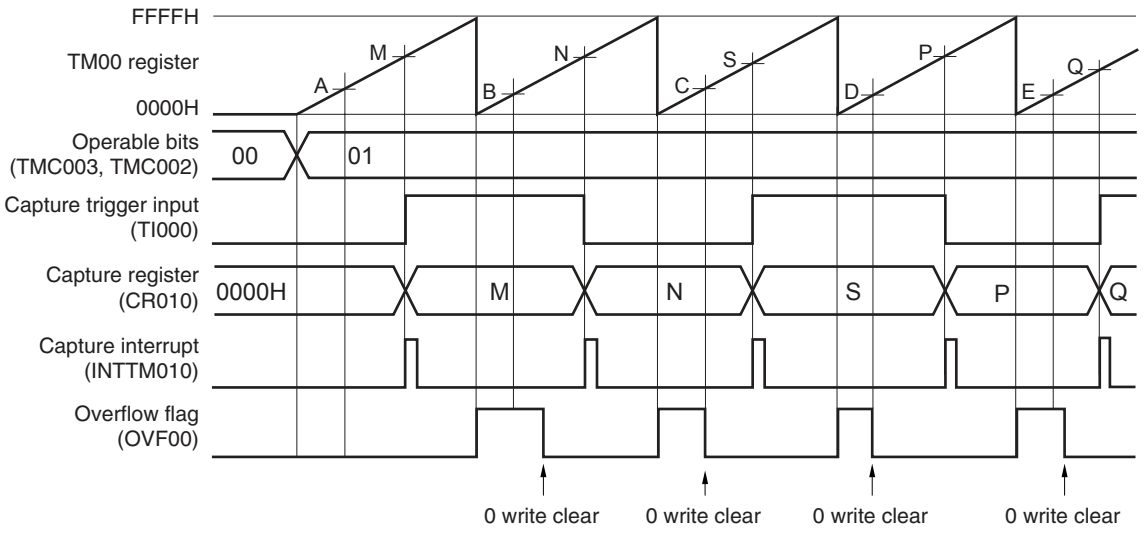
Set the free-running timer mode (TMC003 and TMC002 = 01). When the valid edge of the TI000 pin is detected, the count value of TM00 is captured to CR010. Specify detection of both the edges of the TI000 pin.

By this measurement method, the previous count value is subtracted from the count value captured by the edge of each input signal. Therefore, save the previously captured value to a separate register in advance.

If an overflow occurs, the value becomes negative if the previously captured value is simply subtracted from the current captured value and, therefore, a borrow occurs (bit 0 (CY) of the program status word (PSW) is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

Figure 6-32. Timing Example of Pulse Width Measurement (1)

• TMC00 = 04H, PRM00 = 30H, CRC00 = 04H



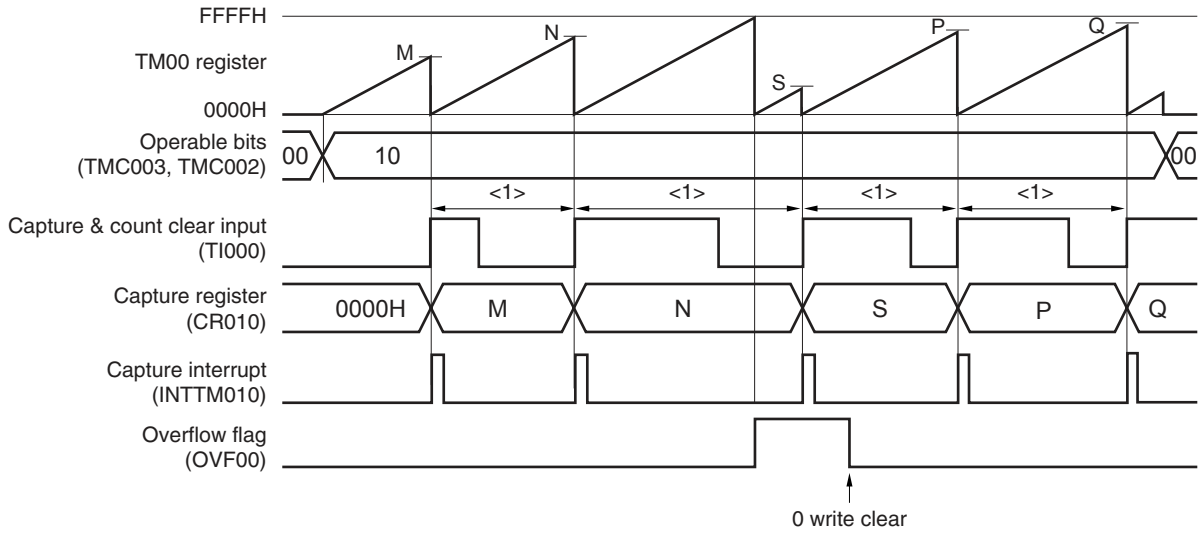
(2) Measuring the pulse width by using input signal of the TI000 pin (clear & start mode entered by the TI000 pin valid edge input)

Set the clear & start mode entered by the TI000 pin valid edge (TMC003 and TMC002 = 10). The count value of TM00 is captured to CR000 in the phase reverse to the valid edge of the TI000 pin, and the count value of TM00 is captured to CR010 and TM00 is cleared (0000H) when the valid edge of the TI000 pin is detected. Therefore, a cycle is stored in CR010 if TM00 does not overflow.

If an overflow occurs, take the value that results from adding 10000H to the value stored in CR010 as a cycle. Clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

Figure 6-33. Timing Example of Pulse Width Measurement (2)

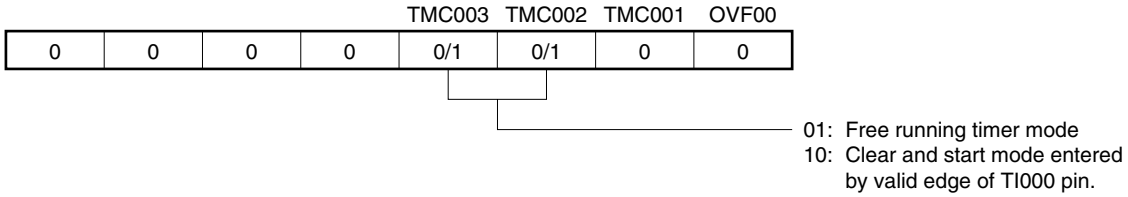
• TMC00 = 08H, PRM00 = 00H, CRC00 = 04H



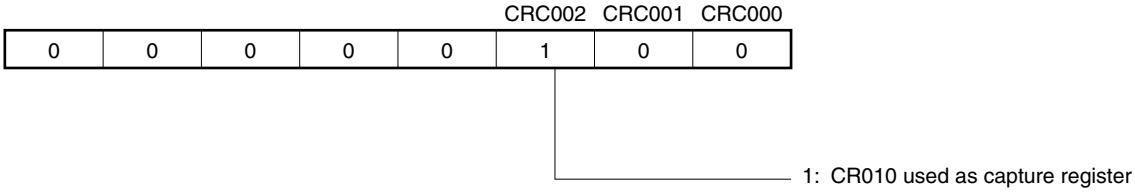
<1> Pulse cycle = (10000H × Number of times OVF00 bit is set to 1 + Captured value of CR010) × Count clock cycle

Figure 6-34. Example of Register Settings for Pulse Width Measurement

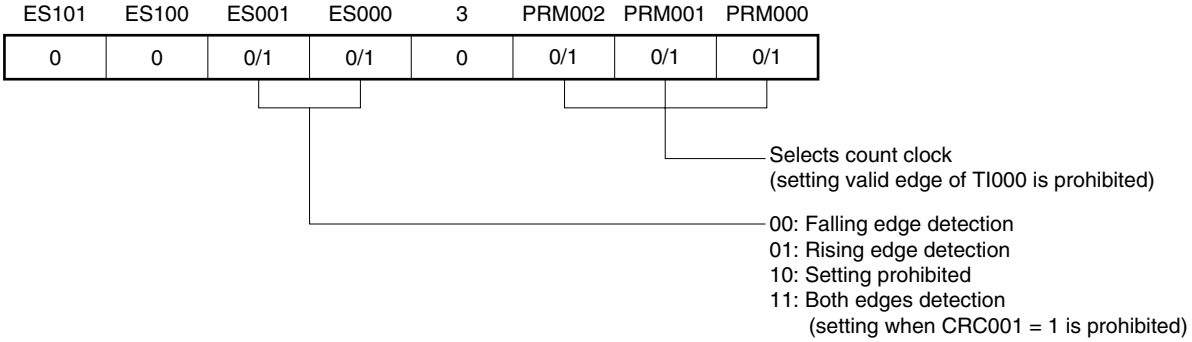
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer counter 00 (TM00)

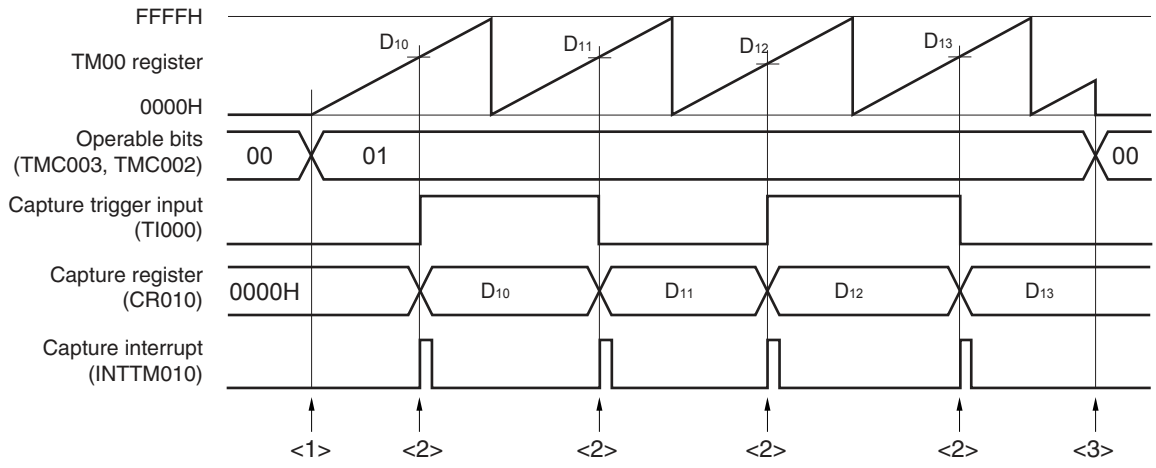
By reading TM00, the count value can be read.

(e) 16-bit capture/compare register 010 (CR010)

This register is used as a capture register. The signal input to the TI000 pin is used as a capture trigger. When the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 6-35. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode



(b) Example of clear & start mode entered by TI000 pin valid edge

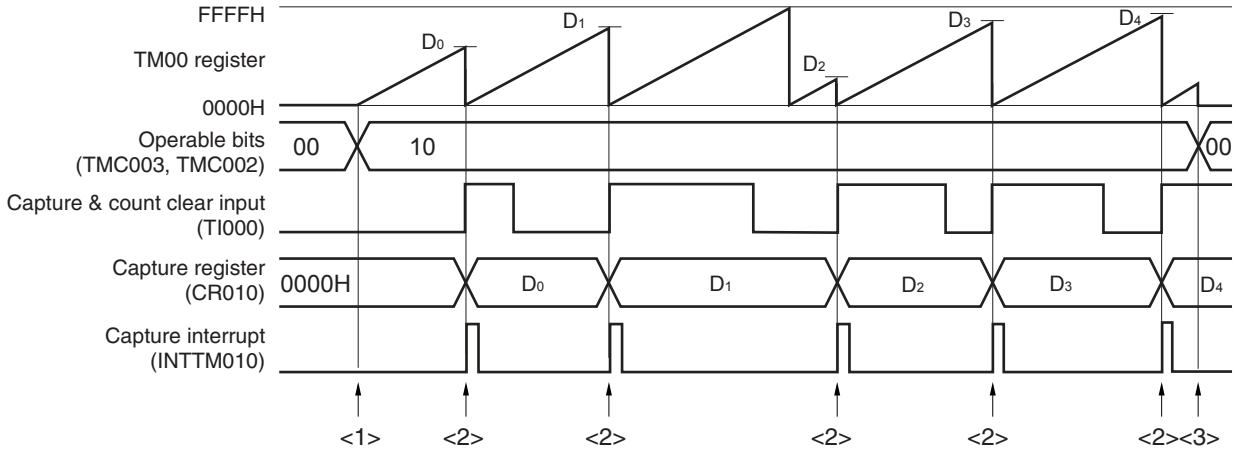
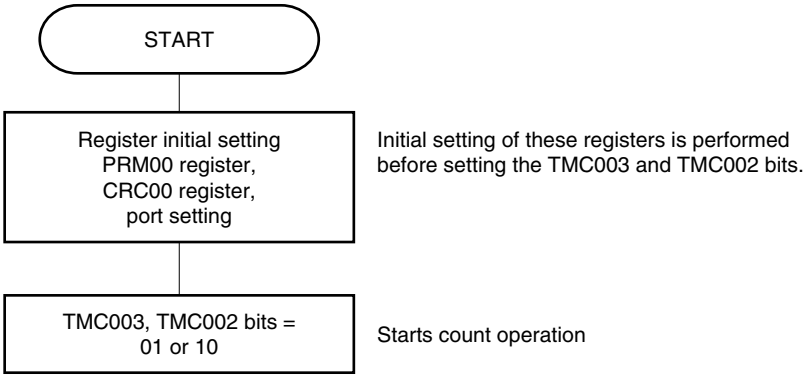
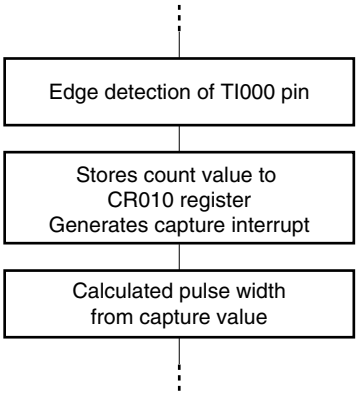


Figure 6-35. Example of Software Processing for Pulse Width Measurement (2/2)

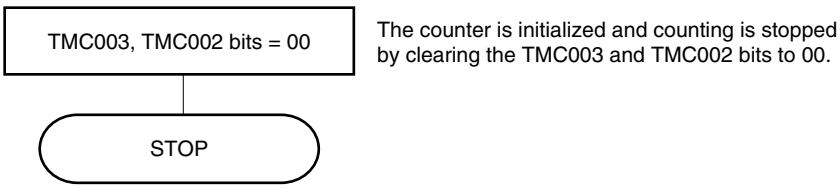
<1> Count operation start flow



<2> Capture trigger input flow



<3> Count operation stop flow

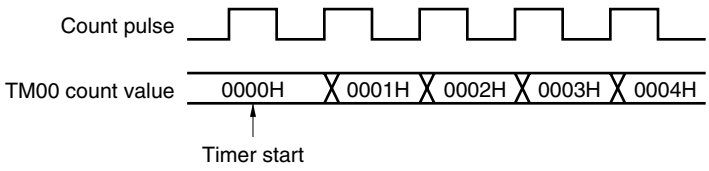


6.5 Cautions for 16-Bit Timer/Event Counter 00

(1) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM00 is started asynchronously to the count pulse.

Figure 6-36. Start Timing of TM00 Count



(2) Setting of CR000 and CR010 (clear & start mode entered upon a match between TM00 and CR000)

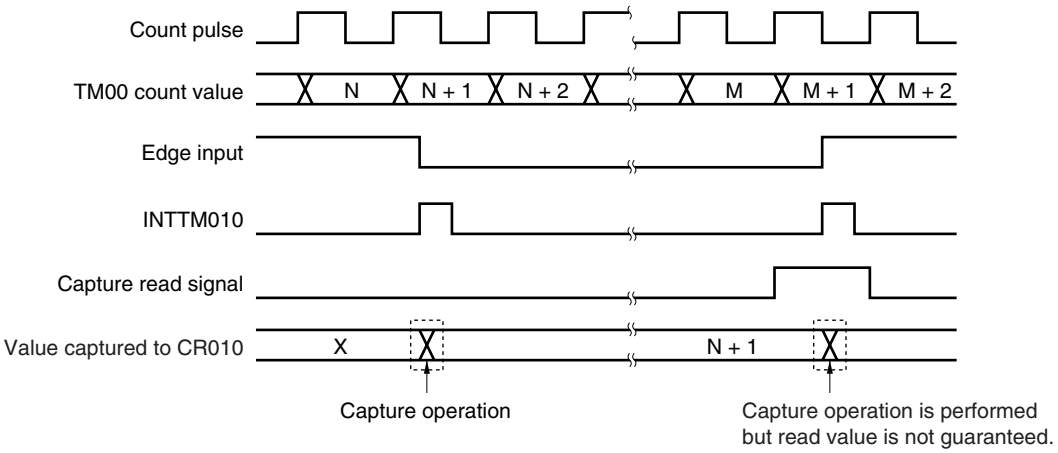
Set a value other than 0000H to CR000 and CR010 (TM00 cannot count one pulse when it is used as an external event counter).

(3) Timing of holding data by capture register

(a) When the valid edge is input to the TI000 pin is detected while CR010 is read, CR010 performs a capture operation but the read value of CR010 is not guaranteed. At this time, an interrupt signal (INTTM010) is generated when the valid edge of the TI000 pin is detected.

When the count value is captured because the valid edge of the TI000 pin was detected, read the value of CR010 after INTTM010 is generated.

Figure 6-37. Timing of Holding Data by Capture Register



(b) The values of CR000 and CR010 are not guaranteed after 16-bit timer/event counter 00 stops.

(4) Setting valid edge

Set the valid edge of the TI000 pin while the timer operation is stopped (TMC003 and TMC002 = 00). Set the valid edge by using ES000 and ES001.

(5) Operation of OVF00 flag

(a) Setting OVF00 flag (1)

The OVF00 flag is set to 1 in the following case, as well as when TM00 overflows.

Select the clear & start mode entered upon a match between TM00 and CR000.

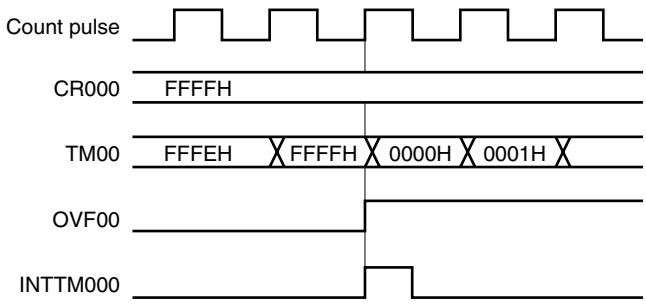
↓

Set CR000 to FFFFH.

↓

When TM00 matches CR000 and TM00 is cleared from FFFFH to 0000H

Figure 6-38. Operation Timing of OVF00 Flag



(b) Clearing OVF00 flag

Even if the OVF00 flag is cleared to 0 after TM00 overflows and before the next count clock is counted (before the value of TM00 becomes 0001H), it is set to 1 again and clearing is invalid.

(6) Capture operation

(a) When valid edge of TI000 is specified as count clock

When the valid edge of TI000 is specified as the count clock, the capture register for which TI000 is specified as a trigger does not operate correctly.

(b) Pulse width to accurately capture value by signals input to TI000 pin

To accurately capture the count value, the pulse input to the TI000 pin as a capture trigger must be wider than two count clocks selected by PRM00 (see **Figure 6-7**).

(c) Generation of interrupt signal

The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM000 and INTTM010) are generated at the rising edge of the next count clock (see **Figure 6-7**).

(7) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 00 is enabled after reset and while the TI000 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI000 pin, then the high level of the TI000 pin is detected as the rising edge. Note this when the TI000 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for eliminating noise

The sampling clock for eliminating noise differs depending on whether the valid edge of TI000 is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM00 is used for sampling.

When the signal input to the TI000 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (see **Figure 6-7**).

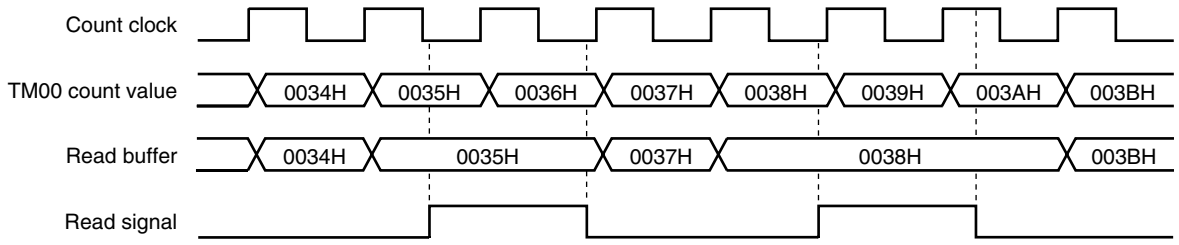
(8) Timer operation

The signal input to the TI000 pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.

(9) Reading of 16-bit timer counter 00 (TM00)

TM00 can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 6-39. 16-bit Timer Counter 00 (TM00) Read Timing



Remark f_{PRS}: Peripheral hardware clock frequency

CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50, 51, AND 52

7.1 Functions of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50, 51, and 52 are mounted onto all 78K0/Lx3-M microcontroller products.

8-bit timer/event counters 50, 51, and 52 have the following functions.

	78K0/LE3-M	78K0/LG3-M
Interval timer	TM50, TM51, TM52	TM50, TM51, TM52
External event counter	–	TM50, TM51
Square-wave output		
PWM output		

Remark In the 78K0/LE3-M, only the interval timer function is mounted

7.2 Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50, 51, and 52 include the following hardware.

Table 7-1. Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

(a) 78K0/LE3-M

Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n)

(b) 78K0/LG3-M

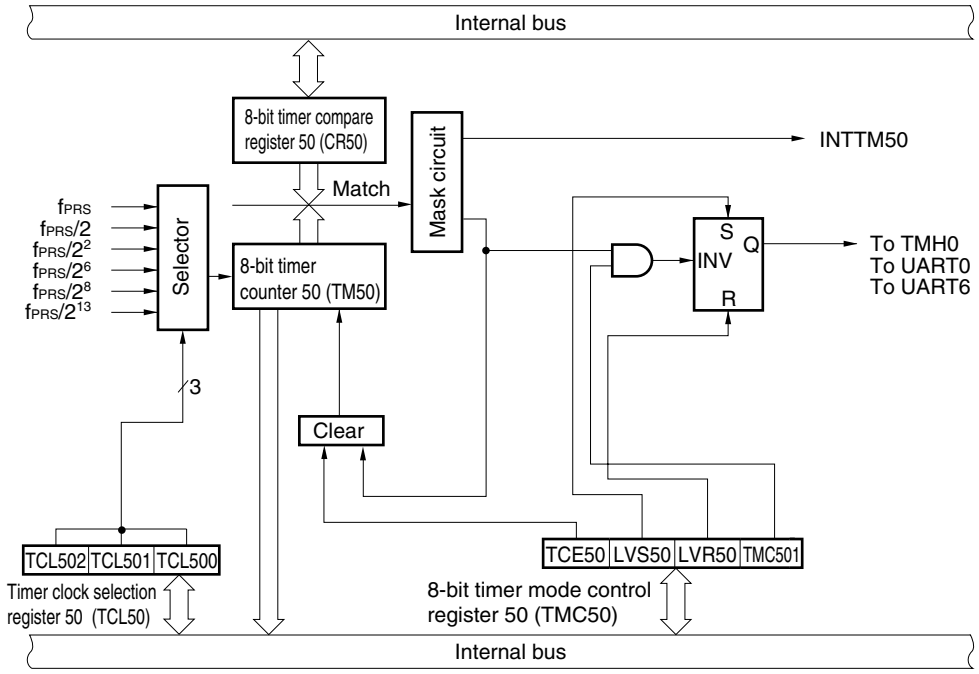
Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Timer input	TI50, TI51
Timer output	TO50, TO51
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) Port mode register 4 (PM4) Port register 4 (P4)

Remark n = 0 to 2

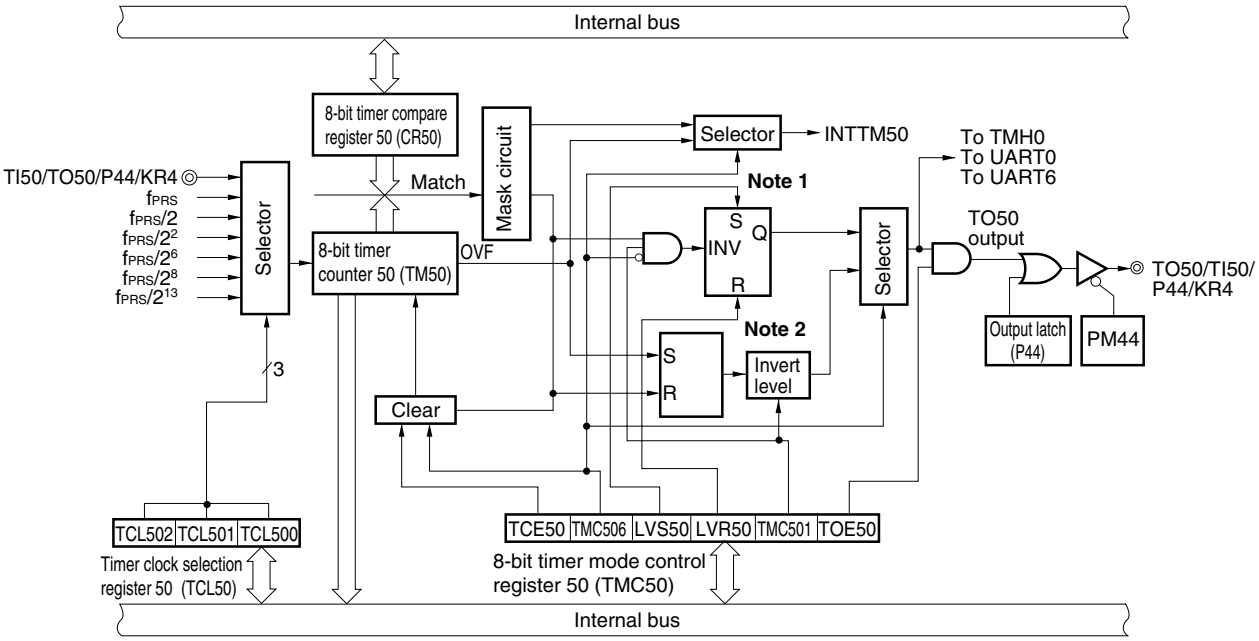
Figures 7-1 to 7-3 show the block diagrams of 8-bit timer/event counters 50, 51, and 52.

Figure 7-1. Block Diagram of 8-Bit Timer/Event Counter 50

(a) 78K0/LE3-M



(b) 78K0/LG3-M

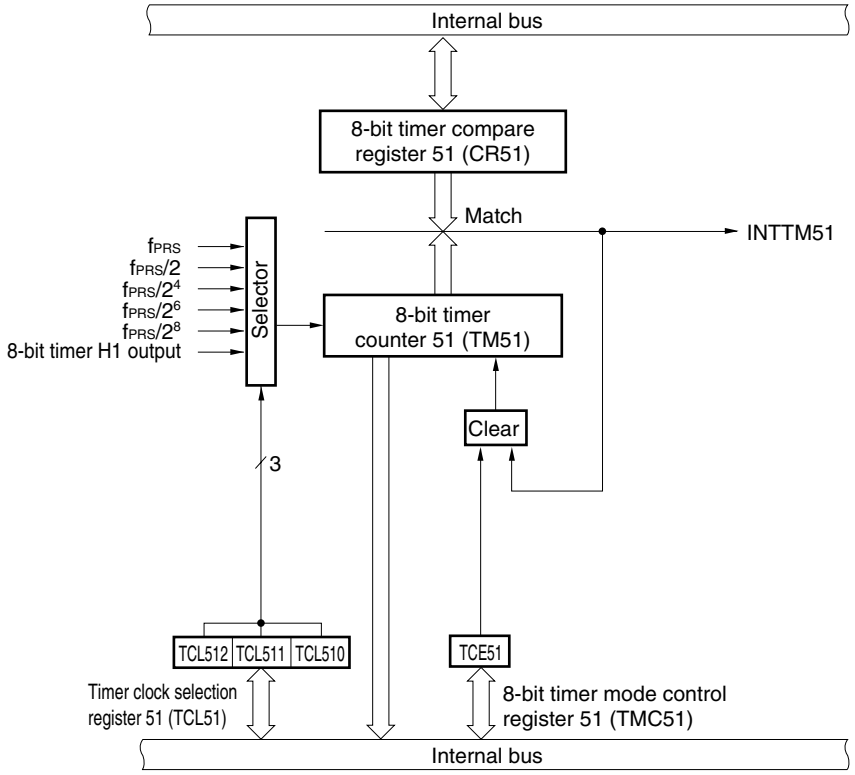


Notes 1. Timer output F/F

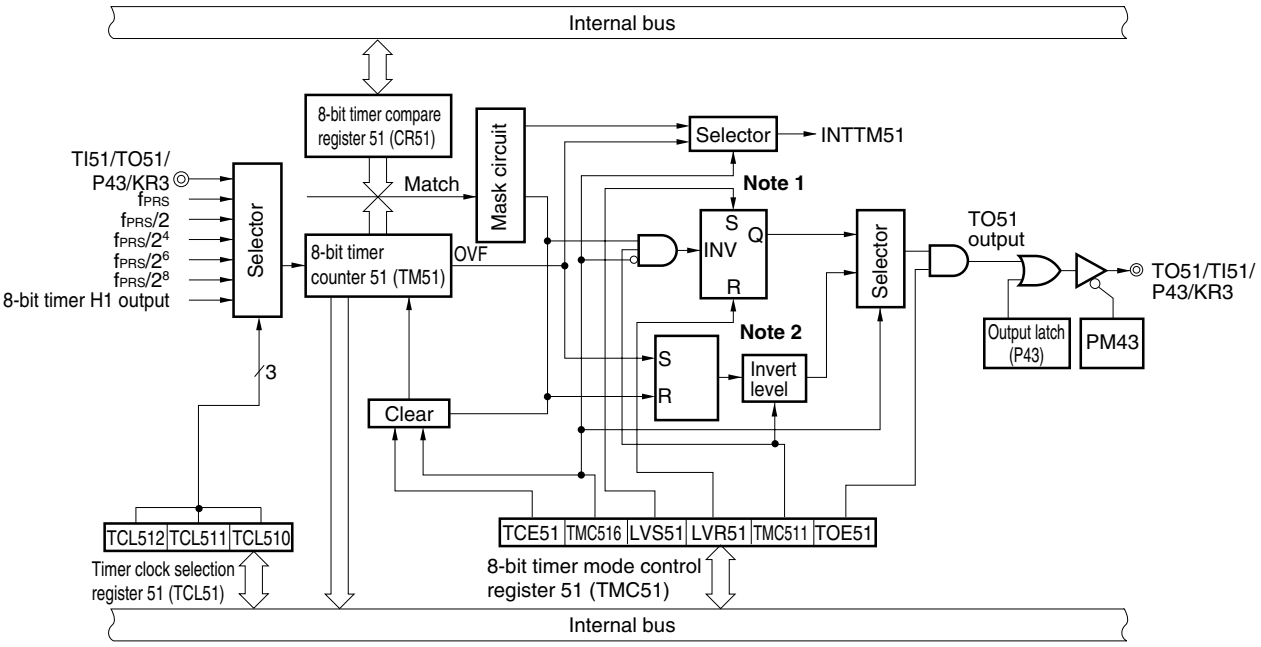
2. PWM output F/F

Figure 7-2. Block Diagram of 8-Bit Timer/Event Counter 51

(a) 78K0/LE3-M



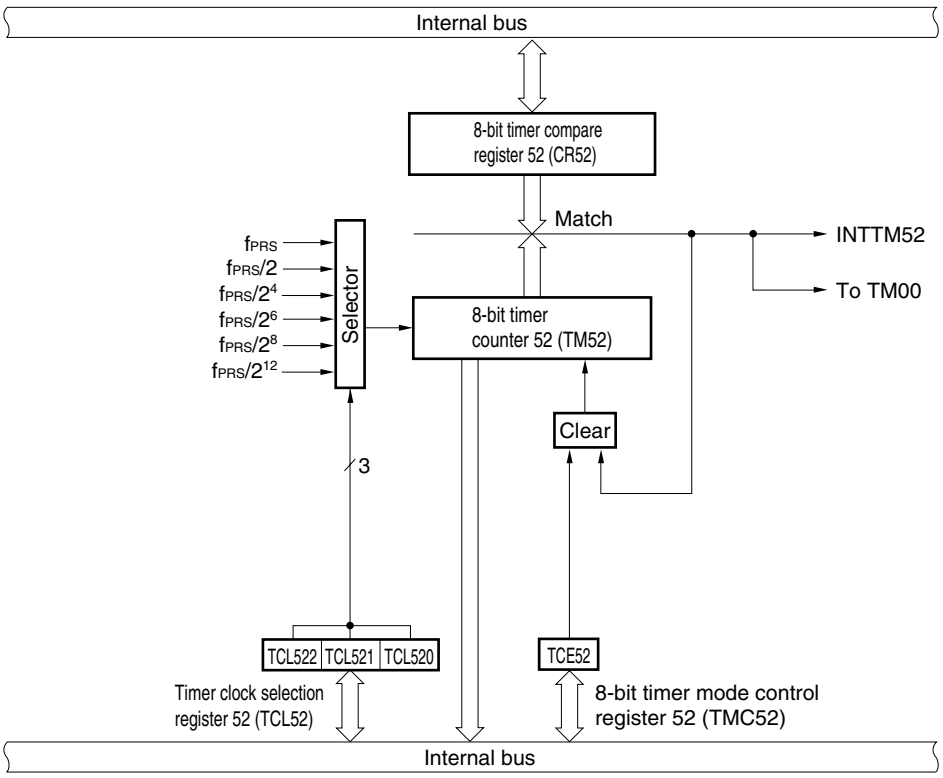
(b) 78K0/LG3-M



Notes 1. Timer output F/F

2. PWM output F/F

Figure 7-3. Block Diagram of 8-Bit Timer/Event Counter 52



(1) 8-bit timer counter 5n (TM5n)

TM5n is an 8-bit register that counts the count pulses and is read-only.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 7-4. Format of 8-Bit Timer Counter 5n (TM5n)

Address: FF16H (TM50), FF6FH (TM51), FF51H (TM52) After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
TM5n (n = 0-2)								

In the following situations, the count value is cleared to 00H.

<1> Reset signal generation

<2> When TCE5n is cleared

<3> When TM5n and CR5n match in the mode in which clear & start occurs upon a match of the TM5n and CR5n.

(2) 8-bit timer compare register 5n (CR5n)

CR5n can be read and written by an 8-bit memory manipulation instruction.

Except in PWM mode, the value set in CR5n is constantly compared with the 8-bit timer counter 5n (TM5n) count value, and an interrupt request (INTTM5n) is generated if they match.

In the PWM mode, the TO5n output becomes inactive when the values of TM5n and CR5n match, but no interrupt is generated.

The value of CR5n can be set within 00H to FFH.

Reset signal generation sets CR5n to 00H.

Figure 7-5. Format of 8-Bit Timer Compare Register 5n (CR5n)

Address: FF17H (CR50), FF41H (CR51), FF59H (CR52) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CR5n (n = 0-2)								

Cautions 1. In the mode in which clear & start occurs on a match of TM5n and CR5n (TMC5n6 = 0), do not write other values to CR5n during operation.

2. In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0 to 2

7.3 Registers Controlling 8-Bit Timer/Event Counters 50, 51, and 52

The following five registers are used to control 8-bit timer/event counters 50, 51, and 52.

- Timer clock selection register 5n (TCL5n)
- 8-bit timer mode control register 5n (TMC5n)
- Port mode register 4 (PM4)
- Port register 4 (P4)

(1) Timer clock selection register 5n (TCL5n)

This register sets the count clock of 8-bit timer/event counter 5n and the valid edge of the TI5n pin input.

TCL5n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets TCL5n to 00H.

Remark n = 0 to 2

Figure 7-6. Format of Timer Clock Selection Register 50 (TCL50)

Address: FF6AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL50	0	0	0	0	0	TCL502	TCL501	TCL500

(a) 78K0/LE3-M

TCL502	TCL501	TCL500	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	Setting prohibited			
0	0	1				
0	1	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	$f_{PRS}/2^{13}$	0.24 kHz	0.61 kHz	1.22 kHz

(b) 78K0/LG3-M

TCL502	TCL501	TCL500	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	TI50 pin falling edge[Note 3]			
0	0	1	TI50 pin rising edge[Note 3]			
0	1	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	$f_{PRS}/2^{13}$	0.24 kHz	0.61 kHz	1.22 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of TCL502, TCL501, TCL500 = 0, 1, 0 (count clock: f_{PRS}) is prohibited.

3. Do not start timer operation with the external clock from the TI50 pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. When rewriting TCL50 to other data, stop the timer operation beforehand.

2. Be sure to clear bits 3 to 7 to "0".

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 7-7. Format of Timer Clock Selection Register 51 (TCL51)

Address: FF8CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL51	0	0	0	0	0	TCL512	TCL511	TCL510

(a) 78K0/LE3-M

TCL512	TCL511	TCL510	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	Setting prohibited			
0	0	1				
0	1	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	Timer H1 output signal			

(b) 78K0/LG3-M

TCL512	TCL511	TCL510	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	TI51 pin falling edge[Note 3]			
0	0	1	TI51 pin rising edge[Note 3]			
0	1	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	Timer H1 output signal			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of TCL512, TCL511, TCL510 = 0, 1, 0 (count clock: f_{PRS}) is prohibited.

3. Do not start timer operation with the external clock from the TI51 pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. When rewriting TCL51 to other data, stop the timer operation beforehand.

2. Be sure to clear bits 3 to 7 to "0".

Figure 7-8. Format of Timer Clock Selection Register 52 (TCL52)

Address: FF5BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL52	0	0	0	0	0	TCL522	TCL521	TCL520

TCL522	TCL521	TCL520	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	Setting prohibited			
0	0	1				
0	1	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of TCL522, TCL521, TCL520 = 0, 1, 0 (count clock: f_{PRS}) is prohibited.

Cautions 1. When rewriting TCL52 to other data, stop the timer operation beforehand.

2. Be sure to clear bits 3 to 7 to "0".

Remark f_{PRS}: Peripheral hardware clock frequency

(2) 8-bit timer mode control register 5n (TMC5n)

TMC5n is a register that performs the following five types of settings.

TMC5n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

<1> 8-bit timer counter 5n (TM5n) count operation control
<2> 8-bit timer counter 5n (TM5n) operating mode selection[Note]
<3> Timer output F/F (flip flop) status setting[Note]
<4> Active level selection in timer F/F control or PWM (free-running) mode[Note]
<5> Timer output control[Note]

Note TM50 and TM51 of 78K0/LG3-M only.

Remark n = 0 to 2

Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (1/2)

(a) 78K0/LE3-M

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	0
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	0

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	Timer F/F control
0	Inversion operation disabled
1	Inversion operation enabled

Note Bits 2 and 3 are write-only.

Cautions 1. Be sure to clear bits 0 and 4 to 6 to "0".

2. Perform <1> to <3> below in the following order, not at the same time.

<1> Set TMC501: Operation mode setting
<2> Set LVS50 and LVR50: Timer F/F setting
<3> Set TCE50

Remark If LVS50 and LVR50 are read, the value is 0.

Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (2/2)

(b) 78K0/LG3-M

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS50 and LVR50 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC501, TMC506: Operation mode setting

<2> Set TOE50 to enable output: Timer output enable

<3> Set LVS50, LVR50(see Caution 1): Timer F/F setting

<4> Set TCE50

3. When TCE50 = 1, setting the other bits of TMC50 is prohibited.

4. The actual TO50/TI50/P44/KR4 is determined depending on PM44 and P44, besides TO5n output.

5. Be sure to clear bits 4 and 5 to "0".

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE50 to 0.

2. If LVS50 and LVR50 are read, the value is 0.

3. The values of the TMC506, LVS50, LVR50, TMC5n1, and TOE50 bits are reflected at the TO50 pin regardless of the value of TCE50.

Figure 7-10. Format of 8-Bit Timer Mode Control Register 51 (TMC51)

(a) 78K0/LE3-M

Address: FF43H After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	3	2	1	0
TMC51	TCE51	0	0	0	0	0	0	0

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

Caution Be sure to clear bits 0 to 6 to "0".

(b) 78K0/LG3-M

Address: FF43H After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC51	TCE51	TMC516	0	0	LVS51	LVR51	TMC511	TOE51

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC516	TM51 operating mode selection
0	Mode in which clear & start occurs on a match between TM51 and CR51
1	PWM (free-running) mode

LVS51	LVR51	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO51 output: low)
1	0	Timer output F/F set (1) (default value of TO51 output: high)
1	1	Setting prohibited

TMC511	In other modes (TMC516 = 0)	In PWM mode (TMC516 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE51	Timer output control
0	Output disabled (TO51 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS51 and LVR51 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC511, TMC516: Operation mode setting

<2> Set TOE51 to enable output: Timer output enable

<3> Set LVS51, LVR51 (see Caution 1): Timer F/F setting

<4> Set TCE51

3. When TCE51 = 1, setting the other bits of TMC51 is prohibited.

4. The actual TO51/TI51/P43/KR3 is determined depending on PM43 and P43, besides TO51 output.

5. Be sure to clear bits 4 and 5 to "0".

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE51 to 0.

2. If LVS51 and LVR51 are read, the value is 0.

3. The values of the TMC516, LVS51, LVR51, TMC511, and TOE51 bits are reflected at the TO51 pin regardless of the value of TCE51.

Figure 7-11. Format of 8-Bit Timer Mode Control Register 52 (TMC52)

Address: FF5CH After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
TMC52	TCE52	0	0	0	0	0	0	0

TCE52	TM52 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

Caution Be sure to clear bits 0 to 6 to "0".

(3) Port mode register 4 (PM4)

This register sets port 4 input/output in 1-bit units.

PM4 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

When using the P44/TO50/TI50/KR4 and P43/TO51/TI51/KR3 pins for timer output, clear PM44 and PM43 and the output latches of P44 and P43 to 0.

When using the P44/TO50/TI50/KR4, P43/TO51/TI51/KR3 pins for timer input, set PM44 and PM43 to 1. The output latches of P44 and PM43 at this time may be 0 or 1.

Figure 7-12. Format of Port Mode Register 4 (PM4) (78K0/LG3-M)

Address: FF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PM4n	P4n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

7.4 Operations of 8-Bit Timer/Event Counters 50, 51, and 52

7.4.1 Operation as interval timer

8-bit timer/event counter 5n operates as an interval timer that generates interrupt requests repeatedly at intervals of the count value preset to 8-bit timer compare register 5n (CR5n).

When the count value of 8-bit timer counter 5n (TM5n) matches the value set to CR5n, counting continues with the TM5n value cleared to 0 and an interrupt request signal (INTTM5n) is generated.

The count clock of TM5n can be selected with bits 0 to 2 (TCL5n0 to TCL5n2) of timer clock selection register 5n (TCL5n).

Setting

<1> Set the registers.

- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on a match of TM5n and CR5n.
  (78K0/LE3-M: TMC50 = 0000×××0B, TMC51 = TMC51 = 00000000B)
  (78K0/LG3-M: TMC5n = 0000×××0B) ×: don't care

<2> After TCE5n = 1 is set, the count operation starts.

<3> If the values of TM5n and CR5n match, INTTM5n is generated (TM5n is cleared to 00H).

<4> INTTM5n is generated repeatedly at the same interval.
Set TCE5n to 0 to stop the count operation.

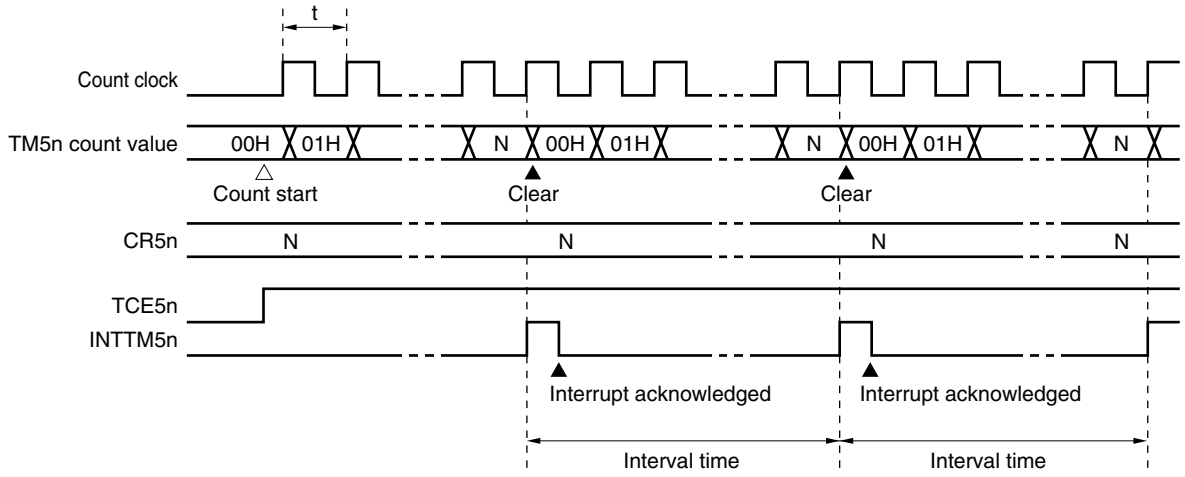
Caution Do not write other values to CR5n during operation.

Remarks 1. For how to enable the INTTM5n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

2. n = 0 to 2

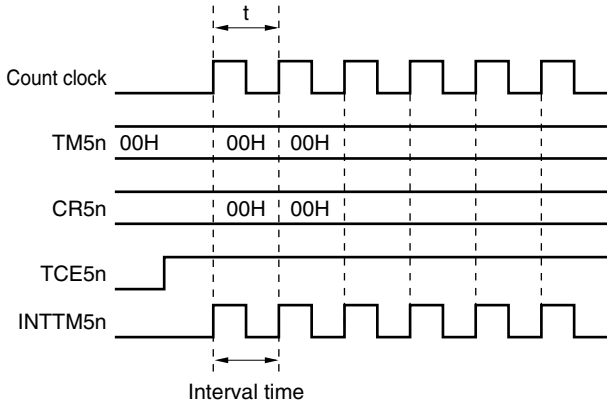
Figure 7-13. Interval Timer Operation Timing (1/2)

(a) Basic operation



Remark Interval time = (N + 1) × t
N = 01H to FFH

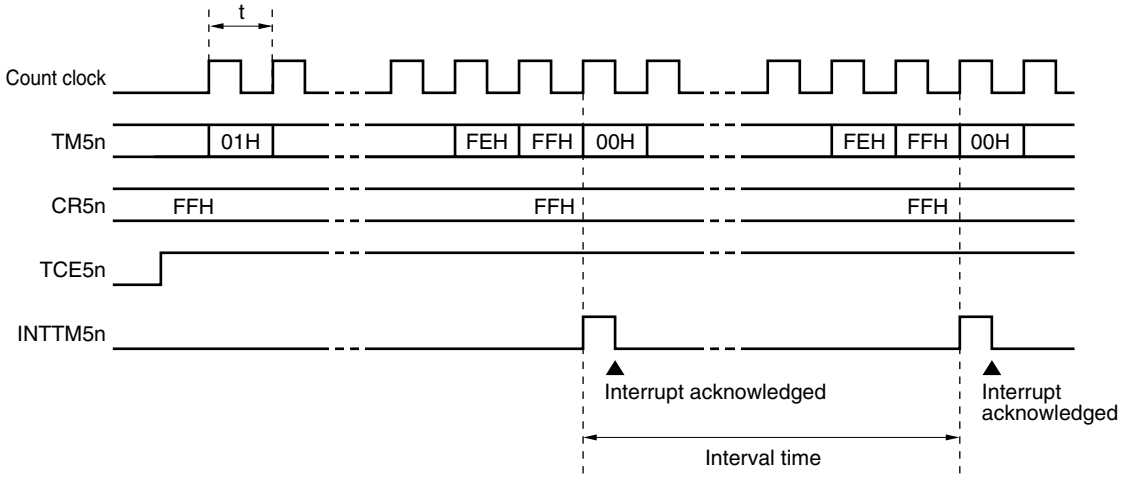
(b) When CR5n = 00H



Remark n = 0 to 2

Figure 7-13. Interval Timer Operation Timing (2/2)

(c) When CR5n = FFH



Remark n = 0 to 2

7.4.2 Operation as external event counter (78K0/LG3-M only)

The external event counter counts the number of external clock pulses to be input to the TI5n pin by 8-bit timer counter 5n (TM5n).

TM5n is incremented each time the valid edge specified by timer clock selection register 5n (TCL5n) is input. Either the rising or falling edge can be selected.

When the TM5n count value matches the value of 8-bit timer compare register 5n (CR5n), TM5n is cleared to 0 and an interrupt request signal (INTTM5n) is generated.

Whenever the TM5n value matches the value of CR5n, INTTM5n is generated.

Setting

<1> Set each register.

- Set the port mode register (PM44 or PM43)[Note] to 1.
- TCL5n: Select TI5n pin input edge.
  TI5n pin falling edge → TCL5n = 00H
  TI5n pin rising edge → TCL5n = 01H
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on match of TM5n and CR5n, disable the timer F/F inversion operation, disable timer output
  (TMC5n = 0000××00B) ×: don't care.

<2> When TCE5n = 1 is set, the number of pulses input from the TI5n pin is counted.

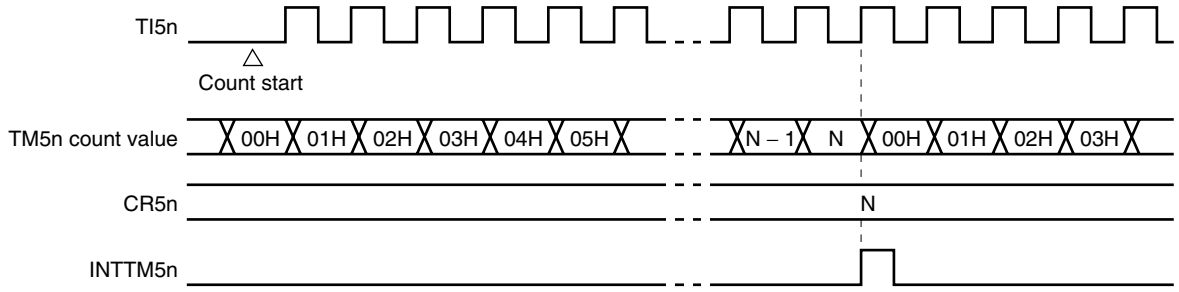
<3> When the values of TM5n and CR5n match, INTTM5n is generated (TM5n is cleared to 00H).

<4> After these settings, INTTM5n is generated each time the values of TM5n and CR5n match.

Note 8-bit timer/event counter 50: PM44
8-bit timer/event counter 51: PM43

Remark For how to enable the INTTM5n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-14. External Event Counter Operation Timing (with Rising Edge Specified)



Remark N = 00H to FFH, n = 0, 1

7.4.3 Square-wave output operation (78K0/LG3-M only)

A square wave with any selected frequency is output at intervals determined by the value preset to 8-bit timer compare register 5n (CR5n).

The TO5n pin output status is inverted at intervals determined by the count value preset to CR5n by setting bit 0 (TOE5n) of 8-bit timer mode control register 5n (TMC5n) to 1. This enables a square wave with any selected frequency to be output (duty = 50%).

Setting

<1> Set each register.

- Clear the port output latch (P44 or P43)[Note] and port mode register (PM44 or PM43)[Note] to 0.
- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on a match of TM5n and CR5n.

LVS5n	LVR5n	Timer Output F/F Status Setting
1	0	Timer output F/F clear (0) (default value of TO5n output: low level)
0	1	Timer output F/F set (1) (default value of TO5n output: high level)

Timer output enabled
(TMC5n = 00001011B or 00000111B)

<2> After TCE5n = 1 is set, the count operation starts.

<3> The timer output F/F is inverted by a match of TM5n and CR5n. After INTTM5n is generated, TM5n is cleared to 00H.

<4> After these settings, the timer output F/F is inverted at the same interval and a square wave is output from TO5n. The frequency is as follows.

- Frequency = 1/2t (N + 1)
  (N: 00H to FFH)

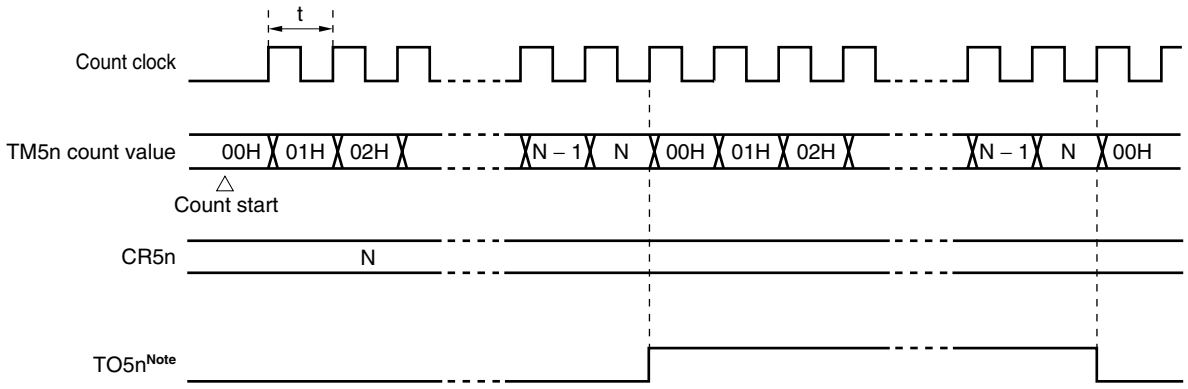
Note 8-bit timer/event counter 50: P44, PM44
8-bit timer/event counter 51: P43, PM43

Caution Do not write other values to CR5n during operation.

Remarks 1. For how to enable the INTTM5n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

2. n = 0, 1

Figure 7-15. Square-Wave Output Operation Timing



Note The initial value of TO5n output can be set by bits 2 and 3 (LVR5n, LVS5n) of 8-bit timer mode control register 5n (TMC5n).

7.4.4 PWM output operation (78K0/LG3-M only)

8-bit timer/event counter 5n operates as a PWM output when bit 6 (TMC5n6) of 8-bit timer mode control register 5n (TMC5n) is set to 1.

The duty pulse determined by the value set to 8-bit timer compare register 5n (CR5n) is output from TO5n.

Set the active level width of the PWM pulse to CR5n; the active level can be selected with bit 1 (TMC5n1) of TMC5n.

The count clock can be selected with bits 0 to 2 (TCL5n0 to TCL5n2) of timer clock selection register 5n (TCL5n).

PWM output can be enabled/disabled with bit 0 (TOE5n) of TMC5n.

Caution In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0, 1

(1) PWM output basic operation

Setting

<1> Set each register.

- Clear the port output latch (P44 or P43)[Note] and port mode register (PM44 or PM43)[Note] to 0.
- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select PWM mode.
  The timer output F/F is not changed.

TMC5n1	Active Level Selection
0	Active-high
1	Active-low

Timer output enabled
(TMC5n = 01000001B or 01000011B)

<2> The count operation starts when TCE5n = 1.
Clear TCE5n to 0 to stop the count operation.

Note 8-bit timer/event counter 50: P44, PM43
8-bit timer/event counter 51: P43, PM43

PWM output operation

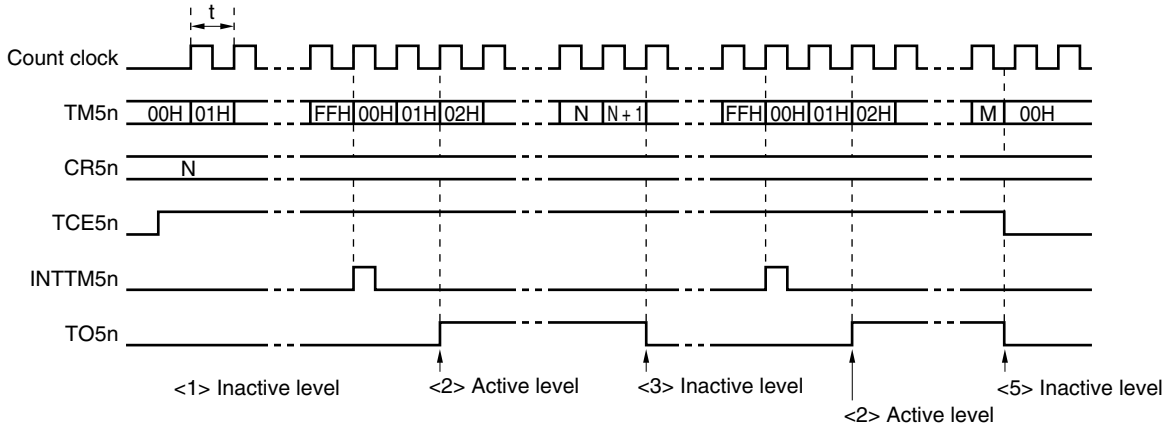
<1> PWM output (TO5n output) outputs an inactive level until an overflow occurs.
<2> When an overflow occurs, the active level is output. The active level is output until CR5n matches the count value of 8-bit timer counter 5n (TM5n).
<3> After the CR5n matches the count value, the inactive level is output until an overflow occurs again.
<4> Operations <2> and <3> are repeated until the count operation stops.
<5> When the count operation is stopped with TCE5n = 0, PWM output becomes inactive.
For details of timing, see **Figure 7-16** and **Figure 7-17**.
The cycle, active-level width, and duty are as follows.

- Cycle = 2^8t
- Active-level width = Nt
- Duty = N/2^8
  (N = 00H to FFH)

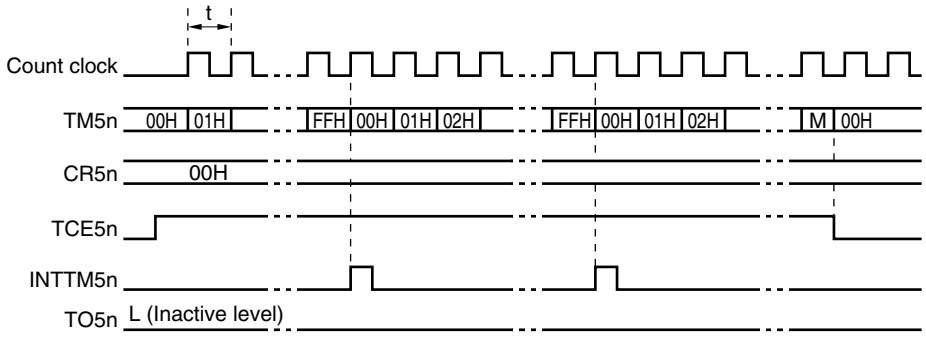
Remark n = 0, 1

Figure 7-16. PWM Output Operation Timing

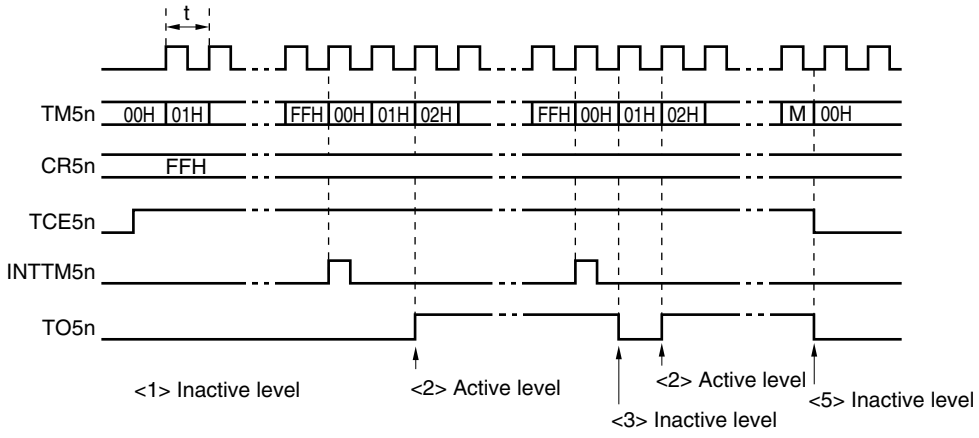
(a) Basic operation (active level = H)



(b) CR5n = 00H



(c) CR5n = FFH



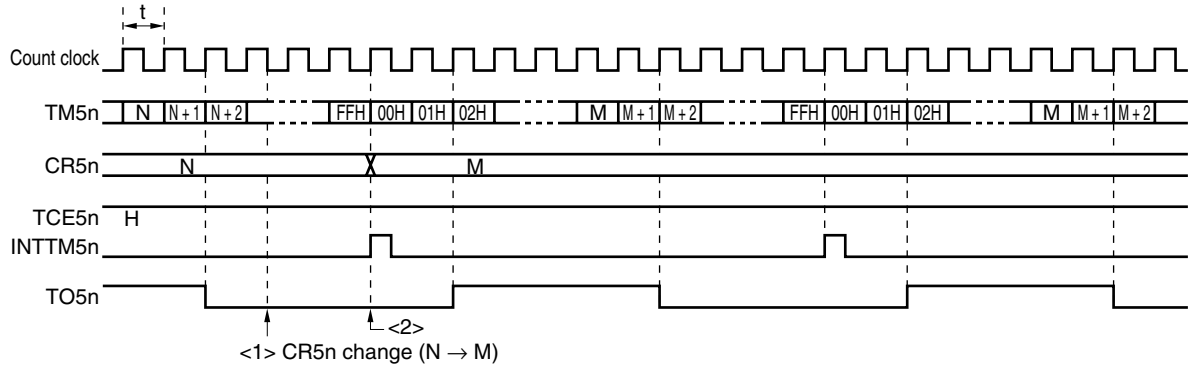
Remarks 1. <1> to <3> and <5> in Figure 7-16 (a) correspond to <1> to <3> and <5> in PWM output operation in **7.4.4 (1) PWM output basic operation**.

2. n = 0, 1

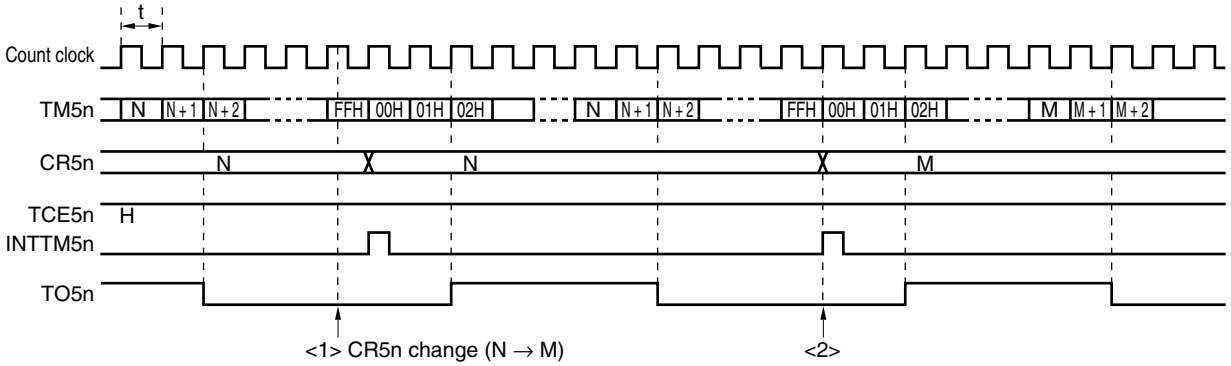
(2) Operation with CR5n changed

Figure 7-17. Timing of Operation with CR5n Changed

(a) CR5n value is changed from N to M before clock rising edge of FFH
→ Value is transferred to CR5n at overflow immediately after change.



(b) CR5n value is changed from N to M after clock rising edge of FFH
→ Value is transferred to CR5n at second overflow.



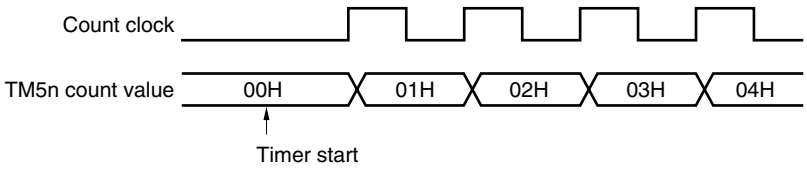
Caution When reading from CR5n between <1> and <2> in Figure 7-17, the value read differs from the actual value (read value: M, actual value of CR5n: N).

7.5 Cautions for 8-Bit Timer/Event Counters 50, 51, and 52

(1) Timer start error

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 8-bit timer counters 50, 51, and 52 (TM50, TM51, and TM52) are started asynchronously to the count clock.

Figure 7-18. Start Timing of 8-Bit Timer Counter 5n (TM5n)

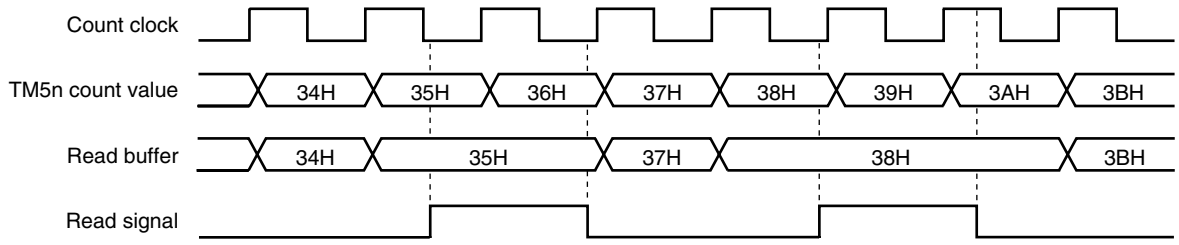


Remark n = 0 to 2

(2) Reading of 8-bit timer counter 5n (TM5n)

TM5n can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 7-19. 8-bit Timer Counter 5n (TM5n) Read Timing



Remark n = 0 to 2

CHAPTER 8 8-BIT TIMERS H0, H1, AND H2

8.1 Functions of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 are mounted onto all 78K0/Lx3-M microcontroller products.

8-bit timers H0, H1, and H2 have the following functions.

	78K0/LE3-M	78K0/LG3-M
Interval timer	TMH0, TMH1, TMH2	TMH0, TMH1, TMH2
Square-wave output	TMH0	TMH0, TMH1
PWM output		
Carrier generator[Note]	TMH1	TMH1

Note TM51 and TMH1 can be used in combination as a carrier generator mode.

8.2 Configuration of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 include the following hardware.

Table 8-1. Configuration of 8-Bit Timers H0, H1, and H2

Item	Configuration
Timer register	8-bit timer counter Hn
Registers	8-bit timer H compare register 0n (CMP0n) 8-bit timer H compare register 1n (CMP1n)
Timer output	78K0/LE3-M : TOH0, Output controller 78K0/LG3-M : TOH0, TOH1, Output controller
Control registers	8-bit timer H mode register n (TMHMDn) 8-bit timer H carrier control register 1 (TMCYC1)[Note] Port mode register 3 (PM3) Port register 3 (P3)

Note 8-bit timer H1 only.

Remarks 1. TMH2 does not have an output pin (TOH2). It can only be used as an internal interrupt (INTTMH2).

2. TMH1 of 78K0/LE3-M does not have an output pin (TOH1). It can only be used as an remote controller output signal.

3. n = 0 to 2.

Figure 8-1 to Figure 8-3 show the block diagrams.

Figure 8-1. Block Diagram of 8-Bit Timer H0

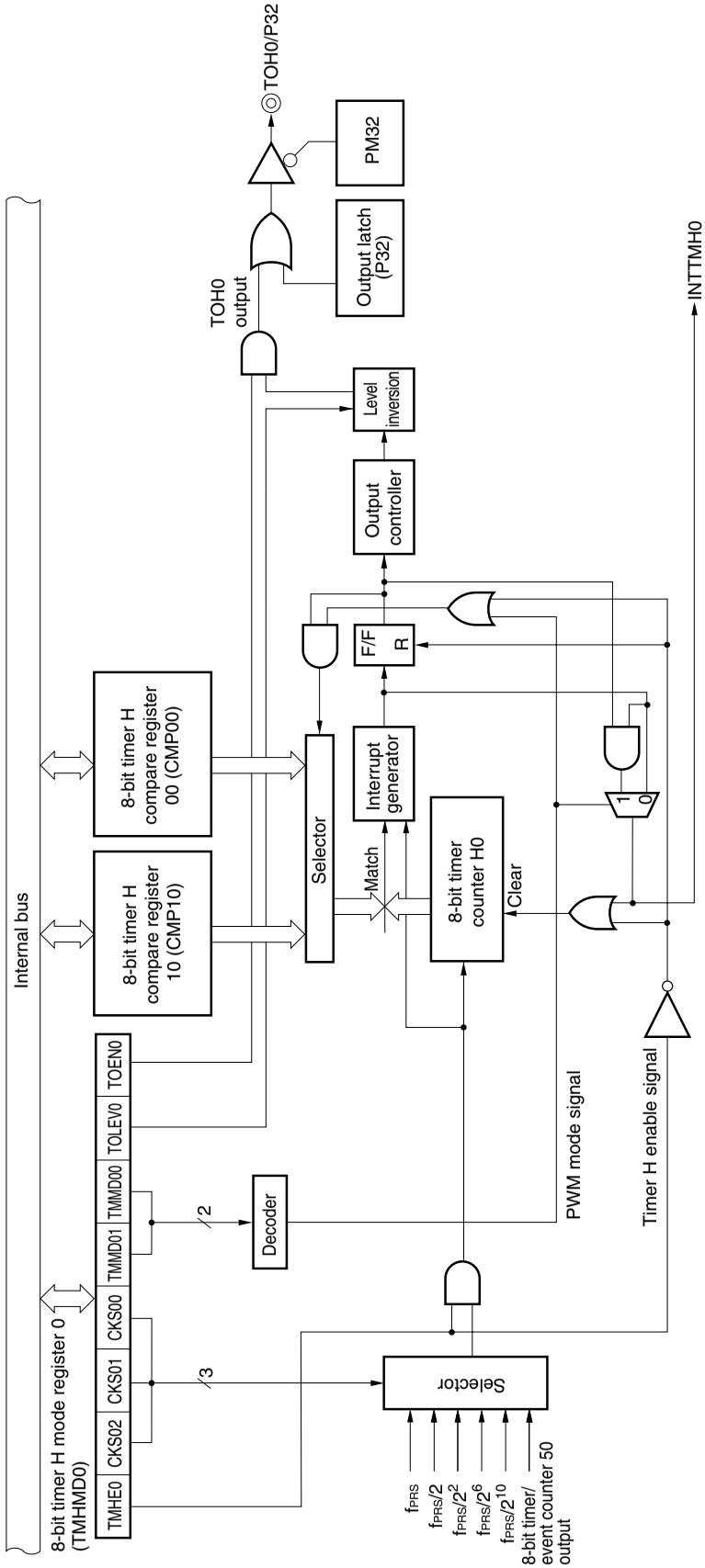


Figure 8-2. Block Diagram of 8-Bit Timer H1 (1/2)

(a) 78K0/LE3-M

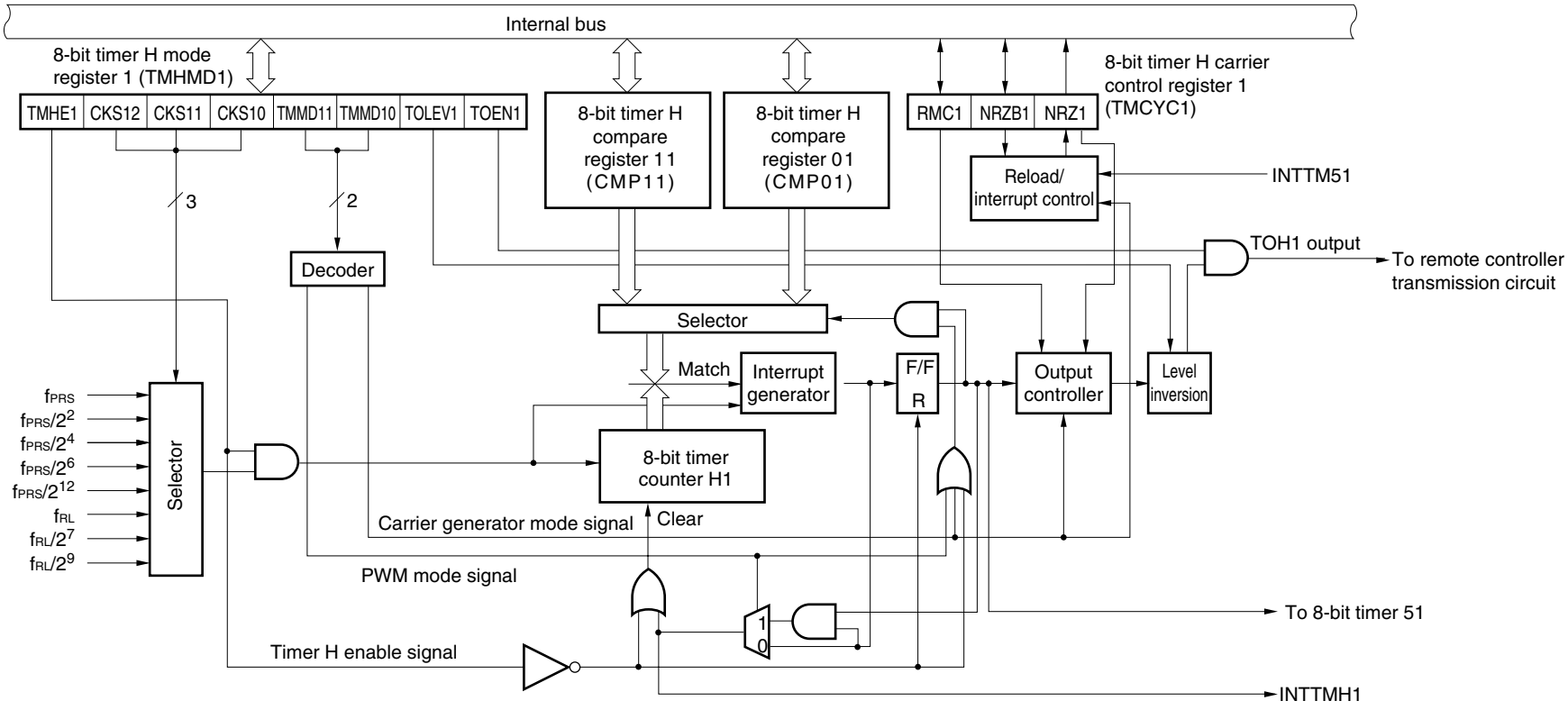


Figure 8-2. Block Diagram of 8-Bit Timer H1 (2/2)

(b) 78K0/LG3-M

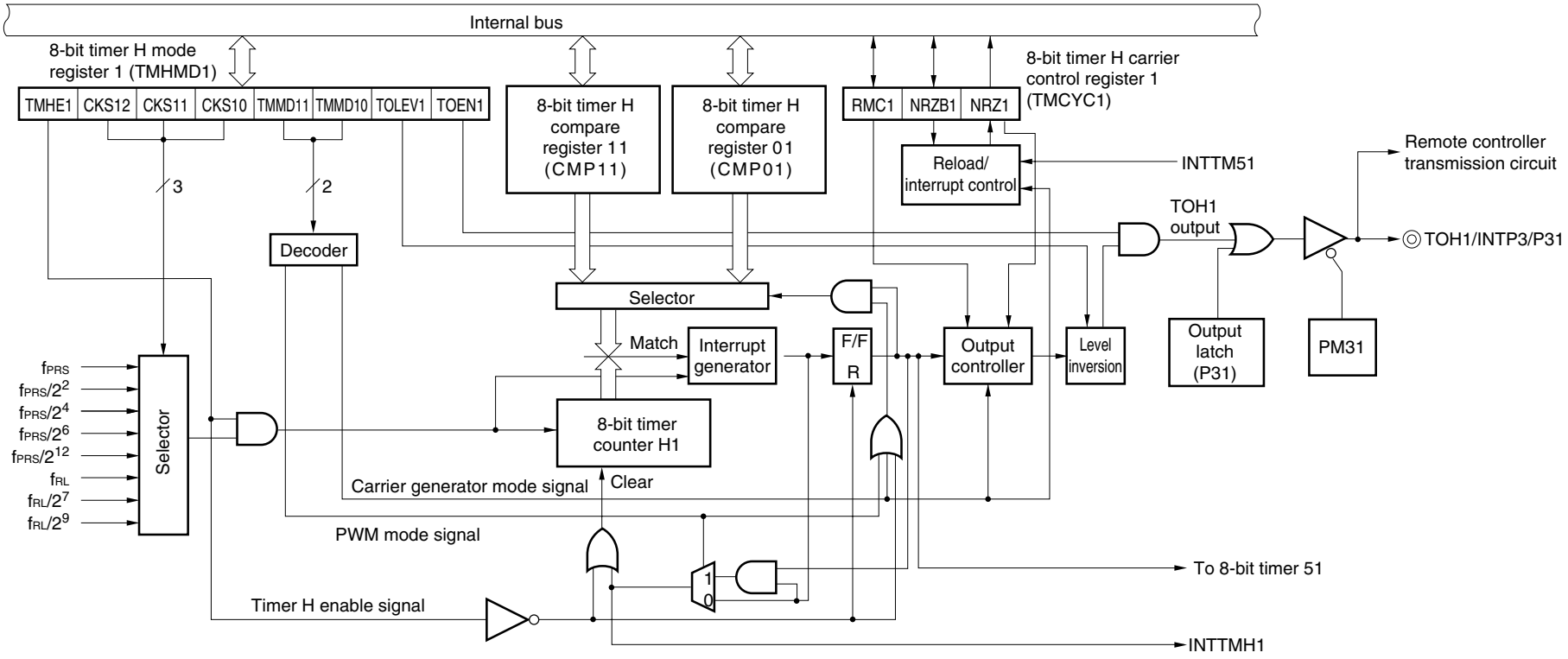
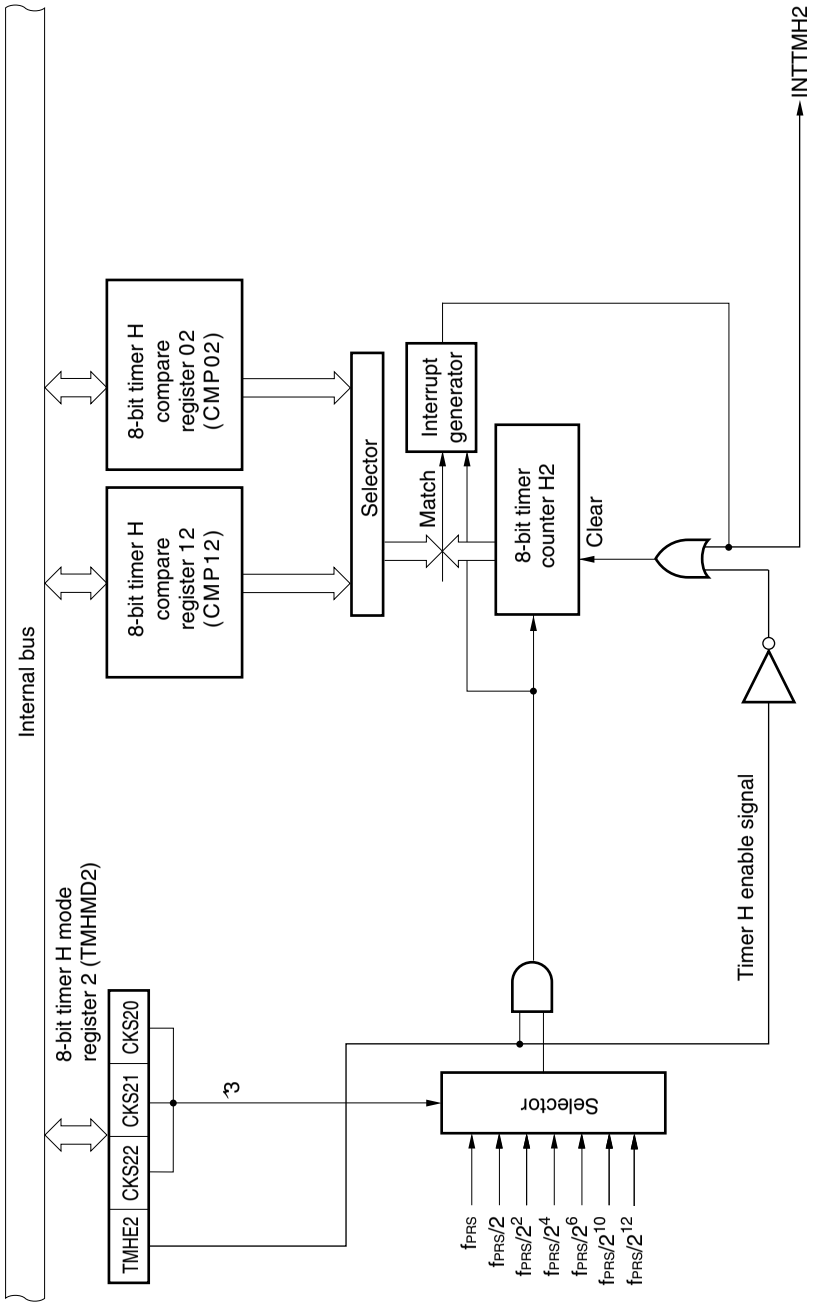


Figure 8-3. Block Diagram of 8-Bit Timer H2



(1) 8-bit timer H compare register 0n (CMP0n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in all of the timer operation modes.

This register constantly compares the value set to CMP0n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn) and inverts the output level of TOHn.

Rewrite the value of CMP0n while the timer is stopped (TMHEn = 0).

A reset signal generation sets this register to 00H.

Figure 8-4. Format of 8-Bit Timer H Compare Register 0n (CMP0n)

Address: FF18H (CMP00), FF1AH (CMP01), FF44H (CMP02) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP0n (n = 0 to 2)								

Caution CMP0n cannot be rewritten during timer count operation. CMP0n can be refreshed (the same value is written) during timer count operation.

(2) 8-bit timer H compare register 1n (CMP1n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, inverts the output level of TOHn. No interrupt request signal is generated.

In the carrier generator mode, the CMP1n register always compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn). At the same time, the count value is cleared.

CMP1n can be rewritten during timer count operation.

If the value of CMP1n is rewritten while the timer is operating, the new value is latched and transferred to CMP1n when the count value of the timer matches the old value of CMP1n, and then the value of CMP1n is changed to the new value. If matching of the count value and the CMP1n value and writing a value to CMP1n conflict, the value of CMP1n is not changed.

A reset signal generation sets this register to 00H.

Figure 8-5. Format of 8-Bit Timer H Compare Register 1n (CMP1n)

Address: FF19H (CMP10), FF1BH (CMP11), FF45H (CMP12) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP1n (n = 0 to 2)								

Caution In the PWM output mode and carrier generator mode, be sure to set CMP1n when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to CMP1n).

Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M, TOH0 and TOH1 only for 78K0/LG3-M.

8.3 Registers Controlling 8-Bit Timers H0, H1, and H2

The following four registers are used to control 8-bit timers H0, H1, and H2.

- 8-bit timer H mode register n (TMHMDn)
- 8-bit timer H carrier control register 1 (TMCYC1)[Note]
- Port mode register 3 (PM3)
- Port register 3 (P3)

Note 8-bit timer H1 only.

(1) 8-bit timer H mode register n (TMHMDn)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Remark n = 0 to 2

Figure 8-6. Format of 8-Bit Timer H Mode Register 0 (TMHMD0)

Address: FF69H After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKS02	CKS01	CKS00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS02	CKS01	CKS00	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz
1	0	1	TM50 output[Note 3]			
Other than above			Setting prohibited			

TMMD01	TMMD00	Timer operation mode
0	0	Interval timer mode
1	0	PWM mode
Other than above		Setting prohibited

TOLEV0	Timer output level control (in default mode)
0	Low level
1	High level

TOEN0	Timer output control
0	Disables output
1	Enables output

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS02 = CKS01 = CKS00 = 0 (count clock: f_{PRS}) is prohibited.

Notes 3. Note the following points when selecting the TM50 output as the count clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of the 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of the 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. When TMHE0 = 1, setting the other bits of TMHMD0 is prohibited. However, TMHMD0 can be refreshed (the same value is written).

2. In the PWM output mode, be sure to set the 8-bit timer H compare register 10 (CMP10) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to CMP10).

3. The actual TOH0/P32 pin output is determined depending on PM32 and P32, besides TOH0 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

Figure 8-7. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz
1	0	1	$f_{RL}/2^7$	1.88 kHz (TYP.)		
1	1	0	$f_{RL}/2^9$	0.47 kHz (TYP.)		
1	1	1	f_{RL}	240 kHz (TYP.)		

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode[Note 3]
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS12 = CKS11 = CKS10 = 0 (count clock: f_{PRS}) is prohibited.

3. 78K0/LG3-M only.

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

4. The actual TOH1/P31/INTP3 pin output is determined depending on PM31 and P31, besides TOH1 output.

5. If using the P13/SO10/TxD0 pin function for the 78K0/LE3-M, do not use the 8-bit timer H1 (TMHE1 = 0).

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. f_{RL}: Internal low-speed oscillation clock frequency

Figure 8-8. Format of 8-Bit Timer H Mode Register 2 (TMHMD2)

Address: FF42H After reset: 00H R/W

	<7>	6	5	4	3	2	1	0
TMHMD2	TMHE2	CKS22	CKS21	CKS20	0	0	0	0

TMHE2	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS22	CKS21	CKS20	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
1	0	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	1	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz
1	1	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz
Other than above			Setting prohibited			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS22 = CKS21 = CKS20 = 0 (count clock: f_{PRS}) is prohibited.

Caution When TMHE2 = 1, setting the other bits of TMHMD2 is prohibited.

Remark f_{PRS}: Peripheral hardware clock frequency

(2) 8-bit timer H carrier control register 1 (TMCYC1)

This register controls the remote control output and carrier pulse output status of 8-bit timer H1.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 8-9. Format of 8-Bit Timer H Carrier Control Register 1 (TMCYC1)

Address: FF6DH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	<0>
TMCYC1	0	0	0	0	0	RMC1	NRZB1	NRZ1

RMC1	NRZB1	Remote control output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

NRZ1	Carrier pulse output status flag
0	Carrier output disabled status (low-level status)
1	Carrier output enabled status (RMC1 = 1: Carrier pulse output, RMC1 = 0: High-level status)

Note Bit 0 is read-only.

Caution Do not rewrite RMC1 when TMHE1 = 1. However, TMCYC1 can be refreshed (the same value is written).

(3) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0 and P31/TOH1/INTP3 pins for timer output, clear PM32 and PM31 and the output latches of P32 and P31 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 8-10. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

8.4 Operation of 8-Bit Timers H0, H1 and H2

8.4.1 Operation as interval timer/square-wave output

When the 8-bit timer counter Hn and compare register 0n (CMP0n) match, an interrupt request signal (INTTMHn) is generated and the 8-bit timer counter Hn is cleared to 00H.

Compare register 1n (CMP1n) is not used in interval timer mode. Since a match of the 8-bit timer counter Hn and the CMP1n register is not detected even if the CMP1n register is set, timer output is not affected.

By setting bit 0 (TOENn) of timer H mode register n (TMHMDn) to 1, a square wave of any frequency (duty = 50%) is output from TOHn.

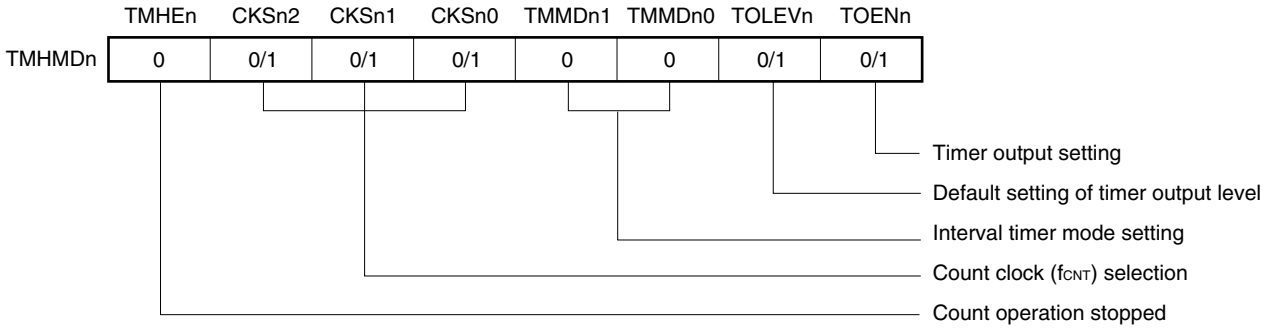
The timer output of TMH2 can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

Figure 8-11. Register Setting During Interval Timer/Square-Wave Output Operation

(i) Setting timer H mode register n (TMHMDn)



(ii) CMP0n register setting

The interval time is as follows if N is set as a comparison value.

- Interval time = (N +1)/f_{CNT}

<2> Count operation starts when TMHEn = 1.

<3> When the values of the 8-bit timer counter Hn and the CMP0n register match, the INTTMHn signal is generated and the 8-bit timer counter Hn is cleared to 00H.

<4> Subsequently, the INTTMHn signal is generated at the same interval. To stop the count operation, clear TMHEn to 0.

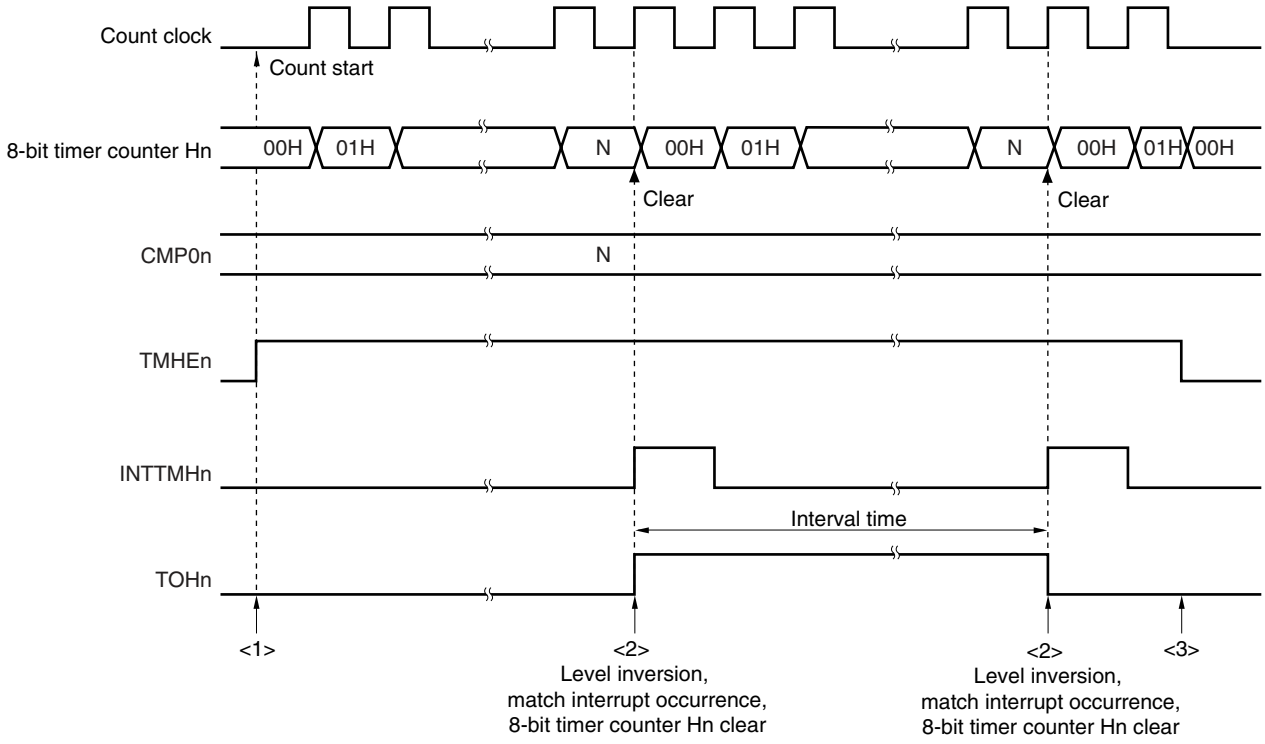
Remarks 1. For the setting of the output pin, see **8.3 (3) Port mode register 3 (PM3)**.

2. For how to enable the INTTMHn signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

3. n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

Figure 8-12. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (Operation When 01H ≤ CMP0n ≤ FEH)



<1> The count operation is enabled by setting the TMHEn bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the value of the 8-bit timer counter Hn matches the value of the CMP0n register, the value of the timer counter is cleared, and the level of the TOHn output is inverted. In addition, the INTTMHn signal is output at the rising edge of the count clock.

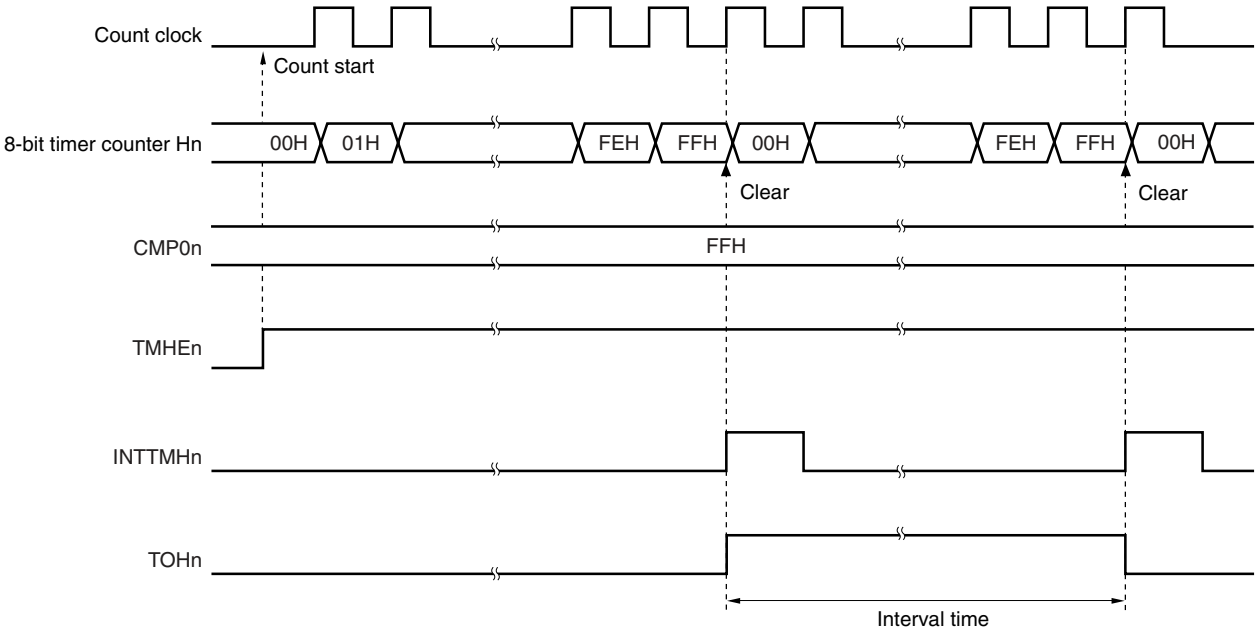
<3> If the TMHEn bit is cleared to 0 while timer H is operating, the INTTMHn signal and TOHn output are set to the default level. If they are already at the default level before the TMHEn bit is cleared to 0, then that level is maintained.

Remarks 1. n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

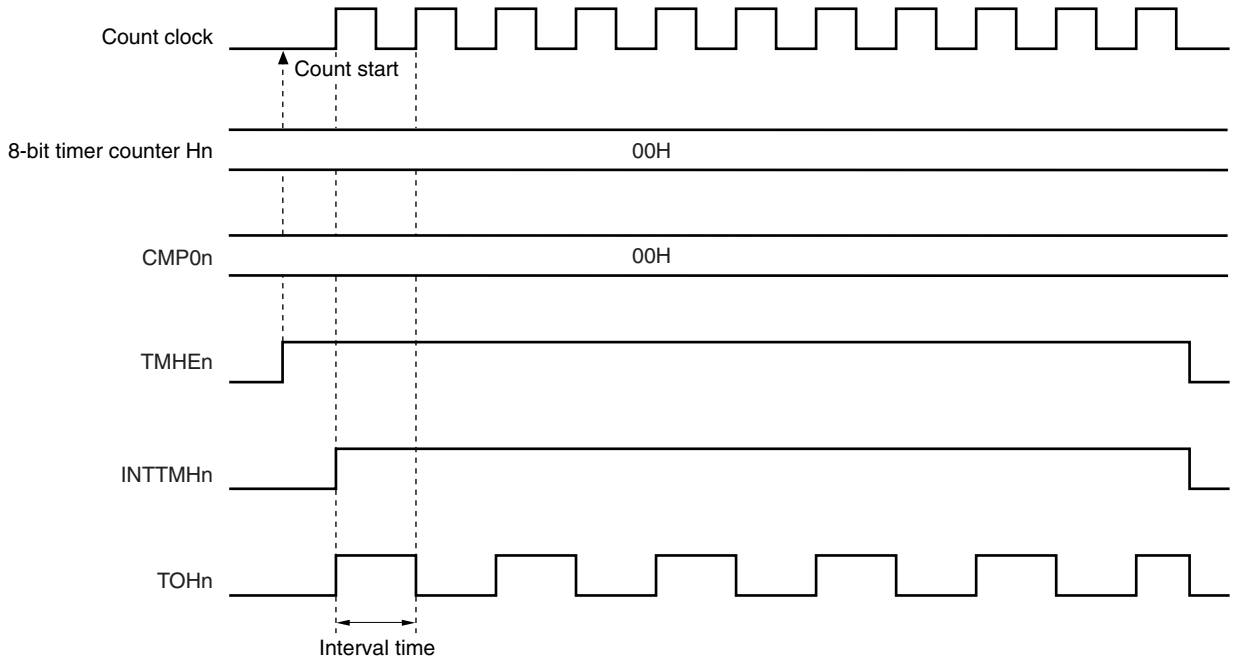
2. 01H ≤ N ≤ FEH

Figure 8-12. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP0n = FFH



(c) Operation when CMP0n = 00H



Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

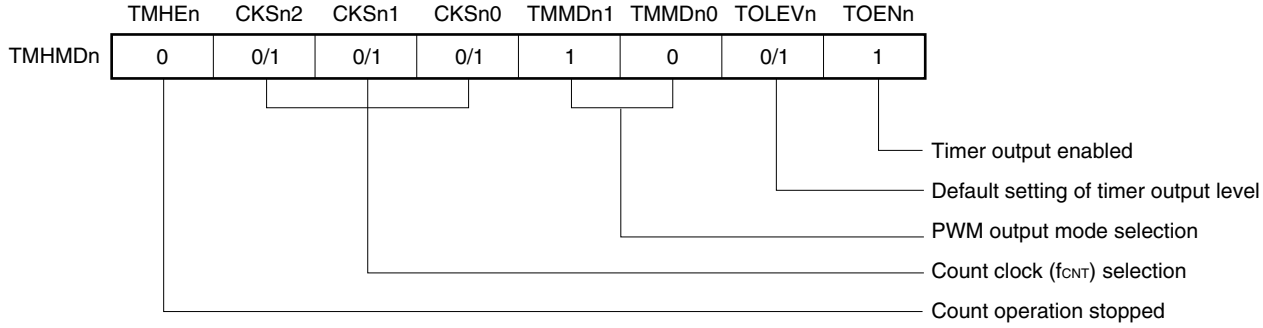
The timer output of TMH2 (PWM output) can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

Figure 8-13. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHEn = 0.

If the setting value of the CMP0n register is N, the setting value of the CMP1n register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP1n register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMDn register) from when the value of the CMP1n register is changed until the value is transferred to the register.

2. Be sure to set the CMP1n register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMP1n register).

3. Make sure that the CMP1n register setting value (M) and CMP0n register setting value (N) are within the following range.

00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

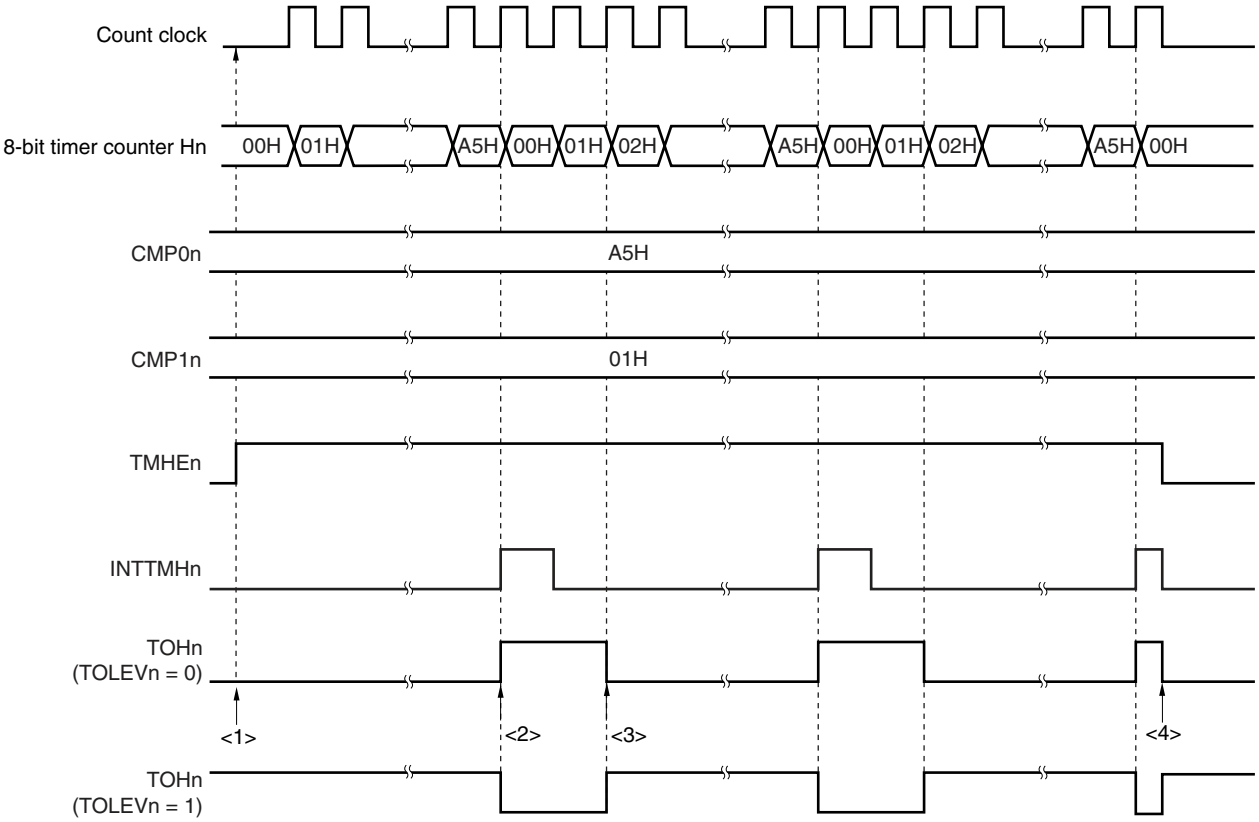
Remarks 1. For the setting of the output pin, see **8.3 (3) Port mode register 3 (PM3)**.

2. For details on how to enable the INTTMHn signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

3. n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

Figure 8-14. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHEn bit to 1. Start 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> When the values of 8-bit timer counter Hn and the CMP0n register match, an active level is output. At this time, the value of 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

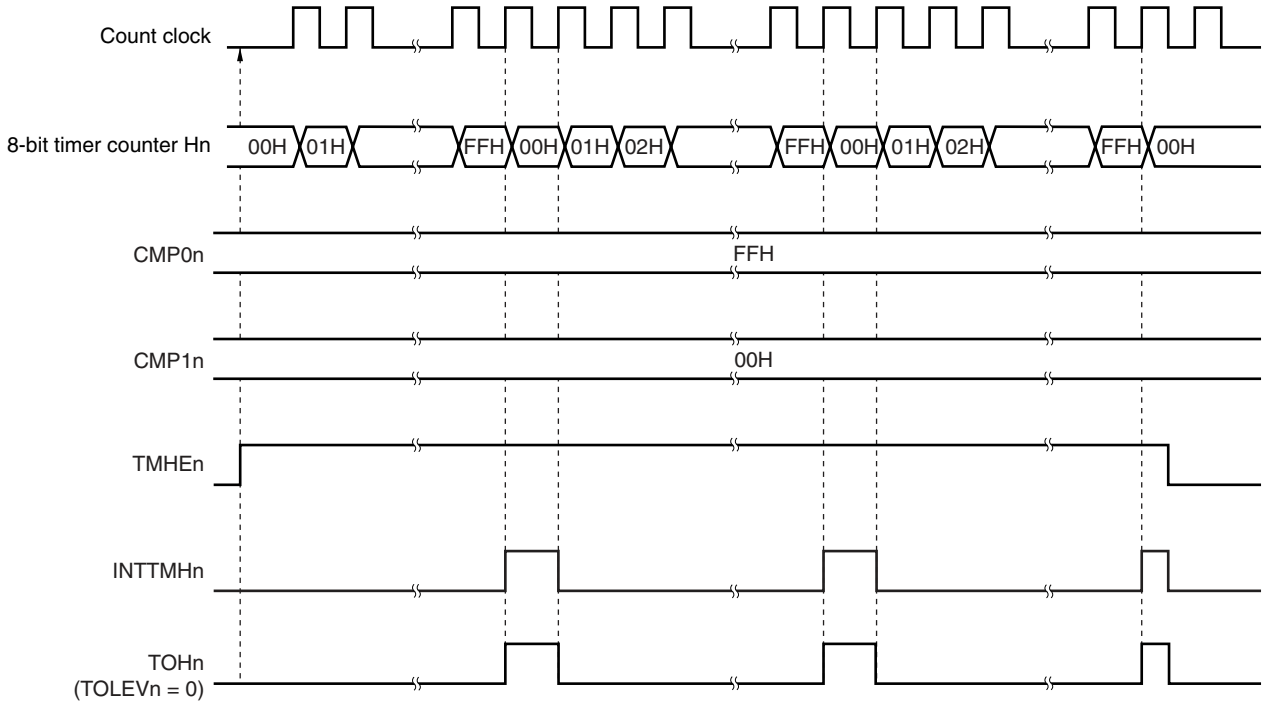
<3> When the values of 8-bit timer counter Hn and the CMP1n register match, an inactive level is output. At this time, the 8-bit counter value is not cleared and the INTTMHn signal is not output.

<4> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

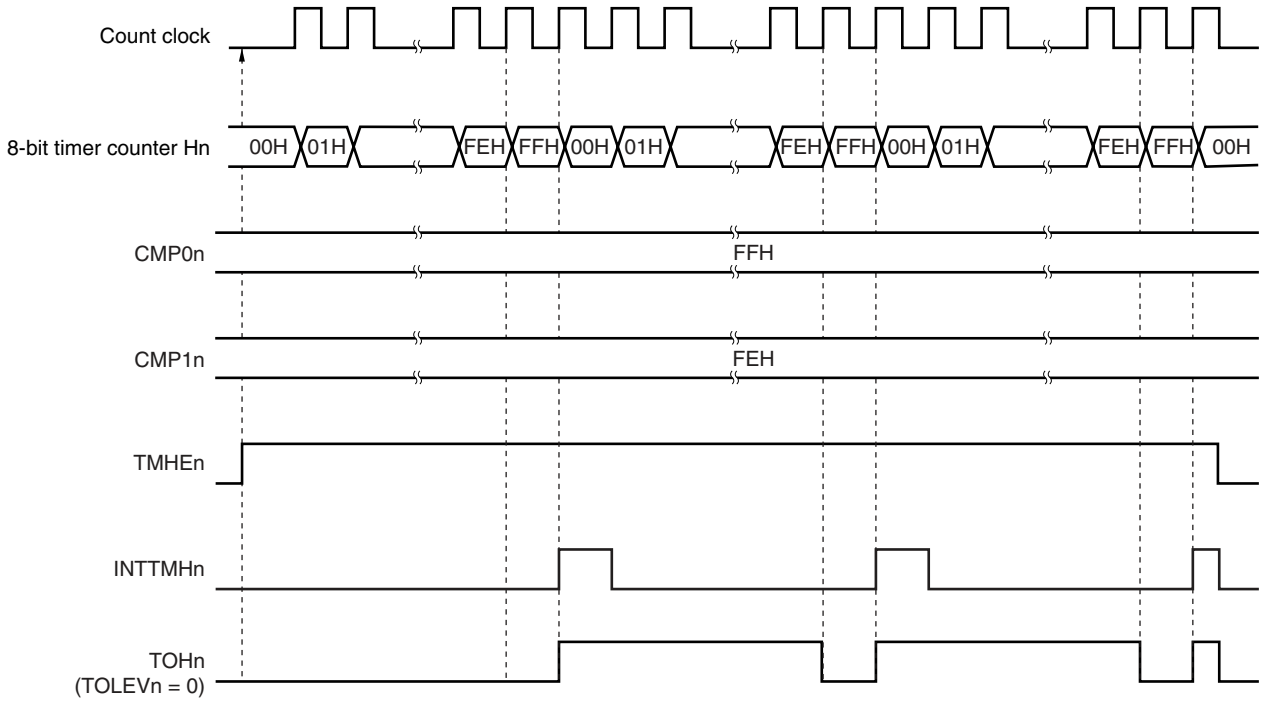
Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

Figure 8-14. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP0n = FFH, CMP1n = 00H



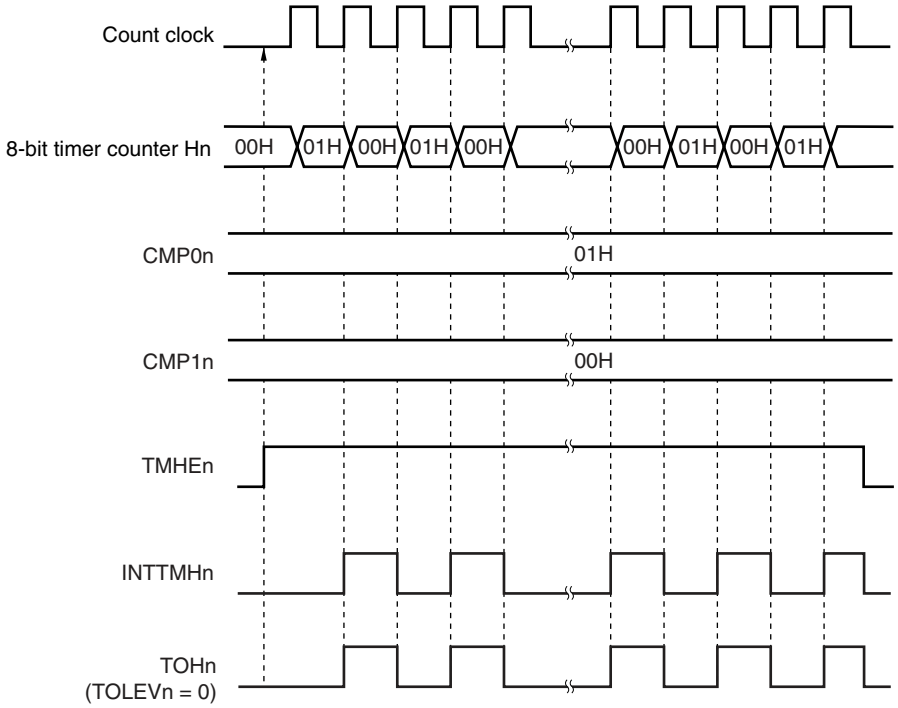
(c) Operation when CMP0n = FFH, CMP1n = FEH



Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

Figure 8-14. Operation Timing in PWM Output Mode (3/4)

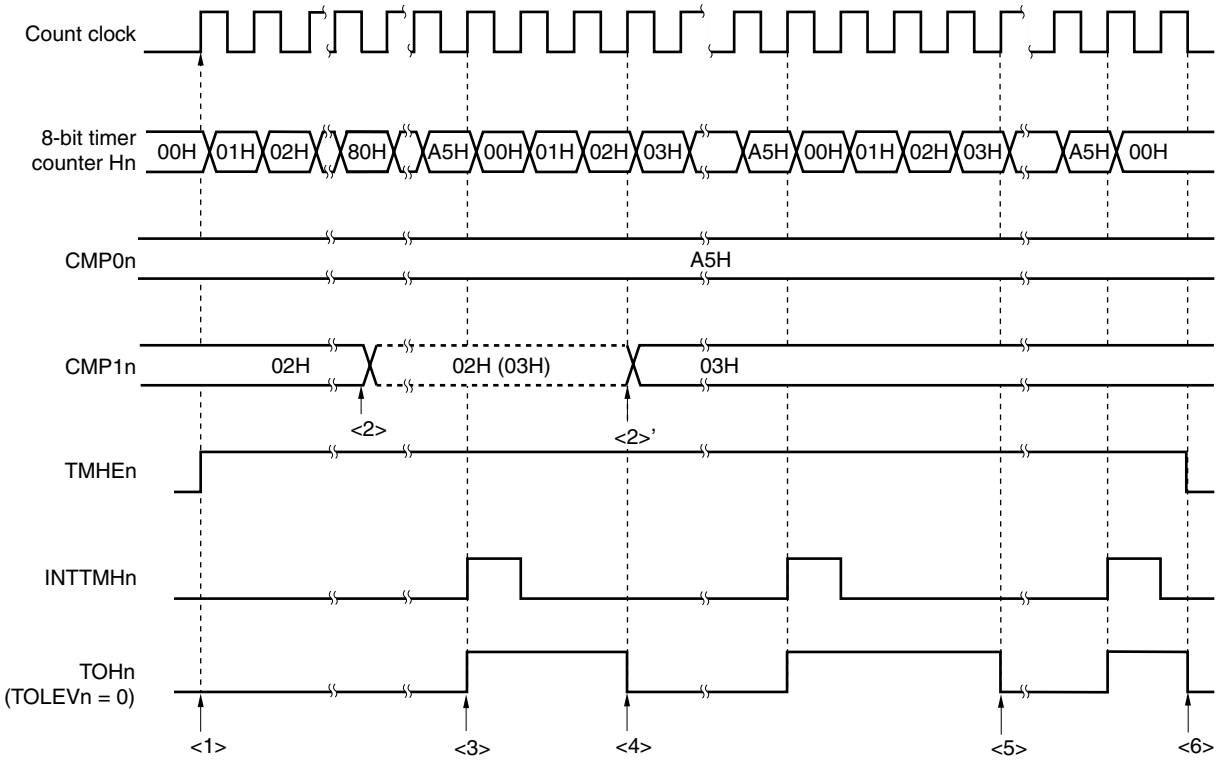
(d) Operation when CMP0n = 01H, CMP1n = 00H



Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

Figure 8-14. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP1n (CMP1n = 02H → 03H, CMP0n = A5H)



<1> The count operation is enabled by setting TMHEn = 1. Start 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> The CMP1n register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of 8-bit timer counter Hn and the CMP0n register match, the value of 8-bit timer counter Hn is cleared, an active level is output, and the INTTMHn signal is output.

<4> If the CMP1n register value is changed, the value is latched and not transferred to the register. When the values of the 8-bit timer counter Hn and the CMP1n register before the change match, the value is transferred to the CMP1n register and the CMP1n register value is changed (<2>').

However, three count clocks or more are required from when the CMP1n register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the values of 8-bit timer counter Hn and the CMP1n register after the change match, an inactive level is output. 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark n = 0 to 2, however, TOH0 only for 78K0/LE3-M. TOH0 and TOH1 only for 78K0/LG3-M.

8.4.3 Carrier generator operation (8-bit timer H1 only)

In the carrier generator mode, the 8-bit timer H1 is used to generate the carrier signal of an infrared remote controller, and the 8-bit timer/event counter 51 is used to generate an infrared remote control signal (time count).

The carrier clock generated by the 8-bit timer H1 is output in the cycle set by the 8-bit timer/event counter 51.

In carrier generator mode, the output of the 8-bit timer H1 carrier pulse is controlled by the 8-bit timer/event counter 51, and the carrier pulse is output from the TOH1 output.

(1) Carrier generation

In carrier generator mode, the 8-bit timer H compare register 01 (CMP01) generates a low-level width carrier pulse waveform and the 8-bit timer H compare register 11 (CMP11) generates a high-level width carrier pulse waveform.

Rewriting the CMP11 register during the 8-bit timer H1 operation is possible but rewriting the CMP01 register is prohibited.

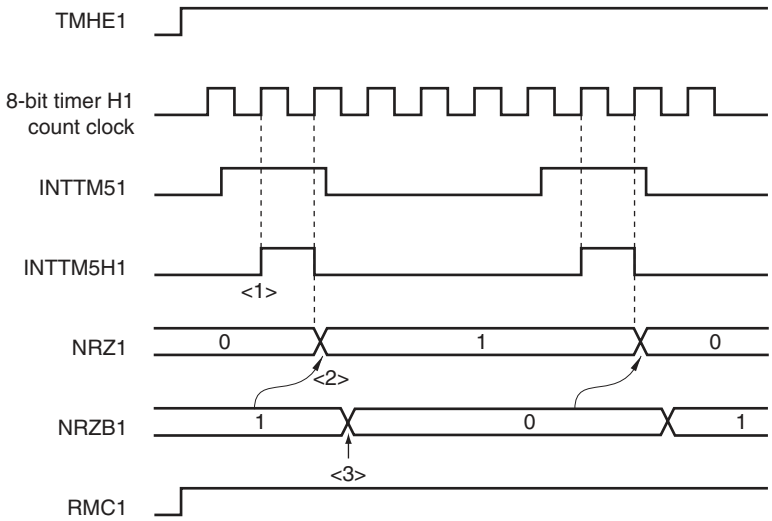
(2) Carrier output control

Carrier output is controlled by the interrupt request signal (INTTM51) of the 8-bit timer/event counter 51 and the NRZB1 and RMC1 bits of the 8-bit timer H carrier control register (TMCYC1). The relationship between the outputs is shown below.

RMC1 Bit	NRZB1 Bit	Output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

To control the carrier pulse output during a count operation, the NRZ1 and NRZB1 bits of the TMCYC1 register have a master and slave bit configuration. The NRZ1 bit is read-only but the NRZB1 bit can be read and written. The INTTM51 signal is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal of the NRZ1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit. The timing for transfer from the NRZB1 bit to the NRZ1 bit is as shown below.

Figure 8-15. Transfer Timing



<1> The INTTM51 signal is synchronized with the count clock of the 8-bit timer H1 and is output as the INTTM5H1 signal.

<2> The value of the NRZB1 bit is transferred to the NRZ1 bit at the second clock from the rising edge of the INTTM5H1 signal.

<3> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

Cautions 1. Do not rewrite the NRZB1 bit again until at least the second clock after it has been rewritten, or else the transfer from the NRZB1 bit to the NRZ1 bit is not guaranteed.

2. When the 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated at the timing of <1>. When the 8-bit timer/event counter 51 is used in a mode other than the carrier generator mode, the timing of the interrupt generation differs.

Remark INTTM5H1 is an internal signal and not an interrupt source.

Setting

<1> Set each register.

Figure 8-16. Register Setting in Carrier Generator Mode

(i) Setting 8-bit timer H mode register 1 (TMHMD1)

(ii) CMP01 register setting

- Compare value

(iii) CMP11 register setting

- Compare value

(iv) TMCYC1 register setting

- RMC1 = 1 ... Remote control output enable bit
- NRZB1 = 0/1 ... carrier output enable bit

(v) TCL51 and TMC51 register setting

- See **7.3 Registers Controlling 8-Bit Timer/Event Counters 50, 51, and 52**.

<2> When TMHE1 = 1, the 8-bit timer H1 starts counting.

<3> When TCE51 of the 8-bit timer mode control register 51 (TMC51) is set to 1, the 8-bit timer/event counter 51 starts counting.

<4> After the count operation is enabled, the first compare register to be compared is the CMP01 register. When the count value of the 8-bit timer counter H1 and the CMP01 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register.

<5> When the count value of the 8-bit timer counter H1 and the CMP11 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register.

<6> By performing procedures <4> and <5> repeatedly, a carrier clock is generated.

<7> The INTTM51 signal is synchronized with count clock of the 8-bit timer H1 and output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.

<8> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

<9> When the NRZ1 bit is high level, a carrier clock is output by TOH1 output.

<10> By performing the procedures above, an arbitrary carrier clock is obtained. To stop the count operation, clear TMHE1 to 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the carrier clock output cycle and duty are as follows.

- Carrier clock output cycle = (N + M + 2)/f_{CNT}
- Duty = High-level width/carrier clock output width = (M + 1)/(N + M + 2)

Cautions 1. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

2. Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

3. Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.

4. The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.

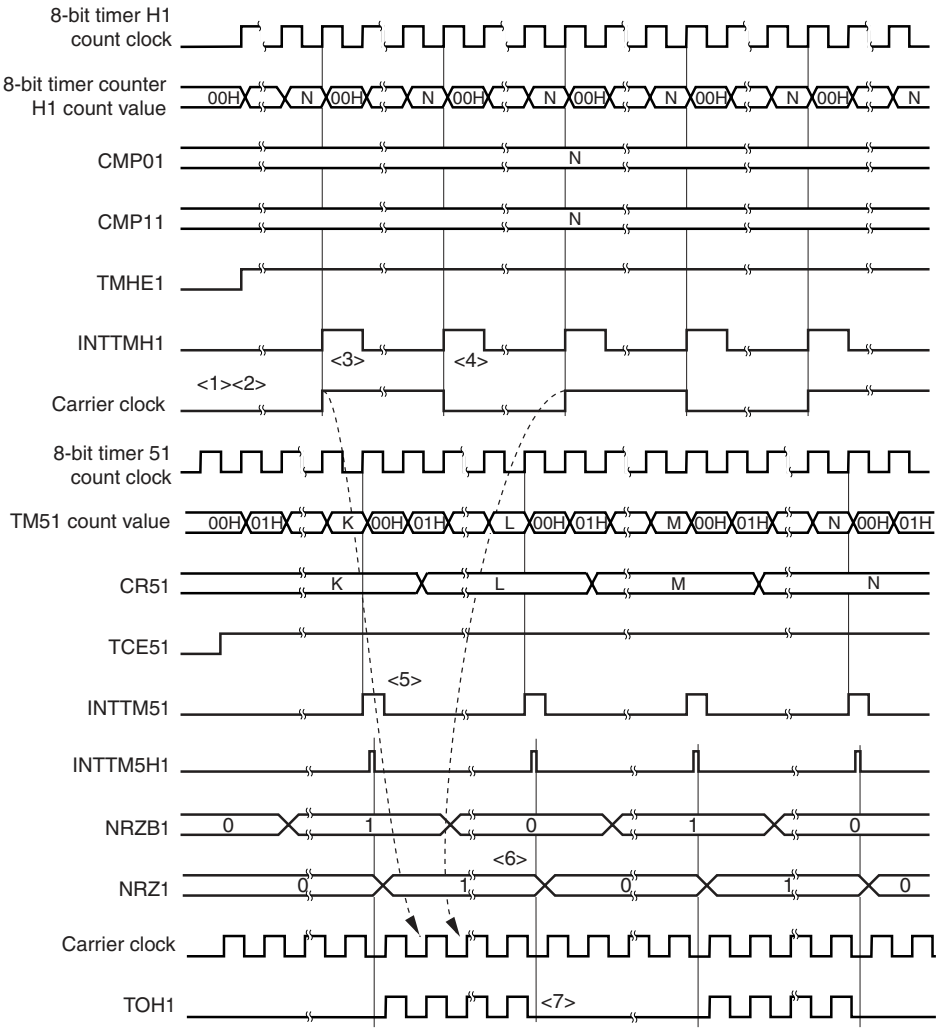
5. Be sure to set the RMC1 bit before the count operation is started.

Remarks 1. For the setting of the output pin, see **8.3 (3) Port mode register 3 (PM3)**.

2. For how to enable the INTTMH1 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 8-17. Carrier Generator Mode Operation Timing (1/3)

(a) Operation when CMP01 = N, CMP11 = N



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

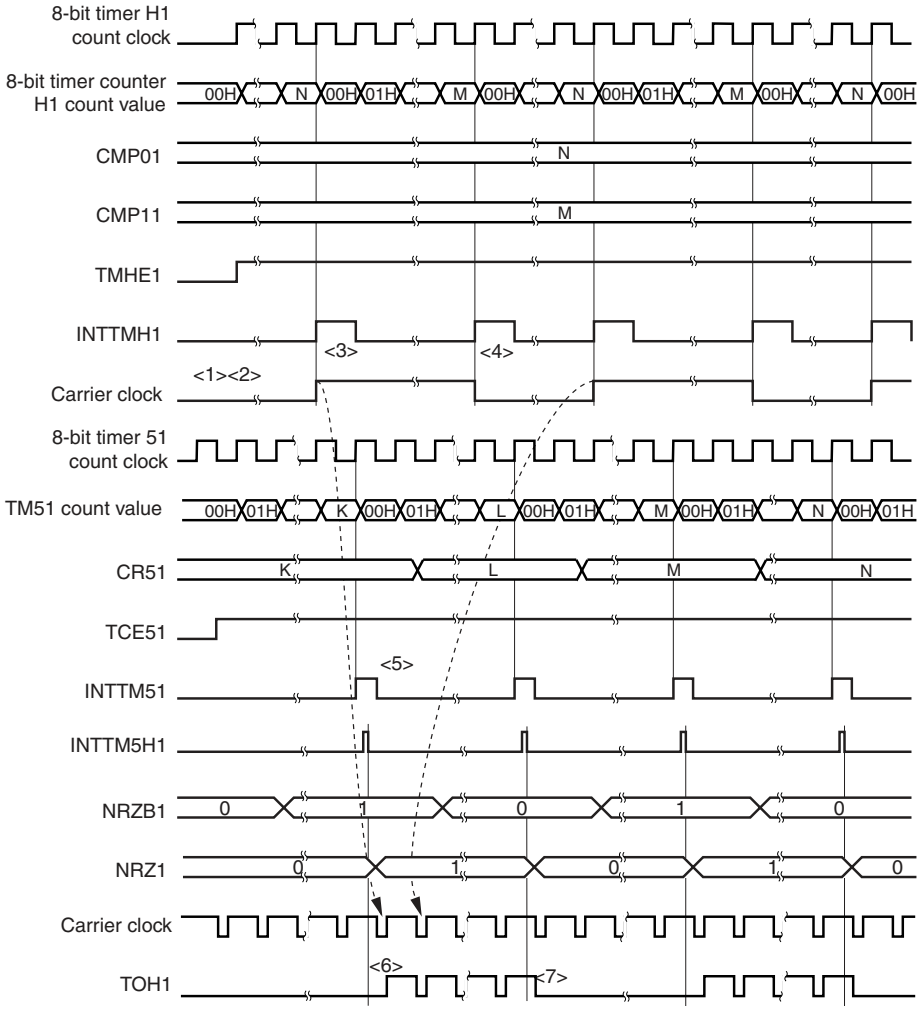
<6> The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.

<7> When NRZ1 = 0 is set, the TOH1 output becomes low level.

Remark INTTM5H1 is an internal signal and not an interrupt source.

Figure 8-17. Carrier Generator Mode Operation Timing (2/3)

(b) Operation when CMP01 = N, CMP11 = M



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to other than 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

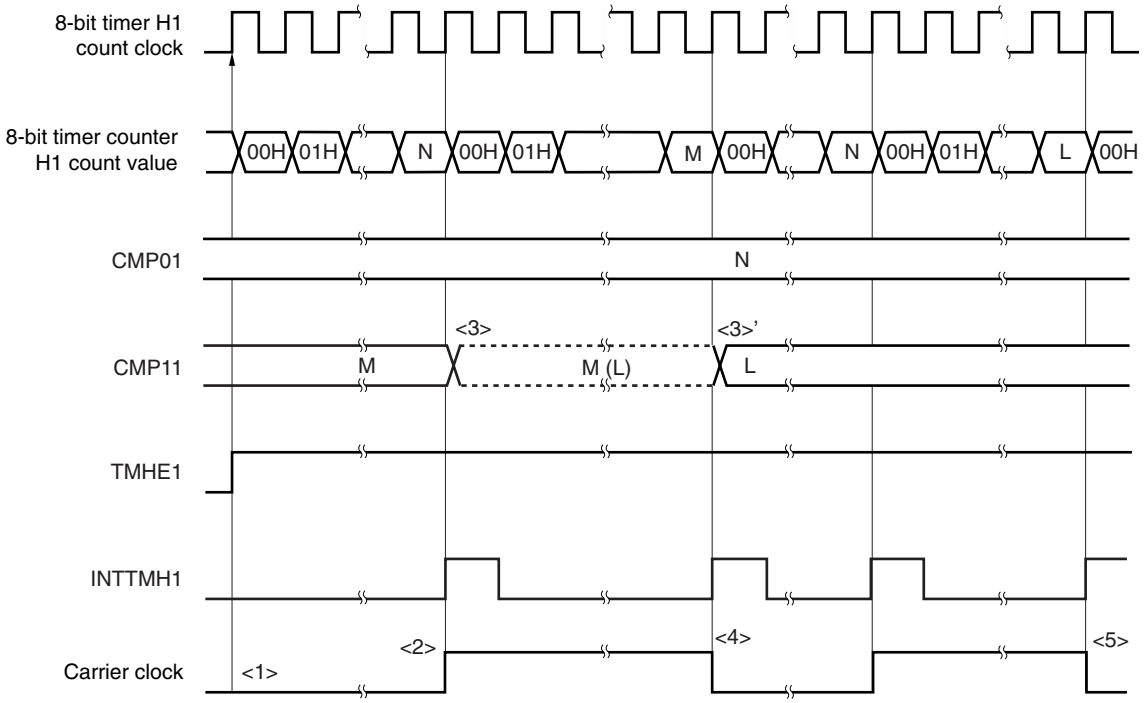
<6> A carrier signal is output at the first rising edge of the carrier clock if NRZ1 is set to 1.

<7> When NRZ1 = 0, the TOH1 output is held at the high level and is not changed to low level while the carrier clock is high level (from <6> and <7>, the high-level width of the carrier clock waveform is guaranteed).

Remark INTTM5H1 is an internal signal and not an interrupt source.

Figure 8-17. Carrier Generator Mode Operation Timing (3/3)

(c) Operation when CMP11 is changed



<1> When TMHE1 = 1 is set, the 8-bit timer H1 starts a count operation. At that time, the carrier clock remains default.

<2> When the count value of the 8-bit timer counter H1 matches the value of the CMP01 register, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<3> The CMP11 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer H1 is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the CMP11 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMP11 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter H1 matches the value (M) of the CMP1 register before the change, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register.

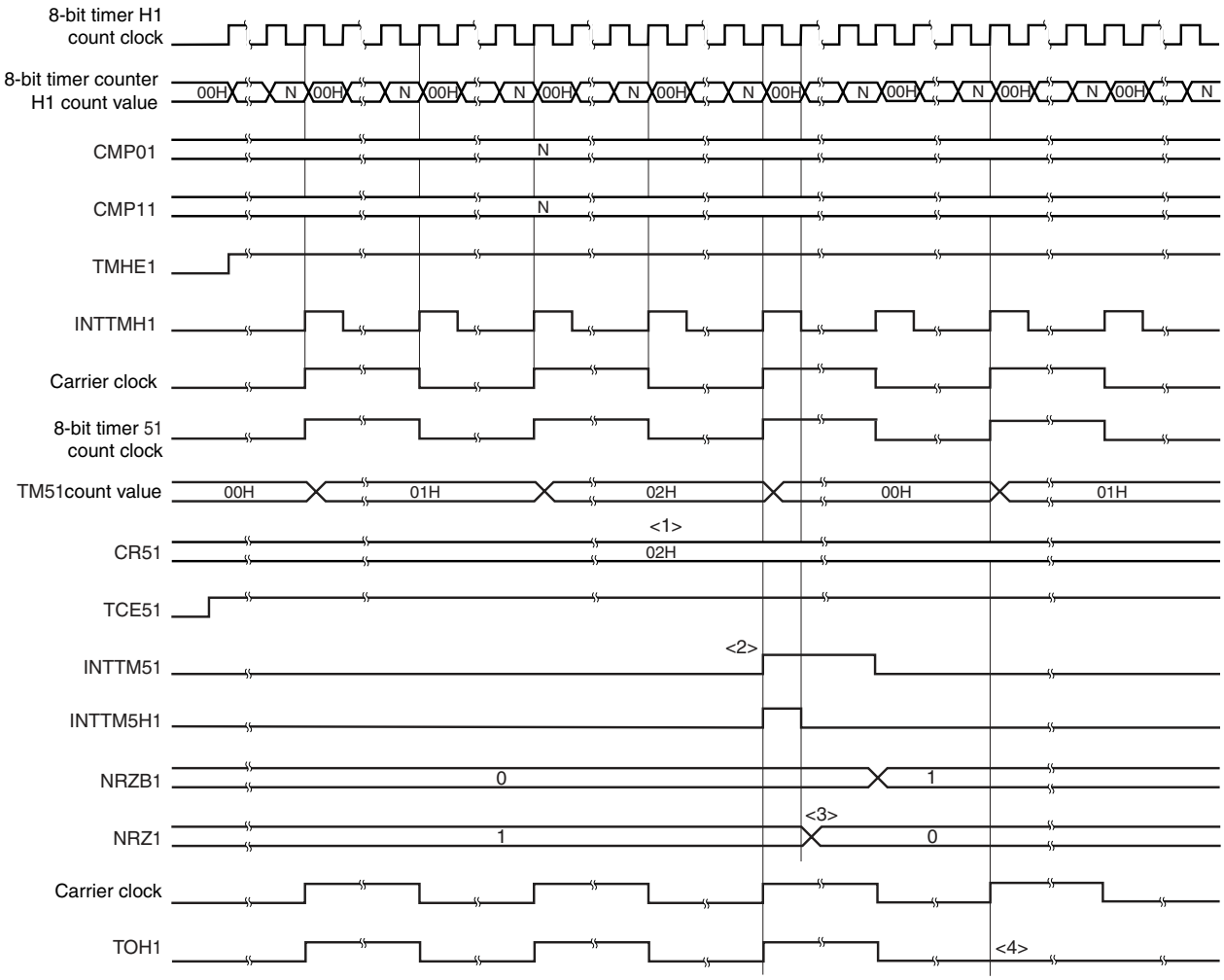
<5> The timing at which the count value of the 8-bit timer counter H1 and the CMP11 register value match again is indicated by the value after the change (L).

8.4.4 Control of number of carrier clocks by timer 51 counter

The number of carrier clocks to be output from the TOH1 pin can be controlled by selecting the timer H1 output signal for the 8-bit timer 51 count clock.

Figure 8-18 shows an example of control when three carrier clocks are to be output from the TOH1 pin

Figure 8-18. Example of Controlling Number of Carrier Clocks by Timer 51 Counter (Setting Timer H1 Output Signal for Timer 51 Count Clock (TCL51 = 07H))



<1> Set the CR51 register to 02H when three carrier clocks are to be output from the TOH1 pin.

<2> The INTTM51 signal is generated when the TM51 count value and the CR51 register value (02H) have matched. The signal is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

<3> The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.
The transfer timing at this time is one timer H1 count clock after a rise of the INTTM5H1 signal.

<4> By setting NRZ1 to 0, the TOH1 output becomes low level after having output the third carrier clock.

Remark INTTM5H1 is an internal signal and not an interrupt source.

CHAPTER 9 REAL-TIME COUNTER

<R> **Caution The real-time counter is only initialized by a reset triggered by the $\overline{\text{RESET}}$ pin. The counter is not initialized by internal resets triggered by the watchdog timer, power-on-clear (POC) circuit, or low-voltage detector (LVI).**

9.1 Functions of Real-Time Counter

The real-time counter is mounted onto all 78K0/Lx3-M microcontroller products.
The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz or 32.768 kHz

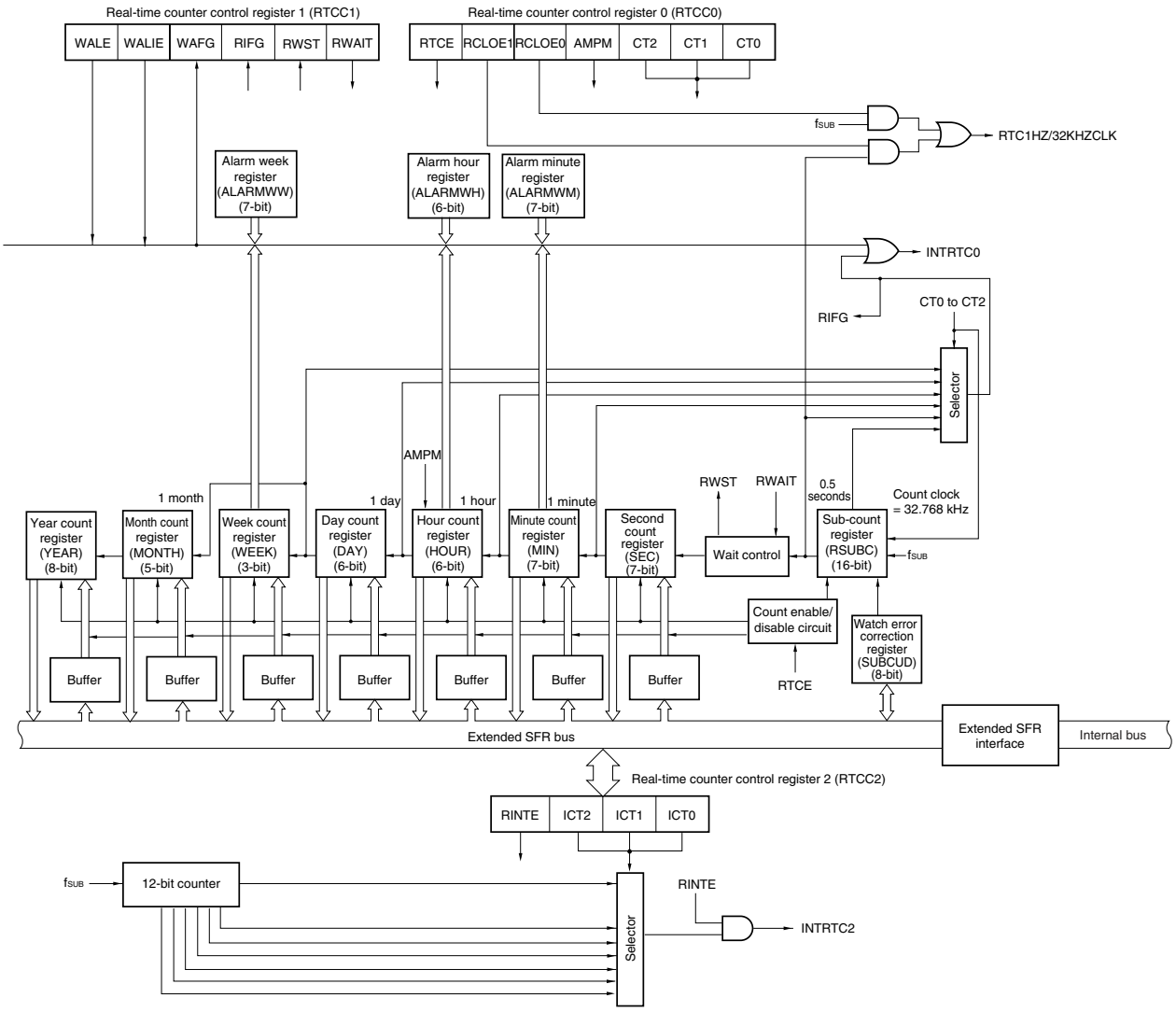
9.2 Configuration of Real-Time Counter

The real-time counter includes the following hardware.

Table 9-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter control register 0 (RTCC0) Real-time counter control register 1 (RTCC1) Real-time counter control register 2 (RTCC2) Real-time counter mode register (RTCMD) Pull-down status control register (PUTCTL) Sub-count register (RSUBC) Second count register (SEC) Minute count register (MIN) Hour count register (HOUR) Day count register (DAY) Week count register (WEEK) Month count register (MONTH) Year count register (YEAR) Watch error correction register (SUBCUD) Alarm minute register (ALARMWM) Alarm hour register (ALARMWH) Alarm week register (ALARMWW)

Figure 9-1. Block Diagram of Real-Time Counter



9.3 Registers Controlling Real-Time Counter

The real-time counter is controlled by the following registers.

These registers are all allocated to the extended SFR space.

For details about how to access the extended SFR space, see **CHAPTER 17 EXTENDED SFR INTERFACE**.

- Real-time counter control register 0 (RTCC0)
- Real-time counter control register 1 (RTCC1)
- Real-time counter control register 2 (RTCC2)
- Real-time counter mode register (RTCMD)
- Pull-down status control register (PUTCTL)
- Sub-count register (RSUBC)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)

(1) Real-time counter control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time counter operation, control the RTC1HZ and 32KHZCLK pins, and set a 12- or 24-hour system and the constant-period interrupt function.

RTCC0 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-2. Format of Real-Time Counter Control Register 0 (RTCC0)

Address: 96H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	2	1	0
RTCC0	RTCE	0	RCLOE1	RCLOE0	AMPM	CT2	CT1	CT0

RTCE	Real-time counter operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1[Note]	RTC1HZ pin output control
0	Disables output of RTC1HZ pin (1 Hz).
1	Enables output of RTC1HZ pin (1 Hz).

RCLOE0[Note]	32KHZCLK pin output control
0	Disables output of 32KHZCLK pin (32.768 kHz).
1	Enables output of 32KHZCLK pin (32.768 kHz).

AMPM	Selection of 12-/24-hour system
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
Rewrite the AMPM value after setting RWAIT (bit 0 of RTCC1) to 1. If the AMPM value is changed, the values of the hour count register (HOUR) change according to the specified time system. Table 9-2 shows the displayed time digits.	

CT2	CT1	CT0	Constant-period interrupt (INTRTC0) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of CT2 to CT0 while the counter operates (RTCE = 1), rewrite the values of CT2 to CT0 after disabling interrupt servicing INTRTC0 by using the interrupt mask flag register. Furthermore, after rewriting the values of CT2 to CT0, enable interrupt servicing after clearing the RIFG and RTC0IF flags.			

<R>

Note RCLOE0 and RCLOE1 must not be enabled at the same time.

Caution If RCLOE0 and RCLOE1 are changed when RTCE = 1, a last pulse with a narrow width may be generated on the 32.768 kHz and 1 Hz output signals.

Remark ×: don't care

(2) Real-time counter control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

RTCC1 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-3. Format of Real-Time Counter Control Register 1 (RTCC1) (1/2)

Address: 97H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC0 by using the interrupt mask flag register. Furthermore, clear the WAFG and RTC0IF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of RTCC1, the ALARMWM register, the ALARMWH register, and the ALARMWW register), set match operation to be invalid (“0”) for the WALE bit.	

<R>

WALIE	Control of alarm interrupt (INTRTC0) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1” one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time counter
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of RWAIT is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

Figure 9-3. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write "1" to it to read or write the counter value.
Because sub-count register (RSUBC) continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0.
When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written.
If RSUBC overflows when RWAIT = 1, it counts up after RWAIT = 0. If the second count register is written, however, it does not count up because RSUBC is cleared.

Caution The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting "1" to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC0). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC0 occurrence.

(3) Real-time counter control register 2 (RTCC2)

The RTCC2 register is an 8-bit register that is used to control the interval interrupt function.

RTCC2 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-4. Format of Real-Time Counter Control Register 2 (RTCC2)

Address: 92H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
RTCC2	RINTE	0	0	0	0	ICT2	ICT1	ICT0

RINTE	ICT2	ICT1	ICT0	Interval interrupt (INTRTC2) selection
0	×	×	×	Interval interrupt is not generated.
1	0	0	0	$2^6/f_{SUB}$ (1.953125 ms)
1	0	0	1	$2^7/f_{SUB}$ (3.90625 ms)
1	0	1	0	$2^8/f_{SUB}$ (7.8125 ms)
1	0	1	1	$2^9/f_{SUB}$ (15.625 ms)
1	1	0	0	$2^{10}/f_{SUB}$ (31.25 ms)
1	1	0	1	$2^{11}/f_{SUB}$ (62.5 ms)
1	1	1	×	$2^{12}/f_{SUB}$ (125 ms)

Caution Change ICT2, ICT1, and ICT0 when RINTE = 0.

(4) Real-time counter mode register (RTCMD)

The RTCMD register is an 8-bit register that is used to set an operation mode of the real-time counter.

RTCMD is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-5. Format of Real-time Counter Mode Register (RTCMD)

Address: CBH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RTCMD	RTCMD7	RTCMD6	RTCMD5	RTCMD4	RTCMD3	RTCMD2	RTCMD1	RTCMD0

RTCMD7 to RTCMD0	Setting of operation mode of real-time counter
01011001 (59H)	The real-time counter operates. The 24-bit ΔΣ-type A/D converter, power calculation circuit, power quality measurement circuit, and digital frequency conversion circuit stop.
Other than above	Normal operation mode

(5) Pull-down status control register (PUTCTL)

This 8-bit register is used to control the pull-down status of pins after release of reset.

PUTCTL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-6. Format of Pull-down Status Control Register (PUTCTL)

Address: 88H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PUTCTL	0	0	0	0	0	0	0	PDCUT

PDCUT	Control whether the pull-down resistor is connected
0	Connects the pull-down resistor.
1	Disconnects the pull-down resistor.

Caution The extended SFR interface is used to access the extended SFR space. After release of reset, until initializing the extended SFR interface finishes, perform pull-down control to prevent the extended SFR interface status from becoming undefined. After the extended SFR interface is initialized, specify 01H for PUTCTL and cancel the pull-down status to reduce current consumption.

(6) Sub-count register (RSUBC)

The RSUBC register is a 16-bit register that counts the reference time of 1 second of the real-time counter.

Usually, it takes a value of 0000H to 7FFFH and counts 1 second with a clock of 32.768 kHz.

RSUBC is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 0000H.

Cautions 1. When a correction is made by using the watch error correction register (SUBCUD), the value may become 8000H or more.

2. This register is also cleared by reset effected by writing the second count register.

3. The value read from this register is not guaranteed if it is read during operation, because a value that is changing is read.

Figure 9-7. Format of Sub-Count Register (RSUBC)

Address: 98H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSUBCL	SUBC7	SUBC6	SUBC5	SUBC4	SUBC3	SUBC2	SUBC1	SUBC0

Address: 99H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSUBCH	SUBC15	SUBC14	SUBC13	SUBC12	SUBC11	SUBC10	SUBC9	SUBC8

(7) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Set a decimal value of 00 to 59 to this register in BCD code.

SEC is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-8. Format of Second Count Register (SEC)

Address: 9AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEC	0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1

(8) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

MIN is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-9. Format of Minute Count Register (MIN)

Address: 9BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

(9) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12, 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time counter control register 0 (RTCC0).If the value of AMPM is changed, the values of the HOUR change according to the specified time system.

HOUR is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit is set to 1 after reset.

Figure 9-10. Format of Hour Count Register (HOUR)

Address: 9CH After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution Bit 5 (HOUR20) of HOUR indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

Table 9-2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

Table 9-2. Displayed Time Digits

24-Hour Display (AMPM bit = 1)		12-Hour Display (AMPM bit = 0)	
Time	HOUR Register	Time	HOUR Register
0	00H	0 a.m.	12H
1	01H	1 a.m.	01H
2	02H	2 a.m.	02H
3	03H	3 a.m.	03H
4	04H	4 a.m.	04H
5	05H	5 a.m.	05H
6	06H	6 a.m.	06H
7	07H	7 a.m.	07H
8	08H	8 a.m.	08H
9	09H	9 a.m.	09H
10	10H	10 a.m.	10H
11	11H	11 a.m.	11H
12	12H	0 p.m.	32H
13	13H	1 p.m.	21H
14	14H	2 p.m.	22H
15	15H	3 p.m.	23H
16	16H	4 p.m.	24H
17	17H	5 p.m.	25H
18	18H	6 p.m.	26H
19	19H	7 p.m.	27H
20	20H	8 p.m.	28H
21	21H	9 p.m.	29H
22	22H	10 p.m.	30H
23	23H	11 p.m.	31H

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.

In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.

(10) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.
It counts up when the hour counter overflows.
This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.
Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.
DAY is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 01H.

Figure 9-11. Format of Day Count Register (DAY)

Address: 9EH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
DAY	0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1

(11) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 06 to this register in BCD code.

WEEK is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-12. Format of Week Count Register (WEEK)

Address: 9DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WEEK	0	0	0	0	0	WEEK4	WEEK2	WEEK1

Caution The value corresponding to the month count register (MONTH) or the day count register (DAY) is not stored in the week count register (WEEK) automatically. After reset release, set the week count register as follow.

Day	WEEK
Sunday	00H
Monday	01H
Tuesday	02H
Wednesday	03H
Thursday	04H
Friday	05H
Saturday	06H

(12) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

MONTH is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 01H.

Figure 9-13. Format of Month Count Register (MONTH)

Address: 9FH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
MONTH	0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1

(13) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month counter overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the month count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

YEAR is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-14. Format of Year Count Register (YEAR)

Address: A0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
YEAR	YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1

(14) Watch error correction register (SUBCUD)

This register is used to correct the watch with high accuracy when it is slow or fast by changing the value (reference value: 7FFFH) that overflows from the sub-count register (RSUBC) to the second count register.

Rewrite the SUBCUD after disabling interrupt servicing INTRTC0 by using the interrupt mask flag register.

Furthermore, after rewriting the SUBCUD, enable interrupt servicing after clearing the interrupt request flags (RTC0IF) and the fixed-cycle interrupt status flags (RIFG). <R>

SUBCUD is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-15. Format of Watch Error Correction Register (SUBCUD)

Address: A1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SUBCUD	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch error when the second digits are at 00, 20, or 40 (every 20 seconds).
1	Corrects watch error only when the second digits are at 00 (every 60 seconds).
Writing to the SUBCUD register at the following timing is prohibited. • When DEV = 0 is set: For a period of SEC = 00H, 20H, 40H • When DEV = 1 is set: For a period of SEC = 00H	

F6	Setting of watch error correction value
0	Increases by {(F5, F4, F3, F2, F1, F0) – 1} × 2.
1	Decreases by {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2.
When (F6, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *), the watch error is not corrected. * is 0 or 1. /F5 to /F0 are the inverted values of the corresponding bits (000011 when 111100). Range of correction value: (when F6 = 0) 2, 4, 6, 8, … , 120, 122, 124 (when F6 = 1) –2, –4, –6, –8, … , –120, –122, –124	

The range of value that can be corrected by using the watch error correction register (SUBCUD) is shown below.

	DEV = 0 (correction every 20 seconds)	DEV = 1 (correction every 60 seconds)
Correctable range	–189.2 ppm to 189.2 ppm	–63.1 ppm to 63.1 ppm
Maximum excludes quantization error	± 1.53 ppm	± 0.51 ppm
Minimum resolution	± 3.05 ppm	± 1.02 ppm

Remark Set DEV to 0 when the correction range is –63.1 ppm or less, or 63.1 ppm or more.

(15) Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

ALARMWM is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Caution Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 9-16. Format of Alarm Minute Register (ALARMWM)

Address: 93H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWM	0	WM40	WM20	WM10	WM8	WM4	WM2	WM1

(16) Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

ALARMWH is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit is set to 1 after reset.

Caution Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 9-17. Format of Alarm Hour Register (ALARMWH)

Address: 94H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWH	0	0	WH20	WH10	WH8	WH4	WH2	WH1

Caution Bit 5 (WH20) of ALARMWH indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

(17) Alarm week register (ALARMWW)

This register is used to set date of alarm.

ALARMWW is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 9-18. Format of Alarm Week Register (ALARMWW)

Address: 95H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWW	0	WW6	WW5	WW4	WW3	WW2	WW1	WW0

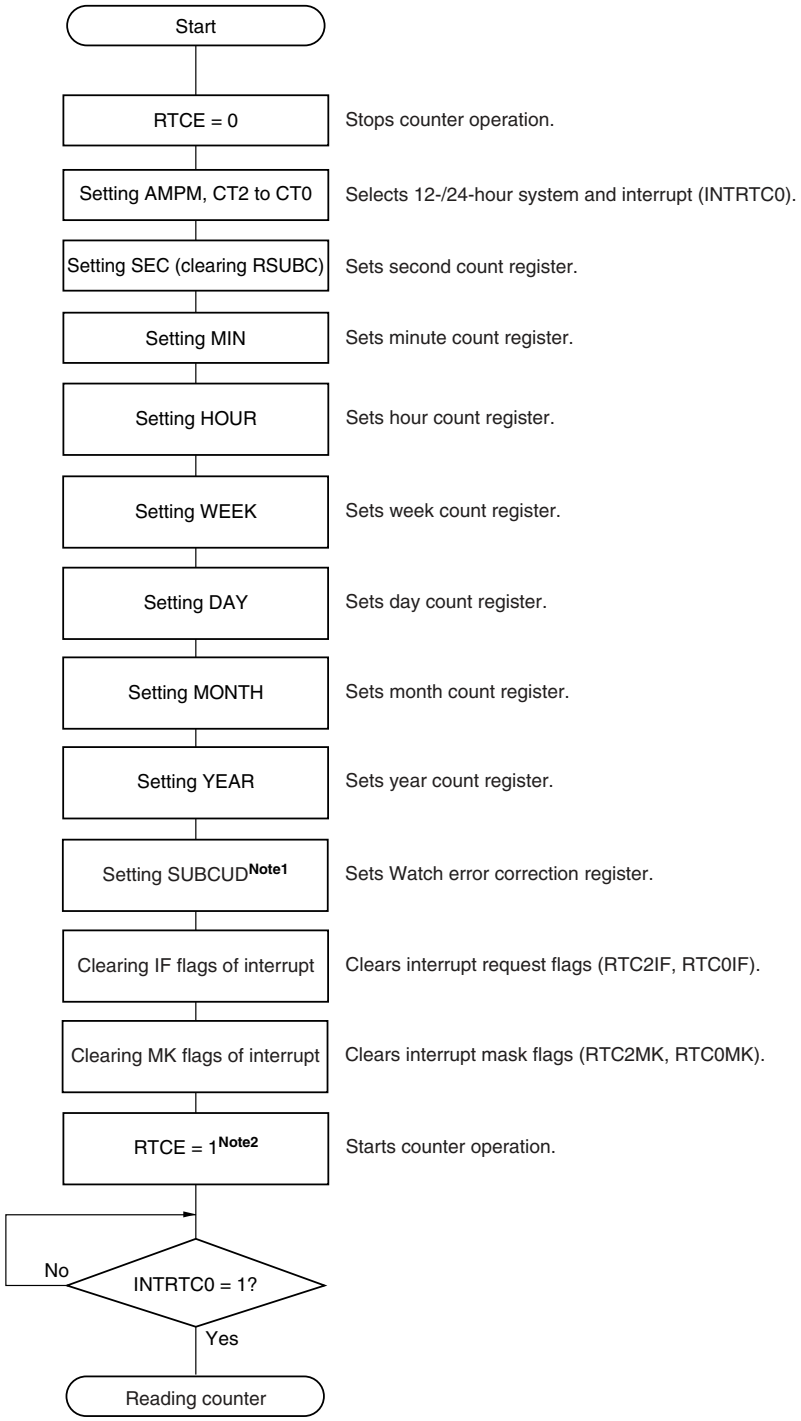
Here is an example of setting the alarm.

Time of Alarm	Day							12-Hour Display				24-Hour Display			
	Sunday WW0	Monday WW1	Tuesday WW2	Wednesday WW3	Thursday WW4	Friday WW5	Saturday WW6	Hour 10	Hour 1	Minute 10	Minute 1	Hour 10	Hour 1	Minute 10	Minute 1
Every day, 0:00 a.m.	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
Every day, 1:30 a.m.	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
Every day, 11:59 a.m.	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
Monday through Friday, 0:00 p.m.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
Sunday, 1:30 p.m.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
Monday, Wednesday, Friday, 11:59 p.m.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

9.4 Real-Time Counter Operation

9.4.1 Starting operation of real-time counter

Figure 9-19. Procedure for Starting Operation of Real-Time Counter



Notes 1. Set up SUBCUD only if the watch error must be corrected. For details about how to calculate the correction value, see **9.4.7 Example of watch error correction of real-time counter.**

2. Confirm the procedure described in **9.4.2 Shifting to STOP mode after starting operation** when shifting to STOP mode without waiting for INTRTC0 = 1 after RTCE = 1.

9.4.2 Shifting to STOP mode after starting operation

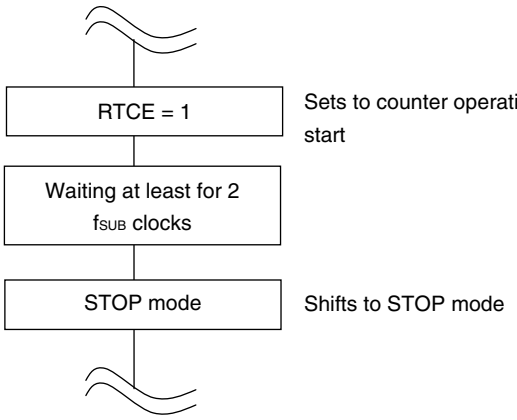
Perform one of the following processing when shifting to STOP mode immediately after setting RTCE to 1.

However, after setting RTCE to 1, this processing is not required when shifting to STOP mode after the first INTRTC0 interrupt has occurred.

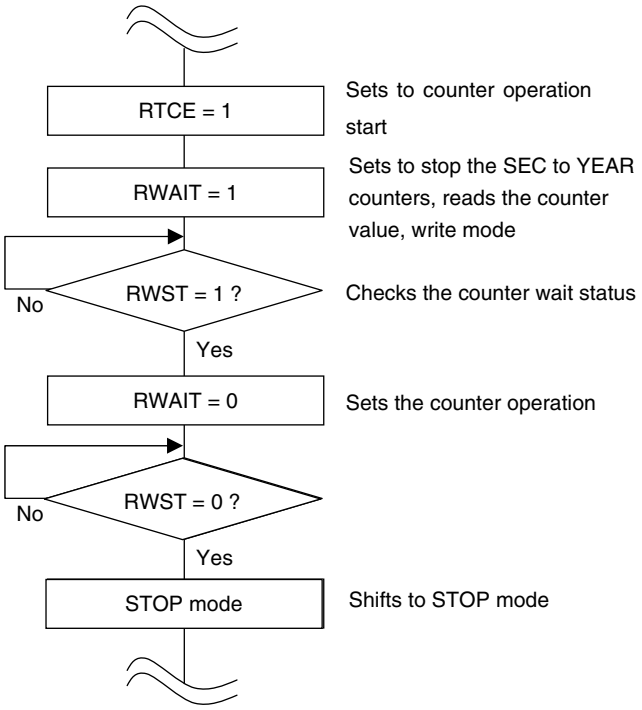
- Shifting to STOP mode when at least two input clocks (f_{SUB}) have elapsed after setting RTCE to 1 (see **Figure 9-20**, **Example 1**).
- Checking by polling RWST to become 1, after setting RTCE to 1 and then setting RWAIT to 1. Afterward, setting RWAIT to 0 and shifting to STOP mode after checking again by polling that RWST has become 0 (see **Figure 9-20**, **Example 2**).

Figure 9-20. Procedure for Shifting to STOP Mode After Setting RTCE to 1

Example 1



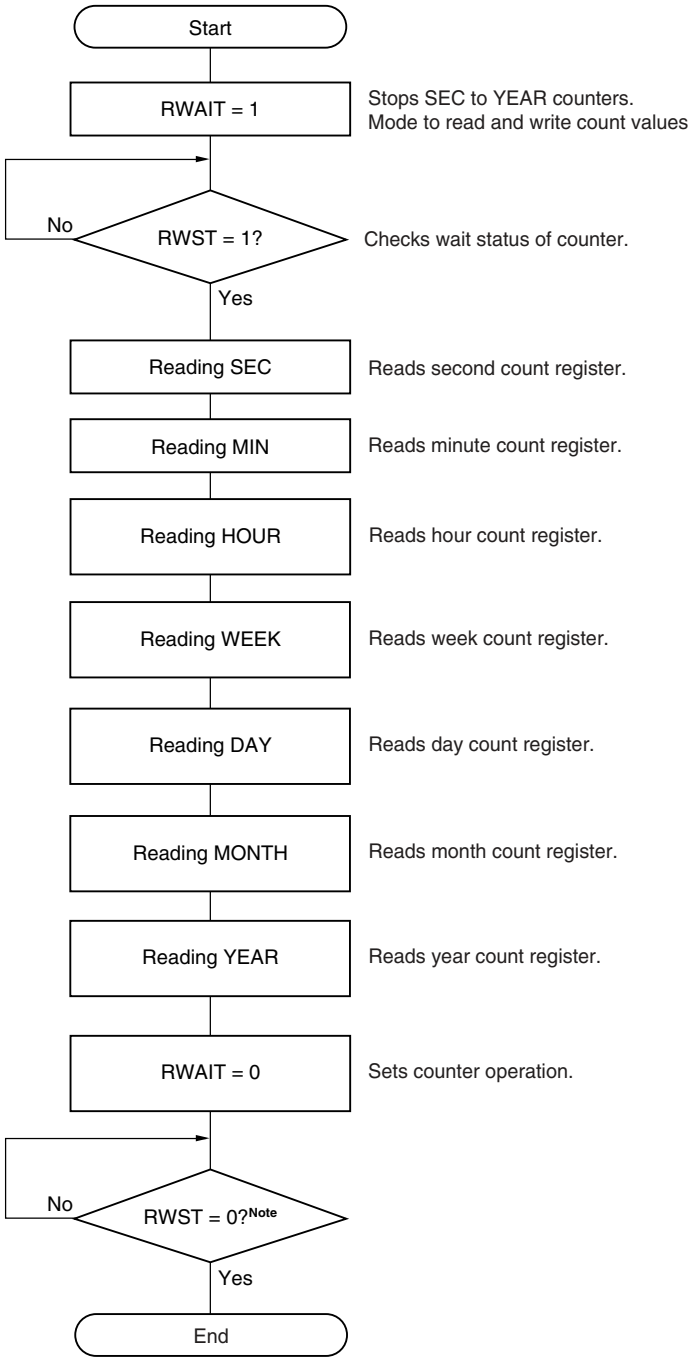
Example 2



9.4.3 Reading/writing real-time counter

Read or write the counter after setting 1 to RWAIT first.

Figure 9-21. Procedure for Reading Real-Time Counter

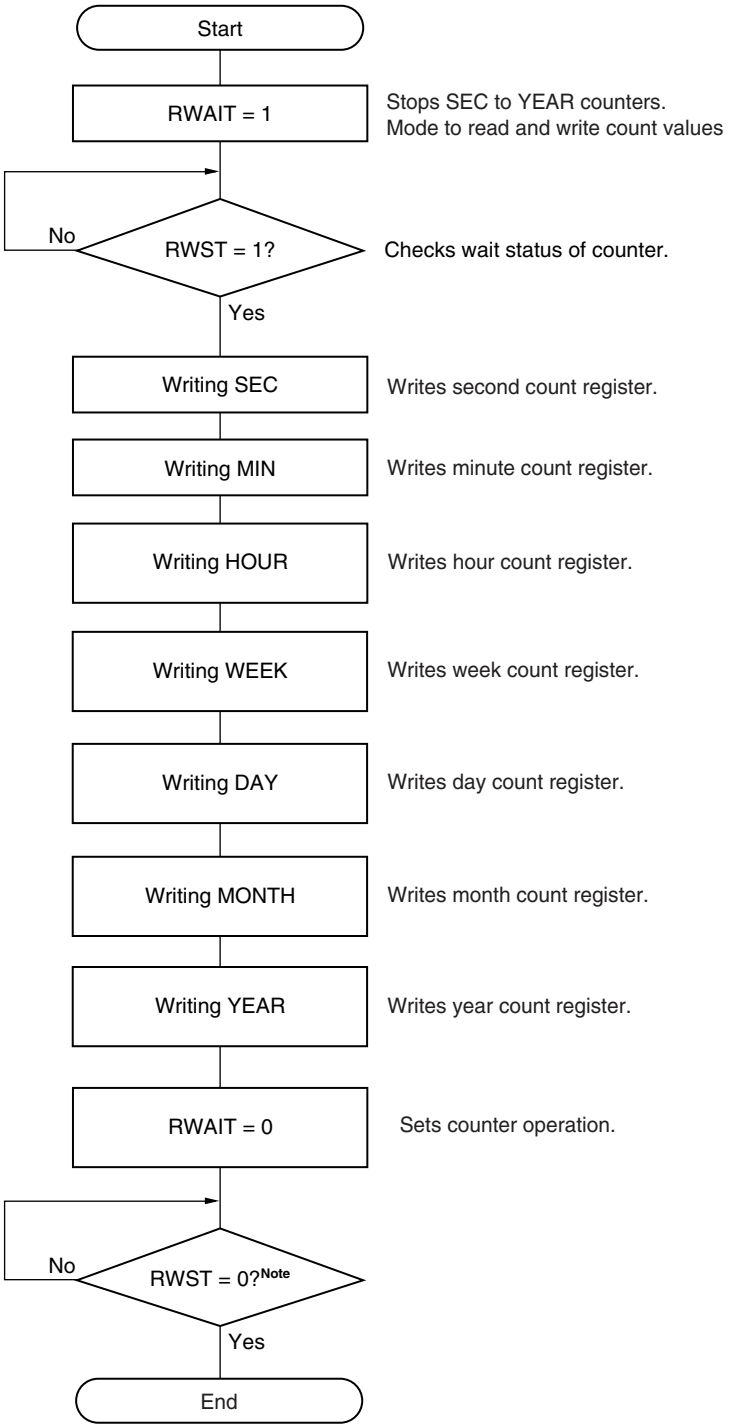


Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations of setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence.
All the registers do not have to be set and only some registers may be read.

Figure 9-22. Procedure for Writing Real-Time Counter



Note Be sure to confirm that RWST = 0 before setting STOP mode.

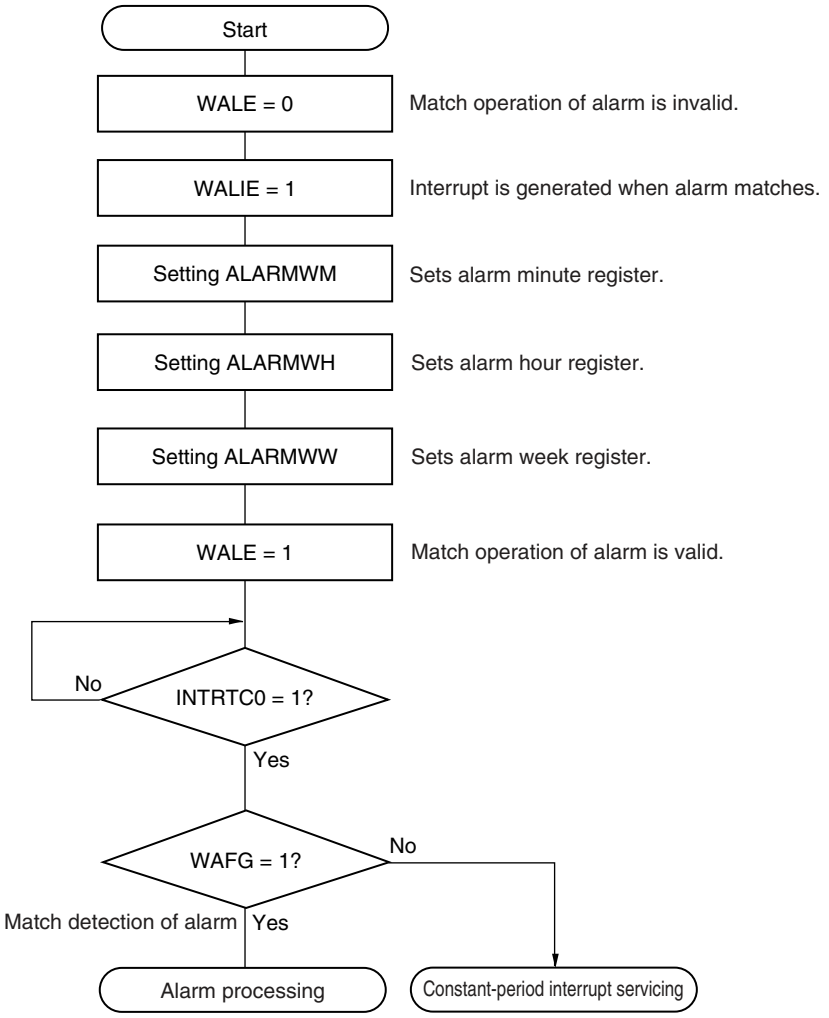
Caution Complete the series of operations of setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be written in any sequence.
All the registers do not have to be set and only some registers may be written.

9.4.4 Setting alarm of real-time counter

Set time of alarm after setting 0 to WALE first.

Figure 9-23. Alarm Setting Procedure

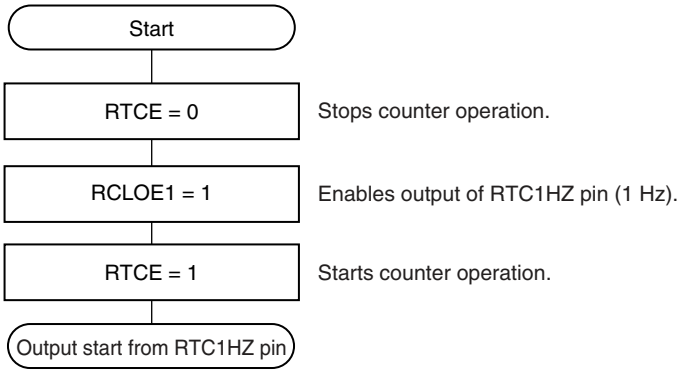


Remarks 1. ALARMWM, ALARMWH, and ALARMWW may be written in any sequence.

2. Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC0). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC0 occurrence.

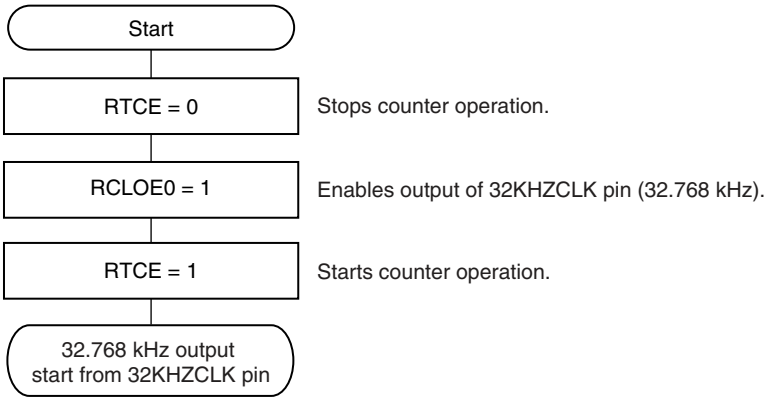
9.4.5 1 Hz output of real-time counter

Figure 9-24. 1 Hz Output Setting Procedure



9.4.6 32.768 kHz output of real-time counter

Figure 9-25. 32.768 kHz Output Setting Procedure



9.4.7 Example of watch error correction of real-time counter

The watch can be corrected with high accuracy when it is slow or fast, by setting a value to the watch error correction register.

Example of calculating the correction value

The correction value used when correcting the count value of the sub-count register (RSUBC) is calculated by using the following expression.

Set DEV to 0 when the correction range is –63.1 ppm or less, or 63.1 ppm or more.

(When DEV = 0)

Correction value[Note] = Number of correction counts in 1 minute ÷ 3 = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60 ÷ 3

(When DEV = 1)

Correction value[Note] = Number of correction counts in 1 minute = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60

Note The correction value is the watch error correction value calculated by using bits 6 to 0 of the watch error correction register (SUBCUD).

(When F6 = 0) Correction value = {(F5, F4, F3, F2, F1, F0) – 1} × 2

(When F6 = 1) Correction value = – {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2

When (F6, F5, F4, F3, F2, F1, F0) is (*, 0, 0, 0, 0, 0, *), watch error correction is not performed. "*" is 0 or 1. /F5 to /F0 are bit-inverted values (000011 when 111100).

Remarks 1. The correction value is 2, 4, 6, 8, … 120, 122, 124 or –2, –4, –6, –8, … –120, –122, –124.

2. The oscillation frequency is the input clock (f_{SUB}) value of the real-time counter (RTC).
It can be calculated from the 32 kHz output frequency of the 32KHZCLK pin or the output frequency of the RTC1HZ pin × 32768 when the watch error correction register is set to its initial value (00H).

3. The target frequency is the frequency resulting after correction performed by using the watch error correction register.

Correction example <1>

Example of correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32 kHz from the 32KHZCLK pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register is set to its initial value (00H).

Note See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the 32KHZCLK pin.

[Calculating the correction value]

(When the output frequency from the 32KHZCLK pin is 32772.3 Hz)

If the target frequency is assumed to be 32768 Hz (32772.3 Hz – 131.2 ppm), the correction range for –131.2 ppm is –63.1 ppm or less, so assume DEV to be 0.

The expression for calculating the correction value when DEV is 0 is applied.

Correction value = Number of correction counts in 1 minute ÷ 3
= (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60 ÷ 3
= (32772.3 ÷ 32768 – 1) × 32768 × 60 ÷ 3
= 86

[Calculating the values to be set to (F6 to F0)]

(When the correction value is 86)

If the correction value is 0 or more (when delaying), assume F6 to be 0.

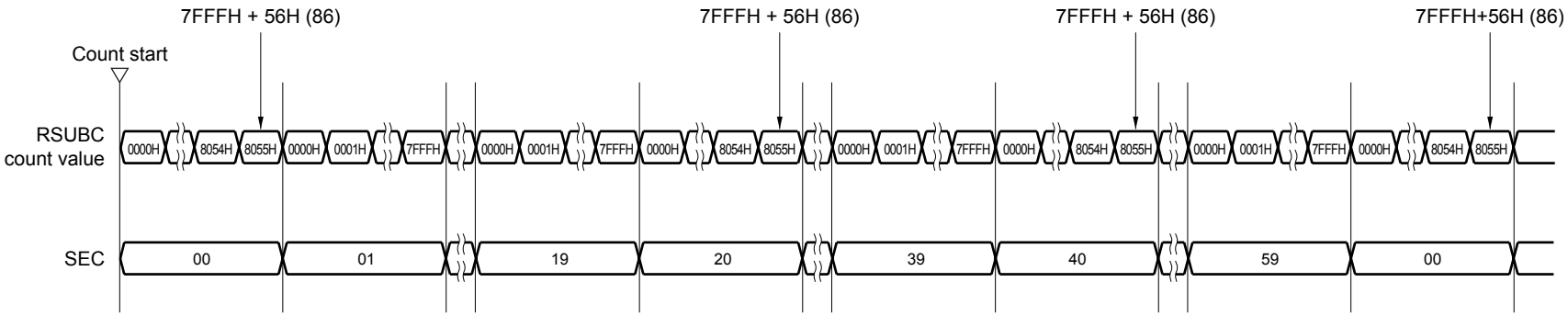
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

{ (F5, F4, F3, F2, F1, F0) – 1} × 2 = 86
(F5, F4, F3, F2, F1, F0) = 44
(F5, F4, F3, F2, F1, F0) = (1, 0, 1, 1, 0, 0)

Consequently, when correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm), setting the correction register such that DEV is 0 and the correction value is 86 (bits 6 to 0 of SUBCUD: 0101100) results in 32768 Hz (0 ppm).

Figure 9-26 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (0, 0, 1, 0, 1, 1, 0, 0).

Figure 9-26. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 1, 0, 1, 1, 0, 0)



Correction example <2>

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32 kHz from the 32KHZCLK pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register is set to its initial value (00H).

Note See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the 32KHZCLK pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

Correction value = Number of correction counts in 1 minute
= (Oscillation frequency ÷ Target frequency − 1) × 32768 × 60
= (32767.4 ÷ 32768 − 1) × 32768 × 60
= −36

[Calculating the values to be set to (F6 to F0)]

(When the correction value is −36)

If the correction value is 0 or less (when speeding up), assume F6 to be 1.

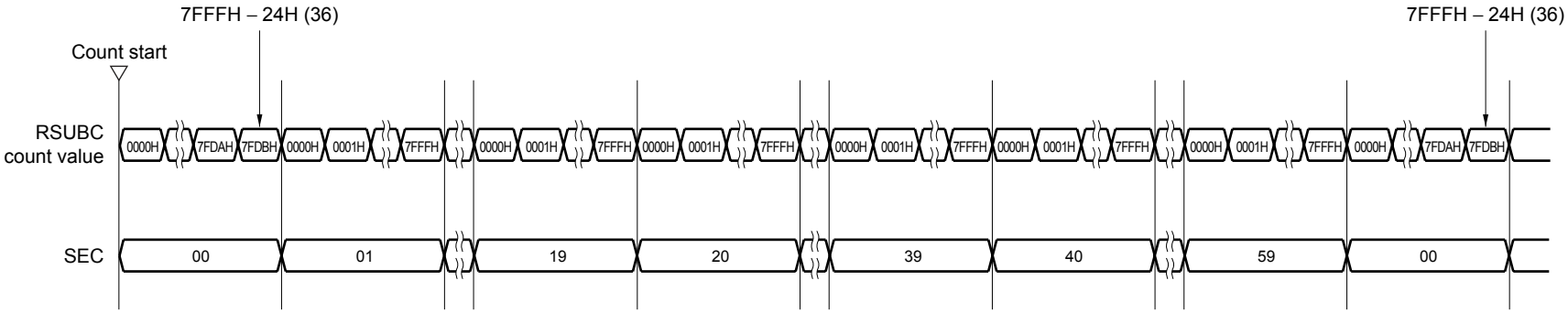
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

− {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2	= −36
(/F5, /F4, /F3, /F2, /F1, /F0)	= 17
(/F5, /F4, /F3, /F2, /F1, /F0)	= (0, 1, 0, 0, 0, 1)
(F5, F4, F3, F2, F1, F0)	= (1, 0, 1, 1, 1, 0)

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is −36 (bits 6 to 0 of SUBCUD: 1101110) results in 32768 Hz (0 ppm).

Figure 9-27 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

Figure 9-27. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)



9.5 RTC Temperature Correction Circuit Function

This function is used to correct the RTC frequency based on the result of temperature measurement using temperature sensors.

During temperature measurement, the temperature at the time of measurement is calculated by using the linearity of the ratio of a temperature-dependent sensor and a temperature-independent sensor. For two points in the reference temperature environment, the values detected by the temperature sensors are measured, and then the slope and offset between the two reference points are calculated in advance. In the actual usage environment, the measured temperature sensor detection values and the calculated slope and offset are used to calculate the temperature.

The calculation method is as follows:

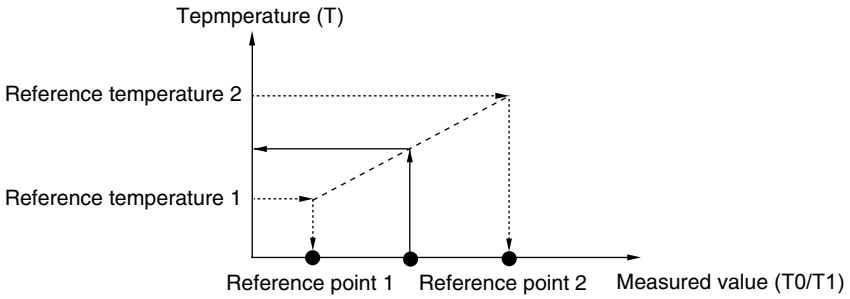
Tnow = (value detected by the temperature sensors – offset)/slope + Tbase
Value detected by the temperature sensors = T0/T1 x 256

T0: Measured value of the temperature-dependent sensor
T1: Measured value of the temperature-independent sensor
Tnow: Temperature during measurement
Tbase: Temperature in the reference environment

Remark The offset and slope are calculated using the measured values of two points in the reference temperature environment.

Caution Do not use these temperature sensors for purposes other than RTC correction. If this function is used, ANI0 and ANI1 cannot be used (100-pin products).

Figure 9-28. Calculation of Measured Temperature Values



RTC correction is performed by calculating the correction value using the temperature measurement results. For the oscillation frequency, RTC correction can correct the frequency error in the range from –189 to +189 ppm.

During RTC correction, the crystal frequency is corrected by using the clock error correction register (SUBCUD). The frequency error can be corrected in the range from –189 to +189 ppm. This digital correction is performed by adding or subtracting pulses from the crystal clock signal. The resolution of the error correction register is ±1.5 ppm/LSB (or ±0.5 ppm/LSB in accordance with the DEV setting of SUBCUD). In other words, the resolution is ±0.13 seconds/day (or ±0.044 seconds/day).

During temperature correction, the previous temperature measurement results are used to calculate the correction value, and then the clock is corrected by specifying the value for SUBCUD.

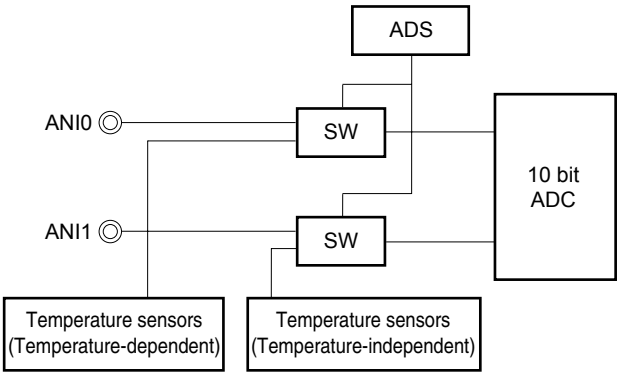
9.5.1 Configuration of RTC temperature correction circuit

Temperature correction is performed by setting the voltage selection flag (ADISS) used for temperature correction to the successive A/D converter. The A/D conversion channel is selected using the ADS register, which is in the successive A/D converter.

For details about selecting the successive A/D conversion channel by using the ADS register, see **CHAPTER 12 10-BIT SUCCESSIVE COMPARISON A/D CONVERTER**.

Caution If the ADISS flag is set to 1, the first conversion result is invalid, so use the second and subsequent conversion results.

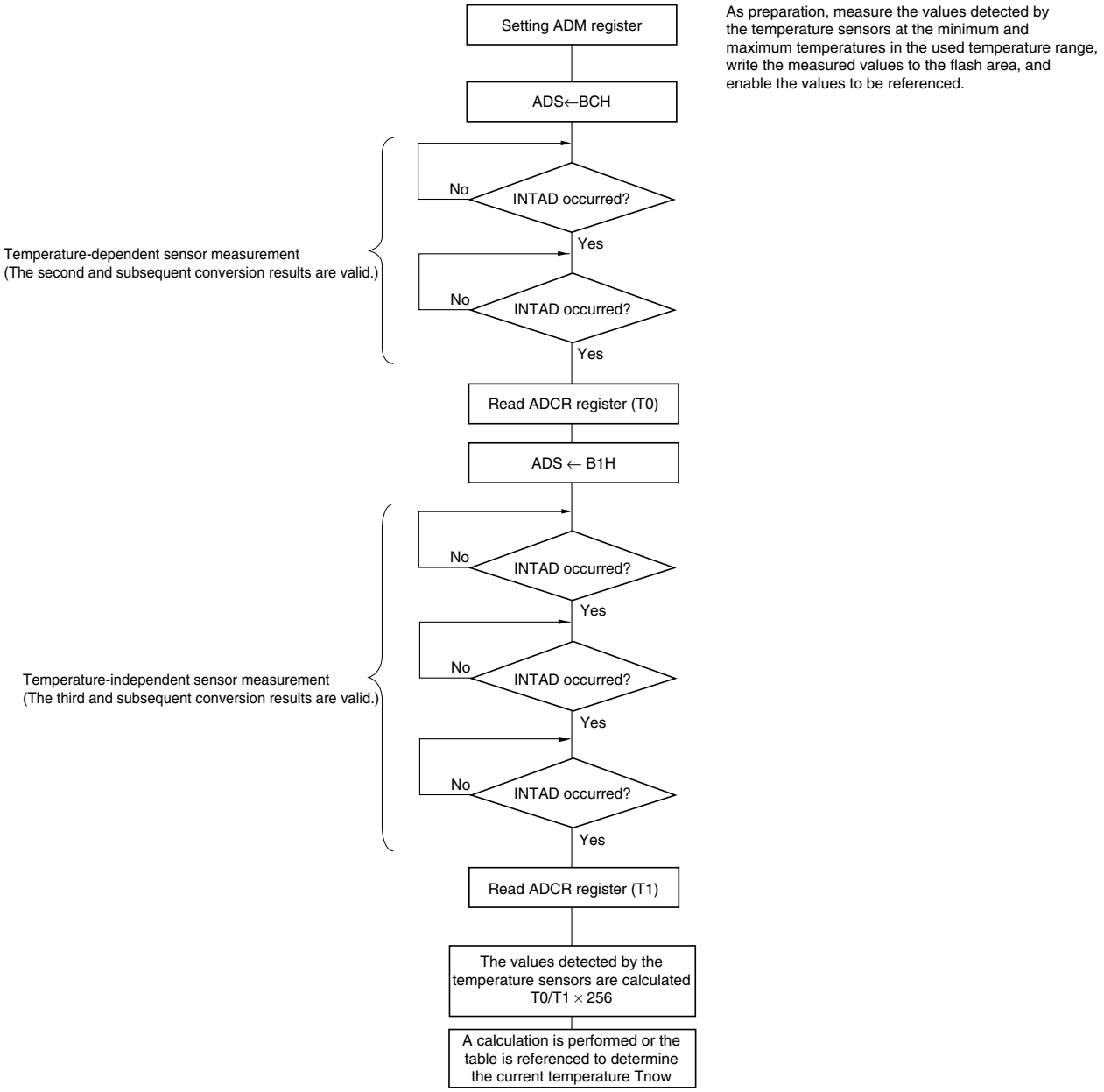
Figure 9-29. Block Diagram of RTC Temperature Correction Circuit



9.5.2 Using RTC temperature correction circuit

(1) Procedure for using the temperature sensors

Figure 9-31. Procedure for Using the Temperature Sensors



(2) RTC correction procedure

The following describes the calculation method.

The maximum and minimum correction sub-counts are 8000H + 7 ch and 8000H – 7 ch, respectively (SUBCUD is set to 3FH or 42H).

Assuming correction is performed three times per minute (at 00 seconds, 20 seconds, and 40 seconds), the total sub-count ranges during one minute of correction are as follows:

Maximum: (8000H x 60) + (7 ch x 3) = 1,966,452 [counts]

Minimum: (8000H x 60) – (7 ch x 3) = 1,965,708 [counts]

Therefore, the average sub-count ranges per second of correction are as follows:

Maximum: (8000H) + (7 ch/20) = 32,774.2 [counts]

Minimum: (8000H) – (7 ch/20) = 32,761.8 [counts]

Based on the above, the frequency ranges for which correction is valid are as follows:

Maximum frequency: 32.7742 kHz (SUBCUD = 3FH)

Minimum frequency: 32.7618 kHz (SUBCUD = 42H)

9.5.3 Notes on temperature correction circuit

(1) If the ADISS flag is set to 1, the first conversion result is invalid, so use the second and subsequent conversion results.

(2) The temperature sensors cannot be used while the internal high-speed oscillator regulator is stopped. In other words, turn on the internal oscillator before using the temperature sensors, and wait 2 μs before starting measurement.

(3) The temperature sensors can only be used during normal operation. During a power outage or when power is being supplied by batteries, the temperature sensors are not used because RTC correction is not performed.

CHAPTER 10 WATCHDOG TIMER

10.1 Functions of Watchdog Timer

The watchdog timer is mounted onto all 78K0/Lx3-M microcontroller products.

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to WDTE
- If data is written to WDTE during a window close period
- If the instruction is fetched from an area not set by the IMS and IXS registers[Note] (detection of an invalid check while the CPU hangs up)
- If the CPU accesses an area that is not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

Note A product that does not have an internal expansion RAM is not provided with the IXS register.

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

10.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 10-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

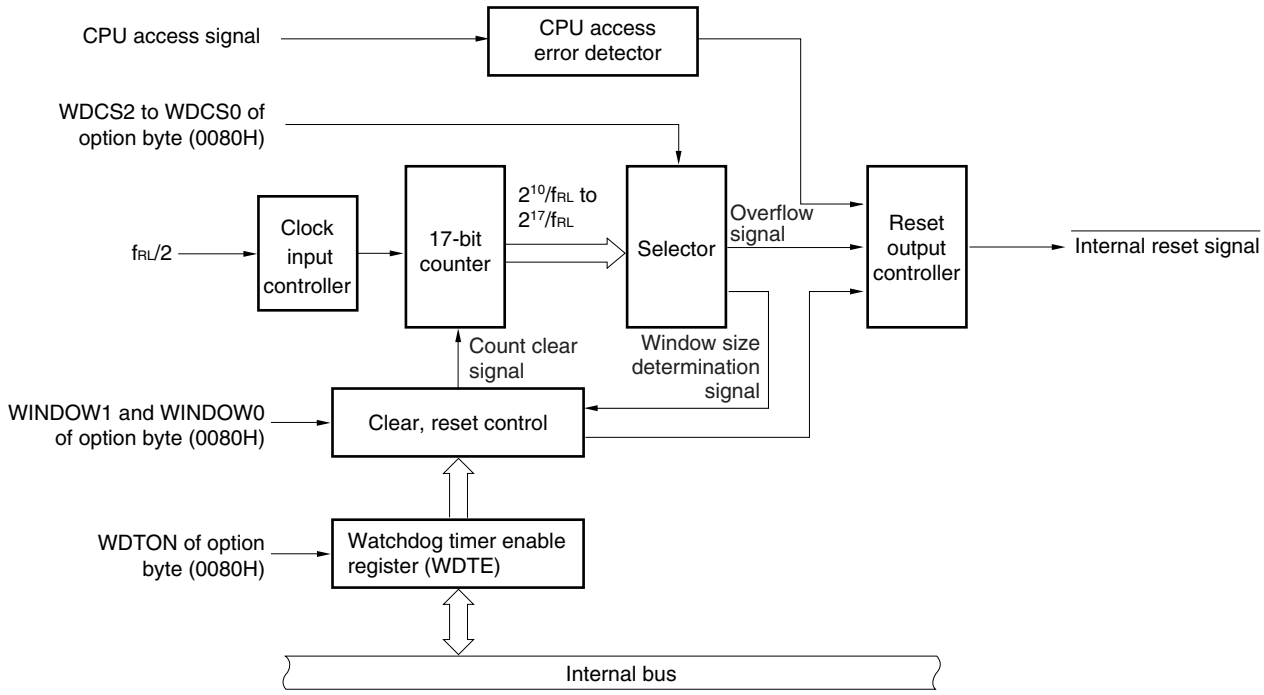
How the counter operation is controlled, overflow time, and window open period are set by the option byte.

Table 10-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (0080H)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)

Remark For the option byte, see **CHAPTER 29 OPTION BYTE**.

Figure 10-1. Block Diagram of Watchdog Timer



10.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 10-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FF99H After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE reset value differs depending on the WDTON setting value of the option byte (0080H). To operate watchdog timer, set WDTON to 1.

WDTON Setting Value	WDTE Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

3. The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).

10.4 Operation of Watchdog Timer

10.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (0080H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (0080H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 29**).

WDTON	Operation Control of Watchdog Timer Counter/Illegal Access Detection
0	Counter operation disabled (counting stopped after reset release), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset release), illegal access detection operation enabled

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H) (for details, see **10.4.2** and **CHAPTER 29**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (0080H) (for details, see **10.4.3** and **CHAPTER 29**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to WDTE after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write WDTE the second time or later after a reset release during the window open period. If WDTE is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to WDTE, an internal reset signal is generated.
   A internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
   - If data other than “ACH” is written to WDTE
   - If the instruction is fetched from an area not set by the IMS and IXS registers[Note] (detection of an invalid check during a CPU program loop)
   - If the CPU accesses an area not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

Note A product that does not have an internal expansion RAM is not provided with the IXS register.

Cautions 1. The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{RL} seconds.

3. The watchdog timer can be cleared immediately before the count value overflows (FFFFH).

Cautions 4. The operation of the watchdog timer in the HALT and STOP modes differs as follows depending on the set value of bit 0 (LSROSC) of the option byte.

	LSROSC = 0 (Internal Low-Speed Oscillator Can Be Stopped by Software)	LSROSC = 1 (Internal Low-Speed Oscillator Cannot Be Stopped)
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		

If LSROSC = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is not cleared to 0 but starts counting from the value at which it was stopped.

If oscillation of the internal low-speed oscillator is stopped by setting LSRSTOP (bit 1 of the internal oscillation mode register (RCM) = 1) when LSROSC = 0, the watchdog timer stops operating. At this time, the counter is not cleared to 0.

5. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

10.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to WDTE during the window open period before the overflow time.

The following overflow time is set.

Table 10-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer
0	0	0	$2^{10}/f_{RL}$ (3.88 ms)
0	0	1	$2^{11}/f_{RL}$ (7.76 ms)
0	1	0	$2^{12}/f_{RL}$ (15.52 ms)
0	1	1	$2^{13}/f_{RL}$ (31.03 ms)
1	0	0	$2^{14}/f_{RL}$ (62.06 ms)
1	0	1	$2^{15}/f_{RL}$ (124.12 ms)
1	1	0	$2^{16}/f_{RL}$ (248.24 ms)
1	1	1	$2^{17}/f_{RL}$ (496.48 ms)

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remarks 1. f_{RL}: Internal low-speed oscillation clock frequency

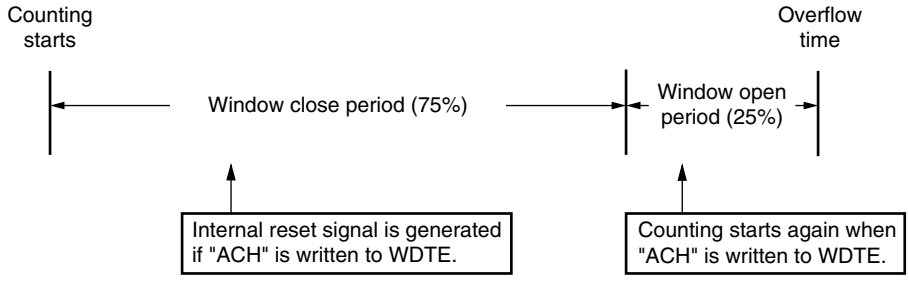
2. ( ): f_{RL} = 264 kHz (MAX.)

10.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (0080H). The outline of the window is as follows.

- If “ACH” is written to WDTE during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to WDTE during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 25%



Caution The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

The window open period to be set is as follows.

Table 10-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	25%
0	1	50%
1	0	75%
1	1	100%

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. Setting WINDOW1 = WINDOW0 = 0 is prohibited when using the watchdog timer at 1.8 V ≤ V_{DD} < 2.6 V.

3. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remark If the overflow time is set to $2^{11}/f_{RL}$, the window close time and open time are as follows.

(2.6 V ≤ V_{DD} ≤ 3.6 V)

	Setting of Window Open Period			
	25%	50%	75%	100%
Window close time	0 to 7.11 ms	0 to 4.74 ms	0 to 2.37 ms	None
Window open time	7.11 to 7.76 ms	4.74 to 7.76 ms	2.37 to 7.76 ms	0 to 7.76 ms

<When window open period is 25%>

- Overflow time:
  $2^{11}/f_{RL}$ (MAX.) = 2^{11}/264 kHz (MAX.) = 7.76 ms
- Window close time:
  0 to $2^{11}/f_{RL}$ (MIN.) × (1 − 0.25) = 0 to 2^{11}/216 kHz (MIN.) × 0.75 = 0 to 7.11 ms
- Window open time:
  $2^{11}/f_{RL}$ (MIN.) × (1 − 0.25) to $2^{11}/f_{RL}$ (MAX.) = 2^{11}/216 kHz (MIN.) × 0.75 to 2^{11}/264 kHz (MAX.) = 7.11 to 7.76 ms

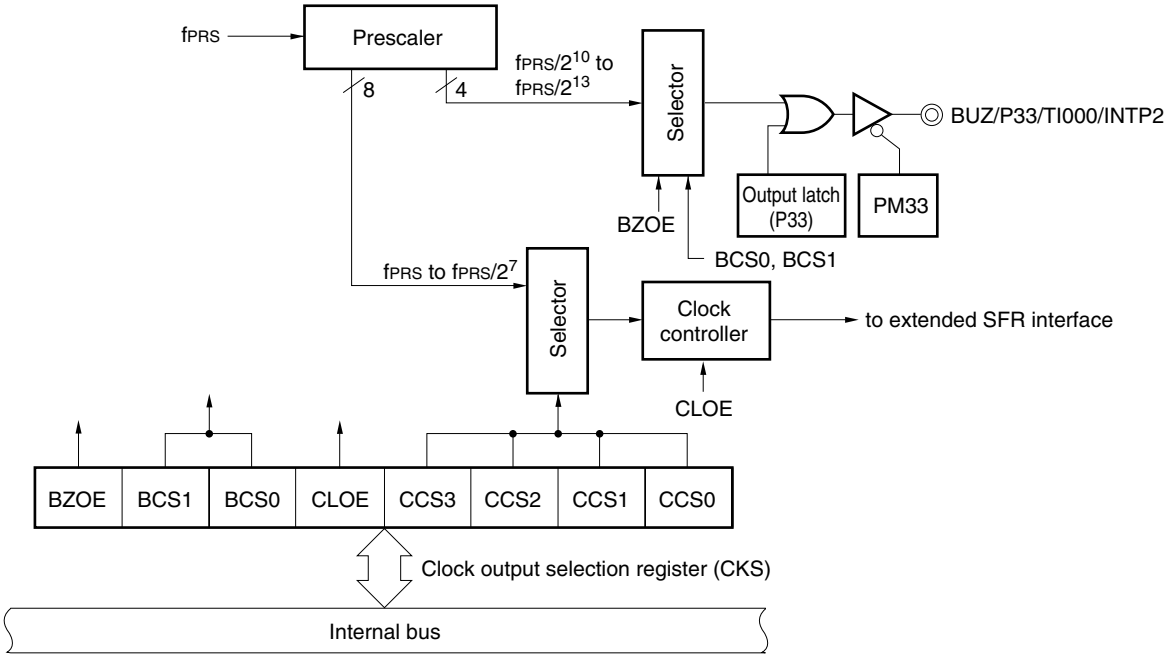
CHAPTER 11 BUZZER OUTPUT CONTROLLER

11.1 Functions of Buzzer Output Controller

The buzzer output is intended for square-wave output of buzzer frequency selected with clock output selection register (CKS).

Figure 11-1 shows the block diagram of buzzer output controller.

Figure 11-1. Block Diagram of Clock Output/Buzzer Output Controller



11.2 Configuration of Buzzer Output Controller

The buzzer output controller includes the following hardware.

Table 11-1. Configuration of Buzzer Output Controller

Item	Configuration
Control registers	Clock output selection register (CKS) Port mode register 3 (PM3) Port register 3 (P3)

11.3 Registers Controlling Buzzer Output Controller

The following two registers are used to control the buzzer output controller.

- Clock output selection register (CKS)
- Port mode register 3 (PM3)

(1) Clock output selection register (CKS)

This register sets output enable/disable for the buzzer frequency output (BUZ), and sets clock supply enable/disable to the extended SFR.

CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

Figure 11-2. Format of Clock Output Selection Register (CKS)

Address: FF40H After reset: 00H R/W

Symbol	<7>	6	5	<4>	3	2	1	0
CKS	BZOE	BCS1	BCS0	CLOE	CCS3	CCS2	CCS1	CCS0

BZOE	BUZ output enable/disable specification
0	Clock division circuit operation stopped. BUZ fixed to low level.
1	Clock division circuit operation enabled. BUZ output enabled.

BCS1	BCS0	BUZ output clock selection		
			f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	$f_{PRS}/2^{10}$	4.88 kHz	9.77 kHz
0	1	$f_{PRS}/2^{11}$	2.44 kHz	4.88 kHz
1	0	$f_{PRS}/2^{12}$	1.22 kHz	2.44 kHz
1	1	$f_{PRS}/2^{13}$	0.61 kHz	1.22 kHz

CLOE	Clock supply enable/disable specification to extended SFR
0	Disables clock supplying to extended SFR
1	Enables clock supplying to extended SFR

CCS3	CCS2	CCS1	CCS0	Selection of clock supplied to extended SFR[Note 1]		
					f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}[Note 2]	5 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$	2.5 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$	1.25 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$	625 kHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$	312.5 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$	156.25 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$	78.125 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$	39.062 kHz	78.125 kHz
Other than above				Setting prohibited		

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CCS3 = CCS2 = CCS1 = CCS0 = 0 (clock: f_{PRS}) is prohibited.

Cautions 1. Set BCS1 and BCS0 when the buzzer output operation is stopped (BZOE = 0).

2. Set CCS3 to CCS0 while the clock supply operation is stopped (CLOE = 0).

3. To use the 24-bit ΔΣ-type A/D converter, supply 10 MHz to the extended SFR.

4. Specify settings so that the clock frequency supplied to extended SFRs is at least 4 times the transfer clock frequency of the extended SFR interface.

Remark f_{PRS}: Peripheral hardware clock frequency

(2) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P33/BUZ/TI000/INTP2 pin for buzzer output, clear PM33 and the output latches of P33 to 0.

PM3 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 11-3. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

11.4 Operations of Buzzer Output Controller

The buzzer clock is output as the following procedure.

<1> Select the clock output frequency with bits 5 and 6 (BCS0 and BCS1) of the clock output selection register (CKS) (buzzer output in disabled status).

<2> Set bit 7 (CLOE) of CKS to 1 to enable clock output.

CHAPTER 12 10-BIT SUCCESSIVE APPROXIMATION TYPE A/D CONVERTER

	78K0/LE3-M	78K0/LG3-M
10-bit successive approximation type A/D converter	1 ch	8 ch

12.1 Function of 10-Bit Successive Approximation Type A/D Converter

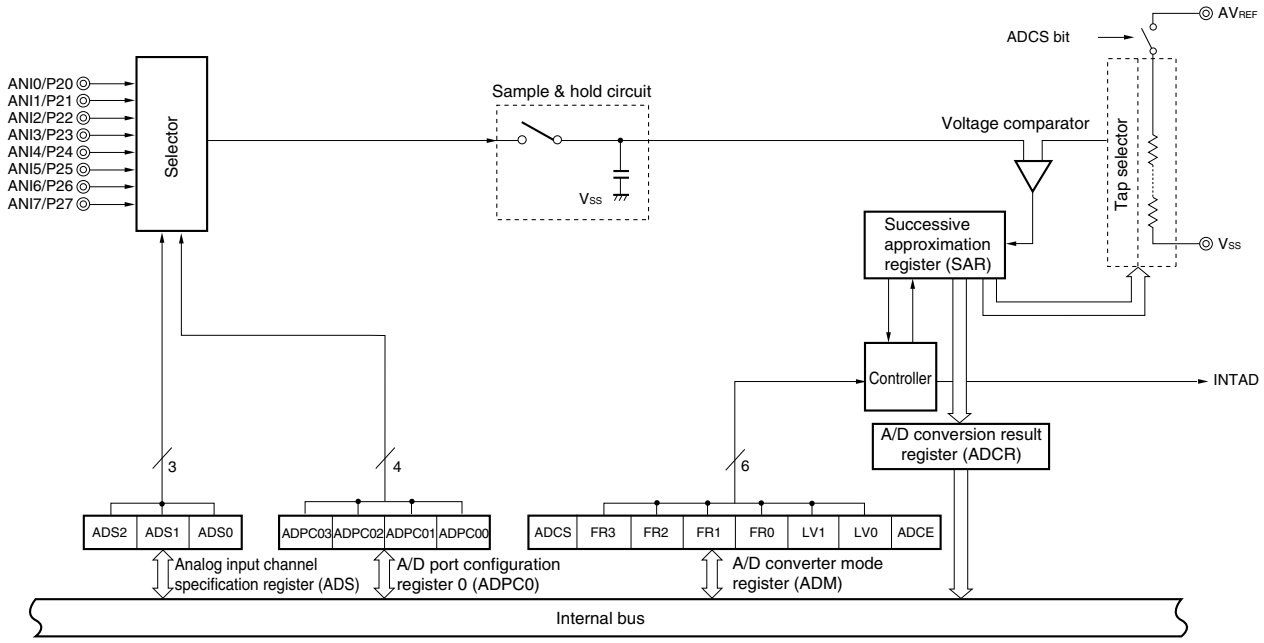
The 10-bit successive approximation type A/D converter converts an analog input signal into a digital value, and consists of up to eight channels (ANI0 to ANI7) with a resolution of 10 bits.

The A/D converter has the following function.

- **10-bit resolution A/D conversion**

  10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI7. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

Figure 12-1. Block Diagram of 10-Bit Successive Approximation type A/D Converter



Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

12.2 Configuration of 10-Bit Successive Approximation Type A/D Converter

The 10-bit successive approximation type A/D converter includes the following hardware.

(1) ANI0 to ANI7 pins

These are the 8-channel analog input pins of the 10-bit successive approximation type A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins or segment output pins (78K0/LG3-M only).

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

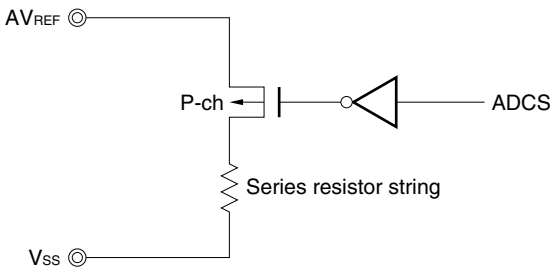
(2) Sample & hold circuit

The sample & hold circuit samples the input voltage of the analog input pin selected by the selector when A/D conversion is started, and holds the sampled voltage value during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AV_{REF} and V_{SS}, and generates a voltage to be compared with the sampled voltage value.

Figure 12-2. Circuit Configuration of Series Resistor String



(4) Voltage comparator

The voltage comparator compares the sampled voltage value and the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register converts the result of comparison by the voltage comparator, starting from the most significant bit (MSB). When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(6) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

Caution When data is read from ADCR and ADCRH, a wait cycle is generated. Do not read data from ADCR and ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. When using at least one port of port 2 as a digital port or for segment output, set it to the same potential as the V_{DD} pin.

The signal input to ANI0 to ANI7 is converted into a digital signal, based on the voltage applied across AV_{REF} and V_{SS}.

(10) V_{SS} pin

This pin is used as the ground potential pin of the A/D converter.

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) A/D port configuration register 0 (ADPC0)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input of 10-bit successive approximation type A/D converter or digital I/O of port.

(13) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(14) Port mode register 2 (PM2)

This register switches the ANI0/P20 to ANI7/P27 pins to input or output.

(15) Port function register 2 (PF2) (78K0/LG3-M only)

This register switches the ANI0/P20 to ANI7/P27 pins to I/O of port, analog input of A/D converter, or segment output.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

12.3 Registers Used in 10-Bit Successive Approximation Type A/D Converter

The A/D converter uses the following seven registers.

- A/D converter mode register (ADM)
- A/D port configuration register 0 (ADPC0)
- Analog input channel specification register (ADS)
- Port function register 2 (PF2)[Note]
- Port mode register 2 (PM2)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)

Note 78K0/LG3-M only.

(1) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

ADM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-3. Format of A/D Converter Mode Register (ADM)

Address: FF8DH After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	FR3[Note 1]	FR2[Note 1]	FR1[Note 1]	FR0[Note 1]	LV1[Note 1]	LV0[Note 1]	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation
1	Enables conversion operation

ADCE	Comparator operation control[Note 2]
0	Stops comparator operation
1	Enables comparator operation

Notes 1. For details of FR3 to FR0, LV1, LV0, and A/D conversion, see **Table 12-2 A/D Conversion Time Selection**.

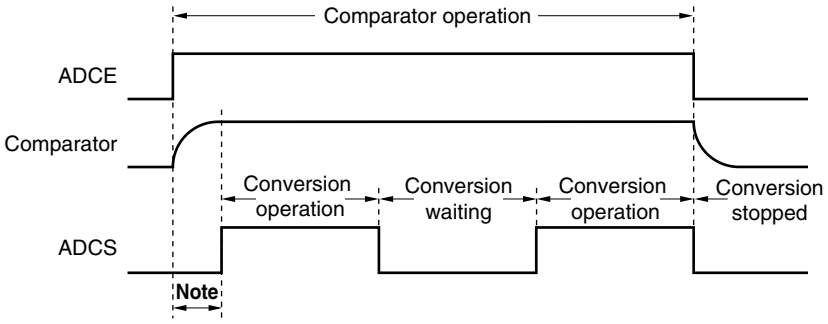
2. The operation of the comparator is controlled by ADCS and ADCE, and it takes 1 μs from operation start to operation stabilization. Therefore, when ADCS is set to 1 after 1 μs or more has elapsed from the time ADCE is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Table 12-1. Settings of ADCS and ADCE

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (comparator operation, only comparator consumes power)
1	0	Conversion mode (comparator operation stopped[Note])
1	1	Conversion mode (comparator operation)

Note Ignore data of the first conversion.

Figure 12-4. Timing Chart When Comparator Is Used



Note To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR3, LV1, and LV0 to values other than the identical data.

2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

Table 12-2. A/D Conversion Time Selection

(1) 2.7 V ≤ AV_{REF} ≤ 3.6 V (LV0 = 0)

A/D Converter Mode Register (ADM)						Conversion Time Selection				Conversion Clock (f_{AD})
FR3	FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz	
1	×	×	×	0	0	352/f_{PRS}	Setting prohibited	44.0 μs	35.2 μs	f_{PRS}/16
0	0	0	0	0	0	264/f_{PRS}		33.0 μs	26.4 μs	f_{PRS}/12
0	0	0	1	0	0	176/f_{PRS}		22.0 μs	17.6 μs	f_{PRS}/8
0	0	1	0	0	0	132/f_{PRS}	66.0 μs	16.5 μs	13.2 μs	f_{PRS}/6
<R> 0	0	1	1	0	0	88/f_{PRS}	44.0 μs	Setting prohibited	Setting prohibited	f_{PRS}/4
0	1	0	0	0	0	66/f_{PRS}	33.0 μs			f_{PRS}/3
0	1	0	1	0	0	44/f_{PRS}	22.0 μs			f_{PRS}/2
Other than above						Setting prohibited				

(2) 2.3 V ≤ AV_{REF} < 3.6 V (LV0 = 1)

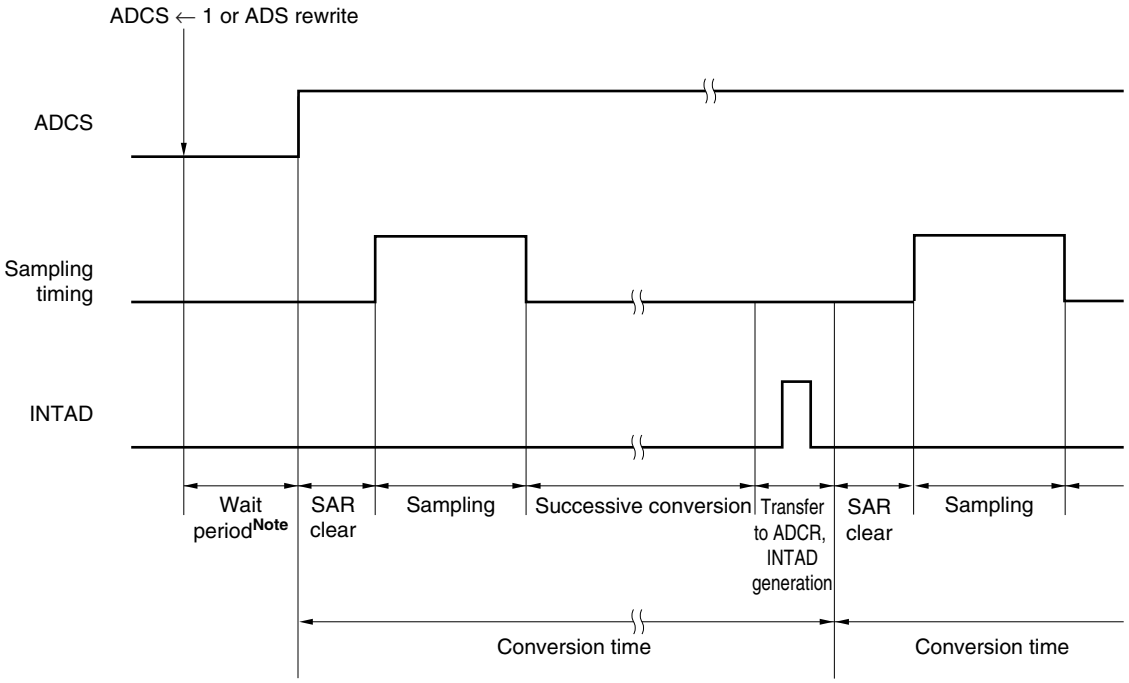
A/D Converter Mode Register (ADM)						Conversion Time Selection				Conversion Clock (f_{AD})
FR3	FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	
1	×	×	×	0	1	640/f_{PRS}	Setting prohibited	Setting prohibited	80.0 μs	f_{PRS}/16
0	0	0	0	0	1	480/f_{PRS}			60.0 μs	f_{PRS}/12
0	0	0	1	0	1	320/f_{PRS}		64.0 μs	40.0 μs	f_{PRS}/8
0	0	1	0	0	1	240/f_{PRS}		48.0 μs	30.0 μs	f_{PRS}/6
0	0	1	1	0	1	160/f_{PRS}	80.0 μs	32.0 μs	Setting prohibited	f_{PRS}/4
0	1	0	0	0	1	120/f_{PRS}	60.0 μs	Setting prohibited		f_{PRS}/3
0	1	0	1	0	1	80/f_{PRS}	40.0 μs			f_{PRS}/2
Other than above						Setting prohibited				

Cautions 1. Set the conversion times with the following conditions.
(1) 2.7 V ≤ AV_{REF} < 3.6 V (LV0 = 0) : f_{AD} = 0.262 to 1.8 MHz
(2) 2.3 V ≤ AV_{REF} < 3.6 V (LV0 = 1)
- **2.7 V ≤ AV_{REF} < 3.6 V: f_{AD} = 0.48 to 1.8 MHz**
- **2.3 V ≤ AV_{REF} < 2.7 V: f_{AD} = 0.48 to 1.48 MHz**

2. When rewriting FR3 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.
3. Change LV1 and LV0 from the default value, when 2.3 V ≤ AV_{REF} < 2.7 V.
4. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 12-5. A/D Converter Sampling and A/D Conversion Timing



Note For details of wait period, see **CHAPTER 35 CAUTIONS FOR WAIT**.

(2) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register. The higher 8 bits of the conversion result are stored in FF07H and the lower 2 bits are stored in the higher 2 bits of FF06H.

ADCR can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 12-6. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FF06H, FF07H After reset: 0000H R

Symbol	FF07H								FF06H							
ADCR											0	0	0	0	0	0

Cautions 1. When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register 0 (ADPC0), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC0. Using timing other than the above may cause an incorrect conversion result to be read.

2. If data is read from ADCR, a wait cycle is generated. Do not read data from ADCR when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(3) 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 10-bit resolution are stored.

ADCRH can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-7. Format of 8-Bit A/D Conversion Result Register (ADCRH)

Address: FF07H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

Cautions 1. When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register 0 (ADPC0), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC0. Using timing other than the above may cause an incorrect conversion result to be read.

2. If data is read from ADCRH, a wait cycle is generated. Do not read data from ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(4) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-8. Format of Analog Input Channel Specification Register (ADS)

Address: FF8EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

Cautions 1. Be sure to clear bits 3 to 7 to "0".
2. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).
3. Do not set a pin to be used as a digital I/O pin with ADPC0 with ADS.
4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(5) A/D port configuration register 0 (ADPC0)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input (analog input of 16-bit ΔΣ type A/D converter or analog input of 10-bit successive approximation type A/D converter) or digital I/O of port.

ADPC0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 08H.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

Figure 12-9. Format of A/D Port Configuration Register 0 (ADPC0)

(a) 78K0/LE3-M

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPC03	0	0	0

ADPC03	Digital I/O (D)/analog Input (A) switching
	P27/ANI7
0	A
1	D

(b) 78K0/LG3-M

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPC03	ADPC02	ADPC01	ADPC00

ADPC03	ADPC02	ADPC01	ADPC00	Digital I/O (D)/analog input (A) switching							
				P27/ANI7	P26/ANI6	P25/ANI5	P24/ANI4	P23/ANI3	P22/ANI2	P21/ANI1	P20/ANI0
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

2. Do not set the pin set by ADPC0 as digital I/O by ADS, ADDS1, or ADDS0.

3. If data is written to ADPC0, a wait cycle is generated. Do not write data to ADPC0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

Caution 4. If pins ANIx/P2x/SEGxx are set to segment output pins via the PF2 register, output is set to segment output, regardless of the ADPC0 setting (for 78K0/LG3-M only).

(6) Port mode register 2 (PM2)

When using the ANI0/P20 to ANI7/P27 pins for analog input port, set PM20 to PM27 to 1. The output latches of P20 to P27 at this time may be 0 or 1.

If PM20 to PM27 are set to 0, they cannot be used as analog input port pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

Figure 12-10. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 2 of 78K0/LG3-M products. For the format of port mode register 2 of 78K0/LE3-M products, see **(1) Port mode registers (PMxx and LPMx)** in **4.3 Registers Controlling Port Function**.

ANI0/P20 to ANI7/P27 pins are as shown below depending on the settings of PF2, ADPC0, PM2, and ADS.

Table 12-3. Setting Functions of P20/ANI0 to P27/ANI7 Pins

PF2[Note]	ADPC0	PM2	ADS	P20/SEG39/ANI0 to P27/SEG32/ANI7 Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output[Note] selection	–	–	–	Segment output[Note]

Note 78K0/LG3-M only.

12.4 10-Bit Successive Approximation Type A/D Converter Operations

12.4.1 Basic operations of A/D converter

<1> Set bit 0 (ADCE) of the A/D converter mode register (ADM) to 1 to start the operation of the comparator.

<2> Set channels for A/D conversion to analog input by using the A/D port configuration register (ADPC0) and set to input mode by using port mode register 2 (PM2).

<3> Set A/D conversion time by using bits 6 to 1 (FR3 to FR0, LV1, and LV0) of ADM.

<4> Select one channel for A/D conversion using the analog input channel specification register (ADS).

<5> Start the conversion operation by setting bit 7 (ADCS) of ADM to 1.
(<6> to <12> are operations performed by hardware.)

<6> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<7> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<8> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<9> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<10> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of SAR is manipulated as follows.

- Analog input voltage ≥ Voltage tap: Bit 8 = 1
- Analog input voltage < Voltage tap: Bit 8 = 0

<11> Comparison is continued in this way up to bit 0 of SAR.

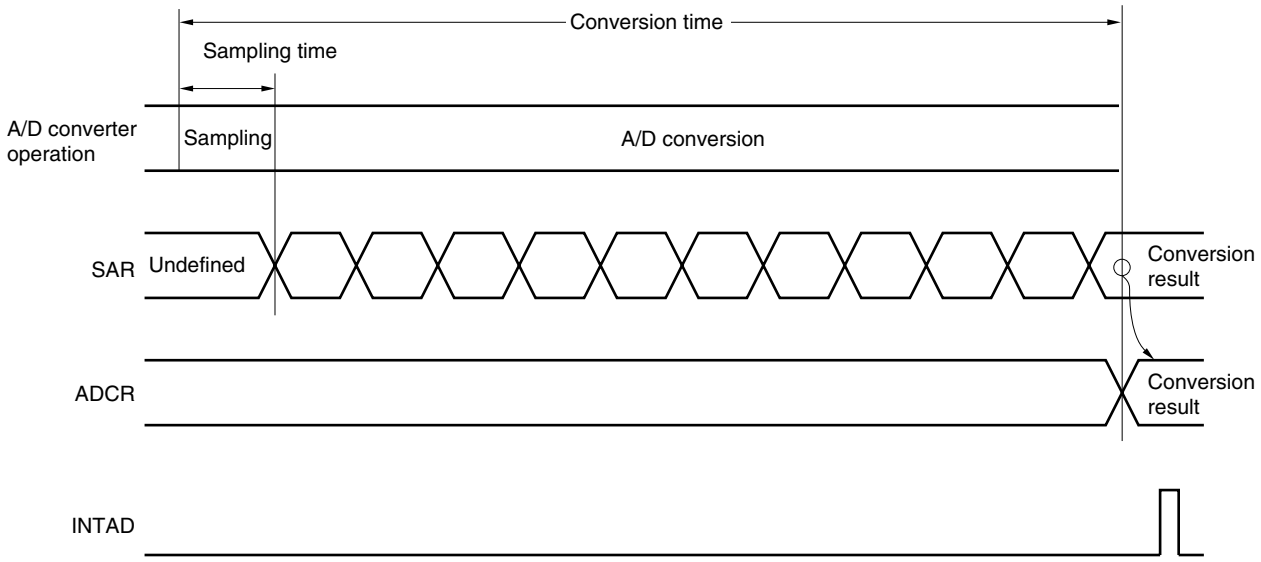
<12> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<13> Repeat steps <6> to <12>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <5>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 μs or longer, and start <5>. To change a channel of A/D conversion, start from <4>.

Caution Make sure the period of <1> to <5> is 1 μs or more.

Remark Two types of A/D conversion result registers are available.
- ADCR (16 bits): Store 10-bit A/D conversion value
- ADCRH (8 bits): Store 8-bit A/D conversion value

Figure 12-11. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

12.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI7) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

AV_{REF}: AV_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

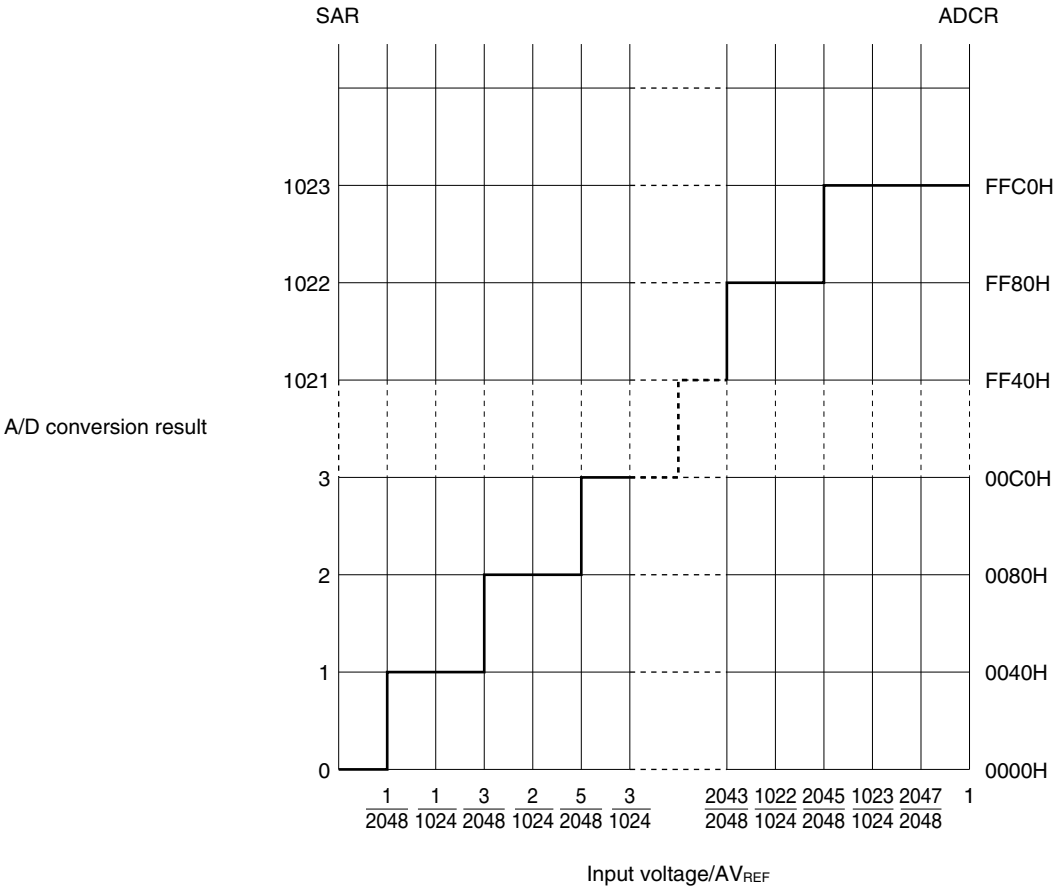
SAR: Successive approximation register

Remark 78K0/LE3-M: ANI7

78K0/LG3-M: ANI0 to ANI7

Figure 12-12 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 12-12. Relationship Between Analog Input Voltage and A/D Conversion Result



12.4.3 A/D converter operation mode

The operation mode of the A/D converter is the select mode. One channel of analog input is selected from ANI0 to ANI7 by the analog input channel specification register (ADS) and A/D conversion is executed.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

(1) A/D conversion operation

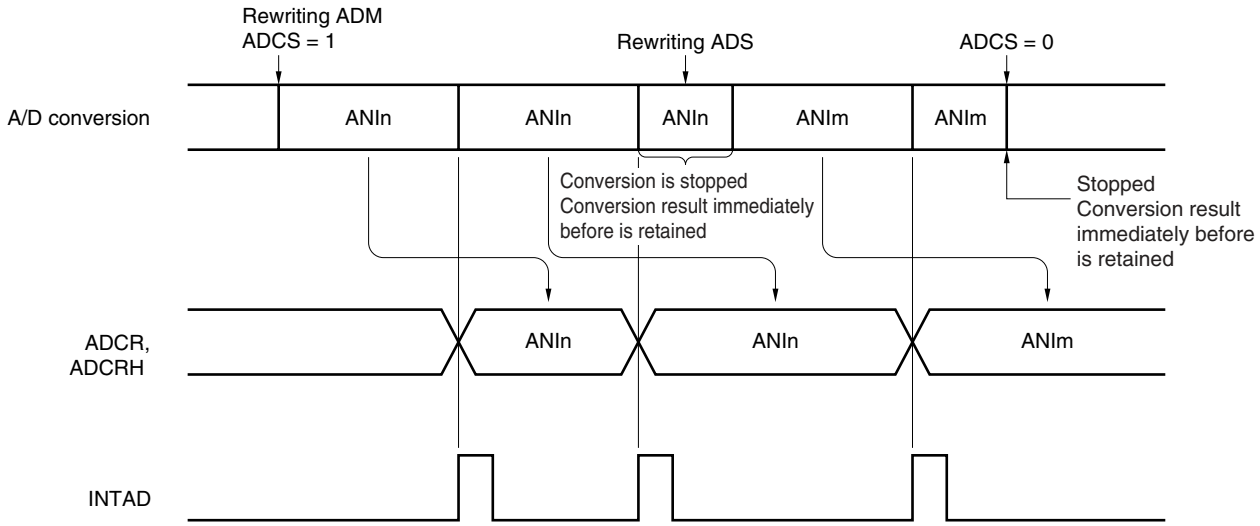
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCR), and an interrupt request signal (INTAD) is generated. When one A/D conversion has been completed, the next A/D conversion operation is immediately started.

If ADS is rewritten during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result immediately before is retained.

Figure 12-13. A/D Conversion Operation



Remark 78K0/LE3-M: n =7, m = 7
78K0/LG3-M: n = 0 to 7, m = 0 to 7

The setting methods are described below.

<1> Set bit 0 (ADCE) of the A/D converter mode register (ADM) to 1.
<2> Set the channel to be used in the analog input mode by using bits 3 to 0 (ADPC03 to ADPC00) of the A/D port configuration register 0 (ADPC0) and bits 7 to 0 (PM27 to PM20) of port mode register 2 (PM2).
<3> Select conversion time by using bits 6 to 1 (FR3 to FR0, LV1, and LV0) of ADM.
<4> Select a channel to be used by using bits 2 to 0 (ADS2 to ADS0) of the analog input channel specification register (ADS).
<5> Set bit 7 (ADCS) of ADM to 1 to start A/D conversion.
<6> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<7> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Change the channel>

<8> Change the channel using bits 2 to 0 (ADS2 to ADS0) of ADS to start A/D conversion.
<9> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<10> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Complete A/D conversion>

<11> Clear ADCS to 0.
<12> Clear ADCE to 0.

Cautions 1. Make sure the period of <1> to <5> is 1 μs or more.
2. <1> may be done between <2> and <4>.
3. <1> can be omitted. However, ignore data of the first conversion after <5> in this case.
4. The period from <6> to <9> differs from the conversion time set using bits 6 to 1 (FR3 to FR0, LV1, LV0) of ADM. The period from <8> to <9> is the conversion time set using FR3 to FR0, LV1, and LV0.

12.5 How to Read Successive Approximation Type A/D Converter Characteristics Table

Here, special terms unique to the successive approximation type A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 12-14. Overall Error

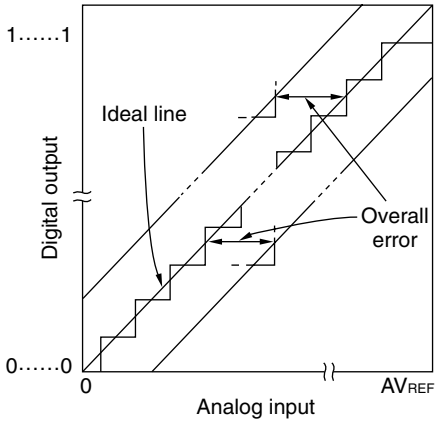
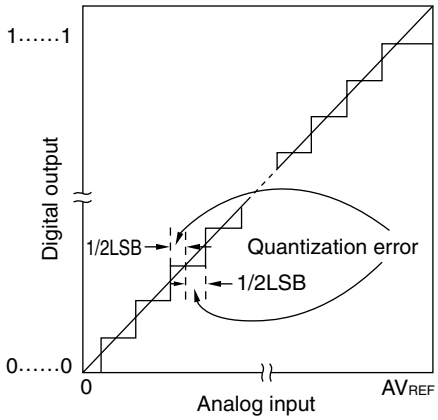


Figure 12-15. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 12-16. Zero-Scale Error

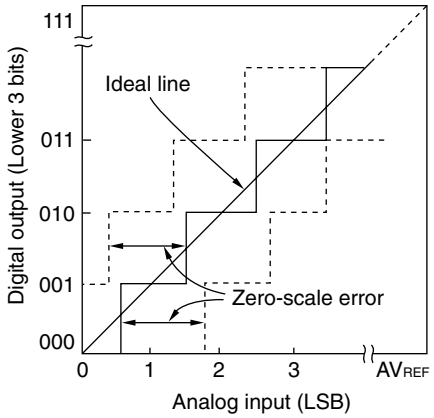


Figure 12-17. Full-Scale Error

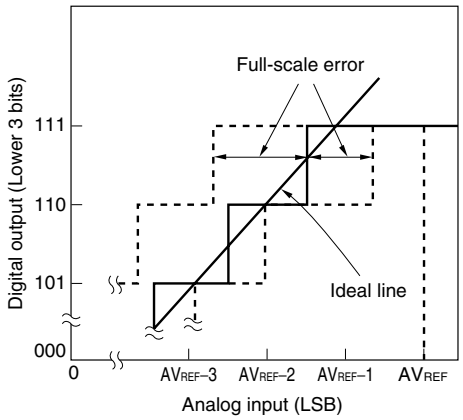


Figure 12-18. Integral Linearity Error

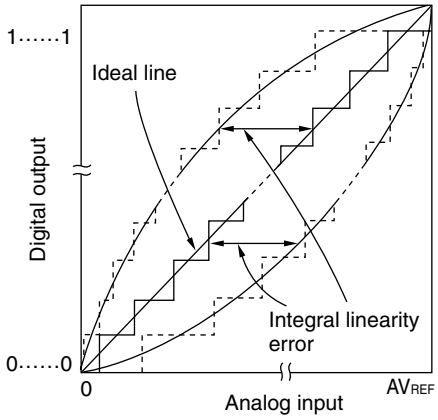
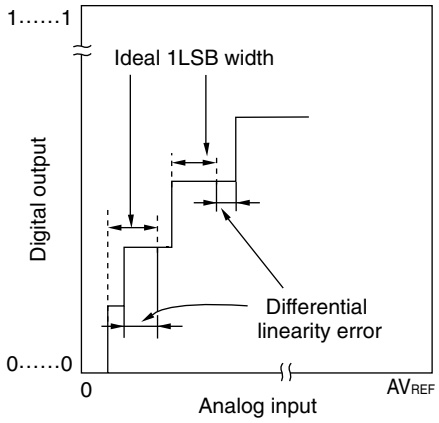


Figure 12-19. Differential Linearity Error



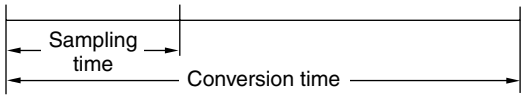
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



12.6 Cautions for 10-bit successive approximation type A/D Converter

(1) Operating current in STOP mode

The A/D converter stops operating in the STOP mode. At this time, the operating current can be reduced by clearing bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI7

Observe the rated range of the ANI0 to ANI7 input voltage. If a voltage of AV_{REF} or higher and V_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between A/D conversion result register (ADCR, ADCRH) write and ADCR or ADCRH read by instruction upon the end of conversion

ADCR or ADCRH read has priority. After the read operation, the new conversion result is written to ADCR or ADCRH.

<2> Conflict between ADCR or ADCRH write and A/D converter mode register (ADM) write, analog input channel specification register (ADS), or A/D port configuration register 0 (ADPC0) write upon the end of conversion

ADM, ADS, or ADPC0 write has priority. ADCR or ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REF} pin and pins ANI0 to ANI7.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

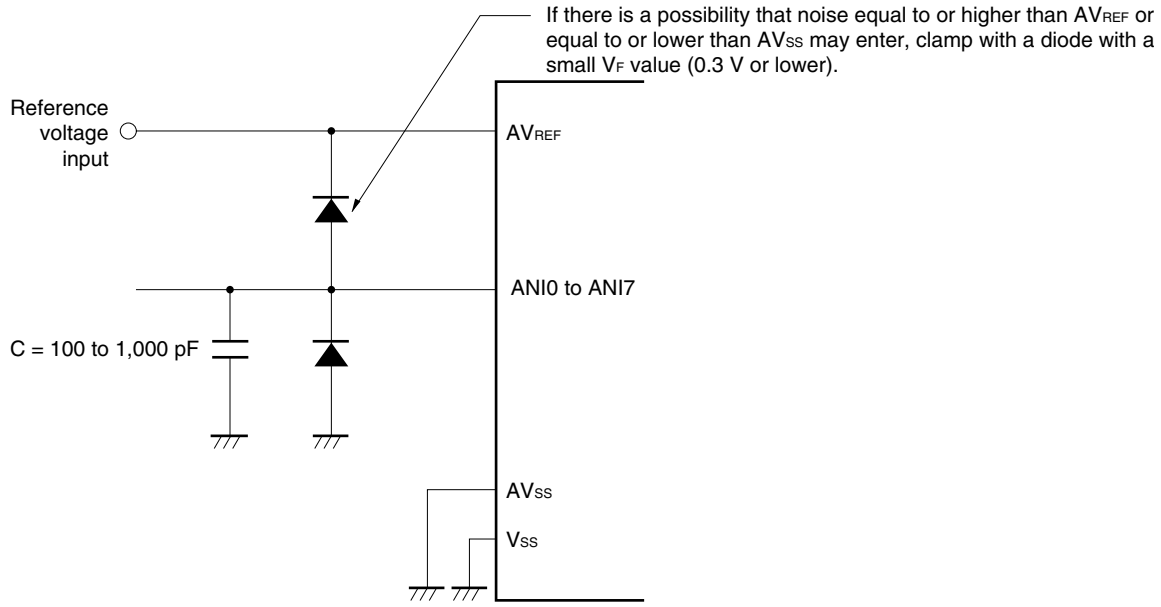
<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 12-20 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

Figure 12-20. Analog Input Pin Connection



(5) ANI7/P27 pins (78K0/LE3-M), ANI0/SEG39/P20 to ANI7/SEG32/P27 pins (78K0/LG3-M)

<1> The analog input pins (ANI0 to ANI7) are also used as I/O port pins (P20 to P27).
When A/D conversion is performed with any of ANI0 to ANI7 selected, do not access P20 to P27 while conversion is in progress; otherwise the conversion resolution may be degraded. It is recommended to any pin of P20 to P27 used as digital I/O port starting with the ANI0/P20 that is the furthest from AVREF.

<2> If a digital pulse is input or output, or segment-output to the pins adjacent to the pins currently used for A/D conversion, the expected value of the A/D conversion may not be obtained due to coupling noise. Therefore, do not input or output a pulse, or segment-output to the pins adjacent to the pin undergoing A/D conversion.

(6) Input impedance of ANI0 to ANI7 pins

This A/D converter charges a sampling capacitor for sampling during sampling time.
Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.
To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 10 kΩ, and to connect a capacitor of about 100 pF to the ANI0 to ANI7 pins (see **Figure 12-20**).

(7) AVREF pin input impedance

A series resistor string of several tens of kΩ is connected between the AVREF and VSS pins.
Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AVREF and VSS pins, resulting in a large reference voltage error.

Remark 78K0/LE3-M: ANI7
78K0/LG3-M: ANI0 to ANI7

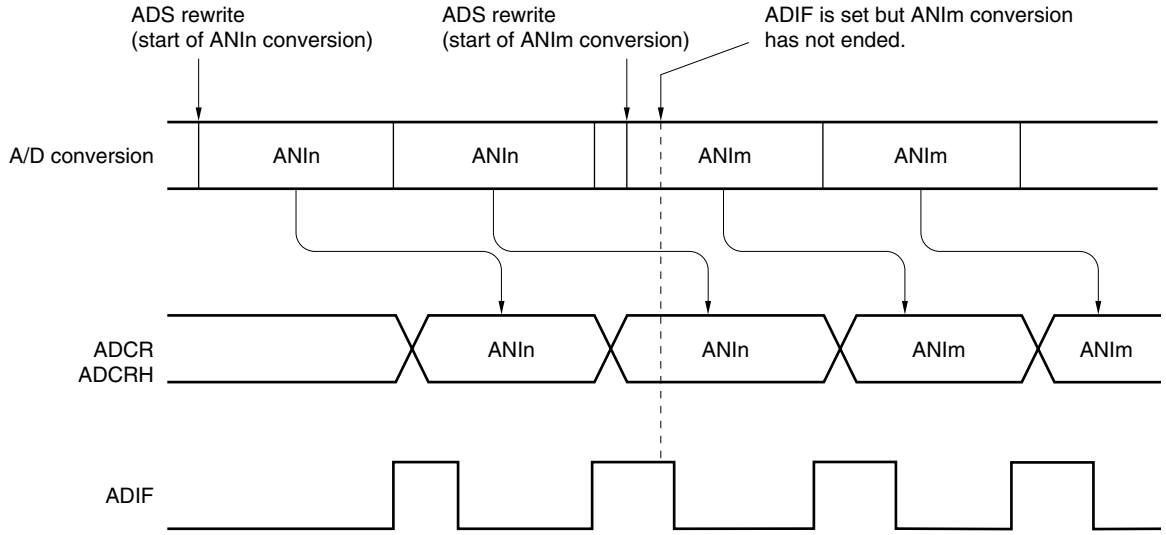
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 12-21. Timing of A/D Conversion End Interrupt Request Generation



Remark 78K0/LE3-M: n =7, m = 7
78K0/LG3-M: n = 0 to 7, m = 0 to 7

(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register 0 (ADPC0), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC0. Using a timing other than the above may cause an incorrect conversion result to be read.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 12-22. Internal Equivalent Circuit of ANIn Pin

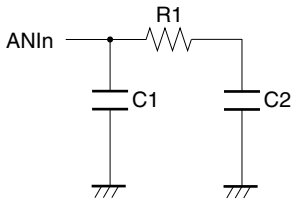


Table 12-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	R1	C1	C2
2.7 V ≤ AV_{REF} < 3.6 V	31 kΩ	8 pF	5 pF
2.3 V ≤ AV_{REF} < 2.7 V	381 kΩ	8 pF	5 pF

Remarks 1. The resistance and capacitance values shown in Table 12-4 are not guaranteed values.

2. 78K0/LE3-M: n = 7, m = 7

78K0/LG3-M: n = 0 to 7

CHAPTER 13 24-BIT ΔΣ-TYPE A/D CONVERTER

	78K0/LE3-M	78K0/LG3-M
24-bit ΔΣ-type A/D converter	3 ch	4 ch

13.1 Functions of 24-bit ΔΣ-Type A/D Converter

The 24-bit ΔΣ-type A/D converter has a 24-bit resolution when converting an analog input signal to digital values.

- ○ S/N ratio: 62 dB min. (when gain of × 16 is selected for channels 1 and 3)
- ○ 24-bit resolution (conversion result register: 24 bit)
- ○ 3 channels (78K0/LE3-M)
  4 channels (78K0/LG3-M)
- ○ Analog input: 6 (positive, negative input/channel) (78K0/LE3-M)
  8 (positive, negative input/channel) (78K0/LG3-M)
- ○ ΔΣ conversion mode
- ○ Pre-amplifier gain selectable: × 2 or × 16 (channels 1 and 3)
- ○ Operating voltage: AV_{DD} = 3.0 to 3.6 V, AV_{SS} = 0 V
- ○ Analog input voltage: ±0.375 V (channels 0 and 2)
  ±0.1875 V (channels 1 and 3, when pre-amplifier gain of × 2 is selected)
  ±23.4 mV (channels 1 and 3, when pre-amplifier gain of × 16 is selected)
- ○ Reference voltage generation (1.226 V (TYP.) can be output)[Note]
- ○ Conversion rate selectable: 4.340 kHz

Note The reference voltage for the 24-bit ΔΣ-type A/D converter can be selected from the external reference potential and internal reference potential.

Table 13-1 Shows the Reference Characteristics

Item	Symbol	MIN.	TYP.	MAX.	Unit
external reference potential (input)	AV_{REFIO1}	1.20		1.25	V
internal reference potential (output)	AV_{REFIO2}	1.165	1.226	1.287	V

Caution To use the 24-bit ΔΣ-type A/D converter, supply 10 MHz to the extended SFR by setting the clock output selection register (CKS) (see CHAPTER 11 BUZZER OUTPUT CONTROLLER).

13.2 Configuration of 24-bit ΔΣ-Type A/D Converter

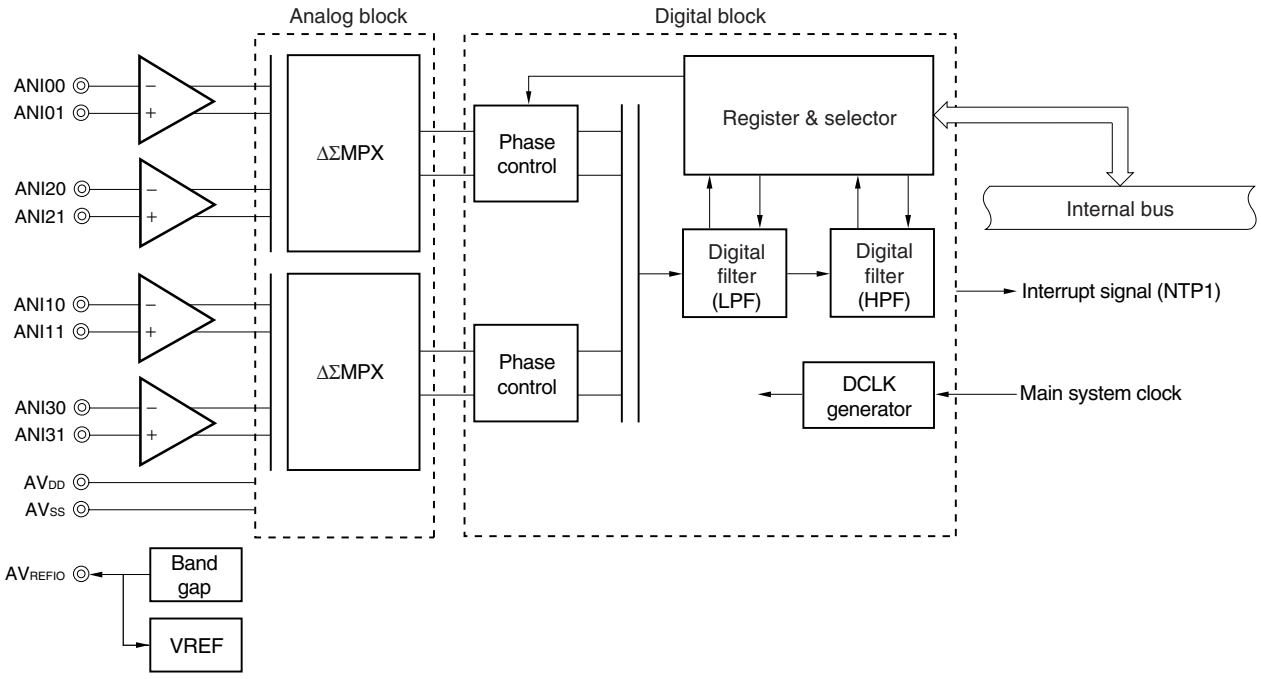
The 24-bit ΔΣ-type A/D converter consists of the following hardware.

Table 13-2. Configuration of 24-bit ΔΣ-Type A/D Converter

Item	Configuration
Analog input	3 channels and 6 inputs (78K0/LE3-M) 4 channels and 8 inputs (78K0/LG3-M)
Registers	24-bit ΔΣ-type A/D converter mode register (ADM2) High-pass filter control register 0 (HPFC0) High-pass filter control register 1 (HPFC1) 24-bit ΔΣ-type A/D conversion result register n (ADCRn) Phase control registers 0 and 1 (PHC0 and PHC1) A/D clock delay setting register (ADLY)
Internal units	Pre-amplifier block ΔΣ converter Phase control Reference voltage generator Digital filter (DF) High-pass filter (HPF)

Remark 78K0/LE3-M: n = 0 to 2
78K0/LG3-M: n = 0 to 3

Figure 13-1. Block Diagram of 24-bit ΔΣ-Type A/D Converter



The channels (voltage and current) supported for each input pin differ depending on whether the two-wire mode or three-wire mode is used.

Connect the voltage channel to the voltage sensor and the current channel to the current sensor in accordance with the following tables.

< In the case of two-wire mode (CHMD = 0) >

Input mode	78K0/LE3-M	78K0/LG3-M
ANI00, ANI01	voltage channel	voltage channel
ANI10, ANI11	current channel 1	current channel 1
ANI20, ANI21	current channel 2	current channel 2
ANI30, ANI31	–	Not used

< In the case of three-wire mode (CHMD = 1) >

Input mode	78K0/LE3-M	78K0/LG3-M
ANI00, ANI01	Not support	voltage channel 1
ANI10, ANI11	Not support	current channel 1
ANI20, ANI21	Not support	voltage channel 2
ANI30, ANI31	–	current channel 2

Remark 78K0/LE3-M: ANI00, ANI01, ANI10, ANI11, ANI20, and ANI21 pins
78K0/LG3-M: ANI00, ANI01, ANI10, ANI11, ANI20, ANI21, ANI30, and ANI31 pins

(1) Pre-amplifier

This unit shifts the signal input to the ANIn0 and ANIn1 pins with AV_{SS} as the reference voltage into the internal reference voltage, and then amplifies the input signal. It supplies its output signal to the ΔΣ circuit.

(2) Multiplex ΔΣ circuit

Two 2-multiplex ΔΣ circuits are provided so that a total of 4 channels[Note] of analog inputs can be converted into digital signals. These two ΔΣ circuits operate synchronously, and one ΔΣ circuit executes analog input conversion of two channels by time division. The input signal is amplified by the pre-amplifier and ΔΣ circuit, and the gain of channels 0 and 2 are fixed to × 1, and that of channels 1 and 3 can be selected from × 2 and × 16. A high-speed mode (4.340 kHz) is selectable as the conversion rate, and the over-sampling frequency in the respective modes is 555.6 kHz (at operation clock = 10 MHz).

Note 78K0/LE3-M: 3 channels
78K0/LG3-M: 4 channels

(3) Phase adjustment circuit

This circuit adjusts the phase of input analog signals. The phase between analog signals is adjusted by using a step of 128 fs.

Phase shifts between input analog signals occur due to external components (such as current sensors). Use the PHC register to correct such phase shifts in advance, because these shifts can decrease the precision of power calculations.

Correcting phase shifts uses 255 steps, and each step is equivalent to a 128 fs (1/128 x 4.34 k) cycle, so the delay time is about 1.8 μs. The phase can be adjusted in 0.0389° units if the line frequency is 60 Hz, or in 0.0324° units if the line frequency is 50 Hz.

(4) Reference voltage generator

An internal reference voltage source (band-gap reference circuit) is provided and a reference voltage is output from the reference voltage I/O pin (AV_{REFIO}). To use an external reference voltage source, input its voltage to the AV_{REFIO} pin.

(5) Digital filter (DF)

This unit eliminates high harmonic noise included in the ΔΣ circuit and thins out the data rate to 1/128.

(6) High-pass filter

This unit eliminates the DC component included in the input signal and the DC offset generated by the analog circuit. Whether the high-pass filter is inserted or not can be selected for each channel.

(7) ANIn0 to ANIn1 pins

These are analog input pins of the A/D converter. One channel inputs two signals. The ANIn0 pin is the negative input, while the ANIn1 pin is the positive input.

Note 78K0/LE3-M: n = 0 to 2
78K0/LG3-M: n = 0 to 3

(8) AV_{DD} pin

This is the analog power supply pin of the A/D converter. Always keep the voltage on this pin the same as that on the V_{DD} pin even when the A/D converter is not used.

(9) AV_{SS} pin

This is the ground pin of the A/D converter. Always keep the voltage on this pin the same as that on the V_{SS} pin even when the A/D converter is not used.

(10) AV_{REFIO} pin

This is the I/O pin of the reference voltage to the A/D converter. This pin is used as an output pin if using an internal reference voltage, or as an input pin if using an external reference voltage.

13.3 Registers Used in 24-Bit ΔΣ-Type A/D Converter

The 24-bit ΔΣ-type A/D converter uses the following registers.
These registers are all allocated to the extended SFR space.
For details about how to access the extended SFR space, see **CHAPTER 17 EXTENDED SFR INTERFACE**.

- 24-bit ΔΣ-type A/D converter mode register (ADM2)
- HPF filter control register 0 (HPFC0)
- HPF filter control register 1 (HPFC1)
- 24-bit ΔΣ-type A/D conversion result register n (ADCRn)
- Phase control registers 0 and 1 (PHC0 and PHC1)
- A/D clock delay setting register (ADLY)

Remark 78K0/LE3-M: n = 0 to 2
78K0/LG3-M: n = 0 to 3

(1) 24-bit ΔΣ-Type A/D converter mode register (ADM2)

This register is used to turn the power supply for the 24-bit ΔΣ-type A/D converter on or off, enable or stop conversion operation, switch the single phase mode, and specify the reference potential and amplifier gain.
ADM2 is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation sets this register to 00H.

Figure 13-2. Format of 24-Bit ΔΣ-Type A/D Converter Control Register (ADM2)

Address: A3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM2	ADPON	ADCE2	CHMD	0	BGCUT	PAGS1	0	0

ADPON	Specification of power to 24-bit ΔΣ-type A/D converter
0	Power OFF
1	Power ON

ADCE2	Specification of operation of 24-bit ΔΣ-type A/D converter
0	Stop conversion operation
1	Enable conversion operation

CHMD[Note]	Switch between the single-phase two-wire mode and the single-phase three-wire mode
0	Single-phase two-wire mode
1	Single-phase three-wire mode

BGCUT	Control signal that stops BGR output
0	Specifies the use of an internal reference potential and the use of AV_{REFIO} as an output pin.
1	Stops BGR output and specifies the use of an external reference potential and the use of AV_{REFIO} as an input pin.

PAGS1	Specification of programmable amplifier gain of channels 1 and 3
0	× 2
1	× 16

Note The channels (voltage and current) supported for each input pin differ depending on whether the two-wire mode or three-wire mode is used.
Connect the voltage channel to the voltage sensor and the current channel to the current sensor in accordance with the following tables.

<In the case of two-wire mode (CHMD = 0) >

Input mode	78K0/LE3-M	78K0/LG3-M
ANI00, ANI01	Voltage channel	Voltage channel
ANI10, ANI11	Current channel 1	Current channel 1
ANI20, ANI21	Current channel 2	Current channel 2
ANI30, ANI31	–	Not used

<In the case of three-wire mode (CHMD = 1) >

Input mode	78K0/LE3-M	78K0/LG3-M
ANI00, ANI01	Not support	Coltage channel 1
ANI10, ANI11	Not support	Current channel 1
ANI20, ANI21	Not support	Voltage channel 2
ANI30, ANI31	–	Current channel 2

Caution Be sure to set bits 0, 1, and 4 to 0.

(2) High-pass filter control register 0 (HPFC0)

This 8-bit register is used to specify insertion of a high-pass filter for each channel.

HPFC0 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation sets this register to 00H.

Figure 13-3. Format of High-Pass Filter Control Register 0 (HPFC0)

Address: A5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
HPFC0	0	0	0	0	THR3	THR2	THR1	THR0

THRn	Specification of insertion of high-pass filter for channel n (n = 0 to 3)
0	Insert high-pass filter
1	Do not insert high-pass filter and through.

Caution Be sure to set bits 4 to 7 to 0.

(3) High-pass filter control register 1 (HPFC1)

This 8-bit register is used to control the high-pass filter operation for each channel.

HPFC1 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation sets this register to 00H.

Figure 13-4. Format of High-Pass Filter Control Register 1 (HPFC1)

Address: A6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
HPFC1	0	0	0	0	DLY3	DLY 2	DLY 1	DLY 0

DLY n	Specify phase delay to add to channel n (n = 0 to 3)
0	Does not add phase delay in the high-pass filter.
1	Adds phase delay in the high-pass filter.

Caution Be sure to set bits 4 to 7 to 0.

(4) 24-Bit ΔΣ-Type A/D conversion result registers n (ADCRn)

These 24-bit registers are used to store the conversion result of each channel.

ADCRn is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

The value of these registers is initialized to 0000H by system reset and when the ADCE2 bit is 0.

Figure 13-5. Format of 24-Bit ΔΣ-Type A/D Conversion Result Registers n (ADCRn)

Address: A7H to A9H After reset: 000000H R

Symbol	ADCR0H (A9H)								ADCR0M (A8H)								ADCR0L (A7H)							
ADCR0																								
	23							16	15							8	7							0

Address: AAH to ACH After reset: 000000H R

Symbol	ADCR1H (ACH)								ADCR1M (ABH)								ADCR1L (AAH)							
ADCR1																								
	23							16	15							8	7							0

Address: ADH to AFH After reset: 000000H R

Symbol	ADCR2H (AFH)								ADCR2M (AEH)								ADCR2L (ADH)							
ADCR2																								
	23							16	15							8	7							0

Address: B0H to B2H After reset: 000000H R

Symbol	ADCR3H (B2H)								ADCR3M (B1H)								ADCR3L (B0H)							
ADCR3																								
	23							16	15							8	7							0

Cautions 1. Read the ADCRn register when the ADCE2 bit is 1, because the register is initialized when the ADCE2 bit is 0.

<R> **2. For full-scale input, the ADCRn register is set to the value below.**

Input voltage (gain 1 time)	ADCRn register value
0.375 V	0x400000
–0.375 V	0xC00000

Remark 78K0/LE3-M: n = 0 to 2
78K0/LG3-M: n = 0 to 3

(5) Phase control registers 0 and 1 (PHC0, PHC1)

These 9-bit registers are used to control the phase adjustment for each channel.

Phase adjustment changes the timing at which one bit of A/D conversion data input from the analog block is output to the digital filter block. These registers can be used to perform 256 steps of adjustment.

PHC0 and PHC1 are allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation sets this register to 0000H.

Figure 13-6. Format of Phase Control Registers 0 and 1 (PHC0, PHC1)

Address: B3H and B4H After reset: 0000H R/W

Symbol	PHC0H (B4H)							PHC0L (B3H)								
PHC0	0	0	0	0	0	0	0	PHC08	PHC07	PHC06	PHC05	PHC04	PHC03	PHC02	PHC01	PHC00
	15							8	7							0

Address: B5H and B6H After reset: 0000H R/W

Symbol	PHC0H (B6H)							PHC0L (B5H)								
PHC1	0	0	0	0	0	0	0	PHC18	PHC17	PHC16	PHC15	PHC14	PHC13	PHC12	PHC11	PHC10
	15							8	7							0

PHC0L (PHC00 to PHC07), PHC1L (PHC10 to PHC17)	Specify phase adjustment amount (one step = 128 fs)
00H	Through (no phase adjustment)
01H	One step
…	
FEH	254 steps
FFH	255 steps

PHC08, PHC18	Select voltage channel or current channel for phase adjustment
0	Specifies that the value specified for PHCnL be used to adjust the phase of voltage channel n (n = 0 or 1).
1	Specifies that the value specified for PHCnL be used to adjust the phase of current channel n (n = 0 or 1).

(6) A/D clock delay setting register (ADLY)

ADLY is a register that controls the phase between the A/D operation clock and the digital clock.

Be sure to clear this register to 00H.

ADLY is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation sets this register to 00H.

Figure 13-7. Format of A/D Clock Delay Setting Register (ADLY)

Address: A4H After reset: 00H R/W

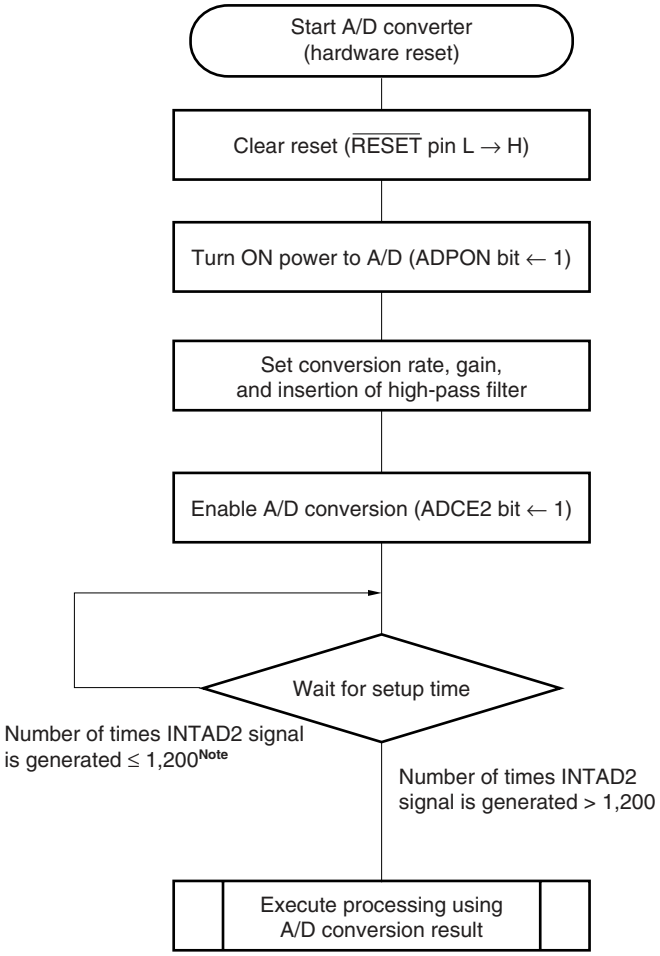
Symbol	7	6	5	4	3	2	1	0
ADLY	0	0	0	0	0	0	0	0

Caution Be sure to set bits 0 to 7 to 0.

13.4 Operation of 24-bit ΔΣ-Type A/D Converter

The A/D converter starts operating when the ADPON bit and ADCE2 bit of ADM2 register are set to 1. The setup time of the analog block and digital filter block is required after power application and start of conversion. Perform initialization in accordance with the flowchart below.

Figure 13-8. Initialization Flowchart



Note The setup time (the number of times the INTAD2 signal is to be generated) when the ADPON bit is set to 1 is subject to change. Consult Renesas Electronics before using this function.

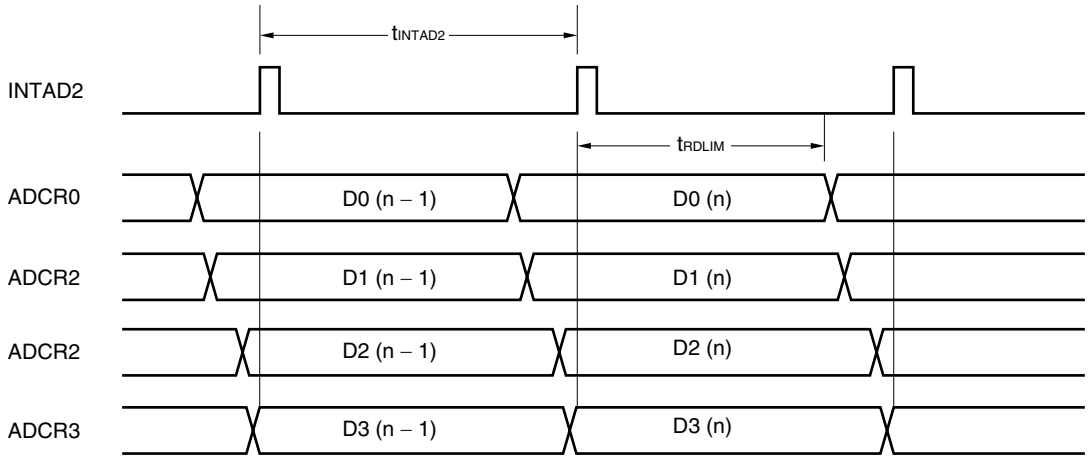
Caution If the A/D converter is temporarily stopped for initialization (ADCE2 bit ← 0 with ADPON bit set to 1) and then restarted, it is necessary to wait for a certain setup time. In this case, the setup time should be equal to 10 A/D conversion end interrupt request signals (INTAD2), which is the delay of the digital filter.

When A/D conversion is enabled, conversion of the signals on the four channels of analog input pins (ANIn0 and ANIn1 pins) is started. Two sets of 2-multiplex ΔΣ circuits are provided, each of which executes conversion of two channels by time division. Each time conversion of all the four channels is completed, the INTAD2 signal is generated to inform the CPU that the conversion result can be read.

To read the ADCRn register by interrupt servicing, the maximum pending time is as shown in **Figure 13-9**. Complete reading of the ADCRn register within this time.

Remark n = 0 to 3

Figure 13-9. Timing of Generation of INTAD2 Signal and Storing in ADCRn Register (operation clock = 10 MHz)



t_{INTAD2}: Interrupt generation cycle : 230.4 μs

t_{RDLIM}: ADCRn register read pending time (MAX.): 223.8 μs (t_{INTAD2} – 5.5 × A/D system clock (operation clock/12))

13.5 Cautions of 24-bit ΔΣ-Type A/D Converter

(1) Read the ADCRn register by A/D conversion end interrupt (INTAD2) servicing. Otherwise, an illegal value may be read because of a conflict between storing the conversion value in the ADCRn register and reading the register. The period of the INTAD2 processing during which reading the ADCRn register is 223.8 μs (at 10 MHz).

(2) After turning ON power to the A/D converter (ADPON bit of ADM2 register is set to 1), the internal setup time of the A/D converter is necessary. Consequently, the data of the first 1,200 conversions is invalid.

(3) The setup time is also necessary when the A/D converter has been temporarily stopped once for initialization (by clearing the ADCE2 bit of ADM2 register with the ADPON bit set to 1) and then restarted. Wait for the duration of 10 INTAD2 signals, which is the delay of the digital filter.

(4) The time required for the correct data to be output after the conversion operation has been enabled (by setting the ADCE2 bit to 1) differs depending on the analog input status at that time. This is because the stabilization time of the high-pass filter changes depending on the analog input status.

(5) Be sure to set the conversion speed and gain, and the HPFC0, HPFC1, and ADLY registers while the A/D converter is stopped (ADCE2 bit = 0).

(6) Because the ADCRn register is initialized when the ADCE2 bit is 0, read the ADCRn register when the ADCE2 bit is 1.

(7) Clear the ADPON bit to 0 before shifting to the software STOP mode. If software STOP mode is entered with the ADPON bit set to 1, a current will flow.

(8) When reading data from the ADCRn register, read the lower bytes of data.

(9) For the digital filter, a gain of approximately 0.962 is added.

(10) To use the 24-bit ΔΣ-type A/D converter, supply 10 MHz to the extended SFR by setting the clock output selection register (CKS) (see **CHAPTER 11 BUZZER OUTPUT CONTROLLER**).

Cautions 1. Count the INTAD2 signal 1,200 times after the A/D converter is started and then load the converted data when the next INTAD2 signal is generated. The setup time is subject to change. Consult Renesas Electronics before using the setup time.

2. Thoroughly evaluate the stabilization time in the environment in which the A/D converter is used.

Remark n = 0 to 3

CHAPTER 14 SERIAL INTERFACE UART0

14.1 Functions of Serial Interface UART0

Serial interface UART0 is mounted onto all 78K0/Lx3-M microcontroller products.

Serial interface UART0 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.

For details, see **14.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

The functions of this mode are outlined below.

For details, see **14.4.2 Asynchronous serial interface (UART) mode** and **14.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD0: Transmit data output pin
  RxD0: Receive data input pin
- Length of communication data can be selected from 7 or 8 bits.
- Dedicated on-chip 5-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full-duplex operation).
- Fixed to LSB-first communication

Cautions 1. If clock supply to serial interface UART0 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART0 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD0 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER0 = 0, RXE0 = 0, and TXE0 = 0.

2. Set POWER0 = 1 and then set TXE0 = 1 (transmission) or RXE0 = 1 (reception) to start communication.

3. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

4. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

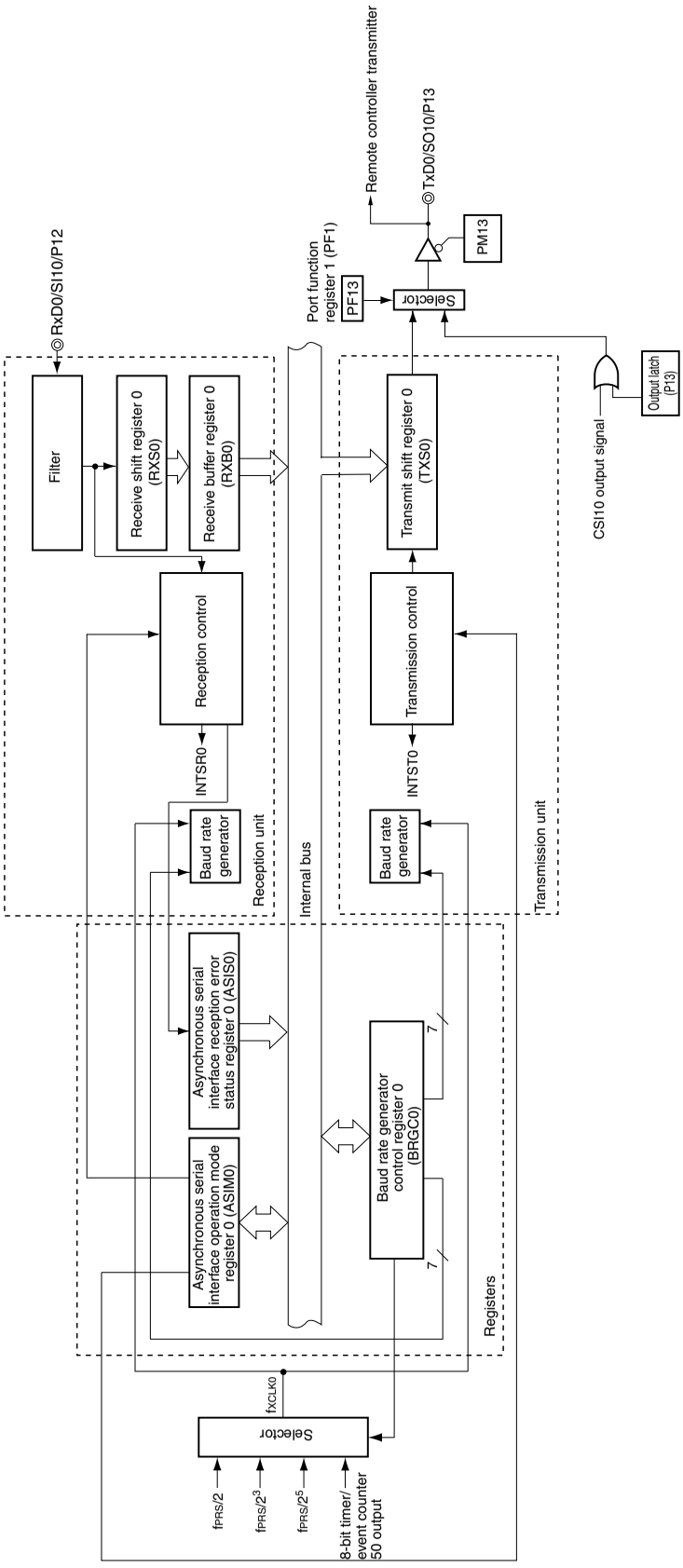
14.2 Configuration of Serial Interface UART0

Serial interface UART0 includes the following hardware.

Table 14-1. Configuration of Serial Interface UART0

Item	Configuration
Registers	Receive buffer register 0 (RXB0) Receive shift register 0 (RXS0) Transmit shift register 0 (TXS0)
Control registers	Asynchronous serial interface operation mode register 0 (ASIM0) Asynchronous serial interface reception error status register 0 (ASIS0) Baud rate generator control register 0 (BRGC0) Port function register 1 (PF1) Port mode register 1 (PM1) Port register 1 (P1)

Figure 14-1. Block Diagram of Serial Interface UART0



(1) Receive buffer register 0 (RXB0)

This 8-bit register stores parallel data converted by receive shift register 0 (RXS0).

Each time 1 byte of data has been received, new receive data is transferred to this register from receive shift register 0 (RXS0).

If the data length is set to 7 bits the receive data is transferred to bits 0 to 6 of RXB0 and the MSB of RXB0 is always 0.

If an overrun error (OVE0) occurs, the receive data is not transferred to RXB0.

RXB0 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation and POWER0 = 0 set this register to FFH.

(2) Receive shift register 0 (RXS0)

This register converts the serial data input to the RxD0 pin into parallel data.

RXS0 cannot be directly manipulated by a program.

(3) Transmit shift register 0 (TXS0)

This register is used to set transmit data. Transmission is started when data is written to TXS0, and serial data is transmitted from the TxD0 pins.

TXS0 can be written by an 8-bit memory manipulation instruction. This register cannot be read.

Reset signal generation, POWER0 = 0, and TXE0 = 0 set this register to FFH.

Cautions 1. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

2. Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.

14.3 Registers Controlling Serial Interface UART0

Serial interface UART0 is controlled by the following six registers.

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)

(1) Asynchronous serial interface operation mode register 0 (ASIM0)

This 8-bit register controls the serial communication operations of serial interface UART0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (1/2)

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock.

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission.

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception.

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (2/2)

PS01	PS00	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL0	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL0	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE0) of asynchronous serial interface reception error status register 0 (ASIS0) is not set and the error interrupt does not occur.

Cautions 1. To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.

2. To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.

3. Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.

4. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

6. Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.

7. Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.

8. Be sure to set bit 0 to 1.

(2) Asynchronous serial interface reception error status register 0 (ASIS0)

This register indicates an error status on completion of reception by serial interface UART0. It includes three error flag bits (PE0, FE0, OVE0).

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER0) or bit 5 (RXE0) of ASIM0 to 0 clears this register to 00H. 00H is read when this register is read. If a reception error occurs, read ASIS0 and then read receive buffer register 0 (RXB0) to clear the error flag.

Figure 14-3. Format of Asynchronous Serial Interface Reception Error Status Register 0 (ASIS0)

Address: FF73H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS0	0	0	0	0	0	PE0	FE0	OVE0

PE0	Status flag indicating parity error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the parity of transmit data does not match the parity bit on completion of reception.

FE0	Status flag indicating framing error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the stop bit is not detected on completion of reception.

OVE0	Status flag indicating overrun error
0	If POWER0 = 0 and RXE0 = 0, or if ASIS0 register is read.
1	If receive data is set to the RXB0 register and the next reception operation is completed before the data is read.

Cautions 1. The operation of the PE0 bit differs depending on the set values of the PS01 and PS00 bits of asynchronous serial interface operation mode register 0 (ASIM0).

2. Only the first bit of the receive data is checked as the stop bit, regardless of the number of stop bits.

3. If an overrun error occurs, the next receive data is not written to receive buffer register 0 (RXB0) but discarded.

4. If data is read from ASIS0, a wait cycle is generated. Do not read data from ASIS0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(3) Baud rate generator control register 0 (BRGC0)

This register selects the base clock of serial interface UART0 and the division value of the 5-bit counter.

BRGC0 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 1FH.

Figure 14-4. Format of Baud Rate Generator Control Register 0 (BRGC0)

Address: FF71H After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC0	TPS01	TPS00	0	MDL04	MDL03	MDL02	MDL01	MDL00

TPS01	TPS00	Base clock (f_{XCLK0}) selection[Note 1]				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	TM50 output[Note 2]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz

MDL04	MDL03	MDL02	MDL01	MDL00	k	Selection of 5-bit counter output clock
0	0	×	×	×	×	Setting prohibited
0	1	0	0	0	8	$f_{XCLK0}/8$
0	1	0	0	1	9	$f_{XCLK0}/9$
0	1	0	1	0	10	$f_{XCLK0}/10$
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	0	1	0	26	$f_{XCLK0}/26$
1	1	0	1	1	27	$f_{XCLK0}/27$
1	1	1	0	0	28	$f_{XCLK0}/28$
1	1	1	0	1	29	$f_{XCLK0}/29$
1	1	1	1	0	30	$f_{XCLK0}/30$
1	1	1	1	1	31	$f_{XCLK0}/31$

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

Notes 2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.
  It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. Make sure that bit 6 (TXE0) and bit 5 (RXE0) of the ASIM0 register = 0 when rewriting the MDL04 to MDL00 bits.

2. Make sure that bit 7 (POWER0) of the ASIM0 register = 0 when rewriting the TPS01 and TPS00 bits.

3. The baud rate value is the output clock of the 5-bit counter divided by 2.

Remarks 1. f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits

2. f_{PRS}: Peripheral hardware clock frequency

3. k: Value set by the MDL04 to MDL00 bits (k = 8, 9, 10, ..., 31)

4. ×: Don't care

5. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

(4) Port function register 1 (PF1)

This register sets the pin functions of P13/TxD0 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 14-5. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	0	0	0	PF13	0	0	0

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

(5) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P13/TxD0 pin for serial interface data output, clear PM13 to 0. The output latch of P13 at this time may be 0 or 1.

When using the P12/RxD0 pin for serial interface data input, set PM12 to 1. The output latch of P12 at this time may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 14-6. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	1	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 4, 6, and 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

14.4 Operation of Serial Interface UART0

Serial interface UART0 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

14.4.1 Operation stop mode

In this mode, serial communication cannot be executed, thus reducing the power consumption. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER0, TXE0, and RXE0) of ASIM0 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 0 (ASIM0).

ASIM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Caution Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.

Remark To use the RxD0/P12 and TxD0/P13 pins as general-purpose port pins, see **CHAPTER 4 PORT FUNCTIONS**.

14.4.2 Asynchronous serial interface (UART) mode

In this mode, 1-byte data is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port mode register 1 (PM1)
- Port register 1 (P1)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the BRGC0 register (see **Figure 14-4**).
<2> Set bits 1 to 4 (SL0, CL0, PS00, and PS01) of the ASIM0 register (see **Figure 14-2**).
<3> Set bit 7 (POWER0) of the ASIM0 register to 1.
<4> Set bit 6 (TXE0) of the ASIM0 register to 1. → Transmission is enabled.
Set bit 5 (RXE0) of the ASIM0 register to 1. → Reception is enabled.
<5> Write data to the TXS0 register. → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 14-2. Relationship Between Register Settings and Pins

POWER0	TXE0	RXE0	PM13	P13	PM12	P12	UART0 Operation	Pin Function	
								TxD0/SO10/P13	RxD0/SI10/P12
0	0	0	×Note	×Note	×Note	×Note	Stop	SO10/P13	SI10/P12
1	0	1	×Note	×Note	1	×	Reception	SO10/P13	RxD0
	1	0	0	×	×Note	×Note	Transmission	TxD0	SI10/P12
	1	1	0	×	1	×	Transmission/ reception	TxD0	RxD0

Note Can be set as port function or serial interface CSI10.

Remarks 1. ×: don't care
POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
PM1×: Port mode register
P1×: Port output latch

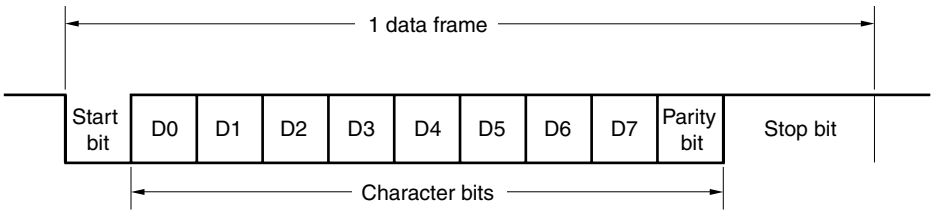
2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

Figure 14-7 and Figure 14-8 show the format and waveform examples of the normal transmit/receive data.

Figure 14-7. Format of Normal UART Transmit/Receive Data



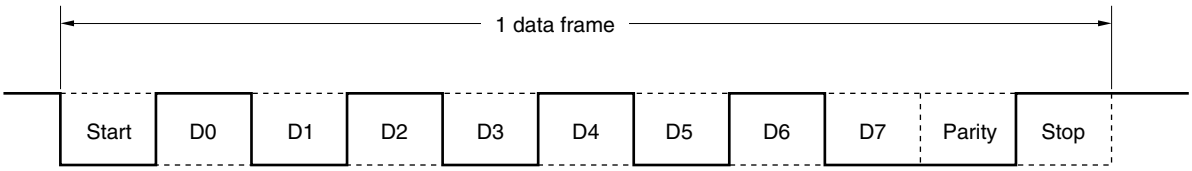
One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits (LSB first)
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

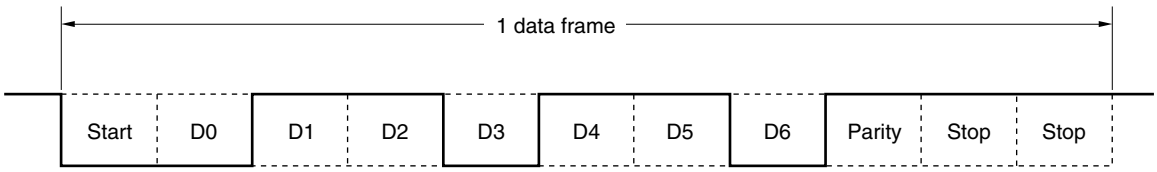
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 0 (ASIM0).

Figure 14-8. Example of Normal UART Transmit/Receive Data Waveform

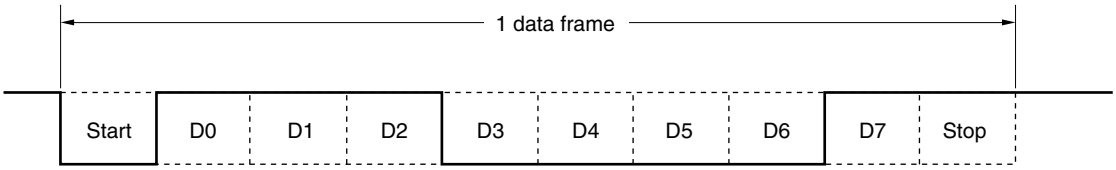
1. Data length: 8 bits, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



2. Data length: 7 bits, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



3. Data length: 8 bits, Parity: None, Stop bit: 1 bit, Communication data: 87H



(b) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmission and reception sides. With even parity and odd parity, a 1-bit (odd number) error can be detected. With zero parity and no parity, an error cannot be detected.

(i) Even parity

- Transmission

  Transmit data, including the parity bit, is controlled so that the number of bits that are "1" is even.
  The value of the parity bit is as follows.

  If transmit data has an odd number of bits that are "1": 1
  If transmit data has an even number of bits that are "1": 0

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is odd, a parity error occurs.

(ii) Odd parity

- Transmission

  Unlike even parity, transmit data, including the parity bit, is controlled so that the number of bits that are "1" is odd.

  If transmit data has an odd number of bits that are "1": 0
  If transmit data has an even number of bits that are "1": 1

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is even, a parity error occurs.

(iii) 0 parity

The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.
The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is "0" or "1".

(iv) No parity

No parity bit is appended to the transmit data.
Reception is performed assuming that there is no parity bit when data is received. Because there is no parity bit, a parity error does not occur.

(c) Transmission

If bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is set to 1 and bit 6 (TXE0) of ASIM0 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit shift register 0 (TXS0). The start bit, parity bit, and stop bit are automatically appended to the data.

When transmission is started, the start bit is output from the TxD0 pin, and the transmit data is output followed by the rest of the data in order starting from the LSB. When transmission is completed, the parity and stop bits set by ASIM0 are appended and a transmission completion interrupt request (INTST0) is generated.

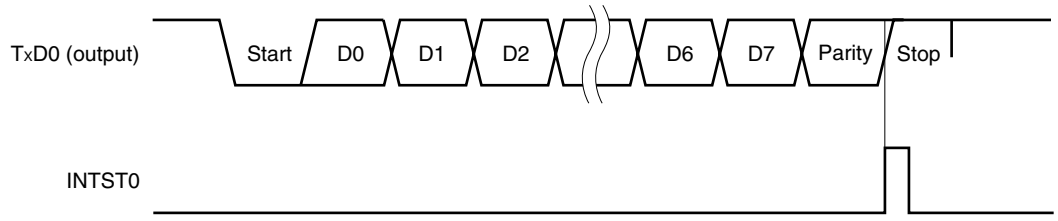
Transmission is stopped until the data to be transmitted next is written to TXS0.

Figure 14-9 shows the timing of the transmission completion interrupt request (INTST0). This interrupt occurs as soon as the last stop bit has been output.

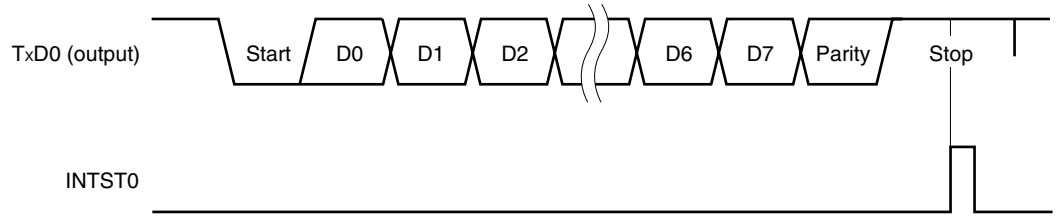
Caution After transmit data is written to TXS0, do not write the next transmit data before the transmission completion interrupt signal (INTST0) is generated.

Figure 14-9. Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2



(d) Reception

Reception is enabled and the RxD0 pin input is sampled when bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is set to 1 and then bit 5 (RXE0) of ASIM0 is set to 1.

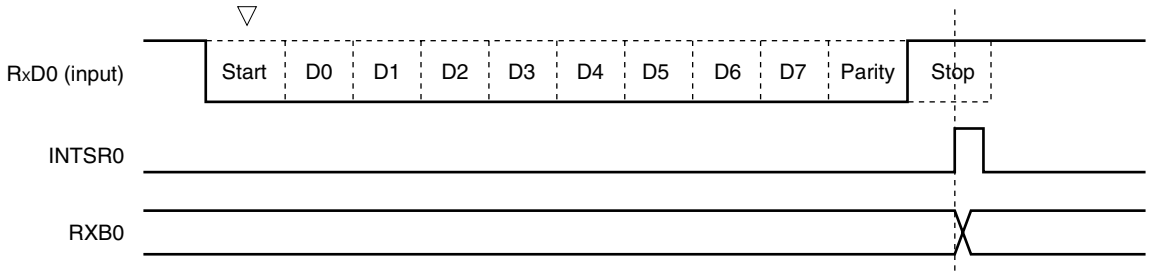
The 5-bit counter of the baud rate generator starts counting when the falling edge of the RxD0 pin input is detected. When the set value of baud rate generator control register 0 (BRGC0) has been counted, the RxD0 pin input is sampled again (▽ in Figure 14-10). If the RxD0 pin is low level at this time, it is recognized as a start bit.

When the start bit is detected, reception is started, and serial data is sequentially stored in receive shift register 0 (RXS0) at the set baud rate. When the stop bit has been received, the reception completion interrupt (INTSR0) is generated and the data of RXS0 is written to receive buffer register 0 (RXB0). If an overrun error (OVE0) occurs, however, the receive data is not written to RXB0.

Even if a parity error (PE0) occurs while reception is in progress, reception continues to the reception position of the stop bit, and an reception error interrupt (INTSR0) is generated after completion of reception.

INTSR0 occurs upon completion of reception and in case of a reception error.

Figure 14-10. Reception Completion Interrupt Request Timing



Cautions 1. If a reception error occurs, read asynchronous serial interface reception error status register 0 (ASIS0) and then read receive buffer register 0 (RXB0) to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.

2. Reception is always performed with the "number of stop bits = 1". The second stop bit is ignored.

(e) Reception error

Three types of errors may occur during reception: a parity error, framing error, or overrun error. If the error flag of asynchronous serial interface reception error status register 0 (ASIS0) is set as a result of data reception, a reception error interrupt (INTSR0) is generated.

Which error has occurred during reception can be identified by reading the contents of ASIS0 in the reception error interrupt (INTSR0) servicing (see **Figure 14-3**).

The contents of ASIS0 are cleared to 0 when ASIS0 is read.

Table 14-3. Cause of Reception Error

Reception Error	Cause
Parity error	The parity specified for transmission does not match the parity of the receive data.
Framing error	Stop bit is not detected.
Overrun error	Reception of the next data is completed before data is read from receive buffer register 0 (RXB0).

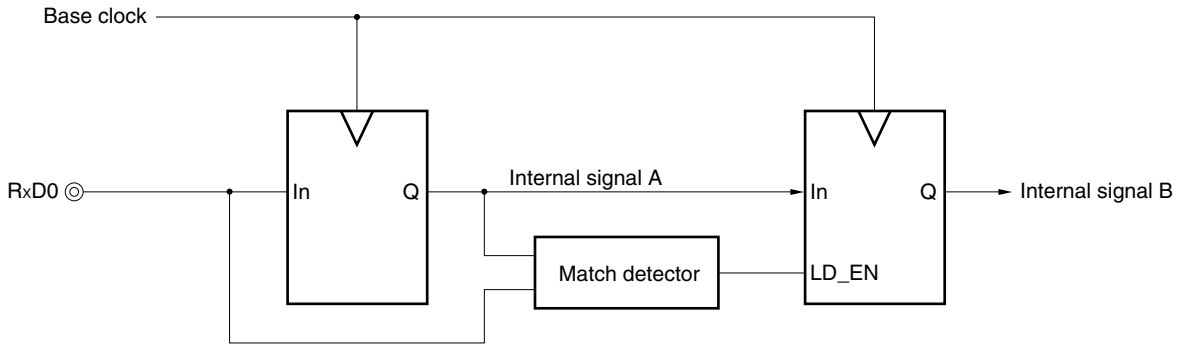
(f) Noise filter of receive data

The RxD0 signal is sampled using the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 14-11, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 14-11. Noise Filter Circuit



14.4.3 Dedicated baud rate generator

The dedicated baud rate generator consists of a source clock selector and a 5-bit programmable counter, and generates a serial clock for transmission/reception of UART0.

Separate 5-bit counters are provided for transmission and reception.

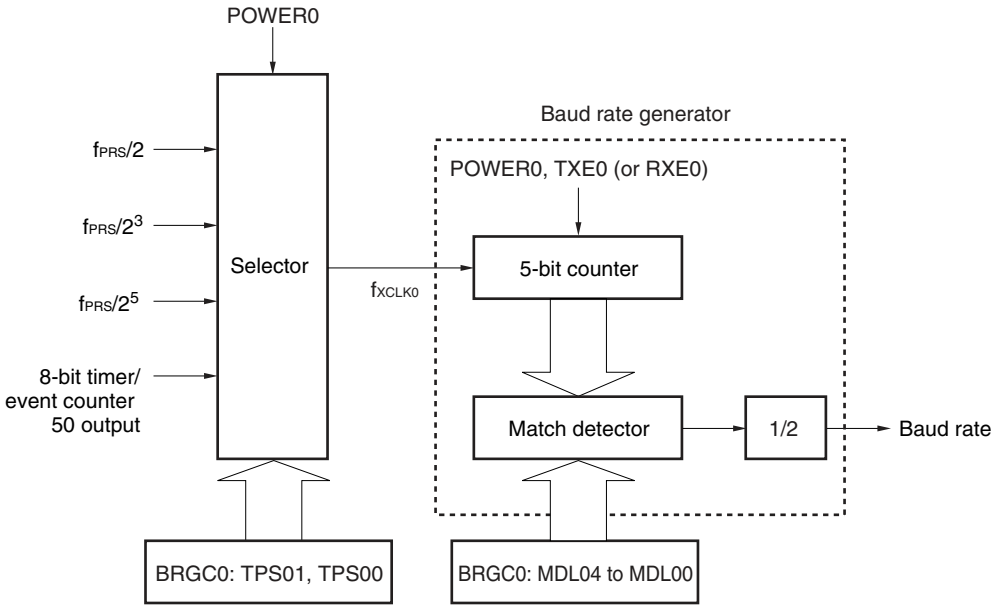
(1) Configuration of baud rate generator

- Base clock
  The clock selected by bits 7 and 6 (TPS01 and TPS00) of baud rate generator control register 0 (BRGC0) is supplied to each module when bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is 1. This clock is called the base clock and its frequency is called f_{XCLK0}. The base clock is fixed to low level when POWER0 = 0.

- Transmission counter
  This counter stops operation, cleared to 0, when bit 7 (POWER0) or bit 6 (TXE0) of asynchronous serial interface operation mode register 0 (ASIM0) is 0.
  It starts counting when POWER0 = 1 and TXE0 = 1.
  The counter is cleared to 0 when the first data transmitted is written to transmit shift register 0 (TXS0).

- Reception counter
  This counter stops operation, cleared to 0, when bit 7 (POWER0) or bit 5 (RXE0) of asynchronous serial interface operation mode register 0 (ASIM0) is 0.
  It starts counting when the start bit has been detected.
  The counter stops operation after one frame has been received, until the next start bit is detected.

Figure 14-12. Configuration of Baud Rate Generator



Remark POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
BRGC0: Baud rate generator control register 0

(2) Generation of serial clock

A serial clock to be generated can be specified by using baud rate generator control register 0 (BRGC0).

Select the clock to be input to the 5-bit counter by using bits 7 and 6 (TPS01 and TPS00) of BRGC0.

Bits 4 to 0 (MDL04 to MDL00) of BRGC0 can be used to select the division value (f_{XCLK0}/8 to f_{XCLK0}/31) of the 5-bit counter.

14.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK0}}{2 \times k}$ [bps]

f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits of the BRGC0 register

k: Value set by the MDL04 to MDL00 bits of the BRGC0 register (k = 8, 9, 10, ..., 31)

Table 14-4. Set Value of TPS01 and TPS00

TPS01	TPS00	Base clock (f_{XCLK0}) selection[Note 1]				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	TM50 output[Note 2]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- Error (%) = $\left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1\right) \times 100$ [%]

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 2.5 MHz = 2,500,000 Hz
Set value of MDL04 to MDL00 bits of BRGC0 register = 10000B (k = 16)
Target baud rate = 76,800 bps

Baud rate = 2.5 M/(2 × 16)
= 2,500,000/(2 × 16) = 78,125 [bps]

Error = (78,125/76,800 − 1) × 100
= 1.725 [%]

(3) Example of setting baud rate

Table 14-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz			
	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]
1200	3H	26	1202	0.16	–	–	–	–	–	–	–	–
2400	3H	13	2404	0.16	–	–	–	–	–	–	–	–
4800	2H	26	4808	0.16	3H	16	4883	1.73	–	–	–	–
9600	2H	13	9615	0.16	3H	8	9766	1.73	3H	16	9766	1.73
10400	2H	12	10417	0.16	2H	30	10417	0.16	3H	15	10417	0.16
19200	1H	26	19231	0.16	2H	16	19531	1.73	3H	8	19531	1.73
24000	1H	21	23810	−0.79	2H	13	24038	0.16	2H	26	24038	0.16
31250	1H	16	31250	0	2H	10	31250	0	2H	20	31250	0
33600	1H	15	33333	−0.79	2H	9	34722	3.34	2H	19	32895	−2.1
38400	1H	13	38462	0.16	2H	8	39063	1.73	2H	16	39063	1.73
56000	1H	9	55556	−0.79	1H	22	56818	1.46	2H	11	56818	1.46
62500	1H	8	62500	0	1H	20	62500	0	2H	10	62500	0
76800	–	–	–	–	1H	16	78125	1.73	2H	8	78125	1.73
115200	–	–	–	–	1H	11	113636	−1.36	1H	22	113636	−1.36
153600	–	–	–	–	1H	8	156250	1.73	1H	16	156250	1.73
312500	–	–	–	–	–	–	–	–	1H	8	312500	0

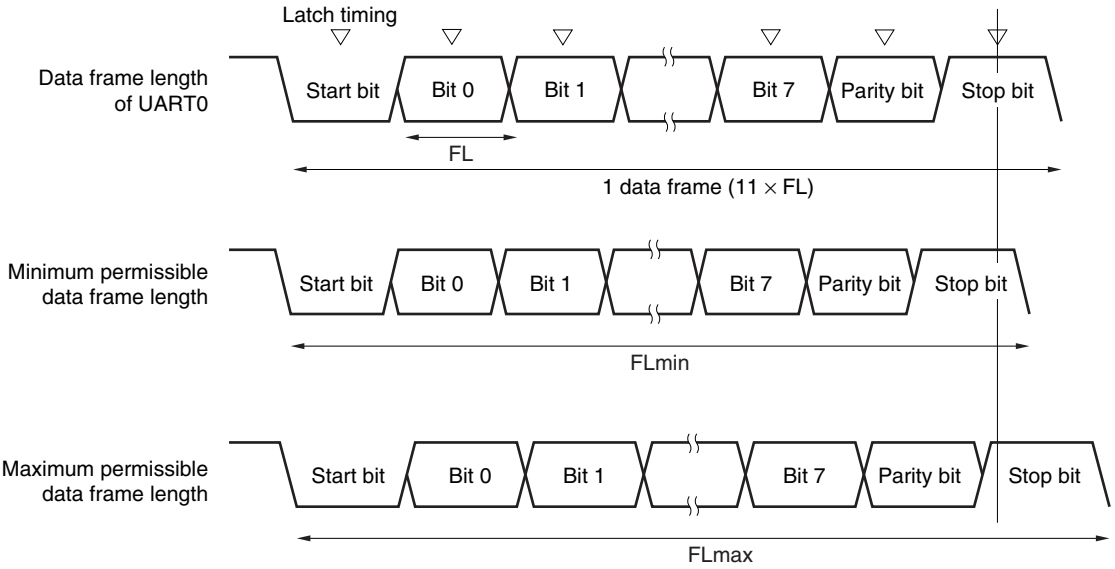
Remark TPS01, TPS00: Bits 7 and 6 of baud rate generator control register 0 (BRGC0) (setting of base clock (f_{XCLK0}))
k: Value set by the MDL04 to MDL00 bits of BRGC0 (k = 8, 9, 10, ..., 31)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 14-13. Permissible Baud Rate Range During Reception



As shown in Figure 14-13, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0
k: Set value of BRGC0
FL: 1-bit data length
Margin of latch timing: 2 clocks

Minimum permissible data frame length: $FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$

Therefore, the maximum receivable baud rate at the transmission destination is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k+2} Brate$$

Similarly, the maximum permissible data frame length can be calculated as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k+2}{2 \times k} \times FL = \frac{21k-2}{2 \times k} FL$$

$$FLmax = \frac{21k-2}{20k} FL \times 11$$

Therefore, the minimum receivable baud rate at the transmission destination is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k-2} Brate$$

The permissible baud rate error between UART0 and the transmission destination can be calculated from the above minimum and maximum baud rate expressions, as follows.

Table 14-6. Maximum/Minimum Permissible Baud Rate Error

Division Ratio (k)	Maximum Permissible Baud Rate Error	Minimum Permissible Baud Rate Error
8	+3.53%	–3.61%
16	+4.14%	–4.19%
24	+4.34%	–4.38%
31	+4.44%	–4.47%

Remarks 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the higher the division ratio (k), the higher the permissible error.

2. k: Set value of BRGC0

CHAPTER 15 SERIAL INTERFACE UART6

15.1 Functions of Serial Interface UART6

Serial interface UART6 is mounted onto all 78K0/Lx3-M microcontroller products.
Serial interface UART6 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.
For details, see **15.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

This mode supports the LIN (Local Interconnect Network)-bus. The functions of this mode are outlined below.
For details, see **15.4.2 Asynchronous serial interface (UART) mode** and **15.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD6: Transmit data output pin
  RxD6: Receive data input pin
- Data length of communication data can be selected from 7 or 8 bits
- Dedicated internal 8-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full duplex operation)
- MSB- or LSB-first communication selectable
- Inverted transmission operation
- Sync break field transmission from 13 to 20 bits
- More than 11 bits can be identified for sync break field reception (SBF reception flag provided)

Cautions 1. The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.

2. If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.

3. Set POWER6 = 1 and then set TXE6 = 1 (transmission) or RXE6 = 1 (reception) to start communication.

4. TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.

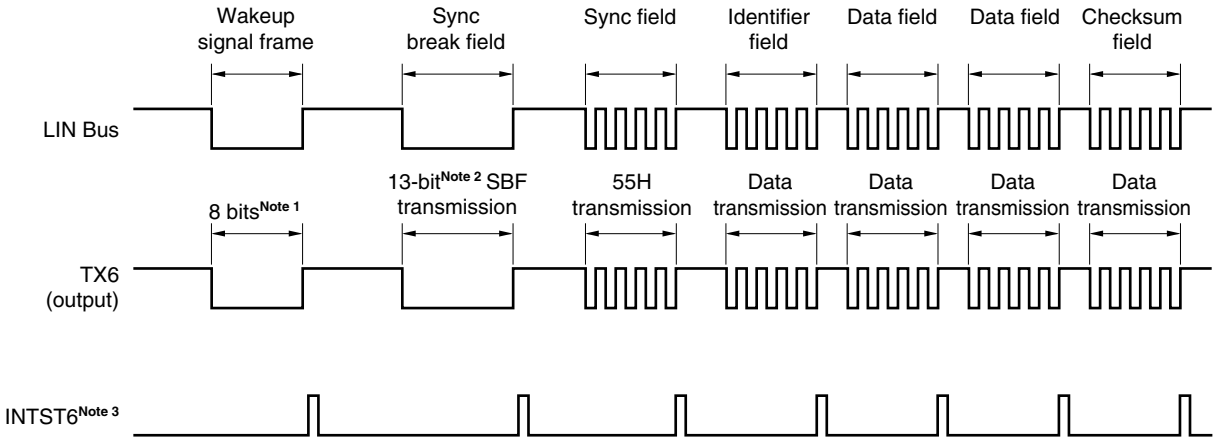
5. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

6. If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface is used in LIN communication operation.

Remark LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol intended to aid the cost reduction of an automotive network.
LIN communication is single-master communication, and up to 15 slaves can be connected to one master.
The LIN slaves are used to control the switches, actuators, and sensors, and these are connected to the LIN master via the LIN network.
Normally, the LIN master is connected to a network such as CAN (Controller Area Network).
In addition, the LIN bus uses a single-wire method and is connected to the nodes via a transceiver that complies with ISO9141.
In the LIN protocol, the master transmits a frame with baud rate information and the slave receives it and corrects the baud rate error. Therefore, communication is possible when the baud rate error in the slave is ±15% or less.

Figure 15-1 and Figure 15-2 outline the transmission and reception operations of LIN.

Figure 15-1. LIN Transmission Operation



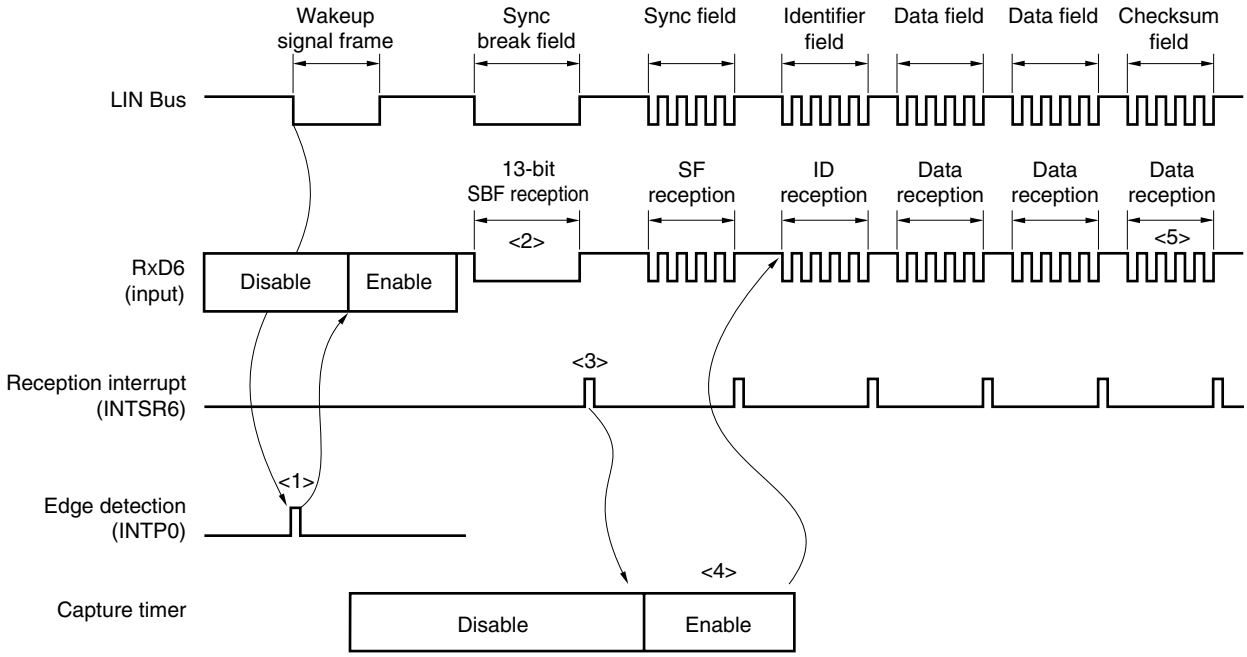
Notes 1. The wakeup signal frame is substituted by 80H transmission in the 8-bit mode.

2. The sync break field is output by hardware. The output width is the bit length set by bits 4 to 2 (SBL62 to SBL60) of asynchronous serial interface control register 6 (ASICL6) (see **15.4.2 (2) (h) SBF transmission**).

3. INTST6 is output on completion of each transmission. It is also output when SBF is transmitted.

Remark The interval between each field is controlled by software.

Figure 15-2. LIN Reception Operation



Reception processing is as follows.

<1> The wakeup signal is detected at the edge of the pin, and enables UART6 and sets the SBF reception mode.

<2> Reception continues until the STOP bit is detected. When an SBF with low-level data of 11 bits or more has been detected, it is assumed that SBF reception has been completed correctly, and an interrupt signal is output. If an SBF with low-level data of less than 11 bits has been detected, it is assumed that an SBF reception error has occurred. The interrupt signal is not output and the SBF reception mode is restored.

<3> If SBF reception has been completed correctly, an interrupt signal is output. Start 16-bit timer/event counter 00 by the SBF reception end interrupt servicing and measure the bit interval (pulse width) of the sync field (see **6.4.5 Pulse width measurement operation**). Detection of errors OVE6, PE6, and FE6 is suppressed, and error detection processing of UART communication and data transfer of the shift register and RXB6 is not performed. The shift register holds the reset value FFH.

<4> Calculate the baud rate error from the bit interval of the sync field, disable UART6 after SF reception, and then re-set baud rate generator control register 6 (BRGC6).

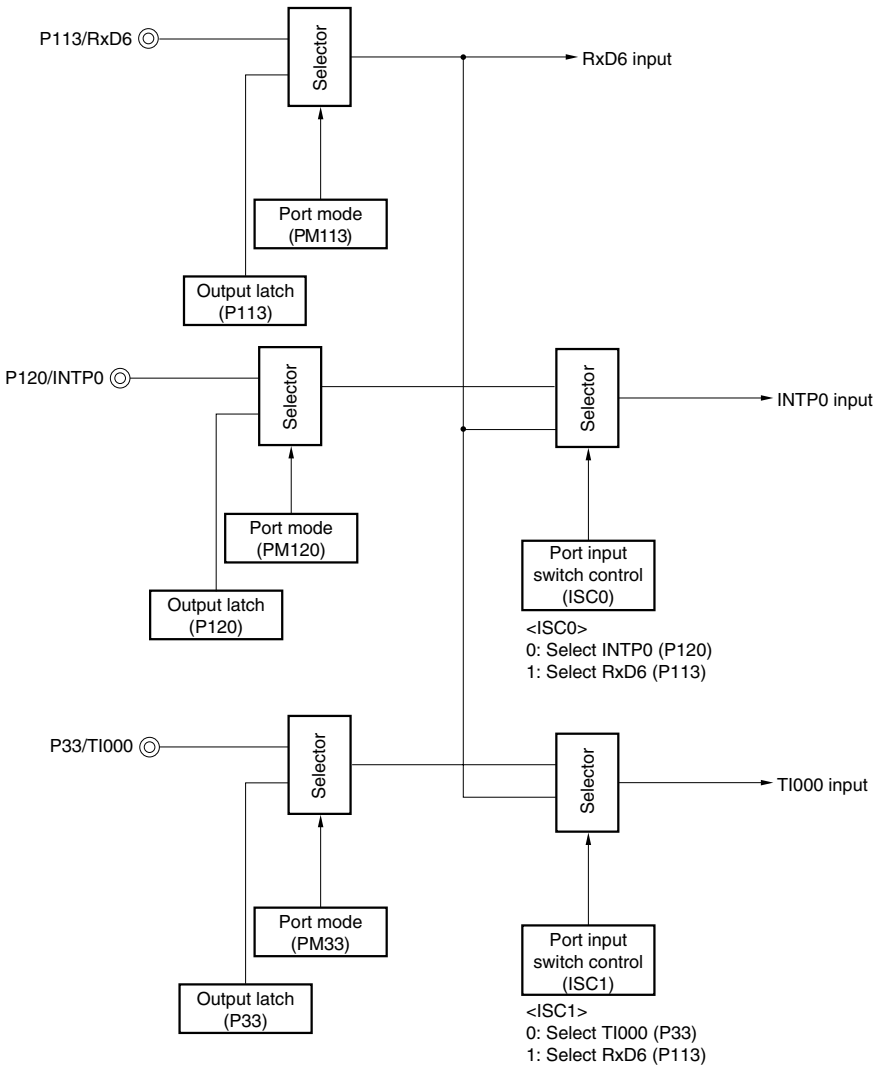
<5> Distinguish the checksum field by software. Also perform processing by software to initialize UART6 after reception of the checksum field and to set the SBF reception mode again.

Figure 15-3 shows the port configuration for LIN reception operation.

The wakeup signal transmitted from the LIN master is received by detecting the edge of the external interrupt (INTP0). The length of the sync field transmitted from the LIN master can be measured using the external event capture operation of 16-bit timer/event counter 00, and the baud rate error can be calculated.

The input source of the reception port input (RxD6) can be input to the external interrupt (INTP0) and 16-bit timer/event counter 00 by port input switch control (ISC0/ISC1), without connecting RxD6 and INTP0/TI000 externally.

Figure 15-3. Port Configuration for LIN Reception Operation



Remark ISC0 and ISC1: Bits 0 and 1 of the input switch control register (ISC) (see **Figure 15-11**)

The peripheral functions used in the LIN communication operation are shown below.

<Peripheral functions used>

- External interrupt (INTP0); wakeup signal detection
  Use: Detects the wakeup signal edges and detects start of communication.
- 16-bit timer/event counter 00 (TI000); baud rate error detection
  Use: Detects the baud rate error (measures the TI000 input edge interval in the capture mode) by detecting the sync field (SF) length and divides it by the number of bits.
- Serial interface UART6

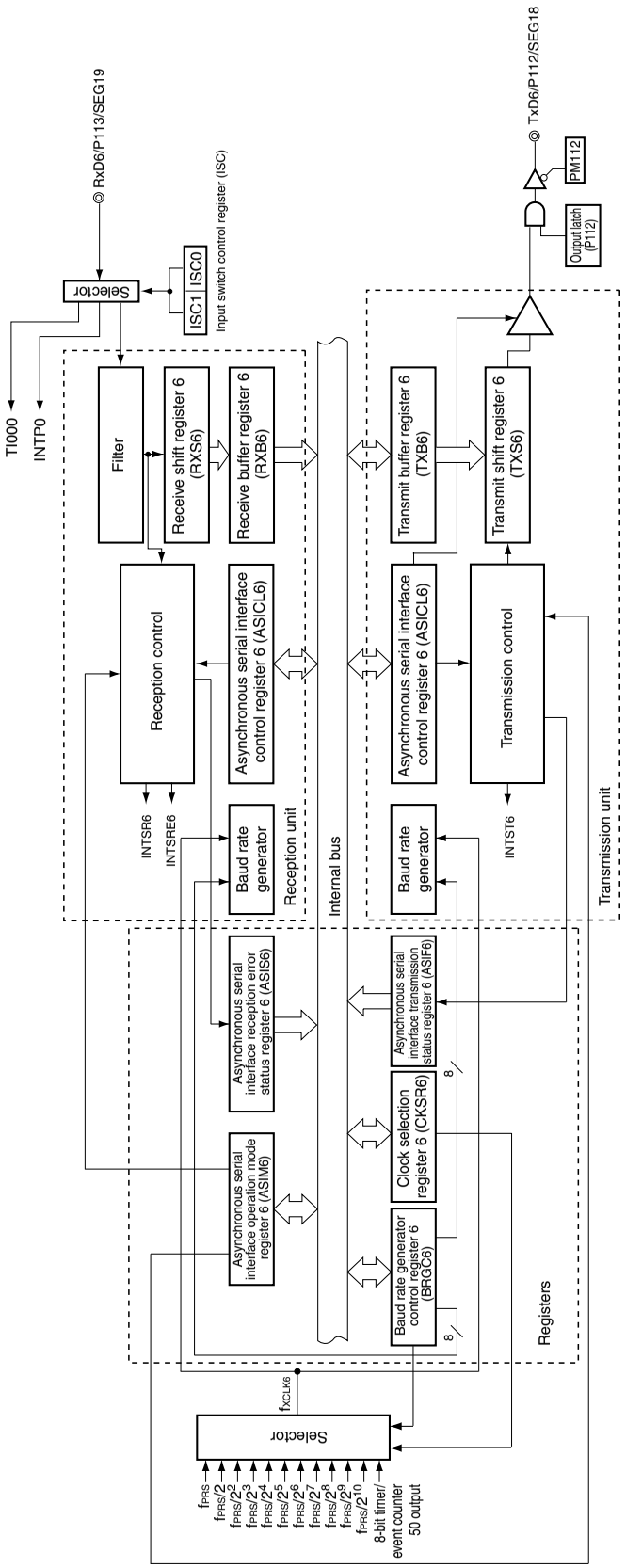
15.2 Configuration of Serial Interface UART6

Serial interface UART6 includes the following hardware.

Table 15-1. Configuration of Serial Interface UART6

Item	Configuration
Registers	Receive buffer register 6 (RXB6) Receive shift register 6 (RXS6) Transmit buffer register 6 (TXB6) Transmit shift register 6 (TXS6)
Control registers	Asynchronous serial interface operation mode register 6 (ASIM6) Asynchronous serial interface reception error status register 6 (ASIS6) Asynchronous serial interface transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) Asynchronous serial interface control register 6 (ASICL6) Input switch control register (ISC) Port mode register 11 (PM11) Port register 11 (P11)

Figure 15-4. Block Diagram of Serial Interface UART6



(1) Receive buffer register 6 (RXB6)

This 8-bit register stores parallel data converted by receive shift register 6 (RXS6).

Each time 1 byte of data has been received, new receive data is transferred to this register from RXS6. If the data length is set to 7 bits, data is transferred as follows.

- In LSB-first reception, the receive data is transferred to bits 0 to 6 of RXB6 and the MSB of RXB6 is always 0.
- In MSB-first reception, the receive data is transferred to bits 1 to 7 of RXB6 and the LSB of RXB6 is always 0.

If an overrun error (OVE6) occurs, the receive data is not transferred to RXB6.

RXB6 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation sets this register to FFH.

(2) Receive shift register 6 (RXS6)

This register converts the serial data input to the RxD6 pin into parallel data.

RXS6 cannot be directly manipulated by a program.

(3) Transmit buffer register 6 (TXB6)

This buffer register is used to set transmit data. Transmission is started when data is written to TXB6.

This register can be read or written by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Cautions 1. Do not write data to TXB6 when bit 1 (TXBF6) of asynchronous serial interface transmission status register 6 (ASIF6) is 1.

2. Do not refresh (write the same value to) TXB6 by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) are 1 or when bits 7 and 5 (POWER6, RXE6) of ASIM6 are 1).

3. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

(4) Transmit shift register 6 (TXS6)

This register transmits the data transferred from TXB6 from the TxD6 pin as serial data. Data is transferred from TXB6 immediately after TXB6 is written for the first transmission, or immediately before INTST6 occurs after one frame was transmitted for continuous transmission. Data is transferred from TXB6 and transmitted from the TxD6 pin at the falling edge of the base clock.

TXS6 cannot be directly manipulated by a program.

15.3 Registers Controlling Serial Interface UART6

Serial interface UART6 is controlled by the following nine registers.

- Asynchronous serial interface operation mode register 6 (ASIM6)
- Asynchronous serial interface reception error status register 6 (ASIS6)
- Asynchronous serial interface transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Asynchronous serial interface control register 6 (ASICL6)
- Input switch control register (ISC)
- Port mode register 11 (PM11)
- Port register 11 (P11)

(1) Asynchronous serial interface operation mode register 6 (ASIM6)

This 8-bit register controls the serial communication operations of serial interface UART6.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Remark ASIM6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (1/2)

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock

TXE6	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission

RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception

Notes 1. If POWER6 = 0 is set while transmitting data, the output of the TxD6 pin will be fixed to high level (if TXDLV6 = 0). Furthermore, the input from the RxD6 pin will be fixed to high level.

2. Asynchronous serial interface reception error status register 6 (ASIS6), asynchronous serial interface transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6), and receive buffer register 6 (RXB6) are reset.

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (2/2)

PS61	PS60	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL6	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL6	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

ISRM6	Enables/disables occurrence of reception completion interrupt in case of error
0	“INTSRE6” occurs in case of error (at this time, INTSR6 does not occur).
1	“INTSR6” occurs in case of error (at this time, INTSRE6 does not occur).

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE6) of asynchronous serial interface reception error status register 6 (ASIS6) is not set and the error interrupt does not occur.

Cautions
1. **To start the transmission, set POWER6 to 1 and then set TXE6 to 1. To stop the transmission, clear TXE6 to 0, and then clear POWER6 to 0.**
2. **To start the reception, set POWER6 to 1 and then set RXE6 to 1. To stop the reception, clear RXE6 to 0, and then clear POWER6 to 0.**
3. **Set POWER6 to 1 and then set RXE6 to 1 while a high level is input to the RxD6 pin. If POWER6 is set to 1 and RXE6 is set to 1 while a low level is input, reception is started.**
4. **TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.**
5. **Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.**
6. **Clear the TXE6 and RXE6 bits to 0 before rewriting the PS61, PS60, and CL6 bits.**
7. **Fix the PS61 and PS60 bits to 0 when used in LIN communication operation.**
8. **Clear TXE6 to 0 before rewriting the SL6 bit. Reception is always performed with “the number of stop bits = 1”, and therefore, is not affected by the set value of the SL6 bit.**
9. **Make sure that RXE6 = 0 when rewriting the ISRM6 bit.**

(2) Asynchronous serial interface reception error status register 6 (ASIS6)

This register indicates an error status on completion of reception by serial interface UART6. It includes three error flag bits (PE6, FE6, OVE6).

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 5 (RXE6) of ASIM6 to 0 clears this register to 00H. 00H is read when this register is read. If a reception error occurs, read ASIS6 and then read receive buffer register 6 (RXB6) to clear the error flag.

Figure 15-6. Format of Asynchronous Serial Interface Reception Error Status Register 6 (ASIS6)

Address: FF53H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS6	0	0	0	0	0	PE6	FE6	OVE6

PE6	Status flag indicating parity error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the parity of transmit data does not match the parity bit on completion of reception

FE6	Status flag indicating framing error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the stop bit is not detected on completion of reception

OVE6	Status flag indicating overrun error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If receive data is set to the RXB6 register and the next reception operation is completed before the data is read.

Cautions 1. The operation of the PE6 bit differs depending on the set values of the PS61 and PS60 bits of asynchronous serial interface operation mode register 6 (ASIM6).

2. For the stop bit of the receive data, only the first stop bit is checked regardless of the number of stop bits.

3. If an overrun error occurs, the next receive data is not written to receive buffer register 6 (RXB6) but discarded.

4. If data is read from ASIS6, a wait cycle is generated. Do not read data from ASIS6 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 35 CAUTIONS FOR WAIT.

(3) Asynchronous serial interface transmission status register 6 (ASIF6)

This register indicates the status of transmission by serial interface UART6. It includes two status flag bits (TXBF6 and TXSF6).

Transmission can be continued without disruption even during an interrupt period, by writing the next data to the TXB6 register after data has been transferred from the TXB6 register to the TXS6 register.

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 6 (TXE6) of ASIM6 to 0 clears this register to 00H.

Figure 15-7. Format of Asynchronous Serial Interface Transmission Status Register 6 (ASIF6)

Address: FF55H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIF6	0	0	0	0	0	0	TXBF6	TXSF6

TXBF6	Transmit buffer data flag
0	If POWER6 = 0 or TXE6 = 0, or if data is transferred to transmit shift register 6 (TXS6)
1	If data is written to transmit buffer register 6 (TXB6) (if data exists in TXB6)

TXSF6	Transmit shift register data flag
0	If POWER6 = 0 or TXE6 = 0, or if the next data is not transferred from transmit buffer register 6 (TXB6) after completion of transfer
1	If data is transferred from transmit buffer register 6 (TXB6) (if data transmission is in progress)

Cautions 1. To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is "0". If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is "1", the transmit data cannot be guaranteed.

2. To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is "0" after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is "1", the transmit data cannot be guaranteed.

(4) Clock selection register 6 (CKSR6)

This register selects the base clock of serial interface UART6.

CKSR6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Remark CKSR6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-8. Format of Clock Selection Register 6 (CKSR6)

Address: FF56H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60

TPS63	TPS62	TPS61	TPS60	Base clock (f_{XCLK6}) selection[Note 1]				
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	8 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	500 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	125 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	62.5 kHz	78.13 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	31.25 kHz	39.06 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	15.625 kHz	19.53 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	7.513 kHz	9.77 kHz
1	0	1	1	TM50 output[Note 3]				
Other than above				Setting prohibited				

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of TPS63 = TPS62 = TPS61 = TPS60 = 0 (base clock: f_{PRS}) is prohibited.

3. Note the following points when selecting the TM50 output as the base clock.
- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Caution Make sure POWER6 = 0 when rewriting TPS63 to TPS60.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

(5) Baud rate generator control register 6 (BRGC6)

This register sets the division value of the 8-bit counter of serial interface UART6.

BRGC6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark BRGC6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-9. Format of Baud Rate Generator Control Register 6 (BRGC6)

Address: FF57H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60

MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	k	Output clock selection of 8-bit counter
0	0	0	0	0	0	×	×	×	Setting prohibited
0	0	0	0	0	1	0	0	4	$f_{XCLK6}/4$
0	0	0	0	0	1	0	1	5	$f_{XCLK6}/5$
0	0	0	0	0	1	1	0	6	$f_{XCLK6}/6$
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	0	252	$f_{XCLK6}/252$
1	1	1	1	1	1	0	1	253	$f_{XCLK6}/253$
1	1	1	1	1	1	1	0	254	$f_{XCLK6}/254$
1	1	1	1	1	1	1	1	255	$f_{XCLK6}/255$

Cautions 1. Make sure that bit 6 (TXE6) and bit 5 (RXE6) of the ASIM6 register = 0 when rewriting the MDL67 to MDL60 bits.

2. The baud rate is the output clock of the 8-bit counter divided by 2.

Remarks 1. f_{XCLK6}: Frequency of base clock selected by the TPS63 to TPS60 bits of CKSR6 register

2. k: Value set by MDL67 to MDL60 bits (k = 4, 5, 6, ..., 255)

3. ×: Don't care

(6) Asynchronous serial interface control register 6 (ASICL6)

This register controls the serial communication operations of serial interface UART6.

ASICL6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 16H.

Caution ASICL6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1). However, do not set both SBRT6 and SBTT6 to 1 by a refresh operation during SBF reception (SBRT6 = 1) or SBF transmission (until INTST6 occurs since SBTT6 has been set (1)), because it may re-trigger SBF reception or SBF transmission.

Figure 15-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (1/2)

Address: FF58H After reset: 16H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6

SBRF6	SBF reception status flag
0	If POWER6 = 0 and RXE6 = 0 or if SBF reception has been completed correctly
1	SBF reception in progress

SBRT6	SBF reception trigger
0	–
1	SBF reception trigger

SBTT6	SBF transmission trigger
0	–
1	SBF transmission trigger

Note Bit 7 is read-only.

Figure 15-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (2/2)

SBL62	SBL61	SBL60	SBF transmission output width control
1	0	1	SBF is output with 13-bit length.
1	1	0	SBF is output with 14-bit length.
1	1	1	SBF is output with 15-bit length.
0	0	0	SBF is output with 16-bit length.
0	0	1	SBF is output with 17-bit length.
0	1	0	SBF is output with 18-bit length.
0	1	1	SBF is output with 19-bit length.
1	0	0	SBF is output with 20-bit length.

DIR6	First-bit specification
0	MSB
1	LSB

TXDLV6	Enables/disables inverting TxD6 output
0	Normal output of TxD6
1	Inverted output of TxD6

Cautions
1. **In the case of an SBF reception error, the mode returns to the SBF reception mode. The status of the SBRF6 flag is held (1).**
2. **Before setting the SBRT6 bit, make sure that bit 7 (POWER6) and bit 5 (RXE6) of ASIM6 = 1. After setting the SBRT6 bit to 1, do not clear it to 0 before SBF reception is completed (before an interrupt request signal is generated).**
3. **The read value of the SBRT6 bit is always 0. SBRT6 is automatically cleared to 0 after SBF reception has been correctly completed.**
4. **Before setting the SBTT6 bit to 1, make sure that bit 7 (POWER6) and bit 6 (TXE6) of ASIM6 = 1. After setting the SBTT6 bit to 1, do not clear it to 0 before SBF transmission is completed (before an interrupt request signal is generated).**
5. **The read value of the SBTT6 bit is always 0. SBTT6 is automatically cleared to 0 at the end of SBF transmission.**
6. **Do not set the SBRT6 bit to 1 during reception, and do not set the SBTT6 bit to 1 during transmission.**
7. **Before rewriting the DIR6 and TXDLV6 bits, clear the TXE6 and RXE6 bits to 0.**
8. **When the TXDLV6 bit is set to 1 (inverted TxD6 output), the TxD6/P112 pin cannot be used as a general-purpose port, regardless of the settings of POWER6 and TXE6. When using the TxD6/P112 pin as a general-purpose port, clear the TXDLV6 bit to 0 (normal TxD6 output).**

(7) Input switch control register (ISC)

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

By setting ISC3 to 1, the P113/RxD6 pin is enabled for input. When ISC3 is cleared to 0, external input is not acknowledged. Thus, after release of reset, a generation of a through current due to an undetermined input state until an output setting is performed is prevented.

The input switch control register (ISC) is used to receive a status signal transmitted from the master during LIN (Local Interconnect Network) reception.

By setting ISC0 and ISC1 to 1, the input sources of INTP0 and TI000 are switched to input signals from the P15/<RxD6> or P113/RxD6 pin.

Figure 15-11. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	ISC3	0	ISC1	ISC0

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P113)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P113)

Caution When using the P113/RxD6/SEGx pin as the P113 or RxD6 pin, set PF11ALL to 0 and ISC3 to 1, after release of reset.

When using the P113/RxD6/SEGx pin as the SEG19 pin, set PF11ALL to 1 and ISC3 to 0, after release of reset.

(8) Port mode register 11 (PM11)

This register sets port 11 input/output in 1-bit units.

When using the P112/TxD6 pin for serial interface data output, clear PM112 to 0 and set the output latch of P112 to 1.

When using the P113/RxD6 pin for serial interface data input, set PM113 to 1. The output latch of P113 at this time may be 0 or 1.

PM11 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 15-12. Format of Port Mode Register 11 (PM11)

Address: FF2BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM11	1	1	1	1	PM113	PM112	PM111	PM110

PM11n	P11n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

15.4 Operation of Serial Interface UART6

Serial interface UART6 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

15.4.1 Operation stop mode

In this mode, serial communication cannot be executed; therefore, the power consumption can be reduced. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER6, TXE6, and RXE6) of ASIM6 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 6 (ASIM6).

ASIM6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE6	Enables/disables transmission
0	Disables transmission operation (synchronously resets the transmission circuit).

RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. If POWER6 = 0 is set while transmitting data, the output of the TxD6 pin will be fixed to high level (if TXDLV6 = 0). Furthermore, the input from the RxD6 pin will be fixed to high level.

2. Asynchronous serial interface reception error status register 6 (ASIS6), asynchronous serial interface transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6), and receive buffer register 6 (RXB6) are reset.

Caution Clear POWER6 to 0 after clearing TXE6 and RXE6 to 0 to stop the operation.
To start the communication, set POWER6 to 1, and then set TXE6 or RXE6 to 1.

Remark To use the RxD6/P113 and TxD6/P112 pins as general-purpose port pins, see **CHAPTER 4 PORT FUNCTIONS**.

15.4.2 Asynchronous serial interface (UART) mode

In this mode, data of 1 byte is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 6 (ASIM6)
- Asynchronous serial interface reception error status register 6 (ASIS6)
- Asynchronous serial interface transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Asynchronous serial interface control register 6 (ASICL6)
- Input switch control register (ISC)
- Port mode register 11 (PM11)
- Port register 11 (P11)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the CKSR6 register (see **Figure 15-8**).
<2> Set the BRGC6 register (see **Figure 15-9**).
<3> Set bits 0 to 4 (ISRM6, SL6, CL6, PS60, PS61) of the ASIM6 register (see **Figure 15-5**).
<4> Set bits 0 and 1 (TXDLV6, DIR6) of the ASICL6 register (see **Figure 15-10**).
<5> Set bit 7 (POWER6) of the ASIM6 register to 1.
<6> Set bit 6 (TXE6) of the ASIM6 register to 1. → Transmission is enabled.
Set bit 5 (RXE6) of the ASIM6 register to 1. → Reception is enabled.
<7> Write data to transmit buffer register 6 (TXB6). → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 15-2. Relationship Between Register Settings and Pins

POWER6	TXE6	RXE6	PM112	P112	PM113	P113	UART6 Operation	Pin Function	
								TxD6/SEG18/P112	RxD6/SEG19/P113
0	0	0	×Note	×Note	×Note	×Note	Stop	SEG18/P112	SEG19/P113
1	0	1	×Note	×Note	1	×	Reception	SEG18/P112	RxD6
	1	0	0	1	×Note	×Note	Transmission	TxD6	SEG19/P113
	1	1	0	1	1	×	Transmission/ reception	TxD6	RxD6

Note Can be set as port function or segment output.

Remark ×: don't care
POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
PM11×: Port mode register
P11×: Port output latch

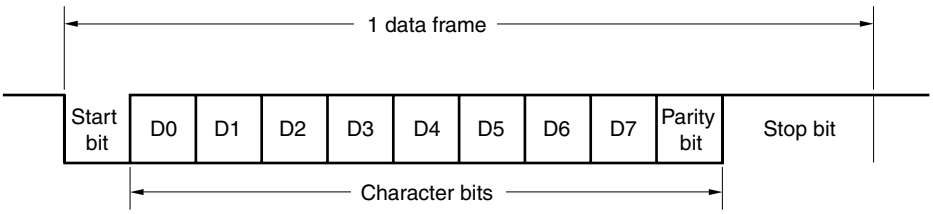
(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

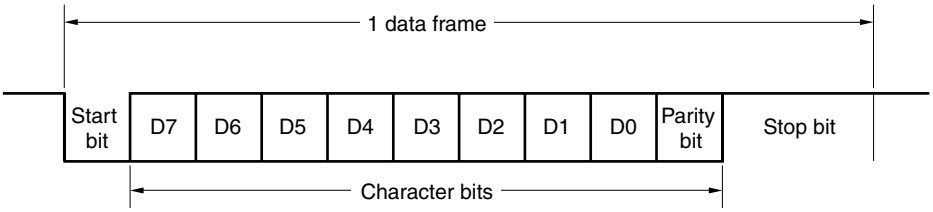
Figure 15-13 and Figure 15-14 show the format and waveform examples of the normal transmit/receive data.

Figure 15-13. Format of Normal UART Transmit/Receive Data

1. LSB-first transmission/reception



2. MSB-first transmission/reception



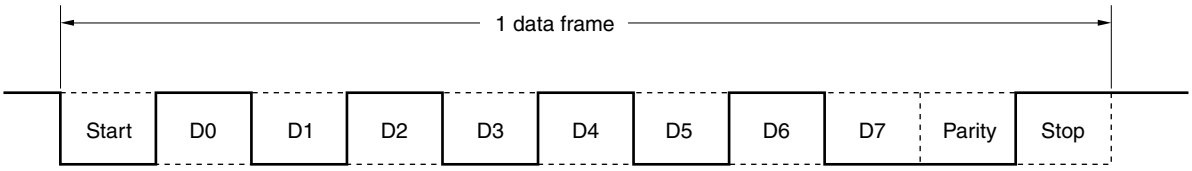
One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

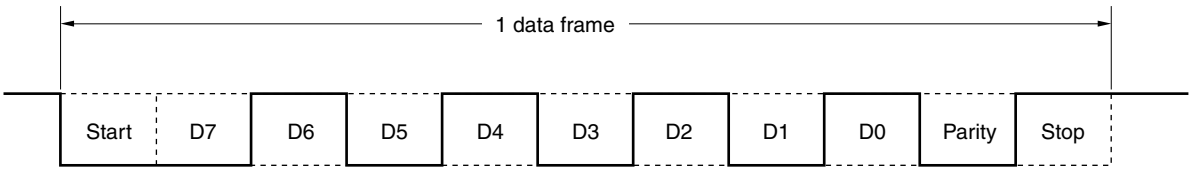
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 6 (ASIM6).
Whether data is communicated with the LSB or MSB first is specified by bit 1 (DIR6) of asynchronous serial interface control register 6 (ASICL6).
Whether the TxD6 pin outputs normal or inverted data is specified by bit 0 (TXDLV6) of ASICL6.

Figure 15-14. Example of Normal UART Transmit/Receive Data Waveform (1/2)

1. Data length: 8 bits, LSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



2. Data length: 8 bits, MSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



3. Data length: 8 bits, MSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H, TxD6 pin inverted output

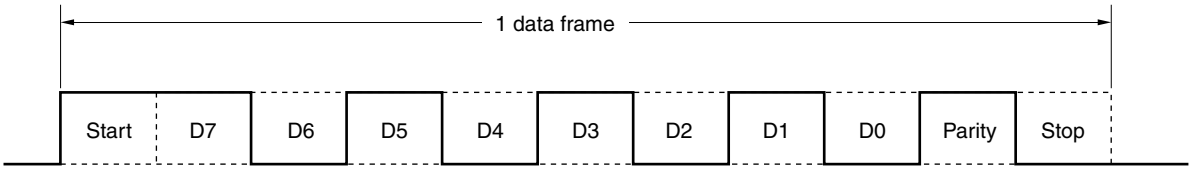
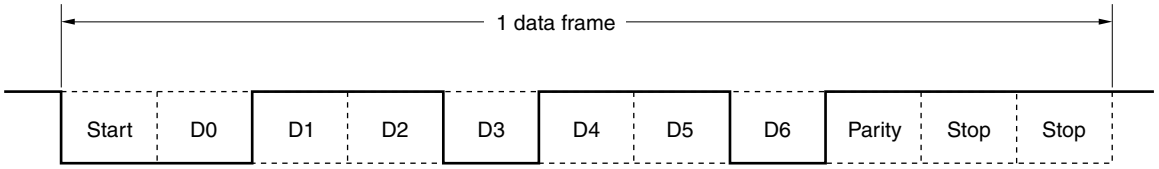
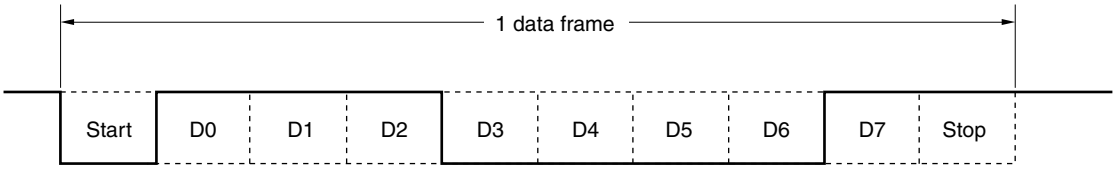


Figure 15-14. Example of Normal UART Transmit/Receive Data Waveform (2/2)

4. Data length: 7 bits, LSB first, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



5. Data length: 8 bits, LSB first, Parity: None, Stop bit: 1 bit, Communication data: 87H



(b) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmission and reception sides. With even parity and odd parity, a 1-bit (odd number) error can be detected. With zero parity and no parity, an error cannot be detected.

Caution Fix the PS61 and PS60 bits to 0 when the device is used in LIN communication operation.

(i) Even parity

- Transmission

  Transmit data, including the parity bit, is controlled so that the number of bits that are “1” is even.
  The value of the parity bit is as follows.

  If transmit data has an odd number of bits that are “1”: 1
  If transmit data has an even number of bits that are “1”: 0

- Reception

  The number of bits that are “1” in the receive data, including the parity bit, is counted. If it is odd, a parity error occurs.

(ii) Odd parity

- Transmission

  Unlike even parity, transmit data, including the parity bit, is controlled so that the number of bits that are “1” is odd.

  If transmit data has an odd number of bits that are “1”: 0
  If transmit data has an even number of bits that are “1”: 1

- Reception

  The number of bits that are “1” in the receive data, including the parity bit, is counted. If it is even, a parity error occurs.

(iii) 0 parity

The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.

The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is “0” or “1”.

(iv) No parity

No parity bit is appended to the transmit data.

Reception is performed assuming that there is no parity bit when data is received. Because there is no parity bit, a parity error does not occur.

(c) Normal transmission

When bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and bit 6 (TXE6) of ASIM6 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit buffer register 6 (TXB6). The start bit, parity bit, and stop bit are automatically appended to the data.

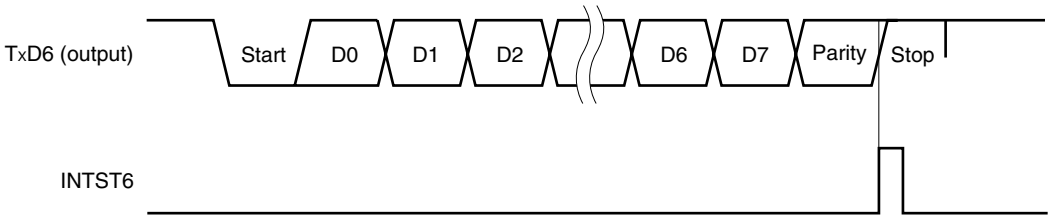
When transmission is started, the data in TXB6 is transferred to transmit shift register 6 (TXS6). After that, the transmit data is sequentially output from TXS6 to the TxD6 pin. When transmission is completed, the parity and stop bits set by ASIM6 are appended and a transmission completion interrupt request (INTST6) is generated.

Transmission is stopped until the data to be transmitted next is written to TXB6.

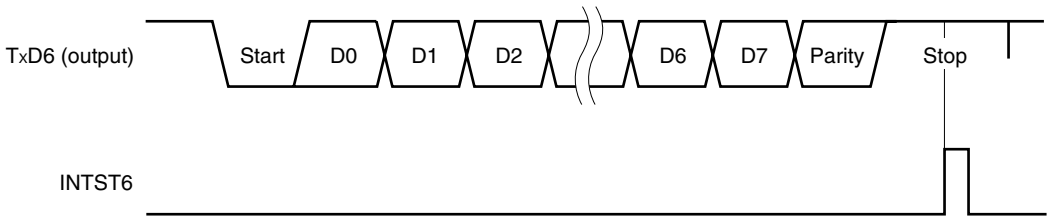
Figure 15-15 shows the timing of the transmission completion interrupt request (INTST6). This interrupt occurs as soon as the last stop bit has been output.

Figure 15-15. Normal Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2



(d) Continuous transmission

The next transmit data can be written to transmit buffer register 6 (TXB6) as soon as transmit shift register 6 (TXS6) has started its shift operation. Consequently, even while the INTST6 interrupt is being serviced after transmission of one data frame, data can be continuously transmitted and an efficient communication rate can be realized. In addition, the TXB6 register can be efficiently written twice (2 bytes) without having to wait for the transmission time of one data frame, by reading bit 0 (TXSF6) of asynchronous serial interface transmission status register 6 (ASIF6) when the transmission completion interrupt has occurred.

To transmit data continuously, be sure to reference the ASIF6 register to check the transmission status and whether the TXB6 register can be written, and then write the data.

Cautions 1. The TXBF6 and TXSF6 flags of the ASIF6 register change from "10" to "11", and to "01" during continuous transmission. To check the status, therefore, do not use a combination of the TXBF6 and TXSF6 flags for judgment. Read only the TXBF6 flag when executing continuous transmission.

2. When the device is use in LIN communication operation, the continuous transmission function cannot be used. Make sure that asynchronous serial interface transmission status register 6 (ASIF6) is 00H before writing transmit data to transmit buffer register 6 (TXB6).

TXBF6	Writing to TXB6 Register
0	Writing enabled
1	Writing disabled

Caution To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is "0". If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is "1", the transmit data cannot be guaranteed.

The communication status can be checked using the TXSF6 flag.

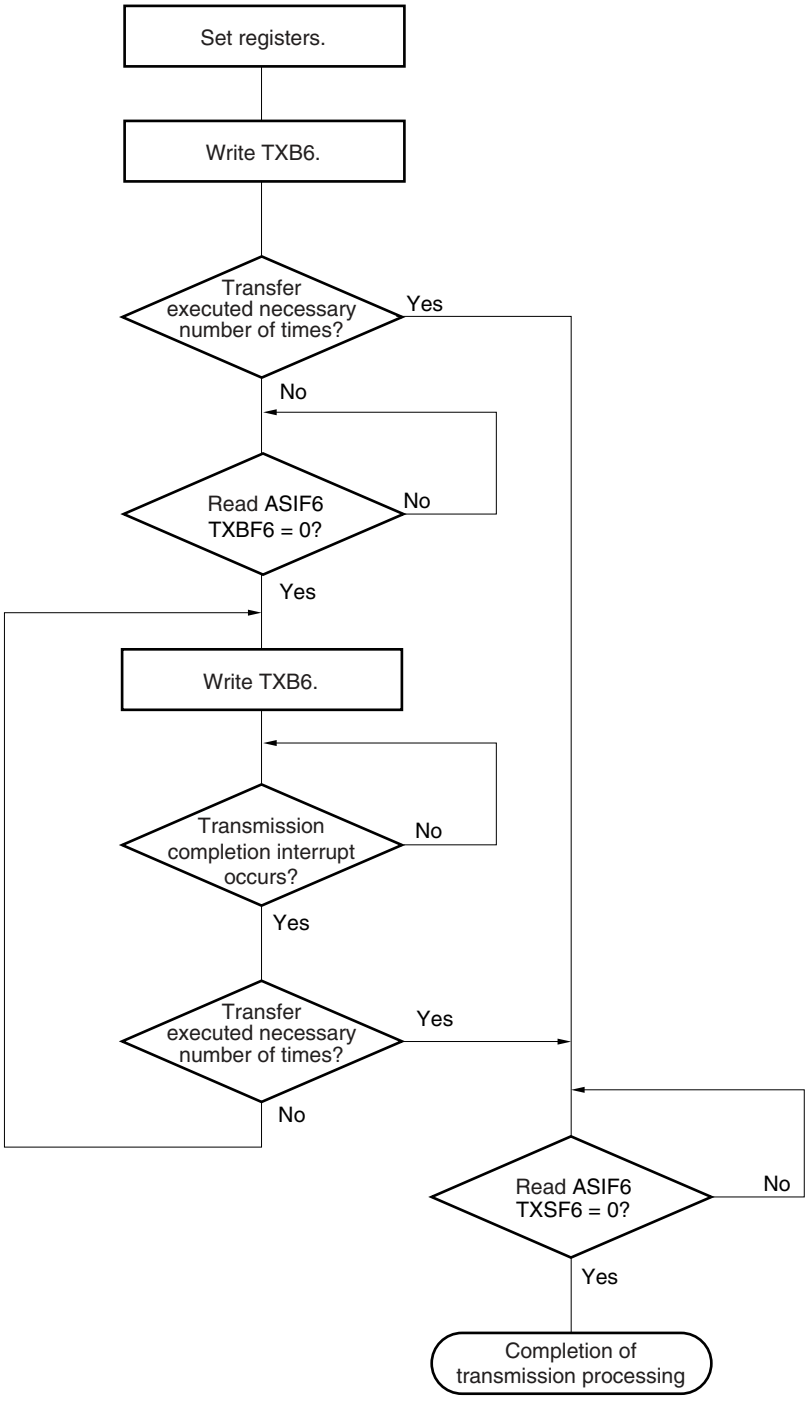
TXSF6	Transmission Status
0	Transmission is completed.
1	Transmission is in progress.

Cautions 1. To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is "0" after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is "1", the transmit data cannot be guaranteed.

2. During continuous transmission, the next transmission may complete before execution of INTST6 interrupt servicing after transmission of one data frame. As a countermeasure, detection can be performed by developing a program that can count the number of transmit data and by referencing the TXSF6 flag.

Figure 15-16 shows an example of the continuous transmission processing flow.

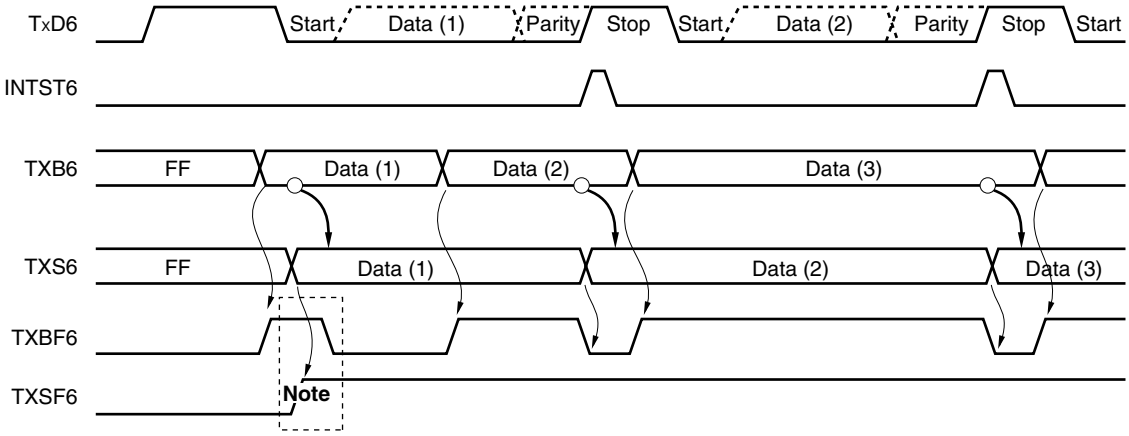
Figure 15-16. Example of Continuous Transmission Processing Flow



Remark TXB6: Transmit buffer register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6 (transmit buffer data flag)
TXSF6: Bit 0 of ASIF6 (transmit shift register data flag)

Figure 15-17 shows the timing of starting continuous transmission, and Figure 15-18 shows the timing of ending continuous transmission.

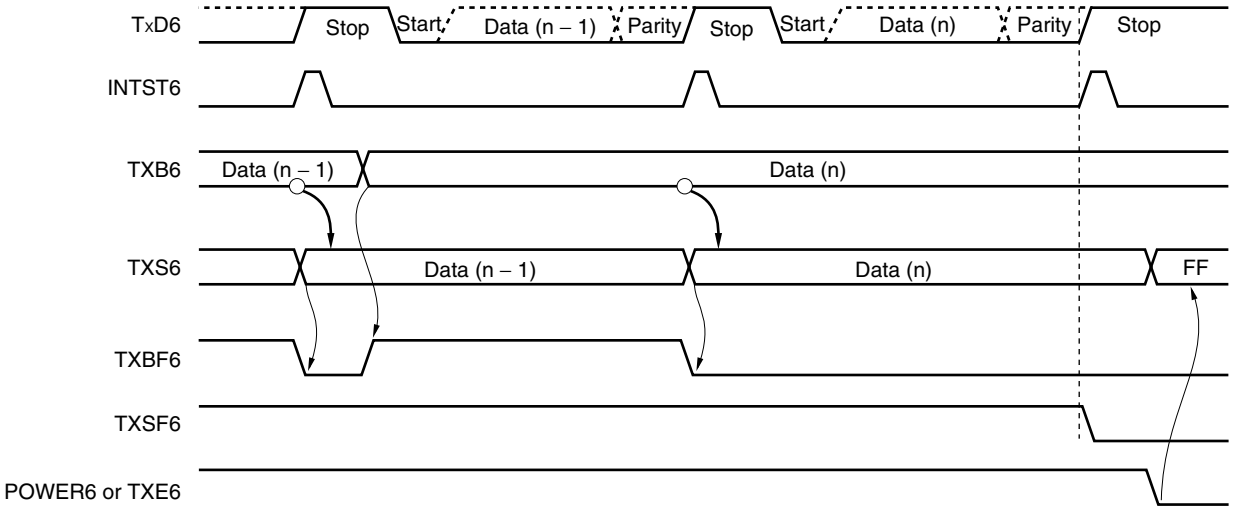
Figure 15-17. Timing of Starting Continuous Transmission



Note When ASIF6 is read, there is a period in which TXBF6 and TXSF6 = 1, 1. Therefore, judge whether writing is enabled using only the TXBF6 bit.

Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6

Figure 15-18. Timing of Ending Continuous Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6
POWER6: Bit 7 of asynchronous serial interface operation mode register (ASIM6)
TXE6: Bit 6 of asynchronous serial interface operation mode register (ASIM6)

(e) Normal reception

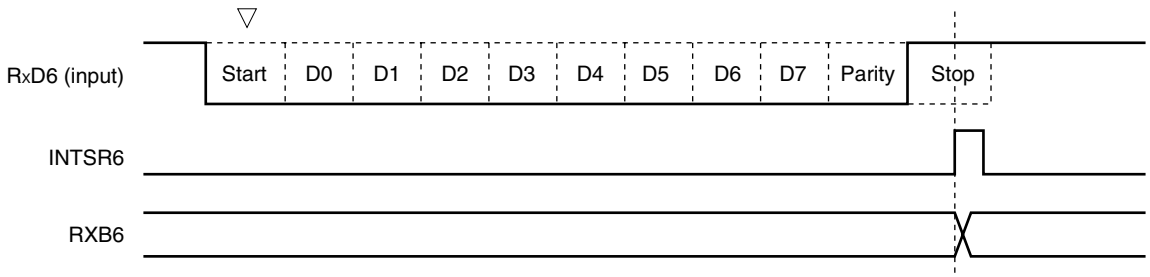
Reception is enabled and the RxD6 pin input is sampled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1.

The 8-bit counter of the baud rate generator starts counting when the falling edge of the RxD6 pin input is detected. When the set value of baud rate generator control register 6 (BRGC6) has been counted, the RxD6 pin input is sampled again (▽ in Figure 15-19). If the RxD6 pin is low level at this time, it is recognized as a start bit.

When the start bit is detected, reception is started, and serial data is sequentially stored in the receive shift register (RXS6) at the set baud rate. When the stop bit has been received, the reception completion interrupt (INTSR6) is generated and the data of RXS6 is written to receive buffer register 6 (RXB6). If an overrun error (OVE6) occurs, however, the receive data is not written to RXB6.

Even if a parity error (PE6) occurs while reception is in progress, reception continues to the reception position of the stop bit, and a reception error interrupt (INTSR6/INTSRE6) is generated on completion of reception.

Figure 15-19. Reception Completion Interrupt Request Timing



Cautions 1. If a reception error occurs, read ASIS6 and then RXB6 to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.

2. Reception is always performed with the "number of stop bits = 1". The second stop bit is ignored.

3. Be sure to read asynchronous serial interface reception error status register 6 (ASIS6) before reading RXB6.

(f) Reception error

Three types of errors may occur during reception: a parity error, framing error, or overrun error. If the error flag of asynchronous serial interface reception error status register 6 (ASIS6) is set as a result of data reception, a reception error interrupt request (INTSR6/INTSRE6) is generated.

Which error has occurred during reception can be identified by reading the contents of ASIS6 in the reception error interrupt (INTSR6/INTSRE6) servicing (see **Figure 15-6**).

The contents of ASIS6 are cleared to 0 when ASIS6 is read.

Table 15-3. Cause of Reception Error

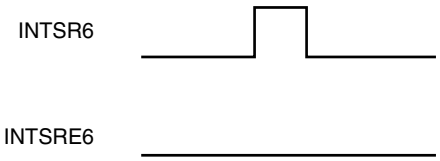
Reception Error	Cause
Parity error	The parity specified for transmission does not match the parity of the receive data.
Framing error	Stop bit is not detected.
Overrun error	Reception of the next data is completed before data is read from receive buffer register 6 (RXB6).

The reception error interrupt can be separated into reception completion interrupt (INTSR6) and error interrupt (INTSRE6) by clearing bit 0 (ISRM6) of asynchronous serial interface operation mode register 6 (ASIM6) to 0.

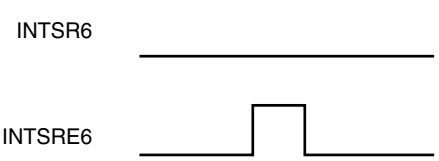
Figure 15-20. Reception Error Interrupt

1. If ISRM6 is cleared to 0 (reception completion interrupt (INTSR6) and error interrupt (INTSRE6) are separated)

(a) No error during reception

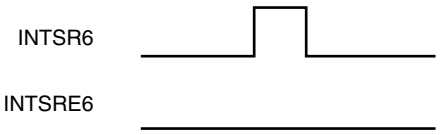


(b) Error during reception

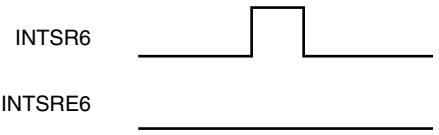


2. If ISRM6 is set to 1 (error interrupt is included in INTSR6)

(a) No error during reception



(b) Error during reception



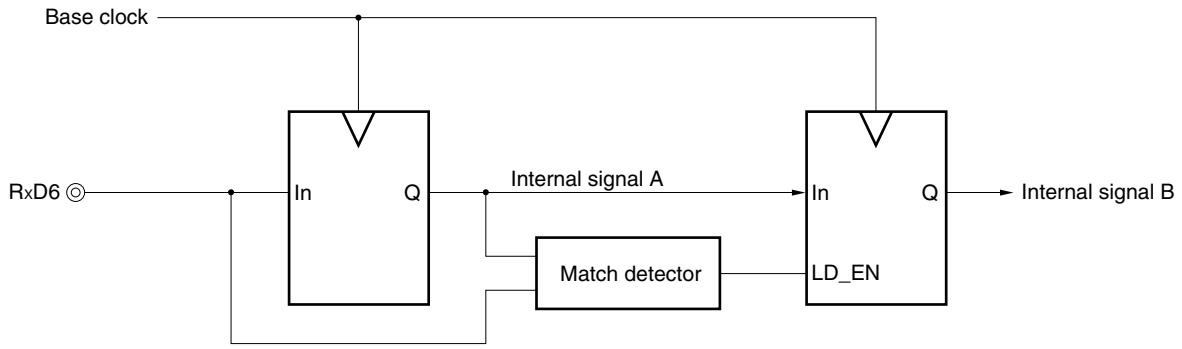
(g) Noise filter of receive data

The RxD6 signal is sampled with the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 15-21, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 15-21. Noise Filter Circuit



(h) SBF transmission

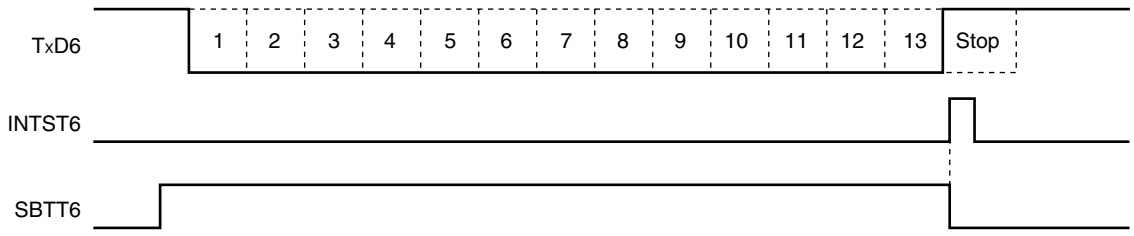
When the device is use in LIN communication operation, the SBF (Synchronous Break Field) transmission control function is used for transmission. For the transmission operation of LIN, see **Figure 15-1 LIN Transmission Operation**.

When bit 7 (POWER6) of asynchronous serial interface mode register 6 (ASIM6) is set to 1, the TxD6 pin outputs high level. Next, when bit 6 (TXE6) of ASIM6 is set to 1, the transmission enabled status is entered, and SBF transmission is started by setting bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

Thereafter, a low level of bits 13 to 20 (set by bits 4 to 2 (SBL62 to SBL60) of ASICL6) is output. Following the end of SBF transmission, the transmission completion interrupt request (INTST6) is generated and SBTT6 is automatically cleared. Thereafter, the normal transmission mode is restored.

Transmission is suspended until the data to be transmitted next is written to transmit buffer register 6 (TXB6), or until SBTT6 is set to 1.

Figure 15-22. SBF Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Transmission completion interrupt request
SBTT6: Bit 5 of asynchronous serial interface control register 6 (ASICL6)

(i) SBF reception

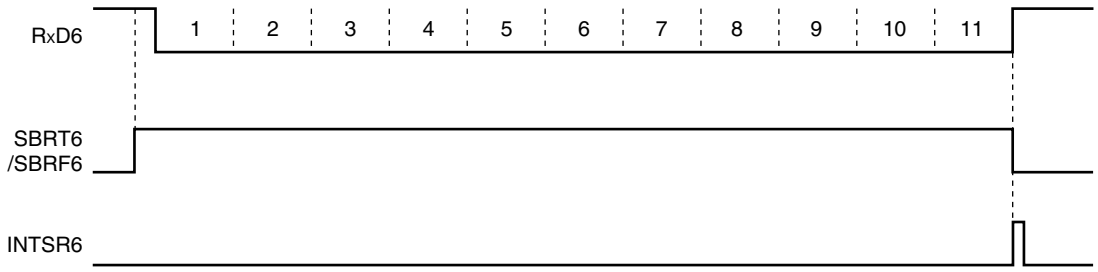
When the device is used in LIN communication operation, the SBF (Synchronous Break Field) reception control function is used for reception. For the reception operation of LIN, see **Figure 15-2 LIN Reception Operation**.

Reception is enabled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1. SBF reception is enabled when bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6) is set to 1. In the SBF reception enabled status, the RxD6 pin is sampled and the start bit is detected in the same manner as the normal reception enable status.

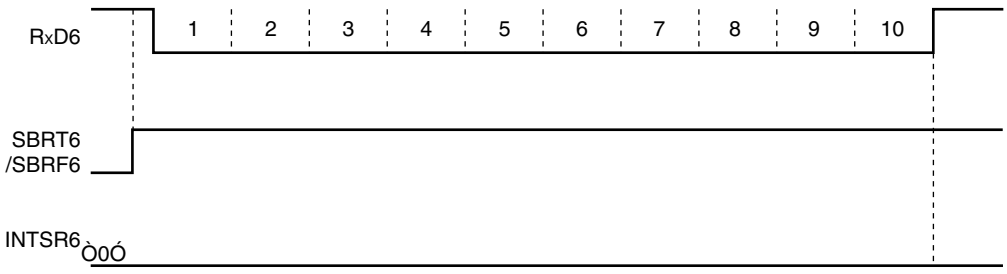
When the start bit has been detected, reception is started, and serial data is sequentially stored in the receive shift register 6 (RXS6) at the set baud rate. When the stop bit is received and if the width of SBF is 11 bits or more, a reception completion interrupt request (INTSR6) is generated as normal processing. At this time, the SBRF6 and SBRT6 bits are automatically cleared, and SBF reception ends. Detection of errors, such as OVE6, PE6, and FE6 (bits 0 to 2 of asynchronous serial interface reception error status register 6 (ASIS6)) is suppressed, and error detection processing of UART communication is not performed. In addition, data transfer between receive shift register 6 (RXS6) and receive buffer register 6 (RXB6) is not performed, and the reset value of FFH is retained. If the width of SBF is 10 bits or less, an interrupt does not occur as error processing after the stop bit has been received, and the SBF reception mode is restored. In this case, the SBRF6 and SBRT6 bits are not cleared.

Figure 15-23. SBF Reception

1. Normal SBF reception (stop bit is detected with a width of more than 10.5 bits)



2. SBF reception error (stop bit is detected with a width of 10.5 bits or less)



Remark RxD6: RxD6 pin (input)
SBRT6: Bit 6 of asynchronous serial interface control register 6 (ASICL6)
SBRF6: Bit 7 of ASICL6
INTSR6: Reception completion interrupt request

15.4.3 Dedicated baud rate generator

The dedicated baud rate generator consists of a source clock selector and an 8-bit programmable counter, and generates a serial clock for transmission/reception of UART6.

Separate 8-bit counters are provided for transmission and reception.

(1) Configuration of baud rate generator

- Base clock

  The clock selected by bits 3 to 0 (TPS63 to TPS60) of clock selection register 6 (CKSR6) is supplied to each module when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is 1. This clock is called the base clock and its frequency is called f_{XCLK6}. The base clock is fixed to low level when POWER6 = 0.

- Transmission counter

  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 6 (TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.

  It starts counting when POWER6 = 1 and TXE6 = 1.

  The counter is cleared to 0 when the first data transmitted is written to transmit buffer register 6 (TXB6).

  If data are continuously transmitted, the counter is cleared to 0 again when one frame of data has been completely transmitted. If there is no data to be transmitted next, the counter is not cleared to 0 and continues counting until POWER6 or TXE6 is cleared to 0.

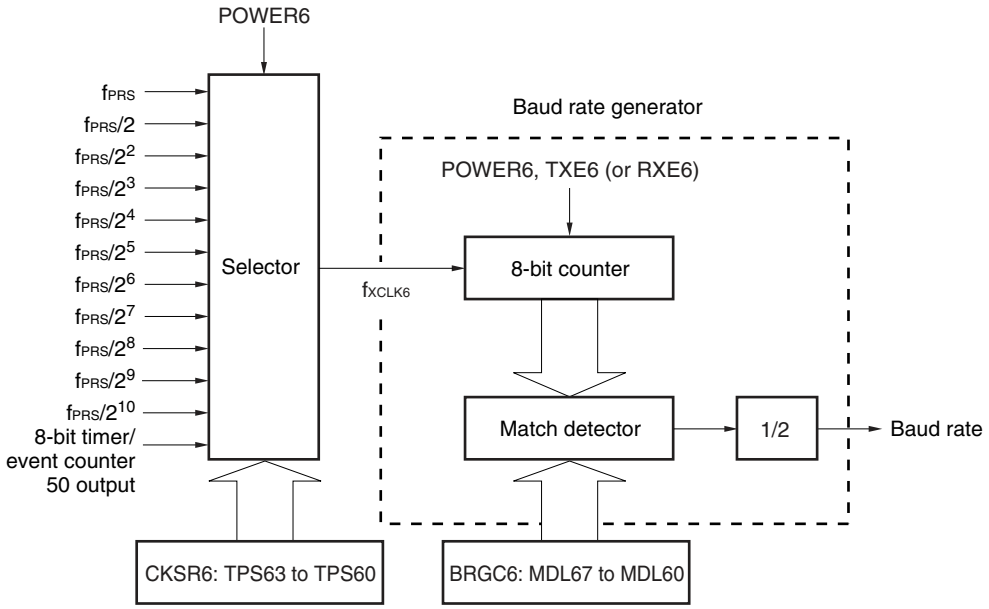
- Reception counter

  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 5 (RXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.

  It starts counting when the start bit has been detected.

  The counter stops operation after one frame has been received, until the next start bit is detected.

Figure 15-24. Configuration of Baud Rate Generator



Remark POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
CKSR6: Clock selection register 6
BRGC6: Baud rate generator control register 6

(2) Generation of serial clock

A serial clock to be generated can be specified by using clock selection register 6 (CKSR6) and baud rate generator control register 6 (BRGC6).

The clock to be input to the 8-bit counter can be set by bits 3 to 0 (TPS63 to TPS60) of CKSR6 and the division value ($f_{XCLK6}/4$ to $f_{XCLK6}/255$) of the 8-bit counter can be set by bits 7 to 0 (MDL67 to MDL60) of BRGC6.

15.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK6}}{2 \times k}$ [bps]

f_{XCLK6}: Frequency of base clock selected by TPS63 to TPS60 bits of CKSR6 register

k: Value set by MDL67 to MDL60 bits of BRGC6 register (k = 4, 5, 6, ..., 255)

Table 15-4. Set Value of TPS63 to TPS60

TPS63	TPS62	TPS61	TPS60	Base Clock (f_{XCLK6}) Selection[Note 1]				
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	8 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	500 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	125 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	62.5 kHz	78.13 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	31.25 kHz	39.06 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	15.625 kHz	19.53 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	7.813 kHz	9.77 kHz
1	0	1	1	TM50 output[Note 3]				
Other than above				Setting prohibited				

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of TPS63 = TPS62 = TPS61 = TPS60 = 0 (base clock: f_{PRS}) is prohibited.

3. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

Baud rate = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(3) Example of setting baud rate

Table 15-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz			
	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]
300	8H	13	301	0.16	7H	65	301	0.16	8H	65	301	0.16
600	7H	13	601	0.16	6H	65	601	0.16	7H	65	601	0.16
1200	6H	13	1202	0.16	5H	65	1202	0.16	6H	65	1202	0.16
2400	5H	13	2404	0.16	4H	65	2404	0.16	5H	65	2404	0.16
4800	4H	13	4808	0.16	3H	65	4808	0.16	4H	65	4808	0.16
9600	3H	13	9615	0.16	2H	65	9615	0.16	3H	65	9615	0.16
19200	2H	13	19231	0.16	1H	65	19231	0.16	2H	65	19231	0.16
24000	1H	21	23810	−0.79	3H	13	24038	0.16	4H	13	24038	0.16
31250	1H	16	31250	0	4H	5	31250	0	5H	5	31250	0
38400	1H	13	38462	0.16	0H	65	38462	0.16	1H	65	38462	0.16
48000	0H	21	47619	−0.79	2H	13	48077	0.16	3H	13	48077	0.16
76800	0H	13	76923	0.16	0H	33	75758	−1.36	0H	65	76923	0.16
115200	0H	9	111111	−3.55	1H	11	113636	−1.36	0H	43	116279	0.94
153600	−	−	−	−	1H	8	156250	1.73	0H	33	151515	−1.36
312500	−	−	−	−	0H	8	312500	0	1H	8	312500	0
625000	−	−	−	−	0H	4	625000	0	1H	4	625000	0

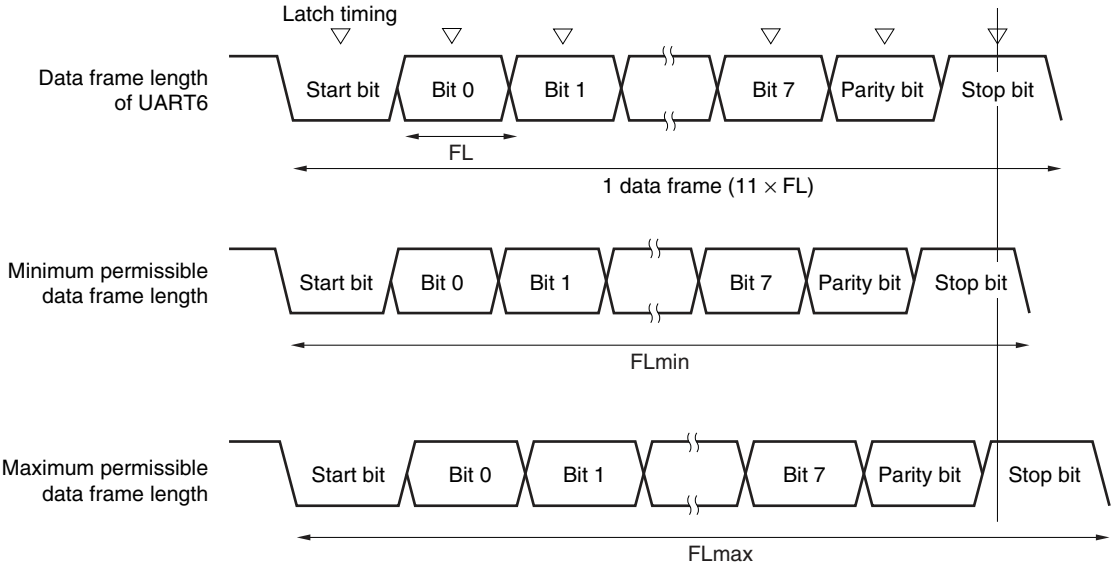
Remark TPS63 to TPS60: Bits 3 to 0 of clock selection register 6 (CKSR6) (setting of base clock (f_{XCLK6}))
k: Value set by MDL67 to MDL60 bits of baud rate generator control register 6 (BRGC6) (k = 4, 5, 6, ..., 255)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 15-25. Permissible Baud Rate Range During Reception



As shown in Figure 15-25, the latch timing of the receive data is determined by the counter set by baud rate generator control register 6 (BRGC6) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.
Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART6
k: Set value of BRGC6
FL: 1-bit data length
Margin of latch timing: 2 clocks

$$\text{Minimum permissible data frame length: } FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$$

Therefore, the maximum receivable baud rate at the transmission destination is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k+2} \text{ Brate}$$

Similarly, the maximum permissible data frame length can be calculated as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k+2}{2 \times k} \times FL = \frac{21k-2}{2 \times k} FL$$

$$FLmax = \frac{21k-2}{20k} FL \times 11$$

Therefore, the minimum receivable baud rate at the transmission destination is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k-2} \text{ Brate}$$

The permissible baud rate error between UART6 and the transmission destination can be calculated from the above minimum and maximum baud rate expressions, as follows.

Table 15-6. Maximum/Minimum Permissible Baud Rate Error

Division Ratio (k)	Maximum Permissible Baud Rate Error	Minimum Permissible Baud Rate Error
4	+2.33%	–2.44%
8	+3.53%	–3.61%
20	+4.26%	–4.31%
50	+4.56%	–4.58%
100	+4.66%	–4.67%
255	+4.72%	–4.73%

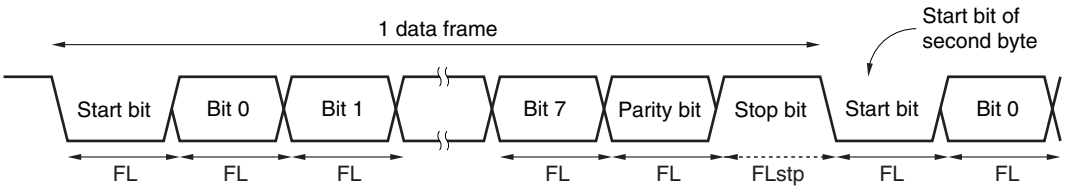
Remarks 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the higher the division ratio (k), the higher the permissible error.

2. k: Set value of BRGC6

(5) Data frame length during continuous transmission

When data is continuously transmitted, the data frame length from a stop bit to the next start bit is extended by two clocks of base clock from the normal value. However, the result of communication is not affected because the timing is initialized on the reception side when the start bit is detected.

Figure 15-26. Data Frame Length During Continuous Transmission



Where the 1-bit data length is FL, the stop bit length is FLstp, and base clock frequency is f_{XCLK6}, the following expression is satisfied.

$$FLstp = FL + 2/f_{XCLK6}$$

Therefore, the data frame length during continuous transmission is:

$$\text{Data frame length} = 11 \times FL + 2/f_{XCLK6}$$

CHAPTER 16 SERIAL INTERFACE CSI10

16.1 Functions of Serial Interface CSI10

Serial interface CSI10 is mounted onto all 78K0/Lx3-M microcontroller products.

Serial interface CSI10 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not performed and can enable a reduction in the power consumption.

For details, see **16.4.1 Operation stop mode**.

(2) 3-wire serial I/O mode (MSB/LSB-first selectable)

This mode is used to communicate 8-bit data using three lines: a serial clock line ($\overline{\text{SCK10}}$) and two serial data lines (SI10 and SO10).

The processing time of data communication can be shortened in the 3-wire serial I/O mode because transmission and reception can be simultaneously executed.

In addition, whether 8-bit data is communicated with the MSB or LSB first can be specified, so this interface can be connected to any device.

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

For details, see **16.4.2 3-wire serial I/O mode**.

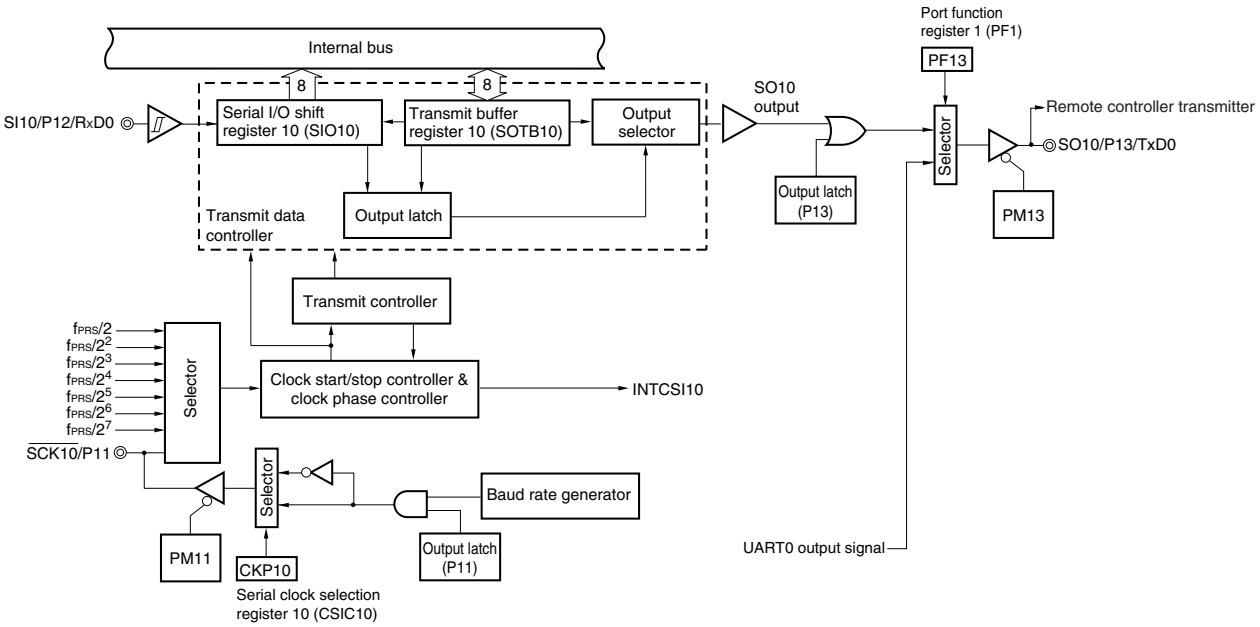
16.2 Configuration of Serial Interface CSI10

Serial interface CSI10 includes the following hardware.

Table 16-1. Configuration of Serial Interface CSI10

Item	Configuration
Controller	Transmit controller Clock start/stop controller & clock phase controller
Registers	Transmit buffer register 10 (SOTB10) Serial I/O shift register 10 (SIO10)
Control registers	Serial operation mode register 10 (CSIM10) Serial clock selection register 10 (CSIC10) Port function register 1 (PF1) Port mode register 1 (PM1) Port register 1 (P1)

Figure 16-1. Block Diagram of Serial Interface CSI10



(1) Transmit buffer register 10 (SOTB10)

This register sets the transmit data.

Transmission/reception is started by writing data to SOTB10 when bit 7 (CSIE10) and bit 6 (TRMD10) of serial operation mode register 10 (CSIM10) is 1.

The data written to SOTB10 is converted from parallel data into serial data by serial I/O shift register 10, and output to the serial output pin (SO10).

SOTB10 can be written or read by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Caution Do not access SOTB10 when CSOT10 = 1 (during serial communication).

(2) Serial I/O shift register 10 (SIO10)

This is an 8-bit register that converts data from parallel data into serial data and vice versa.

This register can be read by an 8-bit memory manipulation instruction.

Reception is started by reading data from SIO10 if bit 6 (TRMD10) of serial operation mode register 10 (CSIM10) is 0.

During reception, the data is read from the serial input pin (SI10) to SIO10.

Reset signal generation sets this register to 00H.

Caution Do not access SIO10 when CSOT10 = 1 (during serial communication).

16.3 Registers Controlling Serial Interface CSI10

Serial interface CSI10 is controlled by the following five registers.

- Serial operation mode register 10 (CSIM10)
- Serial clock selection register 10 (CSIC10)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)

(1) Serial operation mode register 10 (CSIM10)

CSIM10 is used to select the operation mode and enable or disable operation.

CSIM10 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 16-2. Format of Serial Operation Mode Register 10 (CSIM10)

Address: FF80H After reset: 00H R/W[Note 1]

Symbol	<7>	6	5	4	3	2	1	0
CSIM10	CSIE10	TRMD10	0	DIR10	0	0	0	CSOT10

CSIE10[Note 2]	Operation control in 3-wire serial I/O mode
0	Disables operation and asynchronously resets the internal circuit[Note 3].
1	Enables operation

TRMD10[Note 4]	Transmit/receive mode control
0[Note 5]	Receive mode (transmission disabled).
1	Transmit/receive mode

DIR10[Note 6]	First bit specification
0	MSB
1	LSB

CSOT10	Communication status flag
0	Communication is stopped.
1	Communication is in progress.

Notes 1. Bit 0 is a read-only bit.

2. To use P11/$\overline{SCK10}$, P12/SI10, and P13/SO10 as general-purpose port, clear CSIE10 to 0.

3. Bit 0 (CSOT10) of CSIM10 and serial I/O shift register 10 (SIO10) are reset.

4. Do not rewrite TRMD10 when CSOT10 = 1 (during serial communication).

5. The SO10 output (see **Figure 16-1**) is fixed to the low level when TRMD10 is 0. Reception is started when data is read from SIO10.

6. Do not rewrite DIR10 when CSOT10 = 1 (during serial communication).

Cautions 1. When resuming operation from standby status, do so after having cleared (0) bit 2 (CSIIF10) of interrupt request flag register 0H (IF0H).

2. Be sure to clear bits 1 to 3, and 5 to 0.

(2) Serial clock selection register 10 (CSIC10)

This register specifies the timing of the data transmission/reception and sets the serial clock.

CSIC10 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 16-3. Format of Serial Clock Selection Register 10 (CSIC10)

Address: FF81H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CSIC10	0	0	0	CKP10	DAP10	CKS102	CKS101	CKS100

CKP10	DAP10	Specification of data transmission/reception timing	Type
0	0	$\overline{SCK10}$, SO10 (D7 D6 D5 D4 D3 D2 D1 D0), SI10 input timing	1
0	1	$\overline{SCK10}$, SO10 (D7 D6 D5 D4 D3 D2 D1 D0), SI10 input timing	2
1	0	$\overline{SCK10}$, SO10 (D7 D6 D5 D4 D3 D2 D1 D0), SI10 input timing	3
1	1	$\overline{SCK10}$, SO10 (D7 D6 D5 D4 D3 D2 D1 D0), SI10 input timing	4

CKS102	CKS101	CKS100	CSI10 serial clock selection[Notes 1, 2]					Mode
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz	
0	0	0	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	Setting prohibited	Master mode
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2 MHz	2.5 MHz	
0	1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz	
0	1	1	$f_{PRS}/2^4$	125 kHz	312.5 kHz	500 kHz	625 kHz	
1	0	0	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz	
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	125 kHz	156.25 kHz	
1	1	0	$f_{PRS}/2^7$	15.63 kHz	39.06 kHz	62.5 kHz	78.13 kHz	
1	1	1	External clock input from $\overline{SCK10}$[Note 3]					Slave mode

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Set the serial clock to satisfy the following conditions.

- V_{DD} = 2.7 to 3.6 V: serial clock ≤ 4 MHz
- V_{DD} = 1.8 to 2.7 V: serial clock ≤ 2 MHz

3. Do not start communication operation with the external clock from $\overline{SCK10}$ when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).
2. To use P11/$\overline{\text{SCK10}}$ and P13/SO10 as general-purpose ports, set CSIC10 in the default status (00H).
3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock oscillation frequency

(3) Port function register 1 (PF1)

This register sets the pin functions of P13/SO10 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 16-4. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	0	0	0	PF13	0	0	0

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

(4) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using P11/$\overline{\text{SCK10}}$ as the clock output pin of the serial interface, clear PM11 to 0, and set the output latches of P11 to 1.

When using P13/SO10 as the data output pin of the serial interface, clear PM13 and the output latches of P13 to 0.

When using P11/$\overline{\text{SCK10}}$ as the clock input pin of the serial interface and P12/SI10 as the data input pin, set PM11 and PM12 to 1. At this time, the output latches of P11 and P12 may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 16-5. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	1	PM14	PF13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 4, 6, and 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

16.4 Operation of Serial Interface CSI10

Serial interface CSI10 can be used in the following two modes.

- Operation stop mode
- 3-wire serial I/O mode

16.4.1 Operation stop mode

Serial communication is not executed in this mode. Therefore, the power consumption can be reduced. In addition, the P11/$\overline{\text{SCK10}}$, P12/SI10, and P13/SO10 pins can be used as ordinary I/O port pins in this mode.

(1) Register used

The operation stop mode is set by serial operation mode register 10 (CSIM10).

To set the operation stop mode, clear bit 7 (CSIE10) of CSIM10 to 0.

(a) Serial operation mode register 10 (CSIM10)

CSIM10 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets CSIM10 to 00H.

Address: FF80H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM10	CSIE10	TRMD10	0	DIR10	0	0	0	CSOT10

CSIE10	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 1] and asynchronously resets the internal circuit[Note 2].

Notes 1. To use P11/$\overline{\text{SCK10}}$, P12/SI10, and P13/SO10 as general-purpose ports, set CSIM10 in the default status (00H).

2. Bit 0 (CSOT10) of CSIM10 and serial I/O shift register 10 (SIO10) are reset.

16.4.2 3-wire serial I/O mode

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: the serial clock ($\overline{SCK10}$), serial output (SO10), and serial input (SI10) lines.

(1) Registers used

- Serial operation mode register 10 (CSIM10)
- Serial clock selection register 10 (CSIC10)
- Port mode register 1 (PM1)
- Port register 1 (P1)

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set the CSIC10 register (see **Figure 16-3**).
<2> Set bits 4 and 6 (DIR10 and TRMD10) of the CSIM10 register (see **Figure 16-2**).
<3> Set bit 7 (CSIE10) of the CSIM10 register to 1. → Transmission/reception is enabled.
<4> Write data to transmit buffer register 10 (SOTB10). → Data transmission/reception is started.
Read data from serial I/O shift register 10 (SIO10). → Data reception is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 16-2. Relationship Between Register Settings and Pins

CSIE10	TRMD10	PM12	P12	PM13	P13	PM11	P11	CSI10 Operation	Pin Function		
									SI10/RxD0/ P12	SO10/ TxD0/T/P13	$\overline{\text{SCK10}}$/ P11
0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	RxD0/ P12	TxD0/P13 Note 2	P11Note 3
1	0	1	×	×Note 1	×Note 1	1	×	Slave reception Note 4	SI10	TxD0/P13 Note 2	$\overline{\text{SCK10}}$ (input)Note 4
1	1	×Note 1	×Note 1	0	0	1	×	Slave transmission Note 4	RxD0/P12	SO10	$\overline{\text{SCK10}}$ (input)Note 4
1	1	1	×	0	0	1	×	Slave transmission/ reception Note 4	SI10	SO10	$\overline{\text{SCK10}}$ (input)Note 4
1	0	1	×	×Note 1	×Note 1	0	1	Master reception	SI10	TxD0/P13 Note 2	$\overline{\text{SCK10}}$ (output)
1	1	×Note 1	×Note 1	0	0	0	1	Master transmission	RxD0/P12	SO10	$\overline{\text{SCK10}}$ (output)
1	1	1	×	0	0	0	1	Master transmission/ reception	SI10	SO10	$\overline{\text{SCK10}}$ (output)

Notes 1. Can be set as port function.

2. To use P13/SO10/TxD0 as general-purpose port, set the serial clock selection register 10 (CSIC10) in the default status (00H).

3. To use P11/$\overline{\text{SCK10}}$ as port pins, clear CKP10 to 0.

4. To use the slave mode, set CKS102, CKS101, and CKS100 to 1, 1, 1.

Remark ×: don't care
CSIE10: Bit 7 of serial operation mode register 10 (CSIM10)
TRMD10: Bit 6 of CSIM10
CKP10: Bit 4 of serial clock selection register 10 (CSIC10)
CKS102, CKS101, CKS100: Bits 2 to 0 of CSIC10
PM1×: Port mode register
P1×: Port output latch

(2) Communication operation

In the 3-wire serial I/O mode, data is transmitted or received in 8-bit units. Each bit of the data is transmitted or received in synchronization with the serial clock.

Data can be transmitted or received if bit 6 (TRMD10) of serial operation mode register 10 (CSIM10) is 1. Transmission/reception is started when a value is written to transmit buffer register 10 (SOTB10). In addition, data can be received when bit 6 (TRMD10) of serial operation mode register 10 (CSIM10) is 0.

Reception is started when data is read from serial I/O shift register 10 (SIO10).

After communication has been started, bit 0 (CSOT10) of CSIM10 is set to 1. When communication of 8-bit data has been completed, a communication completion interrupt request flag (CSIIF10) is set, and CSOT10 is cleared to 0. Then the next communication is enabled.

Caution Do not access the control register and data register when CSOT10 = 1 (during serial communication).

Figure 16-6. Timing in 3-Wire Serial I/O Mode (1/2)

(a) Transmission/reception timing (Type 1: TRMD10 = 1, DIR10 = 0, CKP10 = 0, DAP10 = 0)

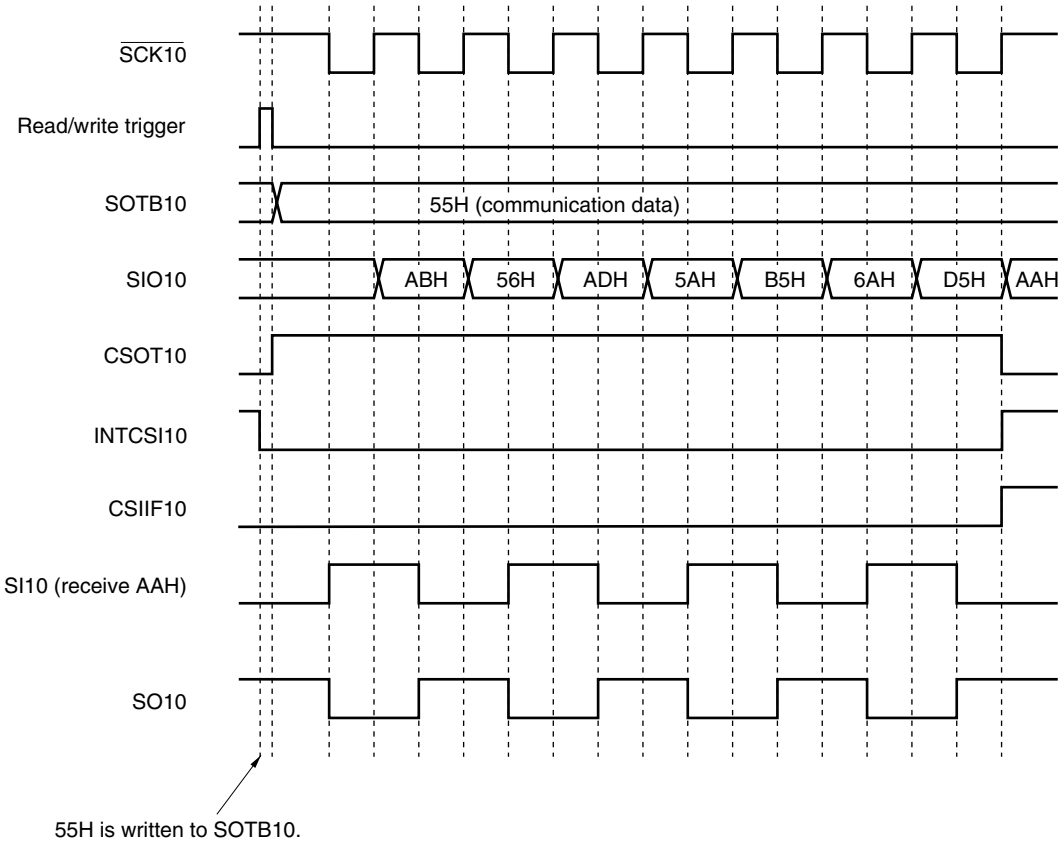


Figure 16-6. Timing in 3-Wire Serial I/O Mode (2/2)

(b) Transmission/reception timing (Type 2: TRMD10 = 1, DIR10 = 0, CKP10 = 0, DAP10 = 1)

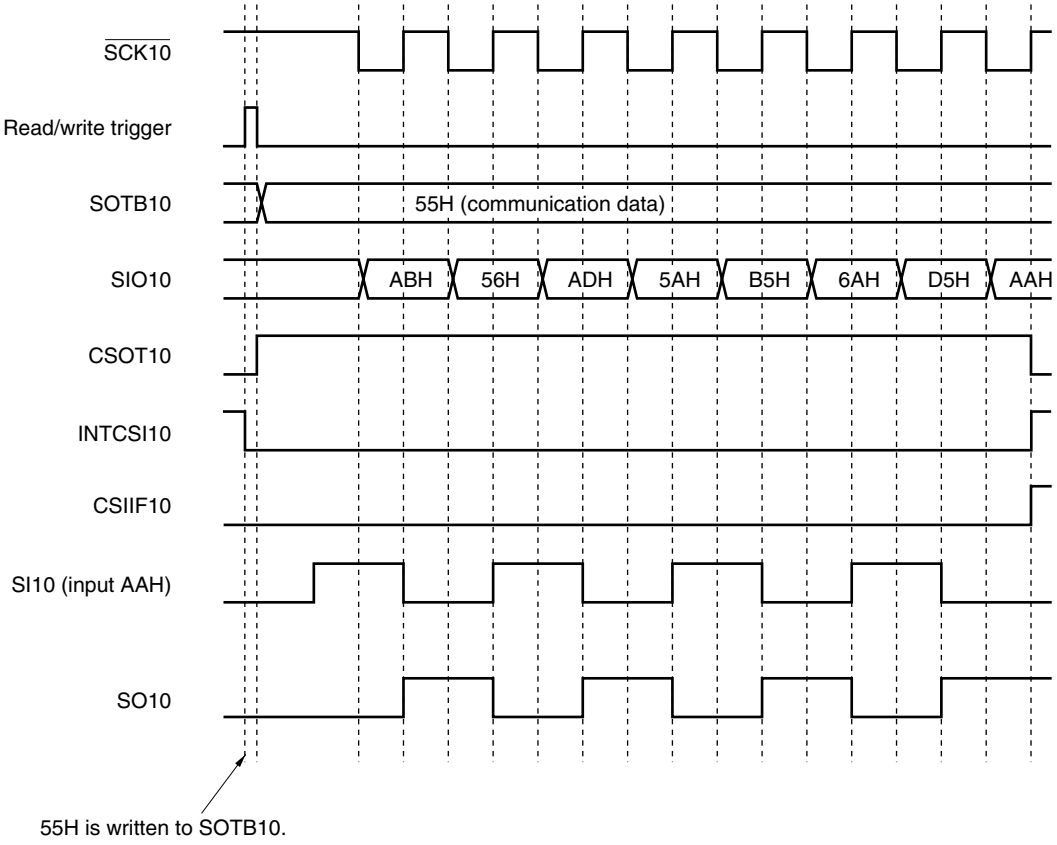
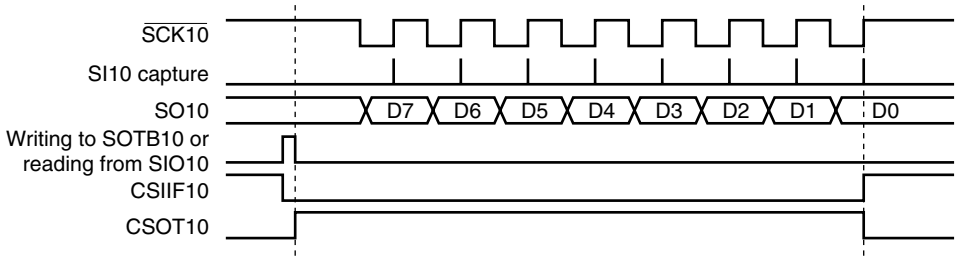
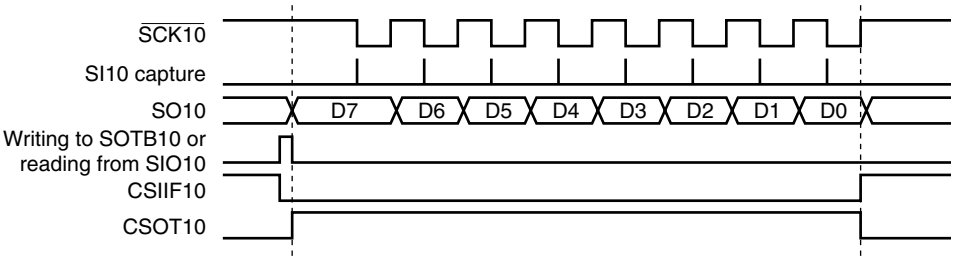


Figure 16-7. Timing of Clock/Data Phase

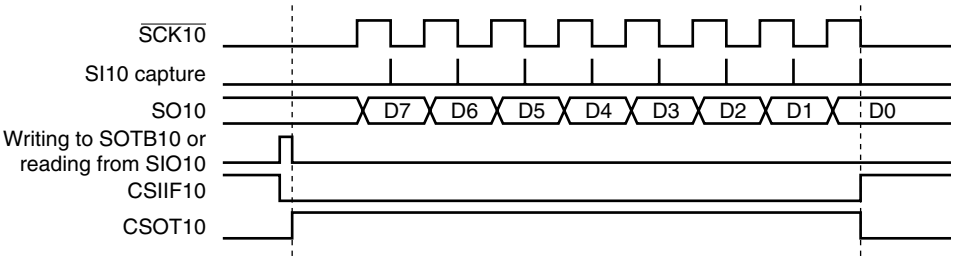
(a) Type 1: CKP10 = 0, DAP10 = 0, DIR10 = 0



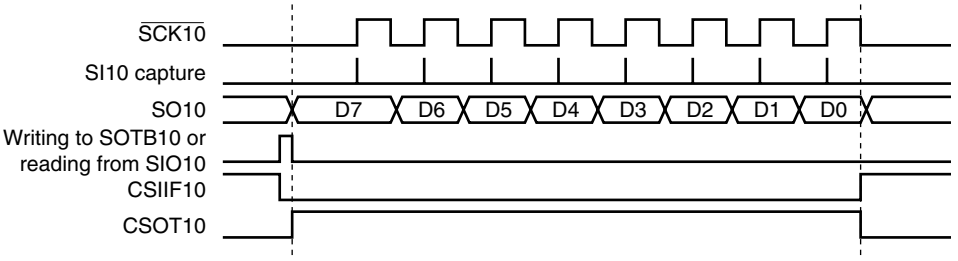
(b) Type 2: CKP10 = 0, DAP10 = 1, DIR10 = 0



(c) Type 3: CKP10 = 1, DAP10 = 0, DIR10 = 0



(d) Type 4: CKP10 = 1, DAP10 = 1, DIR10 = 0



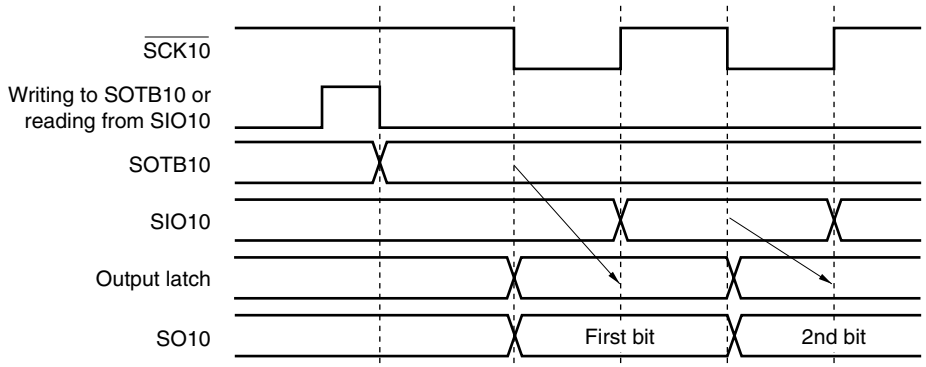
Remark The above figure illustrates a communication operation where data is transmitted with the MSB first.

(3) Timing of output to SO10 pin (first bit)

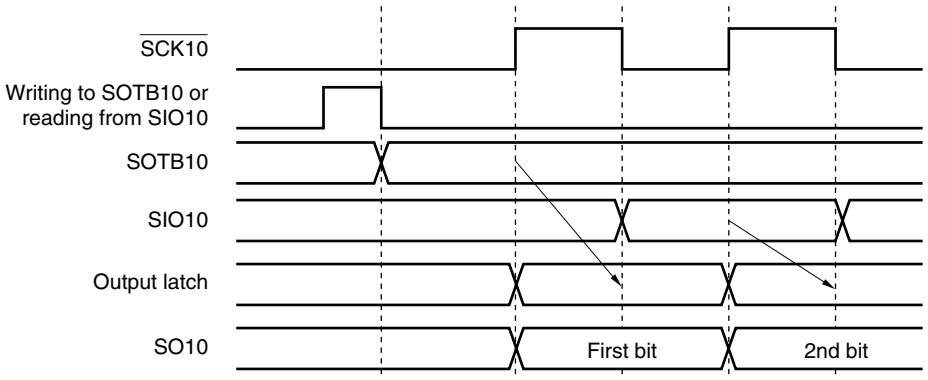
When communication is started, the value of transmit buffer register 10 (SOTB10) is output from the SO10 pin. The output operation of the first bit at this time is described below.

Figure 16-8. Output Operation of First Bit (1/2)

(a) Type 1: CKP10 = 0, DAP10 = 0



(b) Type 3: CKP10 = 1, DAP10 = 0

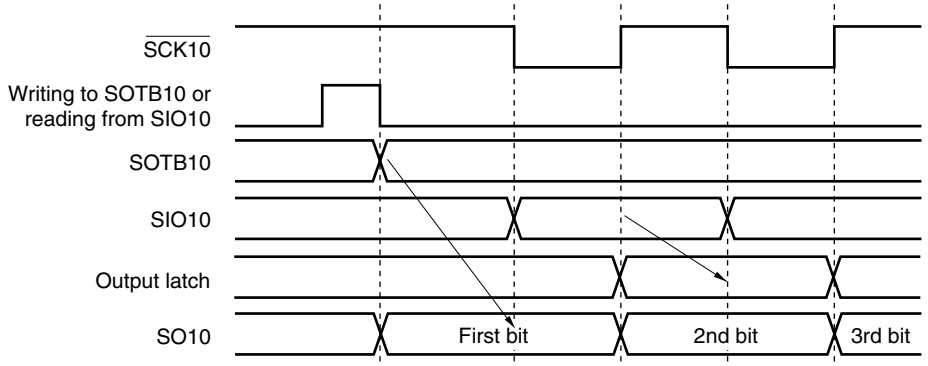


The first bit is directly latched by the SOTB10 register to the output latch at the falling (or rising) edge of $\overline{SCK10}$, and output from the SO10 pin via an output selector. Then, the value of the SOTB10 register is transferred to the SIO10 register at the next rising (or falling) edge of $\overline{SCK10}$, and shifted one bit. At the same time, the first bit of the receive data is stored in the SIO10 register via the SI10 pin.

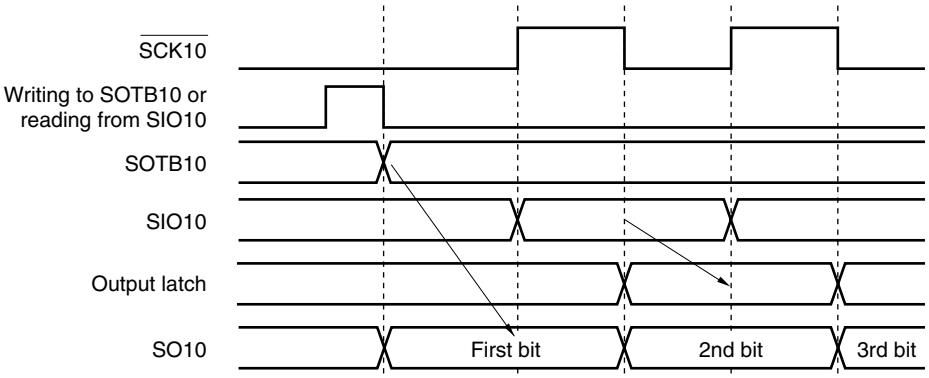
The second and subsequent bits are latched by the SIO10 register to the output latch at the next falling (or rising) edge of $\overline{SCK10}$, and the data is output from the SO10 pin.

Figure 16-8. Output Operation of First Bit (2/2)

(c) Type 2: CKP10 = 0, DAP10 = 1



(d) Type 4: CKP10 = 1, DAP10 = 1



The first bit is directly latched by the SOTB10 register at the falling edge of the write signal of the SOTB10 register or the read signal of the SIO10 register, and output from the SO10 pin via an output selector. Then, the value of the SOTB10 register is transferred to the SIO10 register at the next falling (or rising) edge of $\overline{SCK10}$, and shifted one bit. At the same time, the first bit of the receive data is stored in the SIO10 register via the SI10 pin.

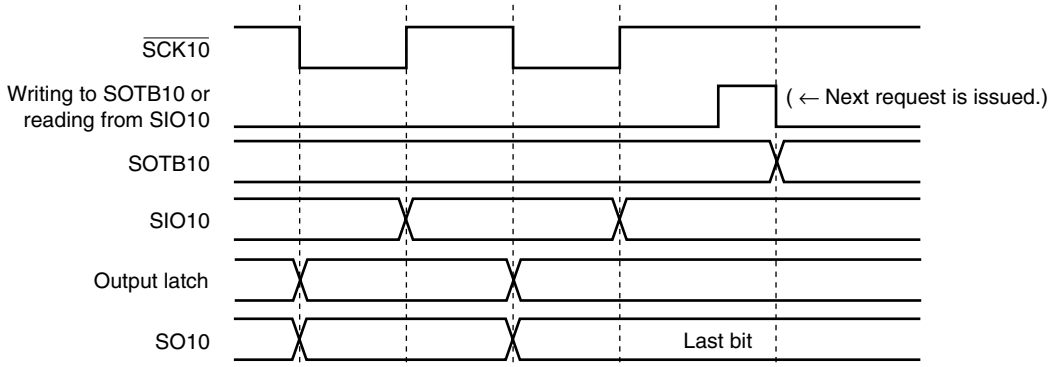
The second and subsequent bits are latched by the SIO10 register to the output latch at the next rising (or falling) edge of $\overline{SCK10}$, and the data is output from the SO10 pin.

(4) Output value of SO10 pin (last bit)

After communication has been completed, the SO10 pin holds the output value of the last bit.

Figure 16-9. Output Value of SO10 Pin (Last Bit) (1/2)

(a) Type 1: CKP10 = 0, DAP10 = 0



(b) Type 3: CKP10 = 1, DAP10 = 0

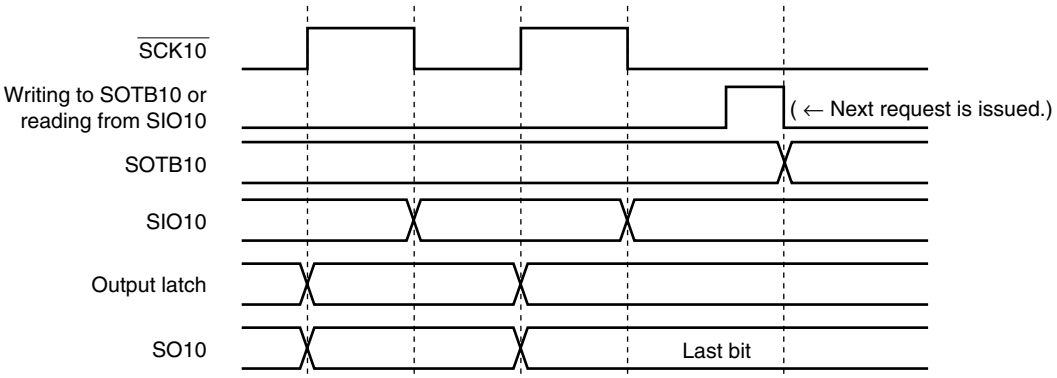
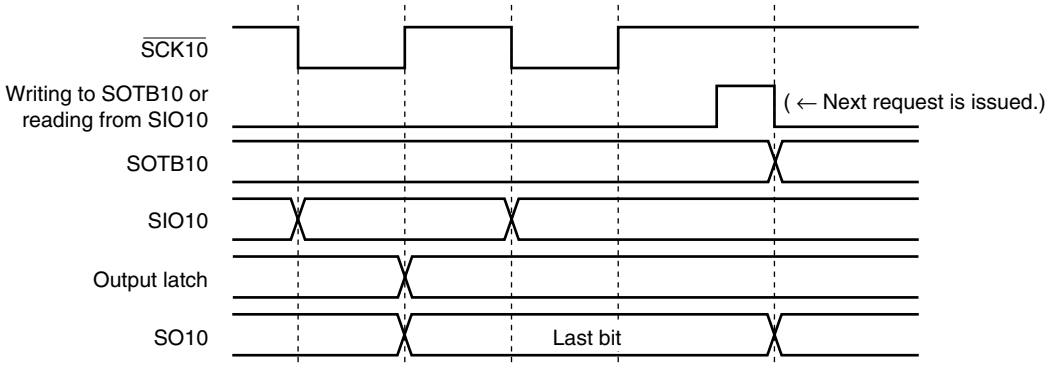
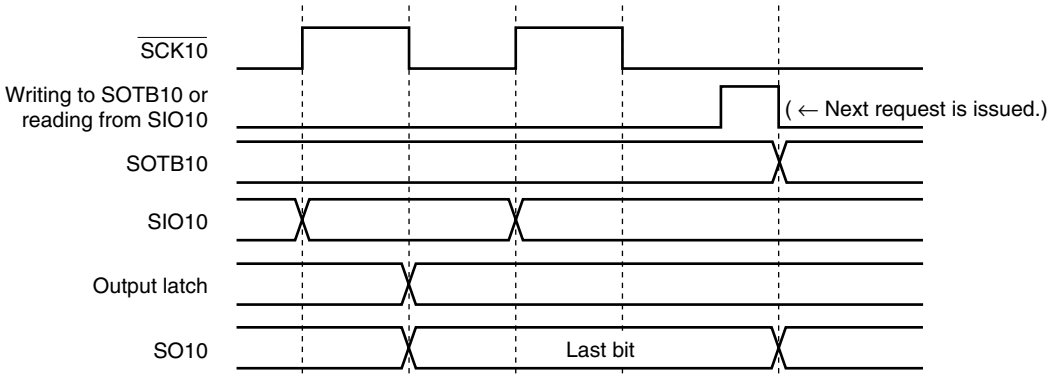


Figure 16-9. Output Value of SO10 Pin (Last Bit) (2/2)

(c) Type 2: CKP10 = 0, DAP10 = 1



(d) Type 4: CKP10 = 1, DAP10 = 1



(5) SO10 output (see Figure 16-1)

The status of the SO10 output is as follows by setting CSIE10, TRMD10, DAP10, and DIR10.

Table 16-3. SO10 Output Status

CSIE10	TRMD10	DAP10	DIR10	SO10 Output[Note 1]
CSIE10 = 0[Note 2]	TRMD10 = 0[Notes 2, 3]	–	–	Outputs low level[Note 2]
	TRMD10 = 1	DAP10 = 0	–	Outputs low leve
		DAP10 = 1	DIR 10 = 0	Value of bit 7 of SOTB10
			DIR 10 = 1	Value of bit 0 of SOTB10
CSIE10 = 1	TRMD10 = 0[Note3]	–	–	Outputs low leve
	TRMD10 = 1	–	–	Transmit data[Note 4]

Notes 1. The actual output of the SO10/P13 pin is determined according to PM13 and P13, as well as the SO10 output.

2. Status after reset.

3. To use P13/SO10 as general-purpose port, set the serial clock selection register 10 (CSIC10) in the default status (00H).

4. After transmission has been completed, the SO1n pin holds the output value of the last bit of transmission data.

Caution If a value is written to CSIE10, TRMD10, DAP10, and DIR10, the output value of SO10 changes.

CHAPTER 17 EXTENDED SFR INTERFACE

17.1 Functions of Extended SFR Interface

The extended SFR interface is implemented using a bank selection signal line and clocked serial communication. The extended SFR can be accessed by combining the bank selection signal line with serial communication.

Extended SFR interface has the following two modes.

(1) Operation stop mode

This mode is used when extended SFR interface communication is not performed and can enable a reduction in the power consumption. For details, see **17.4.1 Operation stop mode**.

(2) Serial I/O mode

In this mode, 8-bit data communication is performed by using two chip select signals (internal signals: P46 and P47), a serial clock (internal signal: $\overline{\text{SCKA0}}$), and serial data (internal signals: SIA0 and SOA0).

For details, see **17.4.2 Serial I/O mode**.

The features of extended SFR interface are as follows.

- Communication data length: 8 bits
- MSB-first data communication
- On-chip dedicated baud rate generator (6/8/16/32 divisions)
- Transmission/reception completion interrupt: INTACSI

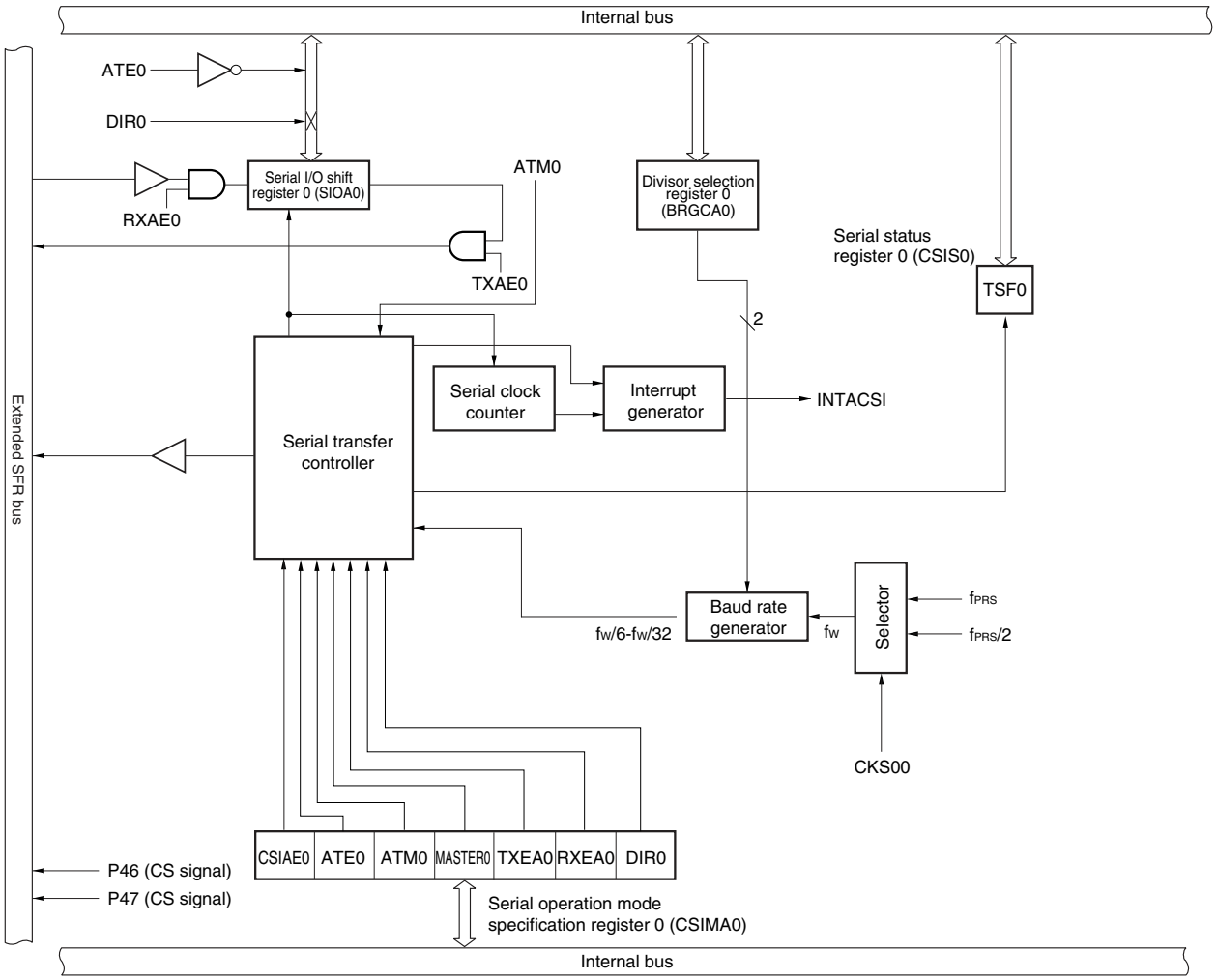
17.2 Configuration of Extended SFR Interface

Extended SFR interface consists of the following hardware.

Table 17-1. Configuration of Extended SFR Interface

Item	Configuration
Controller	Serial transfer controller
Registers	Serial I/O shift register 0 (SIOA0)
Control registers	Serial operation mode specification register 0 (CSIMA0) Serial status register 0 (CSIS0) Divisor selection register 0 (BRGCA0) Port mode register 1 (PM1) Port mode register 4 (PM4) Port register 1 (P1) Port register 4 (P4)

Figure 17-1. Block Diagram of Extended SFR Interface



(1) Serial I/O shift register 0 (SIOA0)

This is an 8-bit register used to store transmit/receive data in 1-byte transfer mode. Writing transmit data to SIOA0 starts the communication. In addition, after a communication completion interrupt request (INTACSI) is output (bit 0 (TSF0) of serial status register 0 (CSIS0) = 0), data can be received by reading data from SIOA0.

This register can be written or read by an 8-bit memory manipulation instruction. However, writing to SIOA0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

Reset signal generation clears this register to 00H.

Caution A communication operation is started by writing to SIOA0. Consequently, when transmission is disabled (bit 3 (TXEA0) of CSIMA0 = 0), write dummy data to the SIOA0 register to start the communication operation, and then perform a receive operation.

For the access to extended SFR, see **17.5 Reading from and Writing to Extended SFRs** .

17.3 Registers Controlling Extended SFR Interface

Serial interface CSIA0 is controlled by the following seven registers.

- Serial operation mode specification register 0 (CSIMA0)
- Serial status register 0 (CSIS0)
- Divisor selection register 0 (BRGCA0)
- Port mode register 1 (PM1)
- Port mode register 4 (PM4)
- Port register 1 (P1)
- Port register 4 (P4)

(1) Serial operation mode specification register 0 (CSIMA0)

This is an 8-bit register used to control the serial communication operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-2. Format of Serial Operation Mode Specification Register 0 (CSIMA0)

Address: FF90H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	1	0
CSIMA0	CSIAE0	0	0	MASTER0	TXEA0	RXEA0	0	0

CSIAE0	Control of extended SFR interface operation enable/disable
0	• Extended SFR interface operation disabled. • Asynchronously resets the internal circuit[Note].
1	Enables extended SFR interface operation

TXEA0	Control of transmit operation enable/disable
0	Transmit operation disabled
1	Transmit operation enabled

RXEA0	Control of receive operation enable/disable
0	Receive operation disabled
1	Receive operation enabled

Cautions 1. Be sure to clear bits 0, 1, 5, and 6 to "0".

2. After reset release, be sure to set bit 4 (MASTER0) to 1.

3. When CSIAE0 is changed from 1 to 0, the registers and bits[Note] mentioned in Note above are asynchronously initialized. To set CSIAE0 = 1 again, be sure to re-set the initialized registers.

Note Serial I/O shift register 0 (SIOA0) and bit 0 (TSF0) of serial status register 0 (CSIS0) are reset.

(2) Serial status register 0 (CSIS0)

This is an 8-bit register used to select the base clock, control the communication operation, and indicate the status of extended SFR interface.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, rewriting CSIS0 is prohibited when bit 0 (TSF0) is 1.

Reset signal generation clears this register to 00H.

Figure 17-3. Format of Serial Status Register 0 (CSIS0)

Address: FF91H After reset: 00H R/W[Note 1]

Symbol	7	6	5	4	3	2	1	0
CSIS0	0	CKS00	0	0	0	0	0	TSF0

CSIAE0		Control of extended SFR interface operation enable/disable[Note 2]		
		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	f_{PRS}[Note 3]	2 MHz	5 MHz	10 MHz
1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz

TSF0	Transfer status detection flag
0	• Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 • At reset input • At the end of the specified transfer
1	During data transfer

Notes 1. Bit 0 is read-only.

2. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 3.6 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

3. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS00 = 0 (base clock: f_{PRS}) is prohibited.

Cautions 1. Be sure to clear bits 1 to 5, and 7 to "0".

2. During transfer (TSF0 = 1), rewriting serial operation mode specification register 0 (CSIMA0), serial status register 0 (CSIS0), divisor selection register 0 (BRGCA0), and serial I/O shift register 0 (SIOA0) are prohibited. However, these registers can be read and re-written to the same value.

Remark f_{PRS}: Peripheral hardware clock frequency

(3) Divisor selection register 0 (BRGCA0)

This is an 8-bit register used to select the base clock divisor of extended SFR register.

This register can be set by an 8-bit memory manipulation instruction. However, when bit 0 (TSF0) of serial status register 0 (CSIS0) is 1, rewriting BRGCA0 is prohibited.

Reset signal generation sets this register to 03H.

Figure 17-4. Format of Divisor Selection Register 0 (BRGCA0)

Address: FF93H After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
BRGCA0	0	0	0	0	0	0	BRGCA01	BRGCA00

BRGCA01	BRGCA00	Selection of base clock (f_W) divisor of extended SFR interface[Note]					
			f_W = 1 MHz	f_W = 2 MHz	f_W = 2.5 MHz	f_W = 5 MHz	f_W = 10 MHz
0	0	f_W/6	166.67 kHz	333.3 kHz	416.67 kHz	833.33 kHz	1.67 MHz
0	1	f_W/8	125 kHz	250 kHz	312.5 kHz	625 kHz	1.25 MHz
1	0	f_W/16	62.5 kHz	125 kHz	156.25 kHz	312.5 kHz	625 kHz
1	1	f_W/32	31.25 kHz	62.5 kHz	78.125 kHz	156.25 kHz	312.5 kHz

Note Set the transfer clock so as to satisfy the following conditions.

- When 2.7 V ≤ V_{DD} < 3.6 V: transfer clock ≤ 833.33 kHz
- When 1.8 V ≤ V_{DD} < 2.7 V: transfer clock ≤ 555.56 kHz

Caution Specify settings so that the clock frequency supplied to extended SFRs is at least 4 times the transfer clock frequency of the extended SFR interface (see 11.3 (1) Clock output selection register (CKS)).

Remark f_W: Base clock frequency selected by CKS00 bit of CSIS0 register

f_{PRS}: Peripheral hardware clock frequency

(4) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

After reset release, be sure to clear PM10, PM14, PM16, and PM17 to 0.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 17-5. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	1	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 4, 6, and 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Cautions 1. Be sure to set bit 5 to 1.

2. After reset release, be sure to clear PM10, PM14, PM16, and PM17 to "0".

(5) Port mode register 4 (PM4)

This register sets port 4 input/output in 1-bit units.

After reset release, be sure to clear PM46 and PM47 to "0".

PM4 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 17-6. Format of Port Mode Register 4 (PM4)

Address: FF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PM4n	P4n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 4 (PM4) of 78K0/LG3-M products. For the format of port mode register 4 (PM4) of 78K0/LE3-M, see **(1) Port mode registers (PMxx and LPMxx)** in **4.3 Registers Controlling Port Function**.

Caution After reset release, be sure to clear PM46 and PM47 to "0".

(6) Port register 1 (P1)

This register write the data that is output from the chip when data is output from a port.

After reset release, be sure to set P14 to 1.

P1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 17-7. Format of Port Register 1 (P1)

Address: FF01H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
P1	P17	0	0	P14	P13	P12	P11	0

P1n	n = 0 to 4 and 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Caution After reset release, be sure to set P14 to 1.
P17 is used to reset the extended SFR (see CHAPTER 26 RESET FUNCTION).

(7) Port register 4 (P4)

P46 and P47 are chip select signals that select the extended SFR space. The range of addresses accessed in the extended SFR is specified by the combination of P46 and P47.

Figure 17-8. Format of Port Register 4 (P4)

Address: FF04H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
P4	P47	P46	P45	P44	P43	P42	P41	P40

P47	P46	Extended SFR address
0	0	Access prohibited
0	1	80H to FFH
1	0	100H to 17FH
1	1	180H to 1FFH

Remark The figure shown above presents the format of port register 4 of 78K0/LG3-M products. For the format of port register 4 of 78K0/LE3-M, see **(2) Port registers (Pxx and LPx)** in **4.3 Registers Controlling Port Function**.

17.4 Operation of Extended SFR Interface

Extended SFR interface has the following two modes.

- Operation stop mode
- Serial I/O mode

17.4.1 Operation stop mode

Extended SFR is not accessed in this mode. Therefore, the power consumption can be reduced.

(1) Register used

The operation stop mode is set by serial operation mode specification register 0 (CSIMA0). To set the operation stop mode, clear bit 7 (CSIAE0) of CSIMA0 to 0.

(a) Serial operation mode specification register 0 (CSIMA0)

This is an 8-bit register used to control the serial communication operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-9. Format of Serial Operation Mode Specification Register 0 (CSIMA0)

Address: FF90H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	1	0
CSIMA0	CSIAE0	0	0	MASTER0	TXEA0	RXEA0	0	0

CSIAE0	Control of extended SFR interface operation enable/disable
0	• Extended SFR interface operation disabled • Asynchronously resets the internal circuit[Note]

Note Serial I/O shift register 0 (SIOA0) and bit 0 (TSF0) of serial status register 0 (CSIS0) are reset.

17.4.2 Serial I/O mode

The 1-byte data transmission/reception is executed.

(1) Registers used

- Serial operation mode specification register 0 (CSIMA0)[Note 1]
- Serial status register 0 (CSIS0)[Note 2]
- Divisor selection register 0 (BRGCA0)
- Port mode register 1 (PM1)
- Port register 1 (P1)
- Port mode register 4 (PM4)
- Port register 4 (P4)

Notes 1. Bits 7, 3, and 2 (CSIAE0, TXEA0, and RXEA0) are used.

2. Bit 6 and 0 (CKS00 and TSF0) are used.

(2) Serial communication

(a) Procedure for data transmission

<1> Set bit 6 (CKS00) of the CSIS0 register (see **Figure 17-3**).
<2> Set the BRGCA0 register (see **Figure 17-4**).
<3> Set bits 3 and 2 (TXEA0 = 1, RXEA0 = x) of the CSIMA0 register (see **Figure 17-2**).
<4> Set bit 7 (CSIAE0) of the CSIMA0 register to 1 and clear bit 6 (ATE0) to 0.
<5> Write data to serial I/O shift register 0 (SIOA0). → Data transmission is started.

(b) Procedure for data reception

<1> Set bit 6 (CKS00) of the CSIS0 register (see **Figure 17-3**).
<2> Set the BRGCA0 register (see **Figure 17-4**).
<3> Set bits 3 and 2 (TXEA0 = x, RXEA0 = 1) of the CSIMA0 register (see **Figure 17-2**).
<4> Set bit 7 (CSIAE0) of the CSIMA0 register to 1 and clear bit 6 (ATE0) to 0.
<5> Write data to serial I/O shift register 0 (SIOA0). → Data reception is started[Note].

Note Even in the case of reception only (TXEA0 = 0 and RXEA0 = 1), reception operation is started by writing the dummy data to SIOA0.

(3) Communication start

Serial communication is started by setting communication data to serial I/O shift register 0 (SIOA0) when the following two conditions are satisfied.

- Extended SFR interface operation control bit (CSIAE0) = 1
- Serial communication is not in progress

Caution If CSIAE0 is set to 1 after data is written to SIOA0, communication does not start.

Upon termination of 8-bit communication, serial communication automatically stops and the interrupt request flag (ACSIIF) is set.

17.5 Reading from and Writing to Extended SFRs

The extended SFR space contains 384 bytes and is divided into 128-byte banks. A combination of bank selection and serial communication is used to access the extended SFRs for reading or writing.

(1) Specifying an extended SFR bank

The extended SFR space consists of three 128-byte banks. Banks are selected by using the bank selection signals (P47 and P46). The bank that corresponds to each chip select signal is as follows.

Table 17-2. Bank That Corresponds to Each Chip Select Signal

P47	P46	Extended SFR address
0	0	Access prohibited
0	1	80H to FFH
1	0	100H to 17FH
1	1	180H to 1FFH

Caution Changing the bank selection signal during serial communication (when TSF0 of serial status register 0 (CSIS0) is 1) is prohibited.

(2) Commands and data

Commands are used to specify extended SFRs to access.

Commands are used to specify whether to access the extended SFRs for reading or writing and to specify a bank-internal address. The type of access is specified for the most significant bit (bit 7), and the bank-internal address is specified for bits 6 to 0.

The following shows the format of access commands and data.

Figure 17-10. Access Command Format

	7	6	5	4	3	2	1	0
Command	R/W	A6	A5	A4	A3	A2	A1	A0

R/W	Specify register reading or writing
0	Reading (This setting specifies reading from the extended SFR).
1	Writing (This setting specifies writing to the extended SFR).

A6 to A0	Specify the lower 7 bits of an extended SFR address.

Figure 17-11. Data Format

	7	6	5	4	3	2	1	0
Data	D7	D6	D5	D4	D3	D2	D1	D0

D7 to D0	8-bit data to be transmitted or received.

(3) Reading extended SFRs

The data in extended SFRs is accessed for reading by performing the following procedure:

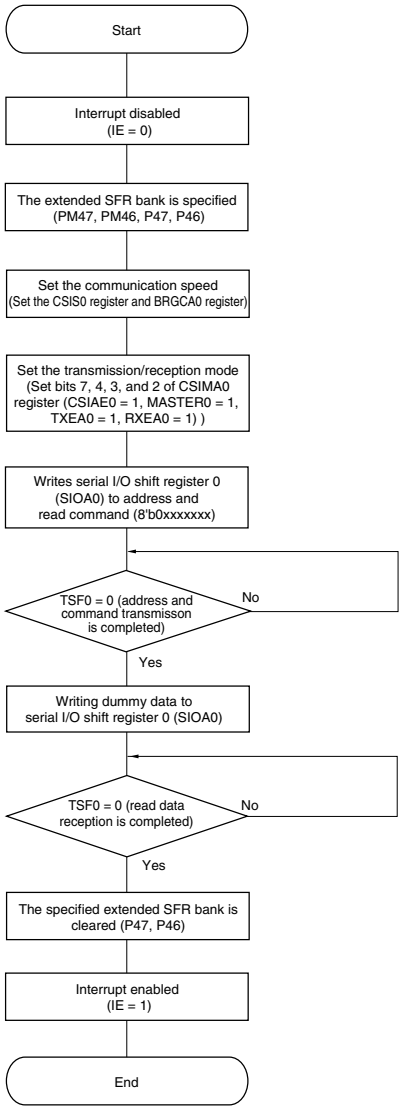
<1> Selecting an extended SFR bank (P47, P46)
<2> Transmitting an access command
<3> Receiving read data
<4> Clearing the extended SFR bank selection (P47, P46)

Cautions 1. Be sure to clear the SFR banks if accessing non-sequential addresses, even if the addresses are in the same bank.
2. Only access the extended SFR register while interrupts are disabled (IE = 0).

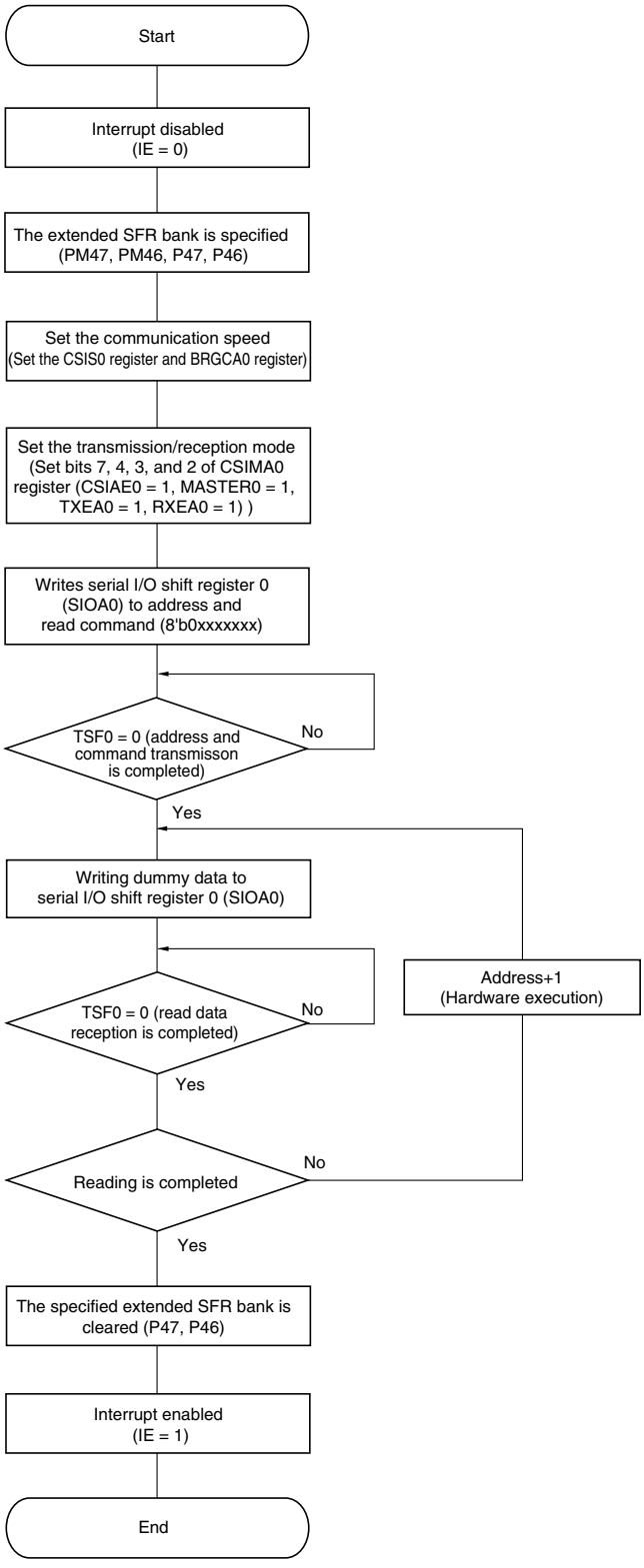
Note that, if reading data at sequential addresses, the second and subsequent command transmissions can be omitted. After the data reading in step <3> finishes, the extended SFR interface increments the address and sequentially reads the data. Because the processing to issue commands can be omitted, data can be read at high speed. The relationship between the register settings and pins is shown below.

Figure 17-12. Accessing Data in Extended SFRs for Reading

(a) If reading non-sequential addresses



(b) If reading sequential addresses



(4) Writing extended SFRs

The data in extended SFRs is accessed for writing by performing the following procedure:

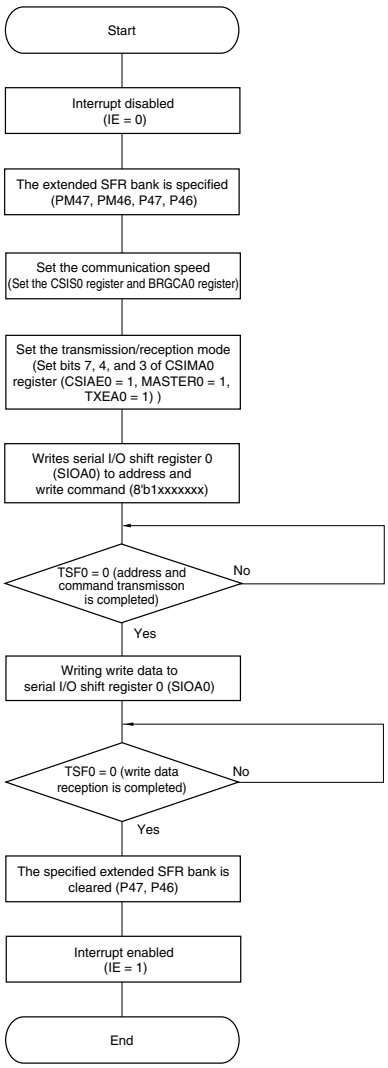
<1> Selecting an extended SFR bank (P47, P46)
<2> Transmitting an access command
<3> Transmitting write data
<4> Clearing the extended SFR bank selection (P47, P46)

Cautions 1. Be sure to clear the SFR banks if accessing non-sequential addresses, even if the addresses are in the same bank.
2. Only access the extended SFR register while interrupts are disabled (IE = 0).
3. If an internal reset is triggered while using the extended SFR interface to transmit data, the data might not be correctly transmitted to an extended SFR.

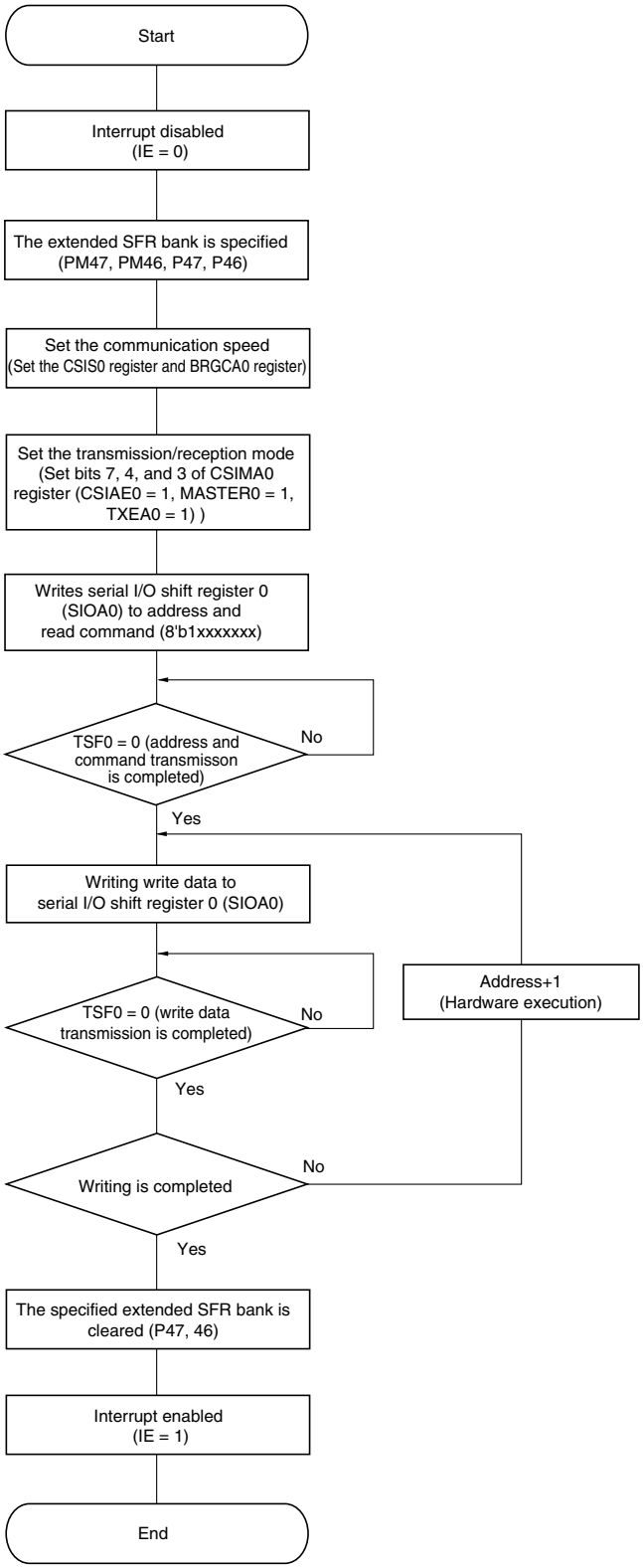
Note that, if writing data at sequential addresses, the second and subsequent command transmissions can be omitted. Repeating the write data transmission in step <3> makes it possible to continuously write data. Because the processing to issue commands can be omitted, data can be written at high speed.

Figure 17-13. Accessing Data in Extended SFRs for Writing

(a) If writing non-sequential addresses



(b) If writing sequential addresses



CHAPTER 18 LCD CONTROLLER/DRIVER

		78K0/LE3-M	78K0/LG3-M
LCD controller/driver	Segment signal	24	40
	Common signal	4	4

18.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the 78K0/Lx3-M microcontrollers are as follows.

(1) The LCD driver voltage generator can switch external resistance division and internal resistance division.
(2) Automatic output of segment and common signals based on automatic display data memory read
(3) Five different display modes:
- Static
- 1/2 duty (1/2 bias)
- 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)

(4) Six different frame frequencies, selectable in each display mode
(5) 78K0/LE3-M: Segment signal outputs: 24 (SEG0 to SEG23),
Common signal outputs: 4 (COM0 to COM3)
78K0/LG3-M: Segment signal outputs: 40 (SEG0 to SEG39),
Common signal outputs: 4 (COM0 to COM3)
(6) Output of LCD segment signals and time division output of segment key source signals in each display mode (except static mode)[Note]
Segment key source signal outputs: Max. 8 (SEG24 (KS0) to SEG31 (KS7))

Note 78K0/LG3-M only.

Table 18-1 lists the maximum number of pixels that can be displayed in each display mode.

Table 18-1. Maximum Number of Pixels

(a) 78K0/LE3-M

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	24	24 (24 segment × 1 common)Note 2
	1/2	2Note 1	COM0, COM1		48 (24 segment × 2 common)Note 3
		3Note 1	COM0 to COM2		72 (24 segment × 3 common)Note 4
	1/3	3Note 1	COM0 to COM2		
		4Note 1	COM0 to COM3		96 (24 segment × 4 common)Note 5

Notes 1. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

2. 3-digit LCD panel, each digit having an 8-segment configuration.

3. 6-digit LCD panel, each digit having a 4-segment configuration.

4. 9-digit LCD panel, each digit having a 3-segment configuration.

5. 12-digit LCD panel, each digit having a 2-segment configuration.

(b) 78K0/LG3-M

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	40	40 (40 segment × 1 common)Note 2
	1/2	2Note 1	COM0, COM1		80 (40 segment × 2 common)Note 3
		3Note 1	COM0 to COM2		120 (40 segment × 3 common)Note 4
	1/3	3Note 1	COM0 to COM2		
		4Note 1	COM0 to COM3		160 (40 segment × 4 common)Note 5

Notes 1. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

2. 5-digit LCD panel, each digit having an 8-segment configuration.

3. 10-digit LCD panel, each digit having a 4-segment configuration.

4. 15-digit LCD panel, each digit having a 3-segment configuration.

5. 20-digit LCD panel, each digit having a 2-segment configuration.

18.2 Configuration of LCD Controller/Driver

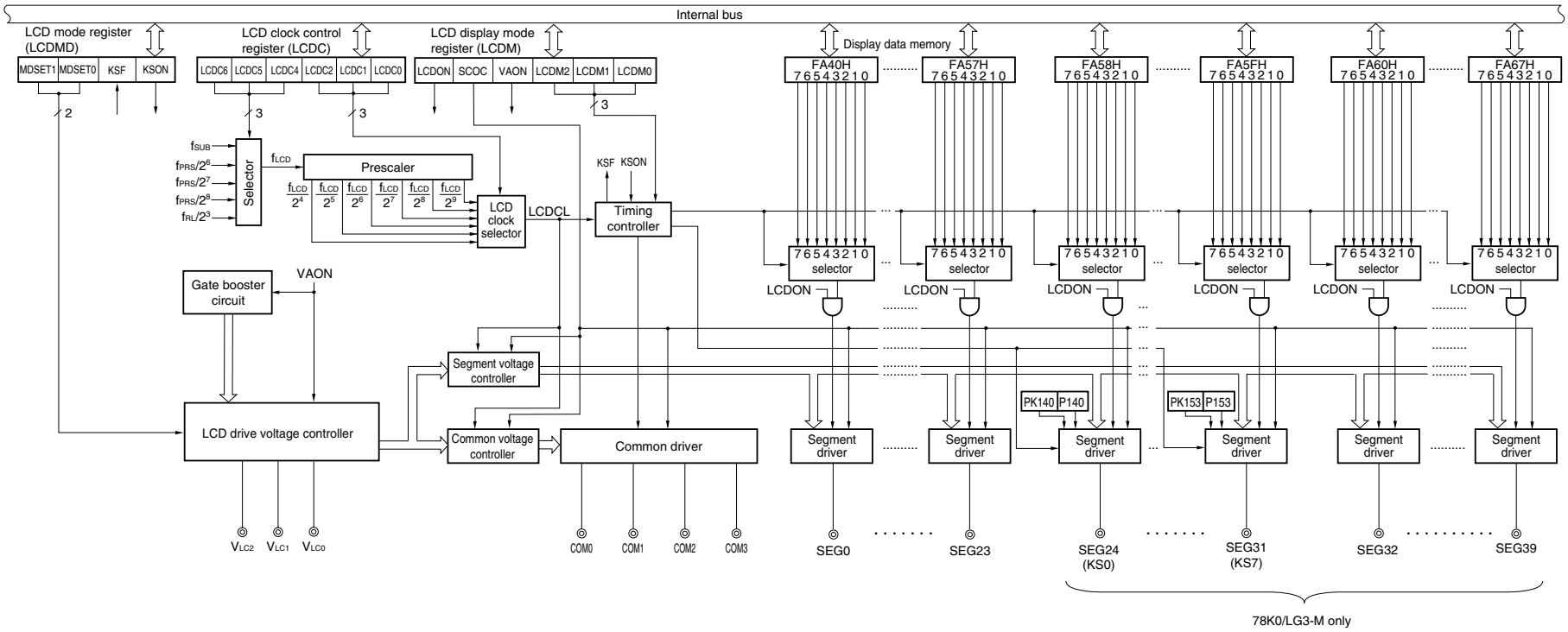
The LCD controller/driver consists of the following hardware.

Table 18-2. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	78K0/LE3-M: Segment signal outputs: 24, Common signals: 4 78K0/LG3-M: Segment signal outputs: 40, Common signals: 4
Segment key source output[Note]	Segment key source signal: 8
Control registers	LCD mode register (LCDMD) LCD display mode register (LCDM) LCD clock control register (LCDC0) Port function register 2 (PF2)[Note] Port function register ALL (PFALL) Key return mode register (KRM) Port mode register 4 (PM4) Pull-up resistor option register 4 (PU4) Port register 14 (P14) Port register 15 (P15)

Note 78K0/LG3-M only.

Figure 18-1. Block Diagram of LCD controller/Driver



Remark 78K0/LE3-M: SEG0 to SEG23
78K0/LG3-M: SEG0 to SEG23, SEG24 (KS0) to SEG31 (KS7), SEG32 to SEG39

18.3 Registers Controlling LCD Controller/Driver

The following registers are used to control the LCD controller/driver.

- LCD mode register (LCDMD)
- LCD display mode register (LCDM)
- LCD clock control register (LCDC0)
- Port function register 2 (PF2)[Note]
- Port function register ALL (PFALL)
- Key return mode register (KRM)
- Port mode register 4 (PM4)
- Pull-up resistor option register 4 (PU4)
- Port register 14 (P14)
- Port register 15 (P15)

Note 78K0/LG3-M only.

(1) LCD mode register (LCDMD)

LCDMD sets the LCD drive voltage generator.

LCDMD is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDMD to 00H.

Figure 18-2. Format of LCD Mode Register (LCDMD)

Address: FFB0H After reset: 00H R/W[note 1]

Symbol	7	6	5	4	3	2	1	0
LCDMD	0	0	MDSET1	MDSET0	0	0	KSF	KSON

MDSET1	MDSET0	LCD drive voltage generator selection
0	0	External resistance division method, internal resistor disconnection
0	1	Internal resistance division method, internal resistor connection (no step-down transforming, Used when $V_{LCD} = V_{DD}$)
Other than above		Setting prohibited

KSF	Segment key scan status
0	LCD display signal being output
1	Segment key scan signal being output

KSON	Segment key scan function control
0	Segment key scan function is not used
1	Segment key scan function is used[note 2]

Notes 1. Bit 1 is read-only.

2. Use the segment key scan function if V_{DD} is equal to V_{LC0}.
Only the KRx pin can be used as input pins for the segment key scan function.

Caution Bits 0 to 2, 3, 6 and 7 must be set to 0.

(2) LCD display mode register (LCDM)

LCDM specifies whether to enable display operation. It also specifies whether to enable segment pin/common pin output, gate booster circuit control, and the display mode.

LCDM is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDM to 00H.

Figure 18-3. Format of LCD Display Mode Register (LCDM)

Address: FFB1H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	2	1	0
LCDM	LCDON	SCOC	0	VAON	0	LCDM2	LCDM1	LCDM0

LCDON	LCD display enable/disable
0	Display off (all segment outputs are deselected.)
1	Display on

SCOC	Segment pin/common pin output control[Note 1]
0	Output ground level to segment/common pin
1	Output deselect level to segment pin and LCD waveform to common pin

VAON	Gate booster circuit control[Notes 1, 2]
0	No gate voltage boosting
1	Gate voltage boosting

LCDM2	LCDM1	LCDM0	LCD controller/driver display mode selection	
			Resistance division method	
			Number of time slices	Bias mode
0	0	0	4 [Note 3]	1/3
0	0	1	3 [Note 3]	1/3
0	1	0	2 [Note 3]	1/2
0	1	1	3 [Note 3]	1/2
1	0	0	Static	
Other than above			Setting prohibited	

(**Note** and **Caution** are listed on the next page.)

Notes 1. When LCD display is not to be performed or not required, power consumption can be reduced by using the following settings.

<1> Set both SCOC and VAON to 0.

<2> When the internal resistance division method is used, assume MDSET1, MDSET0 = (0, 0).

(The current flowing to the internal resistors can be reduced.)

2. This bit is used to control boosting of the internal gate signal of the LCD controller/driver.

If set to "Internal gate voltage boosting", the LCD drive performance can be enhanced.

Set VAON based on the following conditions.

<When set to the static display mode>

- When 2.0 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/3 bias method>

- When 2.5 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method >

- When 2.7 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

3. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

Cautions 1. Bits 3 and 5 must be set to 0.

2. When displaying in a mode with a large number of COMs, V_{LC0} may not be able to obtain sufficient contrast under the low-voltage conditions, depending on the panel characteristics. Use the LCD controller/driver after having performed thorough LCD display evaluation and confirmed that there are no problems regarding the display quality.

(3) LCD clock control register (LCDC0)

LCDC0 specifies the LCD source clock and LCD clock.

The frame frequency is determined according to the LCD clock and the number of time slices.

LCDC0 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDC0 to 00H.

Figure 18-4. Format of LCD Clock Control Register (LCDC0)

Address: FFB2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC0	0	LCDC6	LCDC5	LCDC4	0	LCDC2	LCDC1	LCDC0

LCDC6	LCDC5	LCDC4	LCD source clock (f_{LCD}) selection
0	0	0	f_{XT} (32.768 kHz) Note
0	0	1	$f_{PRS}/2^6$
0	1	0	$f_{PRS}/2^7$
0	1	1	$f_{PRS}/2^8$
1	0	0	$f_{RL}/2^3$
Other than above			Setting prohibited

LCDC2	LCDC1	LCDC0	LCD clock (LCDCL) selection
0	0	0	$f_{LCD}/2^4$
0	0	1	$f_{LCD}/2^5$
0	1	0	$f_{LCD}/2^6$
0	1	1	$f_{LCD}/2^7$
1	0	0	$f_{LCD}/2^8$
1	0	1	$f_{LCD}/2^9$
Other than above			Setting prohibited

Note Before select the f_{XT}, set the EXCLKS and OSCSELS bits of OSCCTL register, EXCLKS2 and FXTOUTEN of PORTCTL register.

Caution Be sure to clear bits 3 and 7 to 0.

Remarks 1. f_{XT}: XT1 clock oscillation frequency

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{RL}: Internal low-speed oscillation clock frequency

(4) Port function register 2 (PF2)[Note]

This register sets whether to use pins P20 to P27 as port pins (other than segment output pins) or segment output pins.

PF2 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF2 to 00H.

Note 78K0/LG3-M only.

Figure 18-5. Format of Port Function Register 2 (PF2)

Address: FFB5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF2	PF27	PF26	PF25	PF24	PF23	PF22	PF21	PF20

PF2n	Port/segment output specification (n = 0 to 7)
0	Used as port (other than segment output)
1	Used as segment output

(5) Port function register ALL (PFALL)

This register sets whether to use pins P8 to P11 and P13 to P15 as port pins (other than segment output pins) or segment output pins.

PFALL is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PFALL to 00H.

Figure 18-6. Format of Port Function Register ALL (PFALL)

(a) 78K0/LE3-M

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	0	0	PF13ALL	PF11ALL	PF10ALL	PF09ALL	PF08ALL

(b) 78K0/LG3-M

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	PF13ALL	PF11ALL	PF10ALL	PF09ALL	PF08ALL

PFnALL	Port/segment output specification (n = 08 to 11, 13 to 15)
0	Used as port (other than segment output)
1	Used as segment output

(6) Key return mode register (KRM)

This register is used to specify that a pin is to be used as a segment key scan input pin when using the segment key scan function[Note].

See Figure 21-2 Format of Key Return Mode Register (KRM) when not using the segment key scan function.

KRM is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Note 78K0/LG3-M only.

Figure 18-7. Format of Key return mode register (KRM) (78K0/LG3-M)

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Setting segment key scan input pin (n = 0 to 5)
0	Does not use specified pin as segment key scan input pin.
1	Uses specified pin as segment key scan input pin.

Cautions 1. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

2. When set not to use the specified pin as a segment key scan input pin (KRMn = 0), the corresponding pin can be used as a normal port.

(7) Port mode register 4 (PM4)

This register sets port 4 input/output in 1-bit units.

When using the segment key scan function[Note], set the port mode register of the port to be used to 1 (PM4n = 1), in order to set the P4n pin as a key scan input pin.

PM4 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets FFH.

Note 78K0/LG3-M only.

Figure 18-8. Format of Port mode register 4 (PM4) (78K0/LG3-M)

Address: FF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PF4n	P4n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution After the reset release, be sure to clear the PM46 and PM47 to "0".

(8) Pull-up resistor option register 4 (PU4)

This register is used to set whether to use the on-chip pull-up resistors of P40 to P45.

When using the segment key scan function[Note], set the pull-up resistor option register of the port to be used to 0 (PU4n = 0), in order to set the P4n pin as a key scan input pin.

An external pull-up resistor cannot be used, because it affects the LCD display output.

PU4 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Note 78K0/LG3-M only.

Figure 18-9. Format of Pull-up Resistor Option Register 4 (PU4)

Address: FF34H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU4	0	0	PU45	PU44	PU43	PU42	PU41	PU40

PF4n	P4n pin on-chip pull-up resistor selection (n = 0 to 5)	
	Pin using segment key scan function	Pin not using segment key scan function
0	On-chip pull-up resistor connected only during segment key scan output period	On-chip pull-up resistor not connected
1	Setting prohibited	On-chip pull-up resistor connected

(9) Port register 14 (P14)

This register is used to perform the first half of KS0 to KS3 output control by using bits 0 to 3, and the latter half of KS0 to KS3 output control by using bits 4 to 7, when using the segment key scan function[Note].

When using the P14n pin for segment key scan output, the P14n and PK14n bits are used for control.

See **4.3 Registers Controlling Port Function (2) Port registers (Pxx and LPx)** when not using the segment key scan function.

P14 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Note 78K0/LG3-M only.

Figure 18-10. Format of Port register 14 (P14)

Address: FF0EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
P14	PK143	PK142	PK141	PK140	P143	P142	P141	P140

P140 to P143	First half of KS0 to KS3 output control
0	Low-level output
1	High-level output

PK140 to PK143	Latter half of KS0 to KS3 output control
0	Low-level output
1	High-level output

(10) Port register 15 (P15)

This register is used to perform the first half of KS4 to KS7 output control by using bits 0 to 3, and the latter half of KS4 to KS7 output control by using bits 4 to 7, when using the segment key scan function[Note].

When using the P15n pin for segment key scan output, the P15n and PK15n bits are used for control.

See **4.3 Registers Controlling Port Function (2) Port registers (Pxx and LPx)** when not using the segment key scan function.

P15 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Note 78K0/LG3-M only.

Figure 18-11. Format of Port register 15 (P15)

Address: FF0FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
P15	PK153	PK152	PK151	PK150	P153	P152	P151	P150

P150 to P153	First half of KS4 to KS7 output control
0	Low-level output
1	High-level output

PK150 to PK153	Latter half of KS4 to KS7 output control
0	Low-level output
1	High-level output

18.4 Setting LCD Controller/Driver

18.4.1 Setting method when not using segment key scan function (KSON = 0)

When not using the segment key scan function (KSON = 0), set the LCD controller/driver as follows. Set the LCD controller/driver using the following procedure.

<1> Set (VAON = 1) internal gate voltage boosting (bit 4 of the LCD display mode register (LCDM)).[Note]
<2> Set the resistance division method via MDSET0 and MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) (MDSET0 = 0: external resistance division method, MDSET0 = 1: internal resistance division method).
<3> Set the pins to be used as segment outputs to the port function registers (PF2m, PFnALL).
<4> Set an initial value to the RAM for LCD display.
<5> Set the number of time slices via LCDM0 to LCDM2 (bits 0 to 2 of the LCD display mode register (LCDM)).
<6> Set the LCD source clock and LCD clock via LCD clock control register 0 (LCDC0).
<7> Set (SCOC = 1) SCOC (bit 6 of the LCD display mode register (LCDM)).
Deselect signals are output from all the segment and common pins, and the non-display status is entered.
<8> Start output corresponding to each data memory by setting (LCDON = 1) LCDON (bit 7 of LCDM).

Subsequent to this procedure, set the data to be displayed in the data memory.

Note Set VAON based on the following conditions.
<When set to the static display mode>
- When 2.0 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/3 bias method>
- When 2.5 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method >
- When 2.7 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

Remarks 1. Use the following procedure to set to the display-off state and disconnect the internal resistors when using the internal resistance division method.
<1> Clear LCDON (bit 7 of LCDM) (LCDON = 0).
Deselect signals are output from all segment pins and common pins, and a non-display state is entered.
<2> Clear SCOC (bit 6 of the LCD display mode register (LCDM)) (SCOC = 0).
Ground levels are output from all segment pins and common pins.
<3> Assume MDSET0, MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) = (0, 0) and set the resistance division method to the external resistance division method.

2. m = 0 to 7, n = 08 to 11, 13 to 15

Caution When displaying in a mode with a large number of COMs, V_{LC0} may not be able to obtain sufficient contrast under the low-voltage conditions, depending on the panel characteristics. Use the LCD controller/driver after having performed thorough LCD display evaluation and confirmed that there are no problems regarding the display quality.

18.4.2 Setting method when using segment key scan function (KSON = 1)

When using the segment key scan function (KSON = 1), set the LCD controller/driver as follows. Set the LCD controller/driver using the following procedure.

<1> Set (VAON = 1) internal gate voltage boosting (bit 4 of the LCD display mode register (LCDM)).[Note 1]
<2> Set the resistance division method via MDSET0 and MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) (MDSET0 = 0: external resistance division method, MDSET0 = 1: internal resistance division method), Set (KSON = 1) KSON (bit 0 of the LCD mode register (LCDMD)).
<3> Set the pins to be used as segment outputs to the port function registers (PF2m, PFnALL).
<4> Use port mode register 4 (PM4) to set the pin to be used as a key scan input pin[Note 2] to PM4m = 1 (input mode).
<5> Use pull-up resistor option register 4 (PU4) to set the pin to be used as a key scan input pin[Note 2] to PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
<6> Use the key return mode register (KRM) to set the pin to be used as a segment key scan input pin to KRMm = 1[Note 3]
<7> Set an initial value to the RAM for LCD display.
<8> Set an initial value of segment key scan output to P14, P15.
<9> Set the number of time slices via LCDM0 to LCDM2 (bits 0 to 2 of the LCD display mode register (LCDM)).
<10> Set the LCD source clock and LCD clock via LCD clock control register 0 (LCDC0).
<11> Set (SCOC = 1) SCOC (bit 6 of the LCD display mode register (LCDM)).
Deselect signals are output from all the segment and common pins, and the non-display status is entered.
<12> Start output corresponding to each data memory by setting (LCDON = 1) LCDON (bit 7 of LCDM).

Hereinafter, set data to the data memory according to the contents displayed, and perform segment key scan output settings for the port registers (P14, P15) according to the contents of the segment key scan output.

Notes 1. Set VAON based on the following conditions.

<When set to the 1/3 bias method>
- When 2.5 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method>
- When 2.7 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

2. When using the segment key scan function, be sure to set port 4 as a segment key scan input pin and the pull-up resistor option register of the port to be used to PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
An external pull-up resistor cannot be used, because it affects the LCD display output.

3. An interrupt request flag may be set when KRM has been changed. Consequently, change the KRM register after having disabled interrupts, and enable interrupts after having cleared the interrupt request flag.

Remarks 1. Use the following procedure to set to the display-off state and disconnect the internal resistors when using the internal resistance division method.

<1> Clear LCDON (bit 7 of LCDM) (LCDON = 0).
Deselect signals are output from all segment pins and common pins, and a non-display state is entered.

<2> Clear SCOC (bit 6 of the LCD display mode register (LCDM)) (SCOC = 0).
Ground levels are output from all segment pins and common pins.

<3> Assume MDSET0, MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) = (0, 0) and set the resistance division method to the external resistance division method.

2. m = 0 to 7, n = 08 to 11, 13 to 15

Caution When displaying in a mode with a large number of COMs, V_{LC0} may not be able to obtain sufficient contrast under the low-voltage conditions, depending on the panel characteristics. Use the LCD controller/driver after having performed thorough LCD display evaluation and confirmed that there are no problems regarding the display quality.

18.5 LCD Display Data Memory

The LCD display data memory is mapped at following addresses of each product.

- 78K0/LE3-M: FA40H to FA55H
- 78K0/LG3-M: FA40H to FA57H

Data in the LCD display data memory can be displayed on the LCD panel using the LCD controller/driver.

Figure 18-12 shows the relationship between the contents of the LCD display data memory and the segment/common outputs.

The areas not to be used for display can be used as normal RAM.

Figure 18-12. Relationship between LCD Display Data Memory Contents and Segment/Common Outputs

	b7	b6	b5	b4	b3	b2	b1	b0	
FA67H	0	0	0	0					SEG39
FA66H	0	0	0	0					SEG38
FA65H	0	0	0	0					SEG37
⋮									
FA45H	0	0	0	0					SEG5
FA44H	0	0	0	0					SEG4
FA43H	0	0	0	0					SEG3
FA42H	0	0	0	0					SEG2
FA41H	0	0	0	0					SEG1
FA40H	0	0	0	0					SEG0
					COM3	COM2	COM1	COM0	

Caution No memory is allocated to the higher 4 bits of FA40H to FA67H. Be sure to set there bits to 0.

Remark 78K0/LE3-M: SEG0 to SEG23 (FA40H to FA57H)
78K0/LG3-M: SEG0 to SEG39 (FA40H to FA67H)

18.6 Common and Segment Signals

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, V_{LCD}). The pixels turn off when the potential difference becomes lower than V_{LCD}.

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, this LCD panel is driven by AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slices at the timing listed in Table 18-3. In the static display mode, the same signal is output to COM0 to COM3.

When using the segment key scan output function (KSON = 1), segment key scan output will be performed for a period of one time slice after one LCD output cycle. The common signal generated at that time will not be displayed when output.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Table 18-3. COM Signals

Number of Time Slices \ COM Signal	COM0	COM1	COM2	COM3
Static display mode				
Two-time-slice mode**Note**			Open	Open
Three-time-slice mode**Note**				Open
Four-time-slice mode**Note**				

Note When using the segment key scan output function (KSON = 1), non-display output will be performed for a period of one time slice after one LCD output cycle.

(2) Segment signals

The segment signals correspond to the LCD display data memory (see **18.5 LCD Display Data Memory**) during an LCD display period, bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins.

Furthermore, segment signals correspond to the setting values of port registers 14 and 15 during a segment key scan output period. Bits 0 to 3 and bits 4 to 7 of each port register will be read in synchronization with the first half and latter half of the segment key scan output period, respectively, and if the content of each bit is 1 or 0, high levels or low levels will be output to the segment pins, respectively.

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data memory, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

LCD display data memory bits 1 to 3, bits 2 and 3, and bit 3 are not used for LCD display in the static display, two-time slot, and three-time slot modes, respectively. So these bits can be used for purposes other than display.

The higher 4 bits of FA40H to FA67H are fixed to 0.

Remark The mounted segment pins vary depending on the product.

- 78K0/LE3-M: SEG0 to SEG23
- 78K0/LG3-M: SEG0 to SEG39

(3) Output waveforms of common signals and segment signals during LCD display signal output period

The voltages shown in Table 18-4 are output to the common signals and segment signals during the LCD display signal output period.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained. The other combinations of the signals correspond to the display off-voltage.

Table 18-4. LCD Drive Voltage

(a) Static display mode (during LCD display signal output period)

Segment Signal / Common Signal	Select Signal Level	Deselect Signal Level
	V_{SS}/V_{LC0}	V_{LC0}/V_{SS}
V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

(b) 1/2 bias method (during LCD display signal output period)

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{LC0}	V_{LC0}/V_{SS}
Select signal level	V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V
Deselect signal level	$V_{LC1} = V_{LC2}$	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$

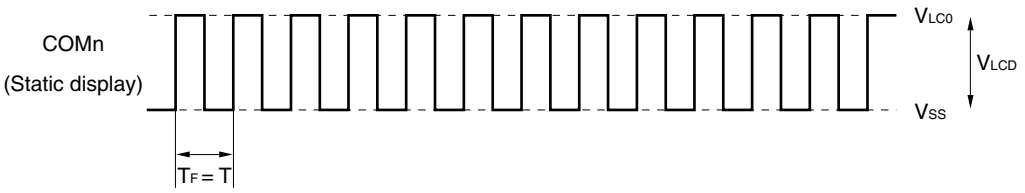
(c) 1/3 bias method (during LCD display signal output period)

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{LC0}	V_{LC1}/V_{LC2}
Select signal level	V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{LC2}/V_{LC1}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$+\frac{1}{3}V_{LCD}/-\frac{1}{3}V_{LCD}$

Figure 18-13 shows the common signal waveforms, and Figure 18-14 shows the voltages and phases of the common and segment signals.

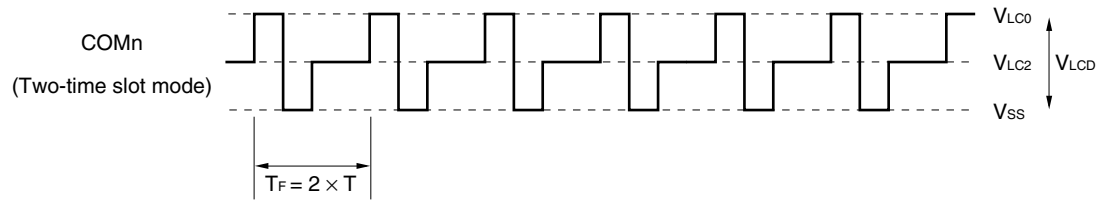
Figure 18-13. Common Signal Waveforms

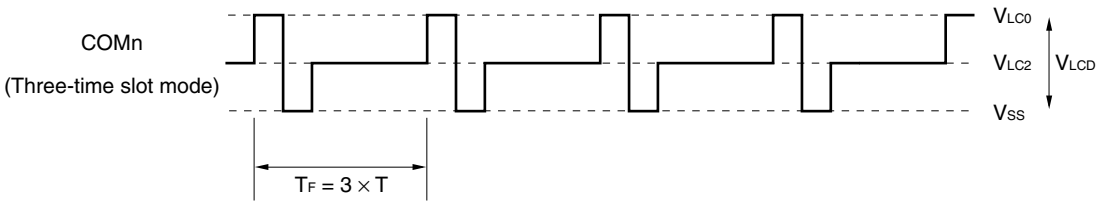
(a) Static display mode



T: One LCD clock period T_F: Frame frequency

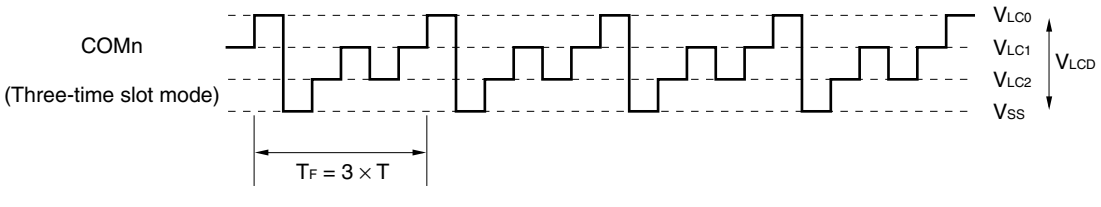
(b) 1/2 bias method

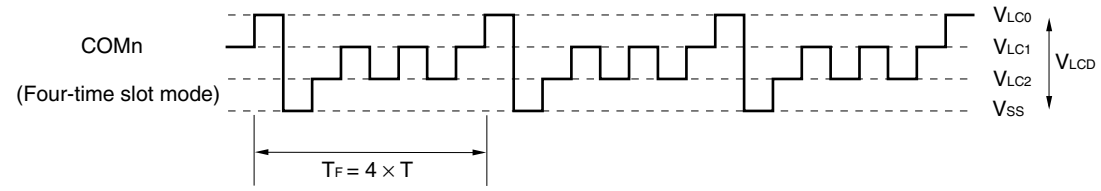




T: One LCD clock period T_F: Frame frequency

(c) 1/3 bias method

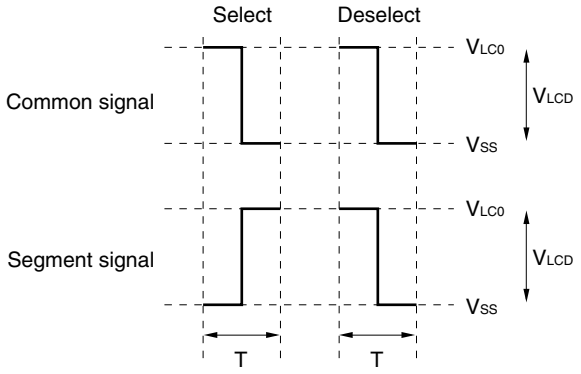




T: One LCD clock period T_F: Frame frequency

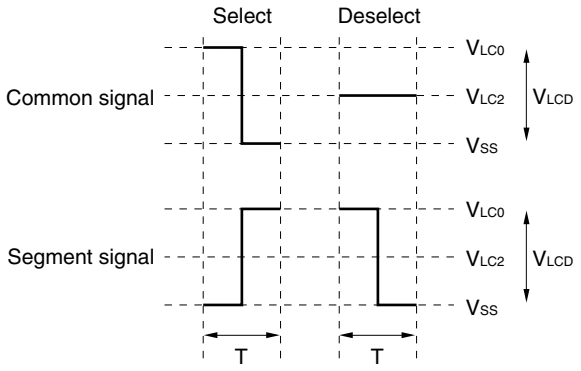
Figure 18-14 Voltages and Phases of Common and Segment Signals

(a) Static display mode



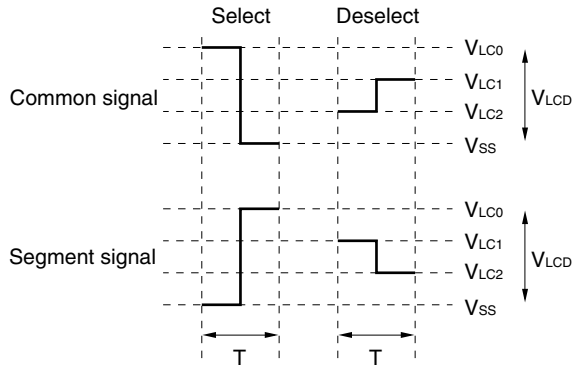
T: One LCD clock period

(b) 1/2 bias method



T: One LCD clock period

(c) 1/3 bias method



T: One LCD clock period

(4) Output waveforms of common and segment signals during segment key scan output period

The voltages shown in Table 18-5 are output to the common signals and segment signals during the segment key scan output period.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained. The other combinations of the signals correspond to the display off-voltage.

Table 18-5. LCD Drive Voltage

(a) 1/2 bias method (during segment key scan output period)

Common Signal \ Key scan Signal		P14x = P15x = 1	P14x = P15x = 0
		V_{D0}	V_{SS}
Deselect signal level	$V_{LC1} = V_{LC2}$	$+\frac{1}{2}V_{LCD}$	$-\frac{1}{2}V_{LCD}$

(b) 1/3 bias method (during segment key scan output period)

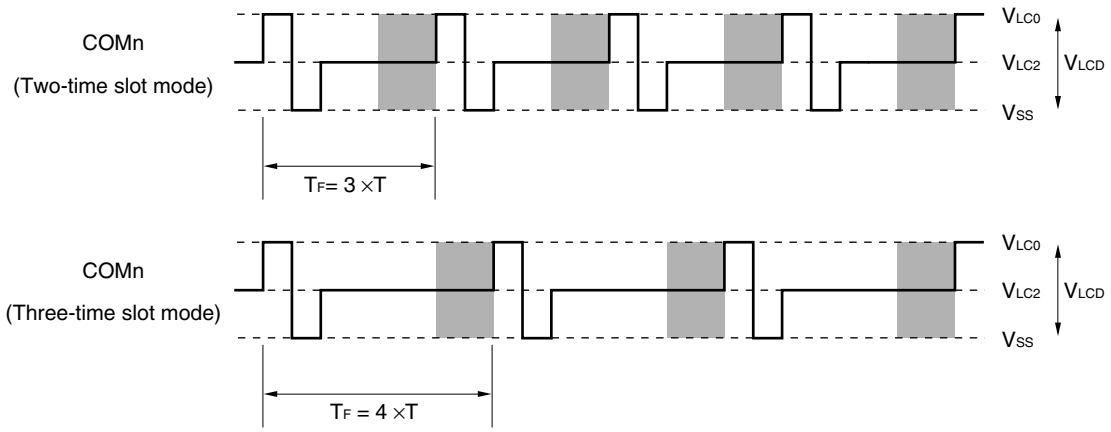
Common Signal \ Key scan Signal		P14x = P15x = 1	P14x = P15x = 0
		V_{DD}	V_{SS}
Deselect signal level	V_{LC2}/V_{LC1}	$+\frac{2}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$-\frac{1}{3}V_{LCD}/-\frac{2}{3}V_{LCD}$

Remark The segment key scan output function cannot be used in the static display mode.

Figure 18-15 shows the common signal waveforms, and Figure 18-16 shows the voltages and phases of the common and segment signals.

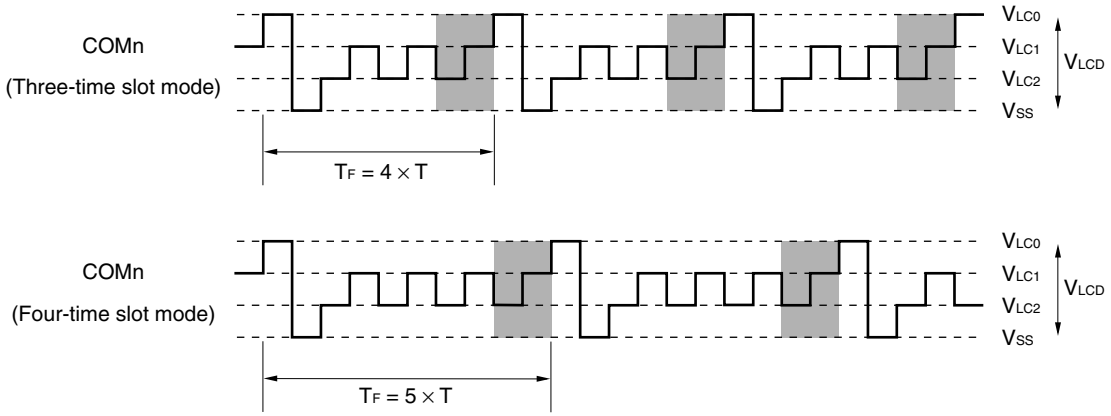
Figure 18-15 Common Signal Waveforms

(a) 1/2 bias method



T: One LCD clock period T_F: Frame frequency Shaded sections: Segment key scan output period

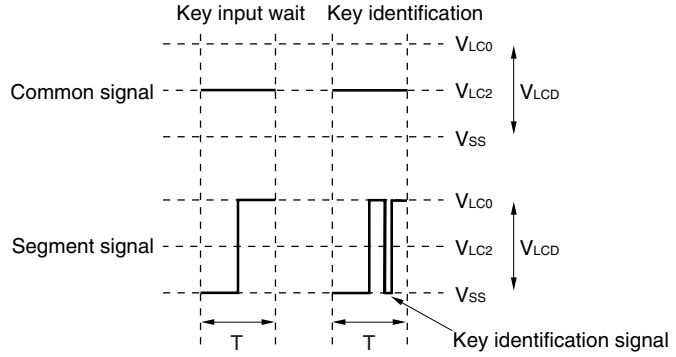
(b) 1/3 bias method



T: One LCD clock period T_F: Frame frequency Shaded sections: Segment key scan output period

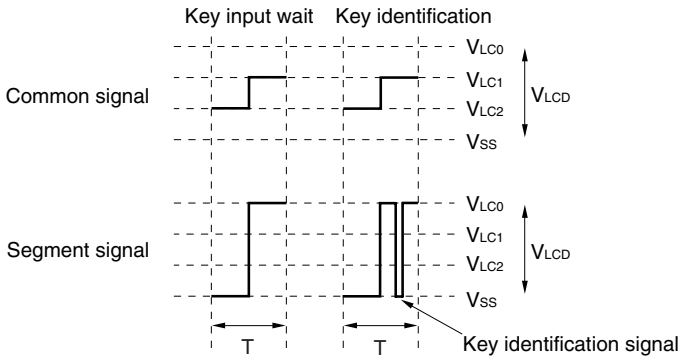
Figure 18-16 Voltages and Phases of Common and Segment Signals

(a) 1/2 bias method



T: One LCD clock period

(b) 1/3 bias method



T: One LCD clock period

Remark Segment key scan signals must be set by using port registers 14 and 15 (P14, P15).

18.7 Display Modes

18.7.1 Static display example

Figure 18-18 shows how the three-digit LCD panel having the display pattern shown in Figure 18-17 is connected to the segment signals (SEG0 to SEG23) and the common signal (COM0) of the 78K0/Lx3-M chip. This example displays data "12.3" in the LCD panel. The contents of the display data memory (FA40H to FA57H) correspond to this display.

The following description focuses on numeral "2." (2.) displayed in the second digit. To display "2." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG8 to SEG15 pins according to Table 18-6 at the timing of the common signal COM0; see **Figure 18-17** for the relationship between the segment signals and LCD segments.

Table 18-6. Select and Deselect Voltages (COM0)

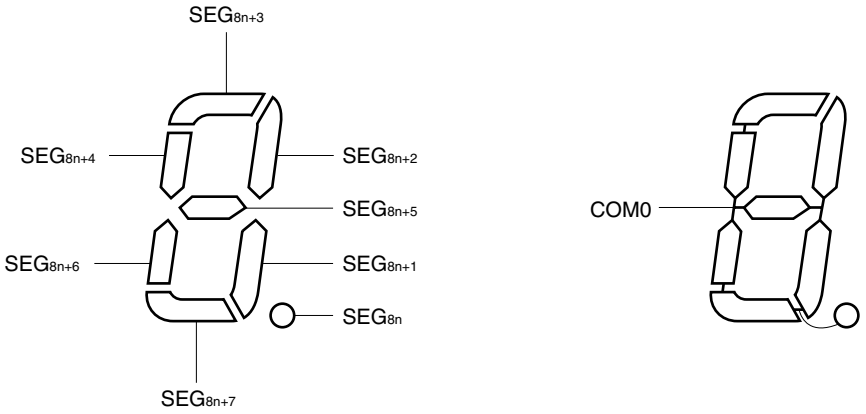
Segment / Common	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM0	Select	Deselect	Select	Select	Deselect	Select	Select	Select

According to Table 18-6, it is determined that the bit-0 pattern of the display data memory locations (FA48H to FA4FH) must be 10110111.

Figure 18-19 shows the LCD drive waveforms of SEG11 and SEG12, and COM0. When the select voltage is applied to SEG11 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

Figure 18-17 Static LCD Display Pattern and Electrode Connections



Remark n = 0 to 2

Figure 18-18. Example of Connecting Static LCD Panel

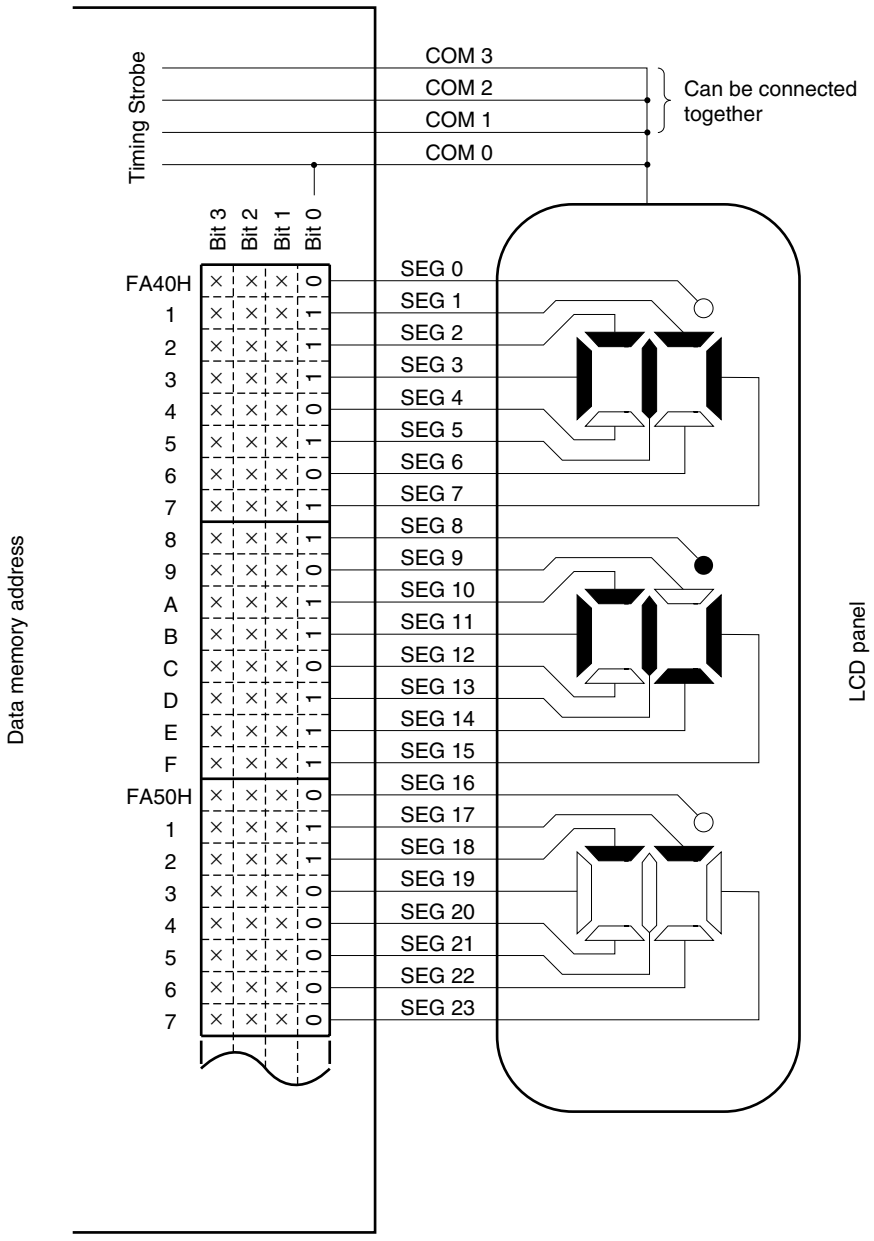
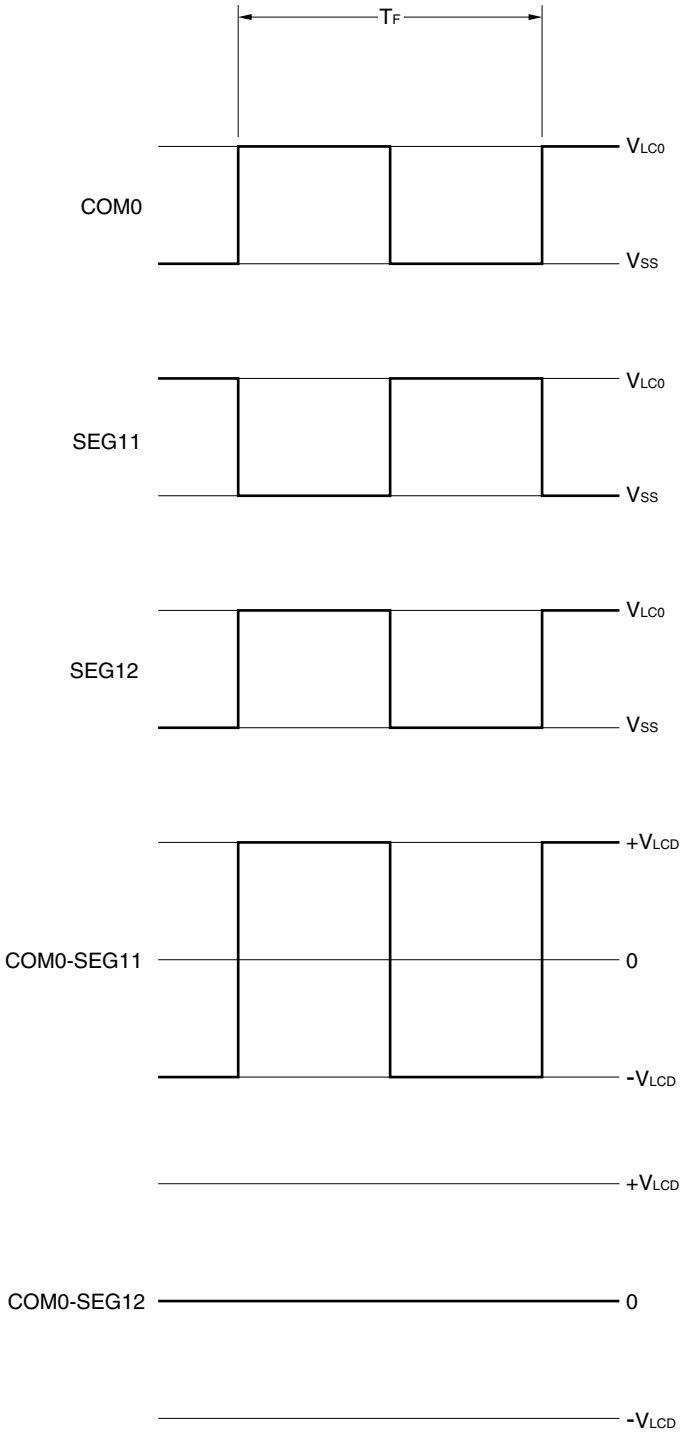


Figure 18-19. Static LCD Drive Waveform Examples



18.7.2 Two-time-slice display example

Figure 18-21 shows how the 6-digit LCD panel having the display pattern shown in Figure 18-20 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 and COM1) of the 78K0/Lx3-M chip. This example displays data "12345.6" in the LCD panel. The contents of the display data memory (FA40H to FA57H) correspond to this display.

The following description focuses on numeral "3" (3) displayed in the fourth digit. To display "3" in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 to SEG15 pins according to Table 18-7 at the timing of the common signals COM0 and COM1; see Figure 18-20 for the relationship between the segment signals and LCD segments.

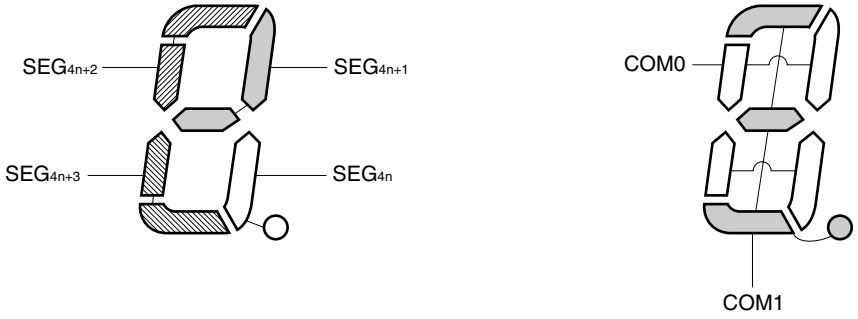
Table 18-7. Select and Deselect Voltages (COM0 and COM1)

Segment / Common	SEG12	SEG13	SEG14	SEG15
COM0	Select	Select	Deselect	Deselect
COM1	Deselect	Select	Select	Select

According to Table 18-7, it is determined that the display data memory location (FA4FH) that corresponds to SEG15 must contain xx10.

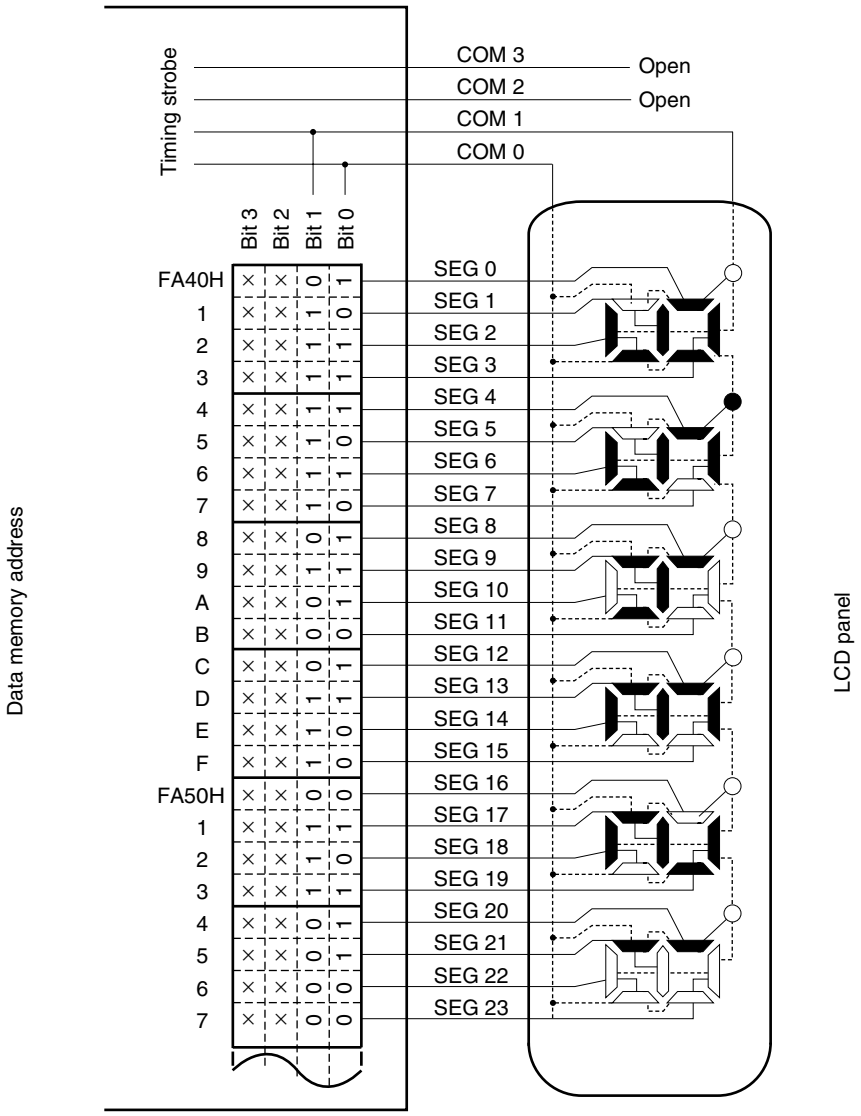
Figure 18-22 shows examples of LCD drive waveforms between the SEG15 signal and each common signal. When the select voltage is applied to SEG15 at the timing of COM1, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 18-20. Two-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 5

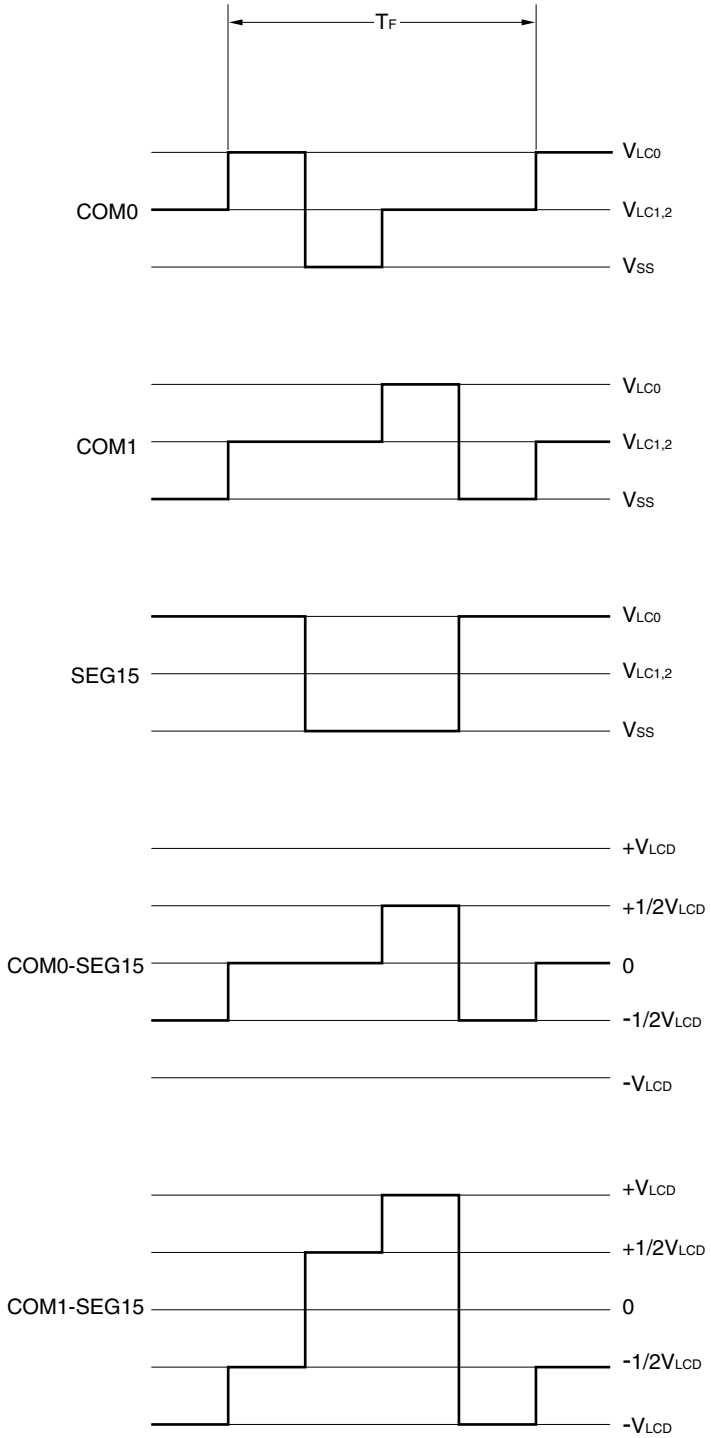
Figure 18-21. Example of Connecting Two-Time-Slice LCD Panel



×: Can always be used to store any data because the two-time-slice mode is being used.

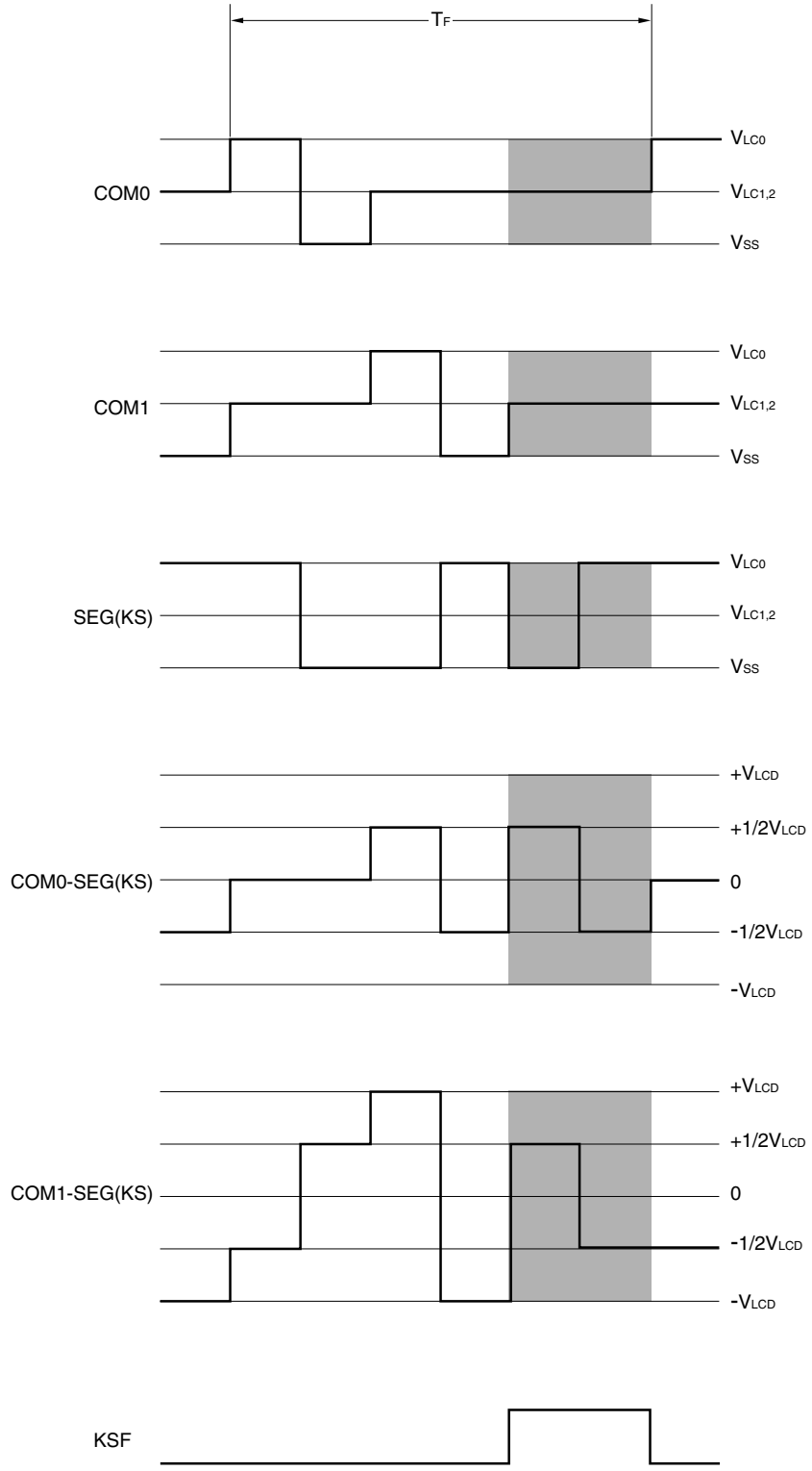
Figure 18-22. Two-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)

(a) When segment key scan function is not used (KSON = 0)



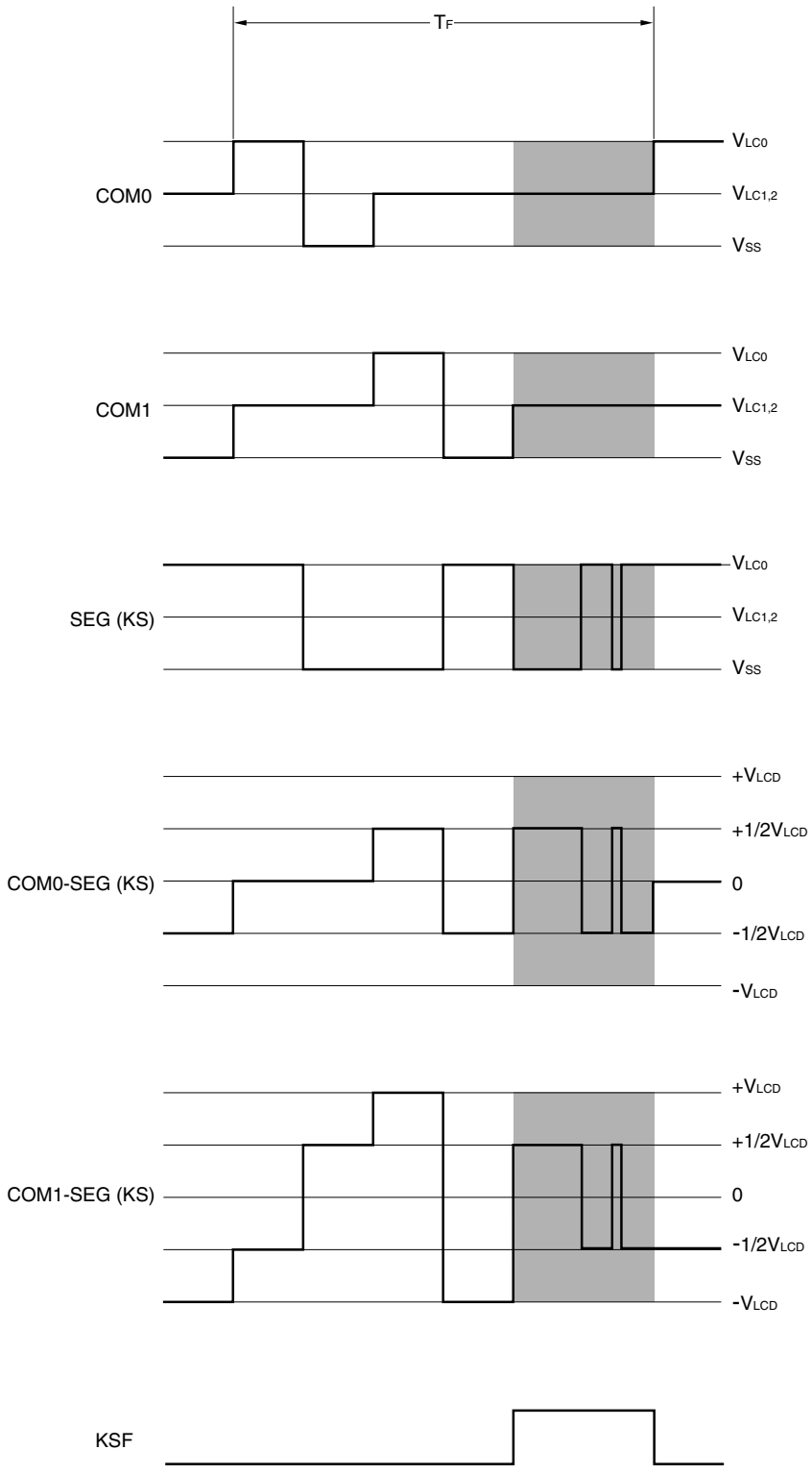
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

18.7.3 Three-time-slice display example

Figure 18-24 shows how the 8-digit LCD panel having the display pattern shown in Figure 18-23 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM2) of the 78K0/Lx3-M chip. This example displays data "123456.78" in the LCD panel. The contents of the display data memory (addresses FA40H to FA57H) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the third digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG6 to SEG8 pins according to Table 18-8 at the timing of the common signals COM0 to COM2; see Figure 18-23 for the relationship between the segment signals and LCD segments.

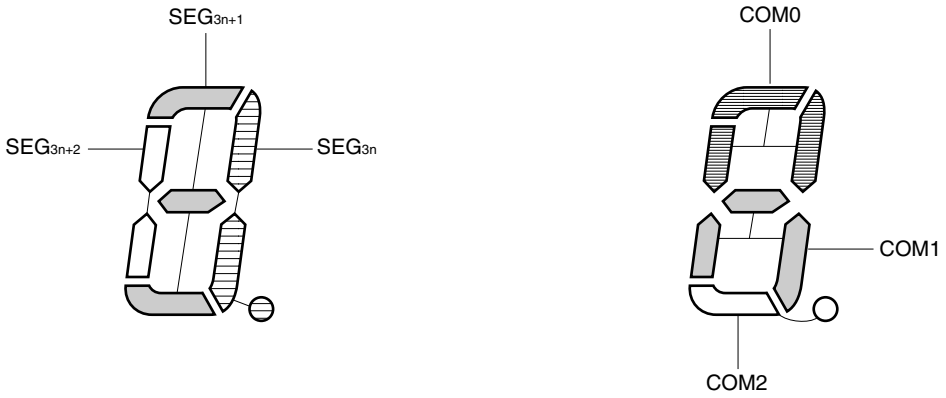
Table 18-8. Select and Deselect Voltages (COM0 to COM2)

Segment / Common	SEG6	SEG7	SEG8
COM0	Deselect	Select	Select
COM1	Select	Select	Select
COM2	Select	Select	–

According to Table 18-8, it is determined that the display data memory location (FA46H) that corresponds to SEG6 must contain x110.

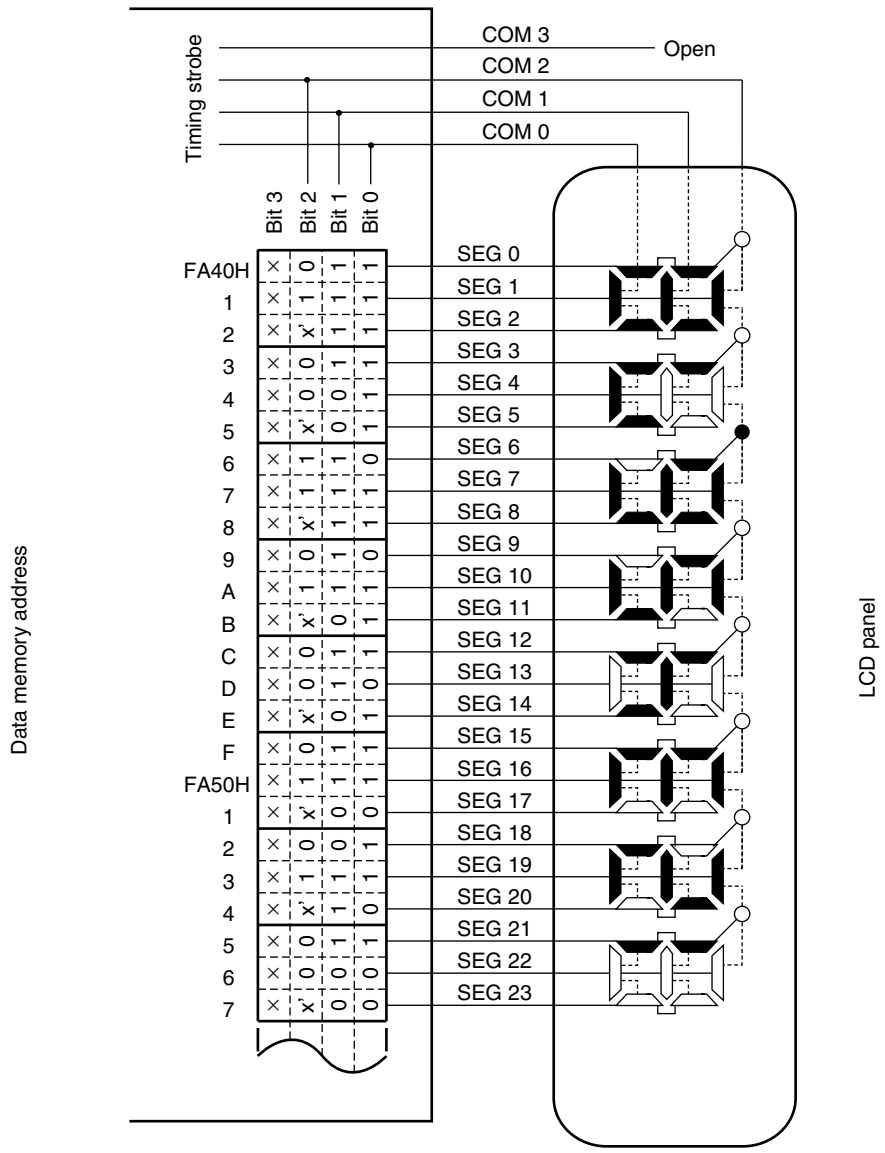
Figure 18-25 and Figure 18-26 show examples of LCD drive waveforms between the SEG6 signal and each common signal in the 1/2 and 1/3 bias methods, respectively. When the select voltage is applied to SEG6 at the timing of COM1 or COM2, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 18-23. Three-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 7

Figure 18-24. Example of Connecting Three-Time-Slice LCD Panel

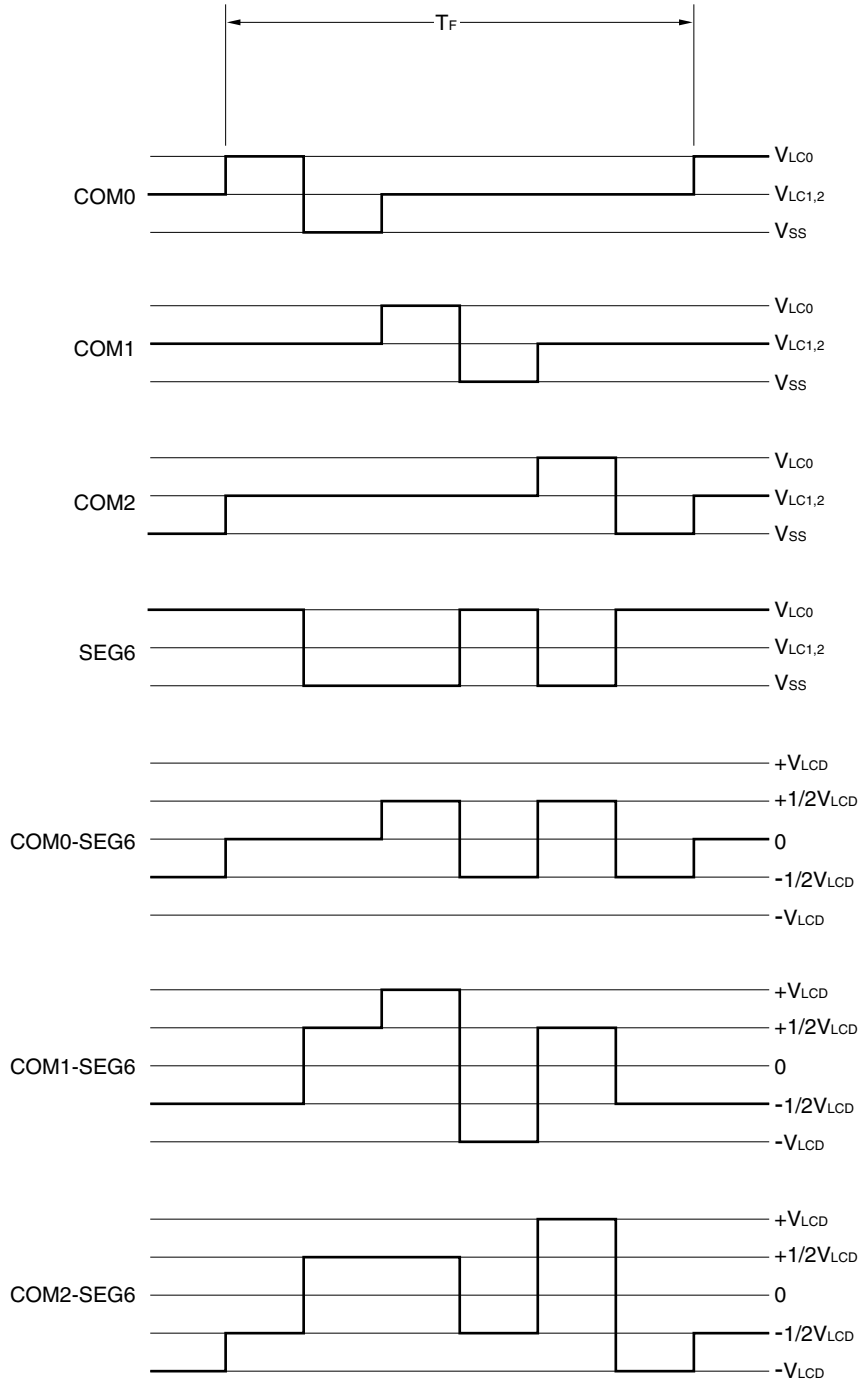


×': Can be used to store any data because there is no corresponding segment in the LCD panel.

×: Can always be used to store any data because the three-time-slice mode is being used.

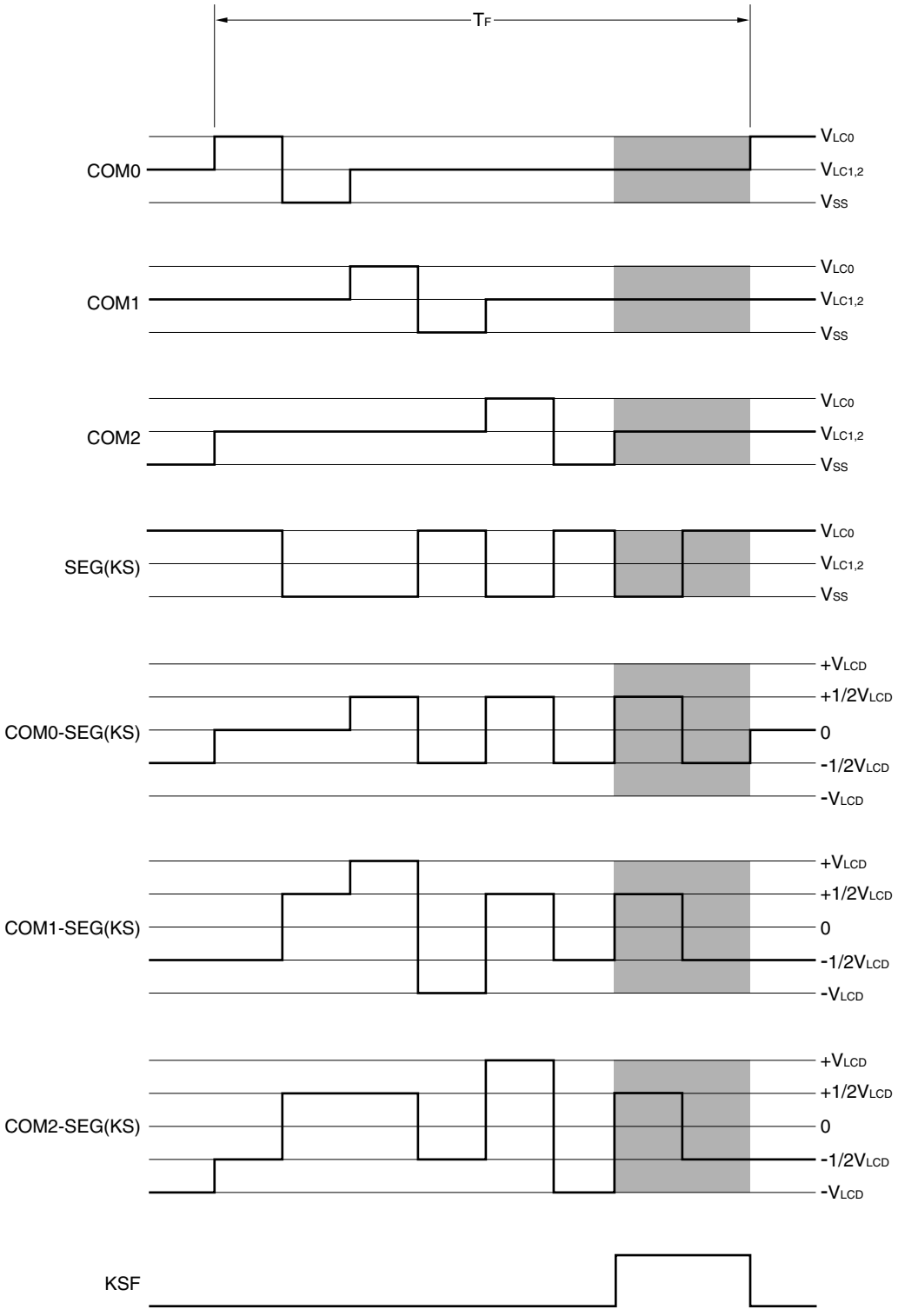
Figure 18-25. Three-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)

(a) When segment key scan function is not used (KSON = 0)



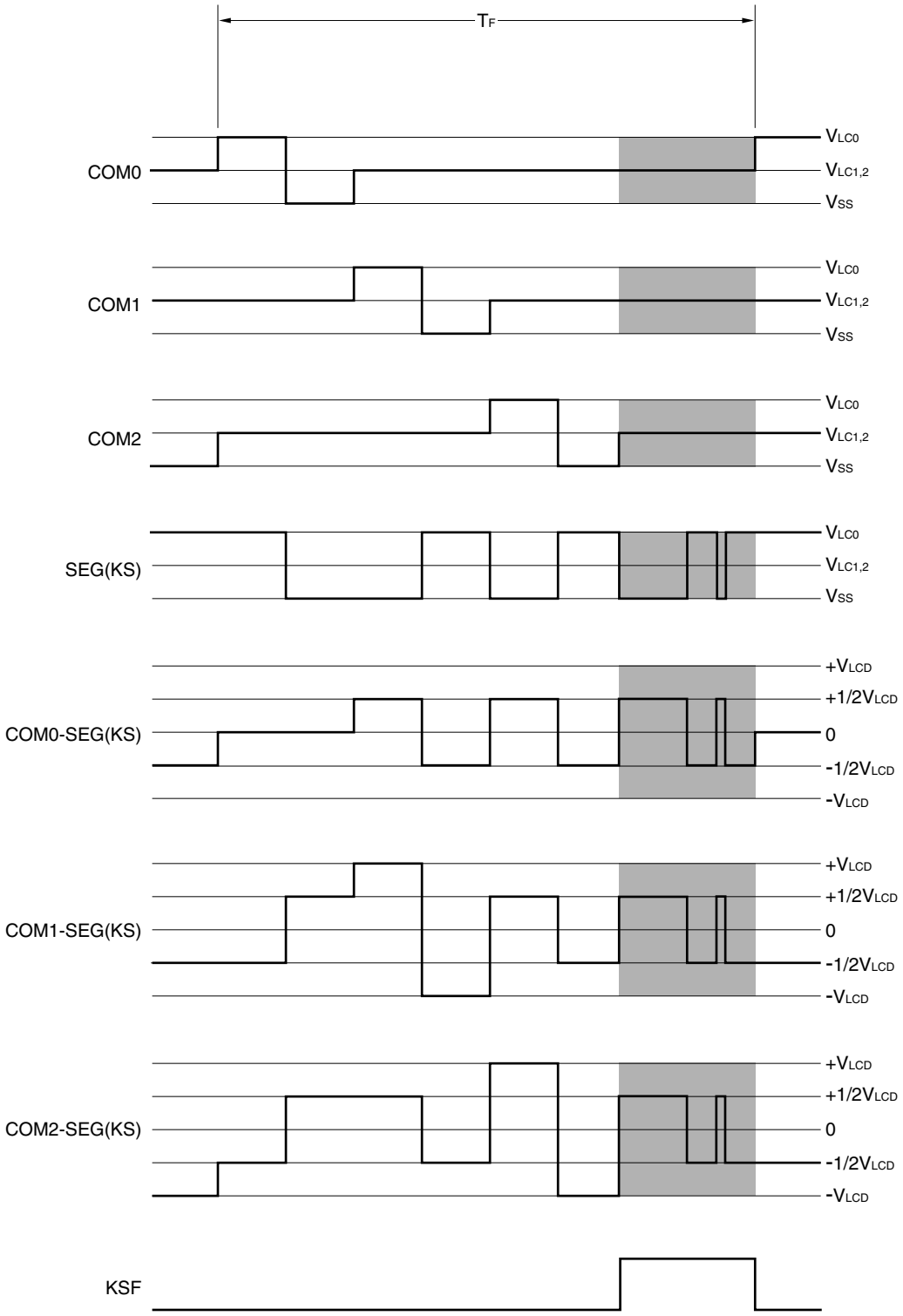
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

<Key identification>

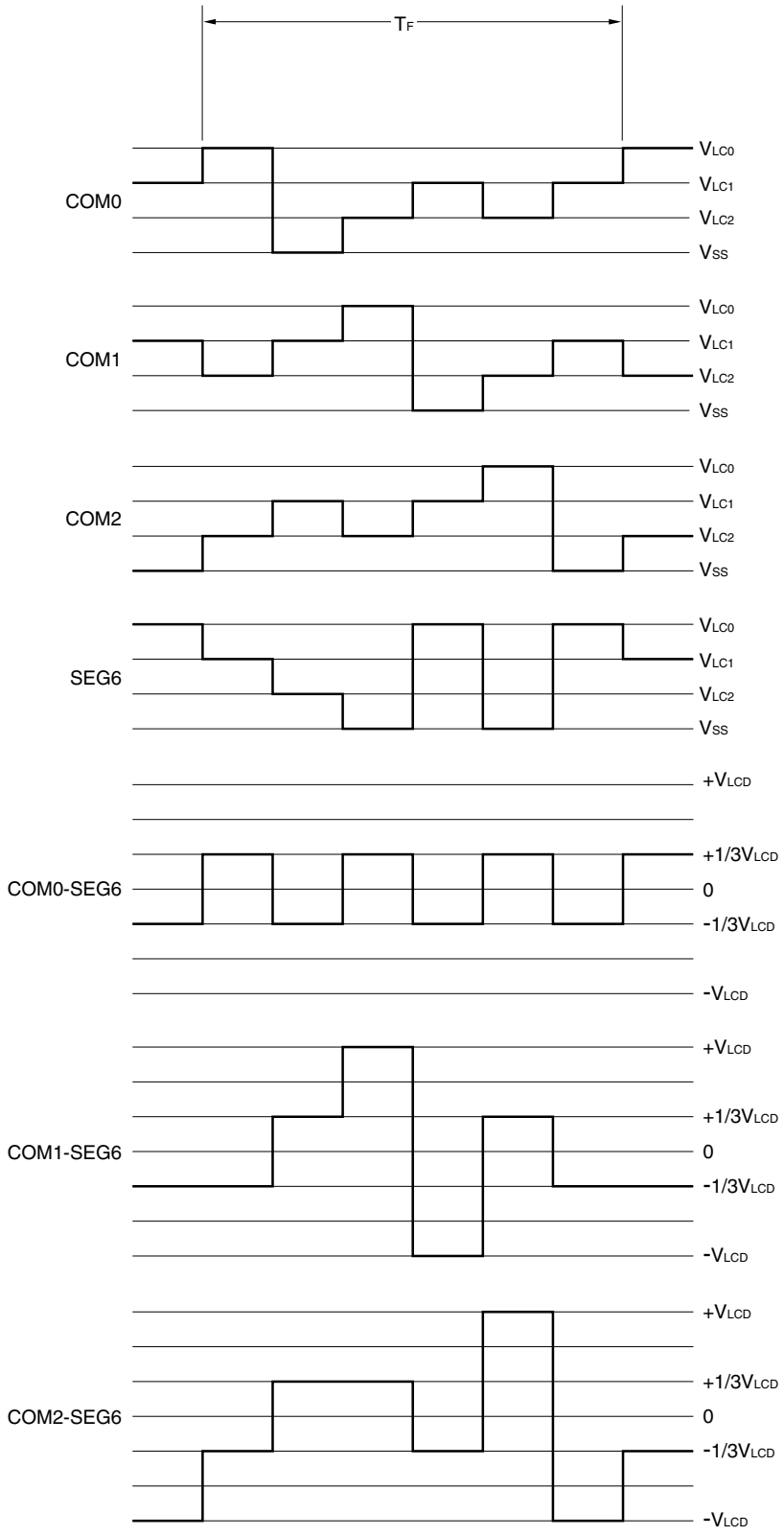


Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

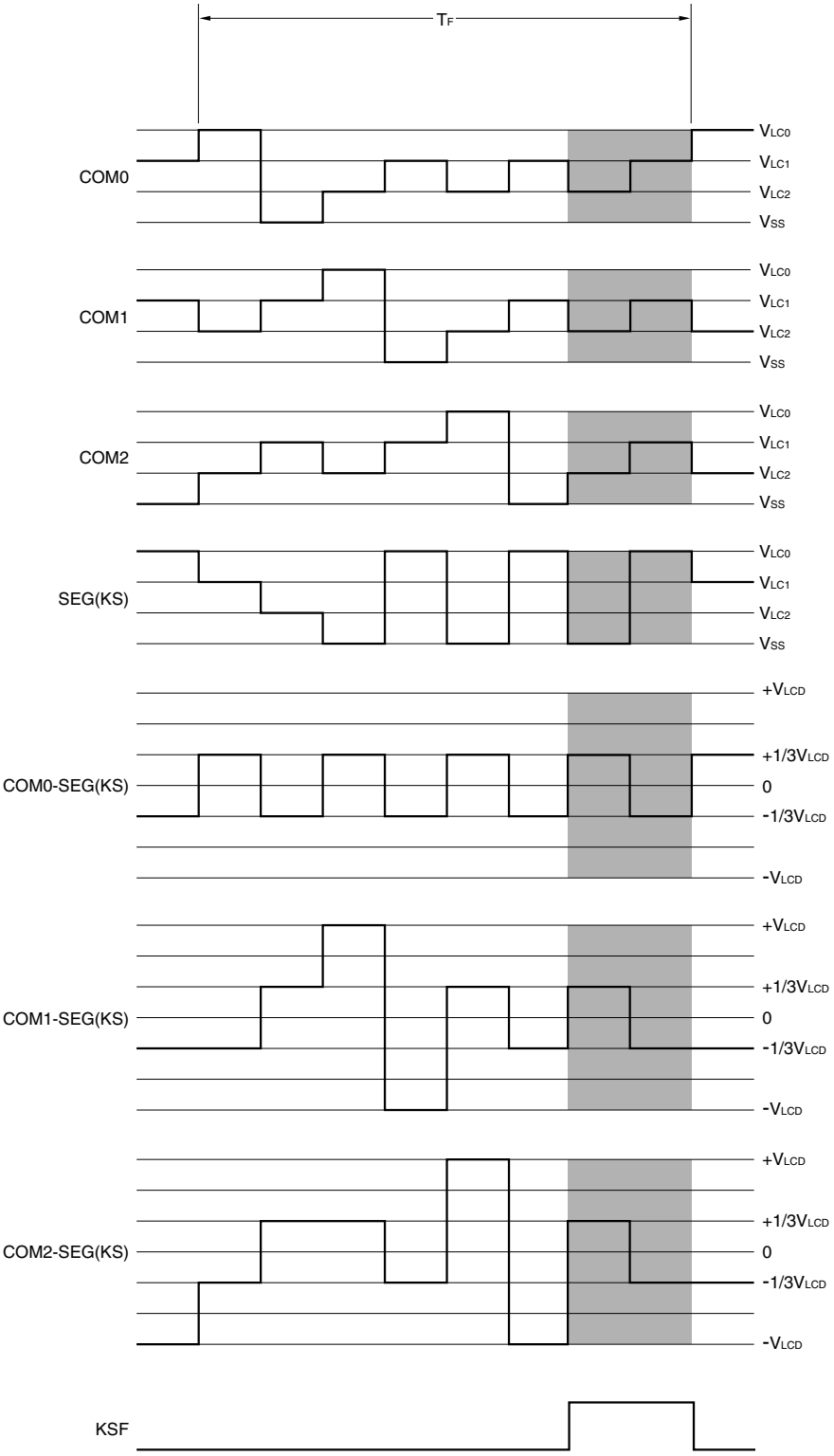
Figure 18-26. Three-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)

(a) When segment key scan function is not used (KSON = 0)



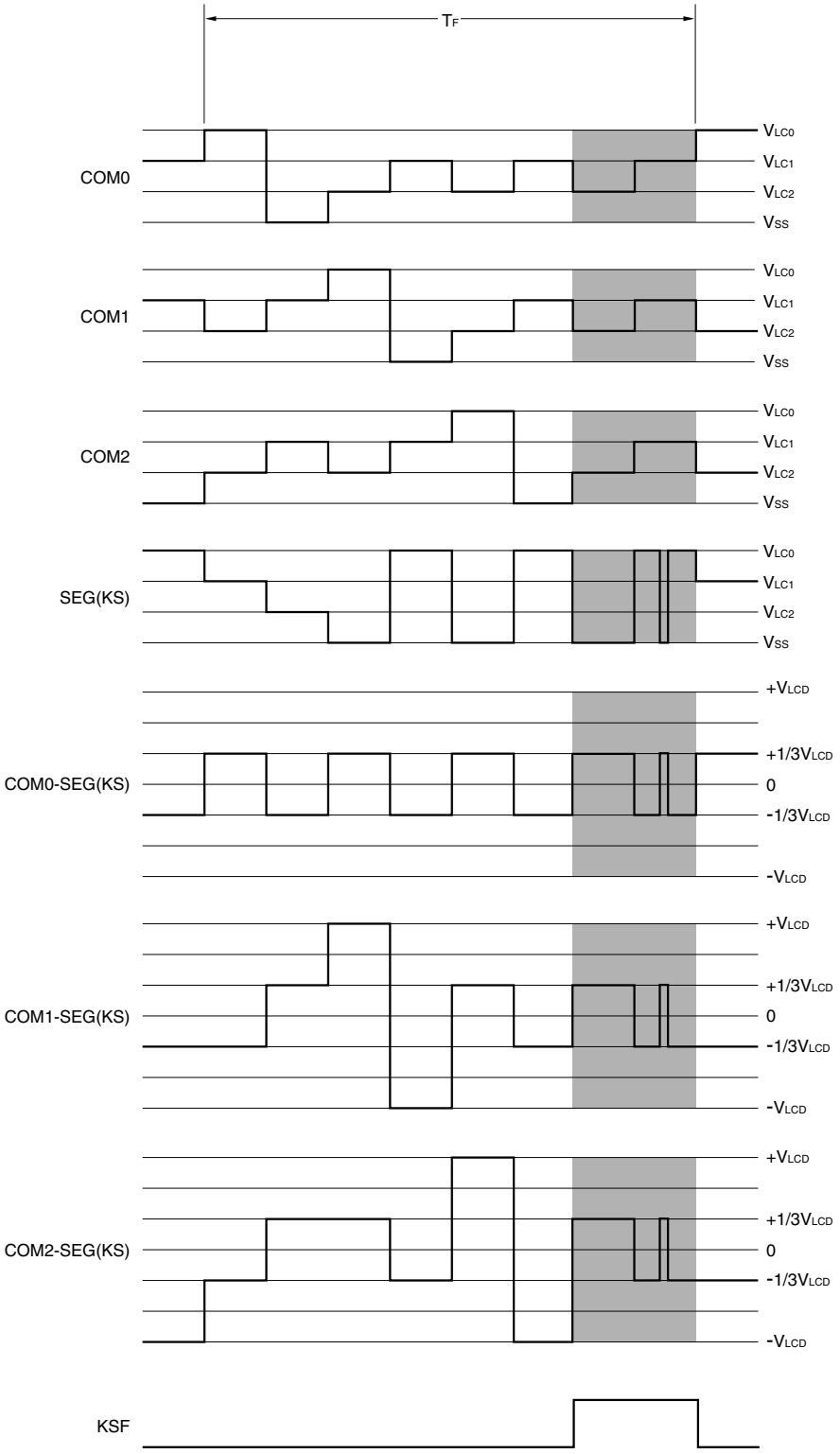
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

18.7.4 Four-time-slice display example

Figure 18-28 shows how the 12-digit LCD panel having the display pattern shown in Figure 18-27 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM3) of the 78K0/Lx3-M chip. This example displays data "123456.789012" in the LCD panel. The contents of the display data memory (addresses FA40H to FA57H) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the seventh digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 and SEG13 pins according to Table 18-9 at the timing of the common signals COM0 to COM3; see Figure 18-27 for the relationship between the segment signals and LCD segments.

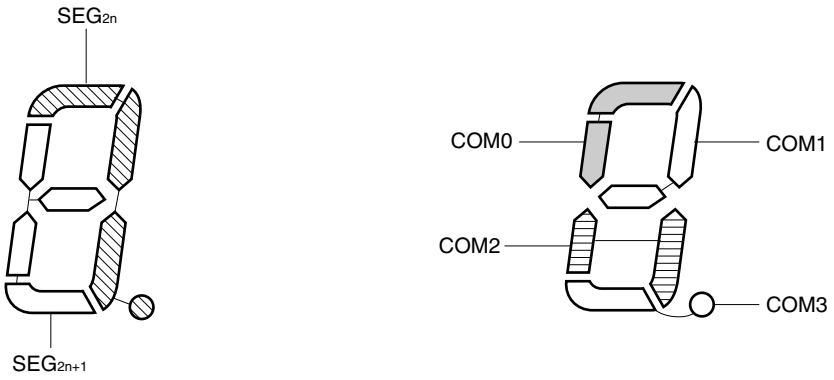
Table 18-9. Select and Deselect Voltages (COM0 to COM3)

Segment / Common	SEG12	SEG13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 18-9, it is determined that the display data memory location (FA4CH) that corresponds to SEG12 must contain 1101.

Figure 18-29 shows examples of LCD drive waveforms between the SEG12 signal and each common signal. When the select voltage is applied to SEG12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 18-27. Four-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 11

Figure 18-28. Example of Connecting Four-Time-Slice LCD Panel

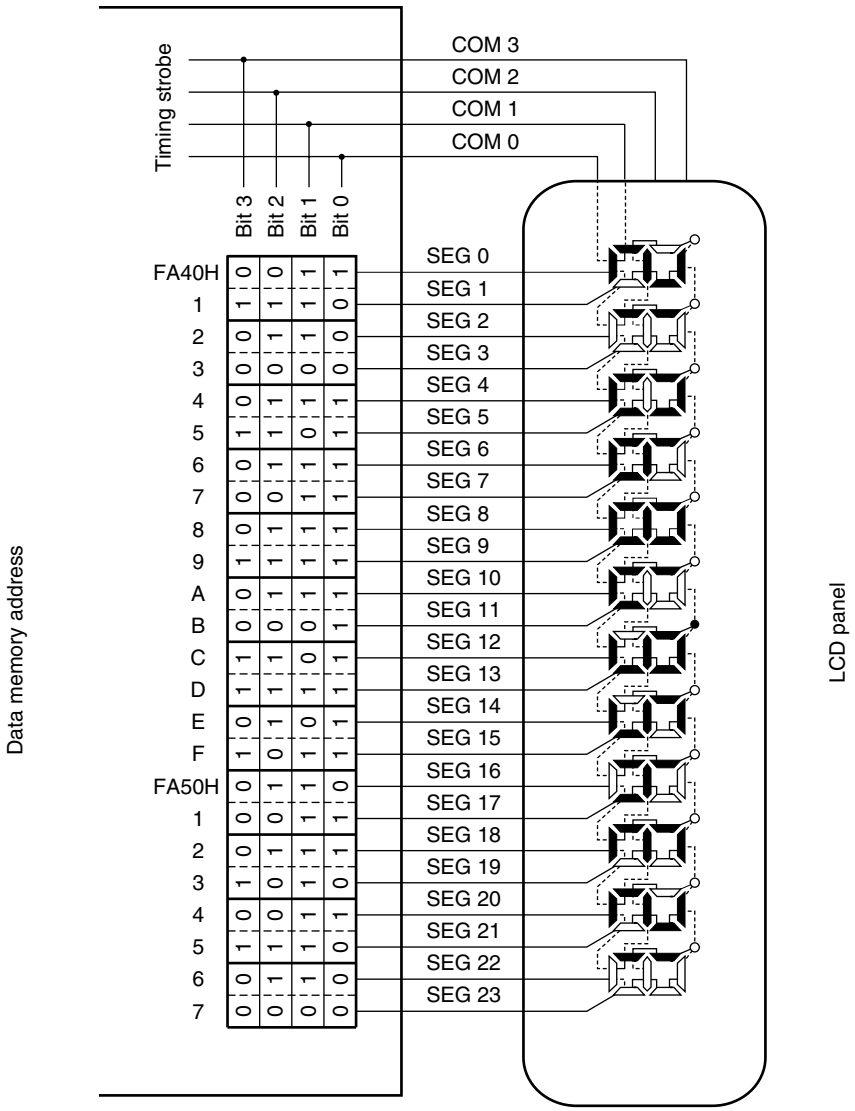
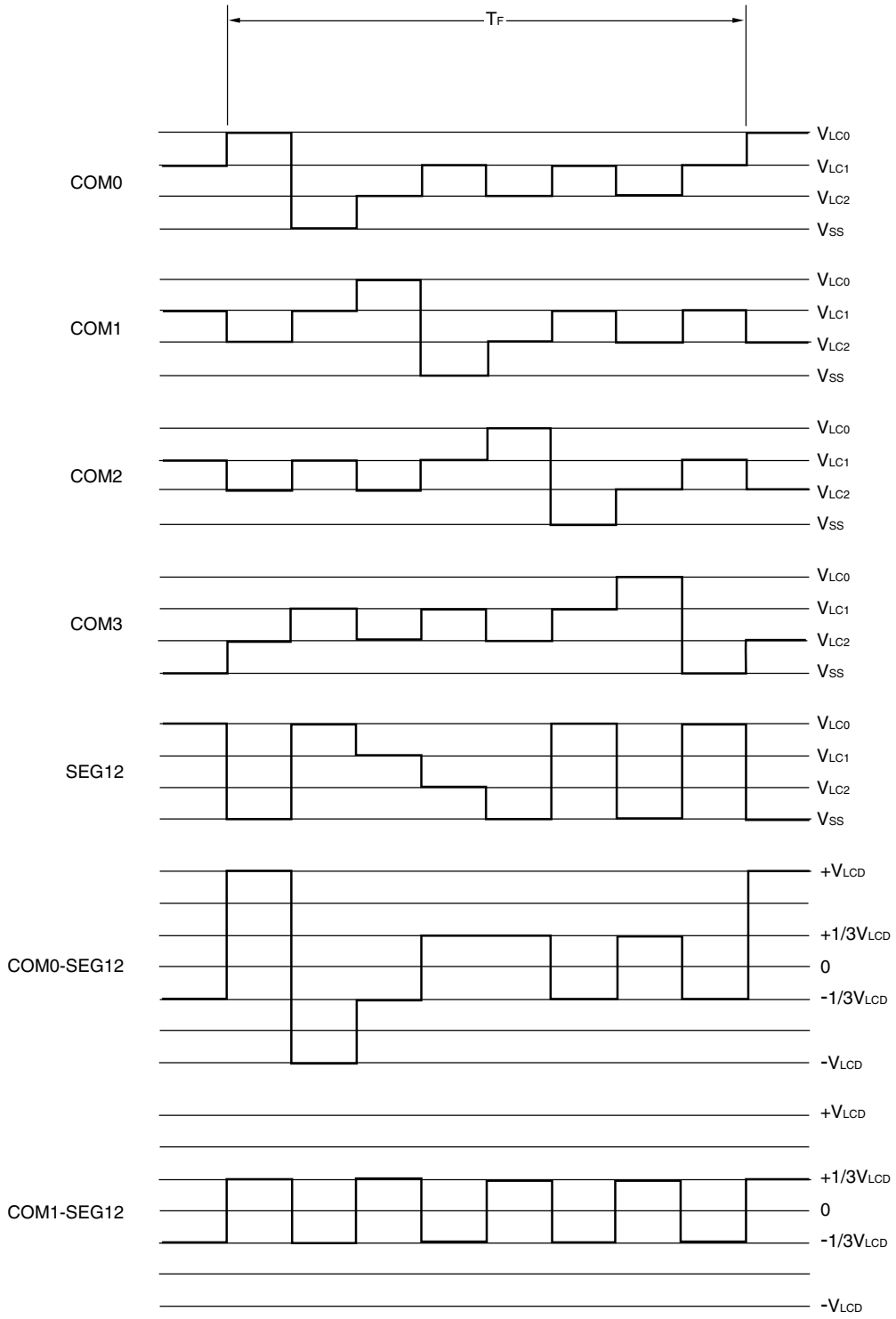


Figure 18-29. Four-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)

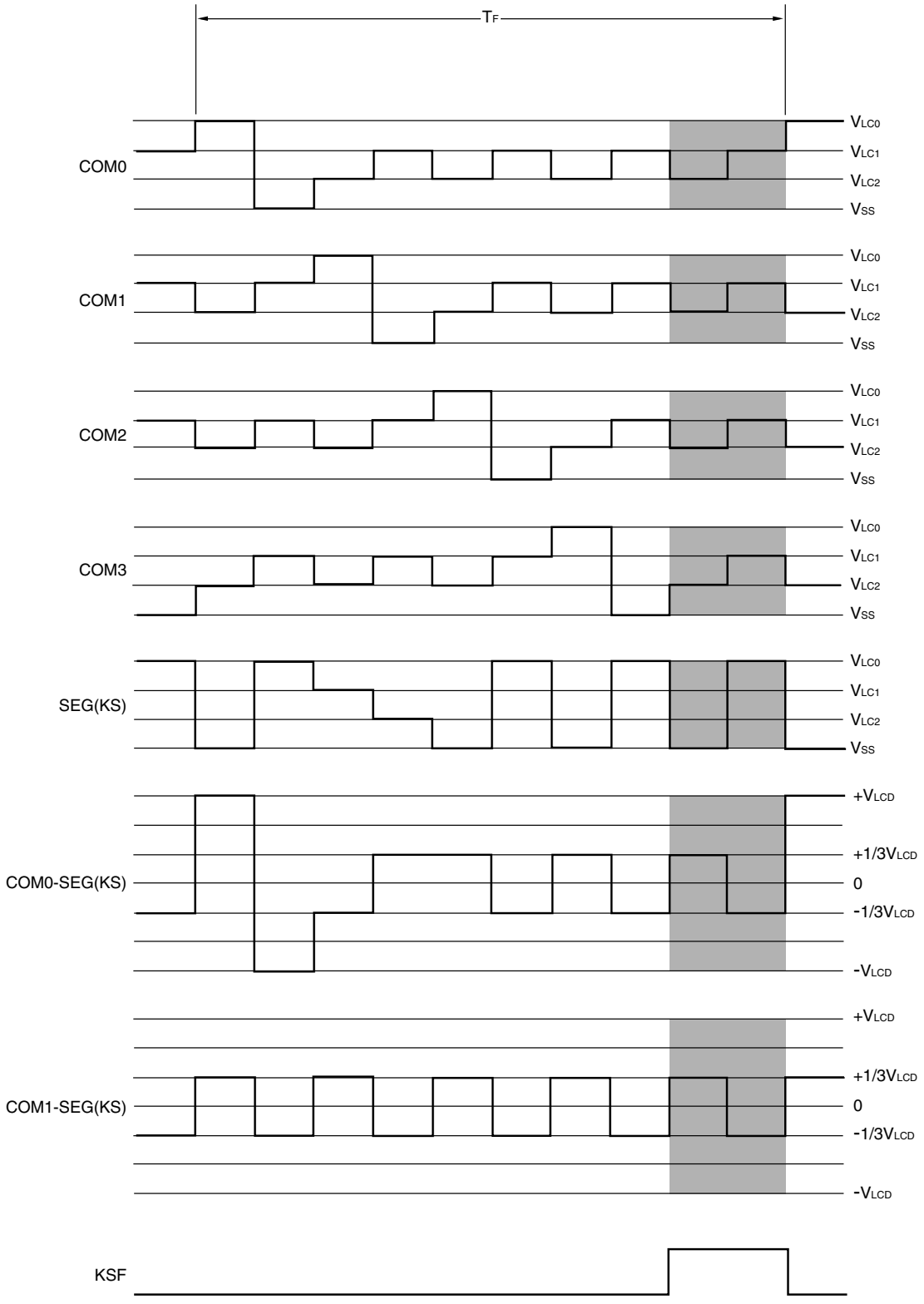
(a) When segment key scan function is not used (KSON = 0)



Remark The waveforms for COM2 to SEG12 and COM3 to SEG12 are omitted.

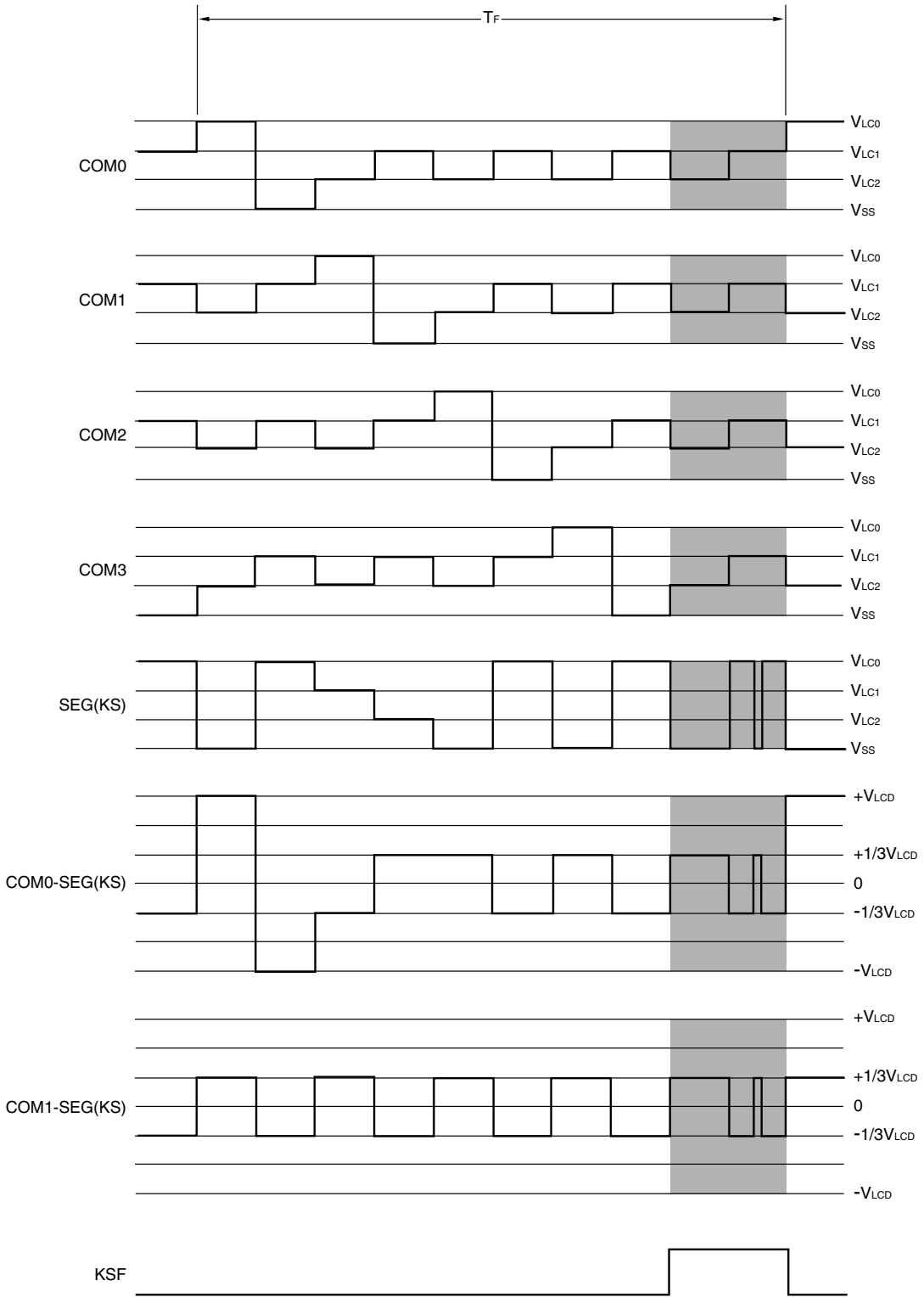
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

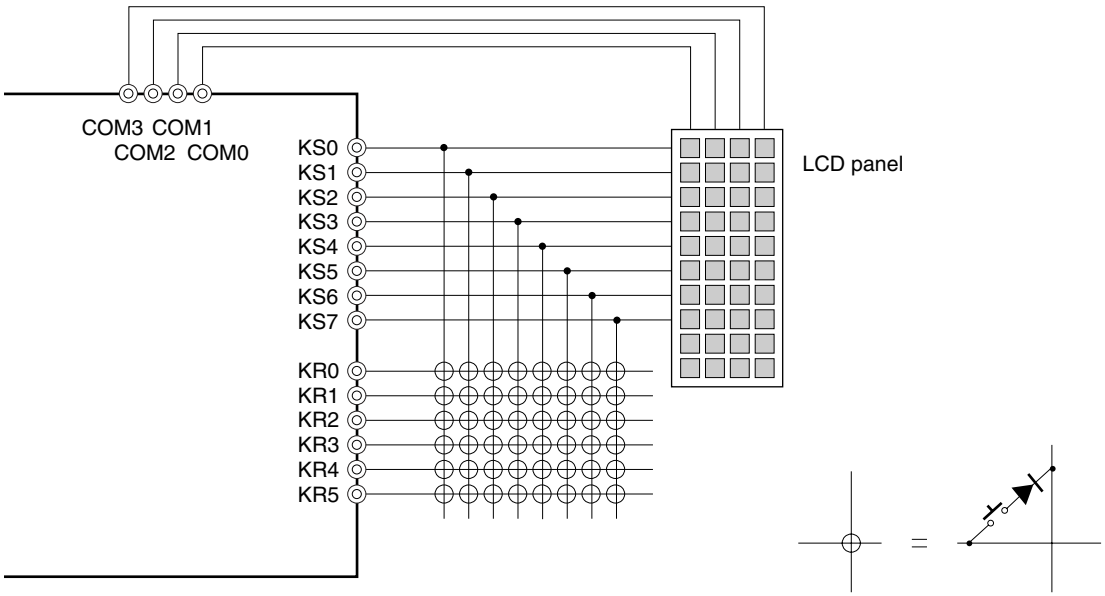
18.8 Operation of Segment Key Scan Function

The segment key scan function is used to reduce the number of pins used by outputting LCD display segment output and key scan signals from the same pin.

Caution This function may affect the LCD panel, depending on how it is used.
Use the function after thorough evaluation.

18.8.1 Circuit configuration example

Figure 18-30. Circuit configuration example



Remark 78K0/LE3-M: KR0, KR1
78K0/LG3-M: KR0 to KR5

18.8.2 Example of procedure for using segment key scan function

Figure 18-31 shows the operation flow of the segment key scan and Figure 18-32 shows the key connection example.

Figure 18-31. Operation Flow of Segment Key Scan

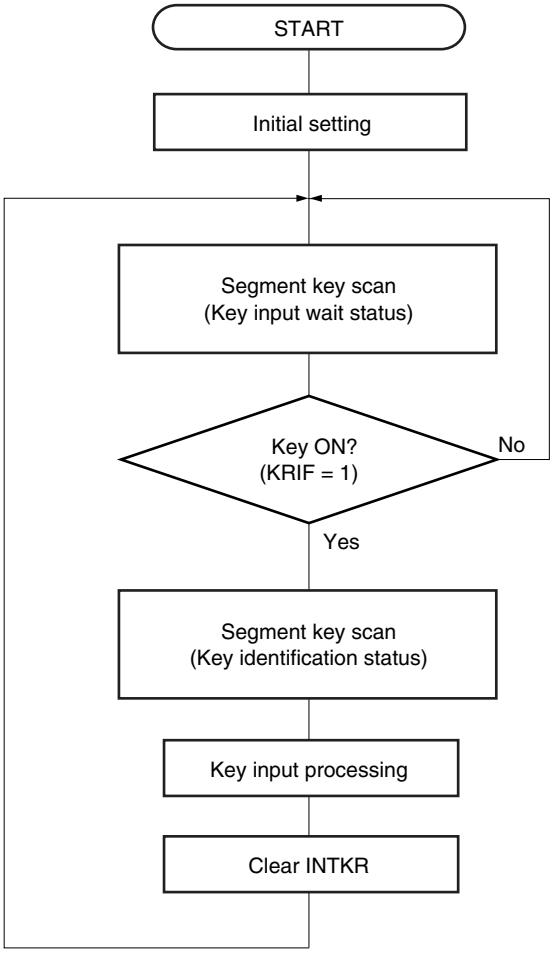
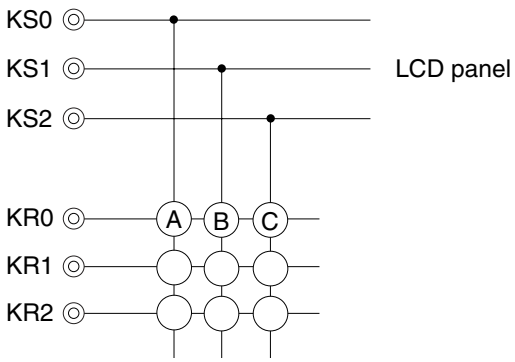
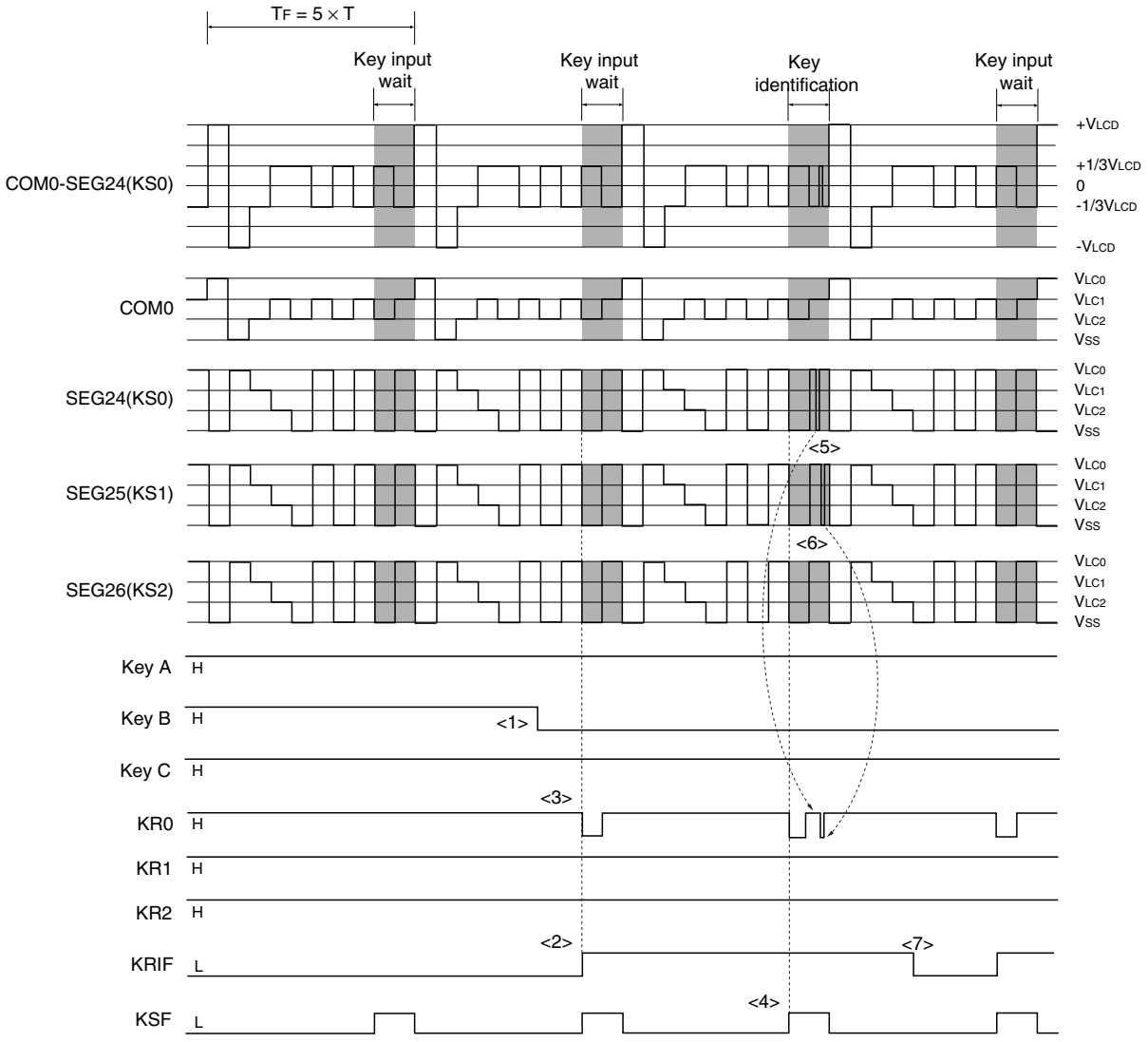


Figure 18-32. Key Connection Example



An example of the segment key scan operation when key B, shown in Figure 18-32, has been pressed is shown below.

Figure 18-33. Example of Segment Key Scan Operation Timing (Four-Time-Slice (1/3 Bias Method))



T: One LCD clock period TF: Frame frequency Shaded sections: Segment key scan output period

<1> Assume key B has been pressed at this timing.

<2> KRIF becomes “1” and the key that has been pressed can be known.

<3> KR0 becomes low level, and whether key A, B, or C has been pressed can be known.
Input to the KR pin will be enabled after two fLCD clocks from the rise of KSF. Consequently, KRIF becomes “1” after two fLCD clocks from the rise of KSF.

<4> A segment key scan operation is started after it has been confirmed that KSF is “1”.

<5> It can be known that key A is not pressed, because KR0 was at high level when the SEG24 (KS0) pin outputs a low level.

<6> It can be known that key B is pressed, because KR0 was at low level when the SEG25 (KS1) pin outputs a low level. Perform the input processing of key B.

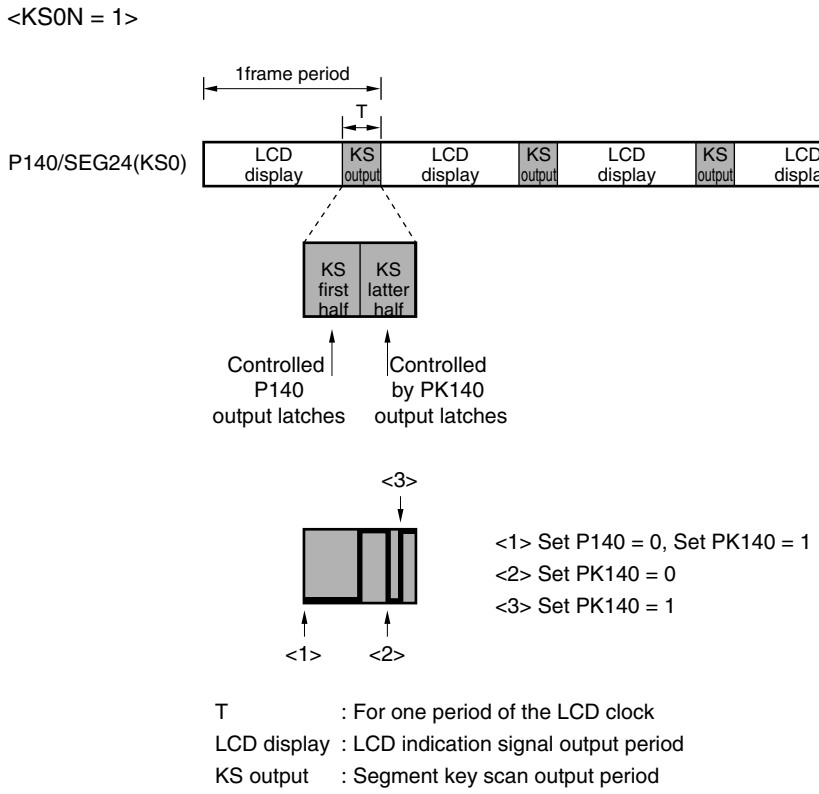
<7> Clear KRIF.

The output values of the SEG (KS) pin during the segment key scan output period correspond to the setting values of port registers 14 and 15, and can be controlled by using port registers 14 and 15.

Bits 0 to 3 and bits 4 to 7 of each port register are used to control the first half and latter half of the segment key scan output period, respectively (see **(9) Port register 14 (P14)** and **(10) Port register 15 (P15)** in **18.3**).

Figure 18-34 shows the relationship between port register 14 and the segment key scan output.

Figure 18-34. Relationship Between Port Register 14 and Segment Key Scan Output (for P140/SEG24(KS0) Pin)



Remark During the segment key scan output period, COM will not be displayed when output.
See **Figure 18-15** and **Figure 18-16** for waveform details.

18.9 Cautions When Using Segment Key Scan Function

(1) Conditions for use

Use the segment key scan function if V_{DD} is equal to V_{LC0}.

(2) Segment key scan input pins

Only the KR0 to KR5 pins can be used as input pins for the segment key scan function.

Other pins cannot be used as input pins for the segment key scan function.

(3) Allowable input range of KR0 to KR5 pins

Due to a delay caused by a pull-up resistor, segment key scan input cannot be performed for the KR pin for a period of two f_{LCD} clocks from the start of the segment key scan output period.

Similarly, due to input end processing, segment key scan input cannot be performed for the KR pin for the period of the last f_{LCD} clock of the segment key scan output period.

(4) Key return mode register (KRM) setting

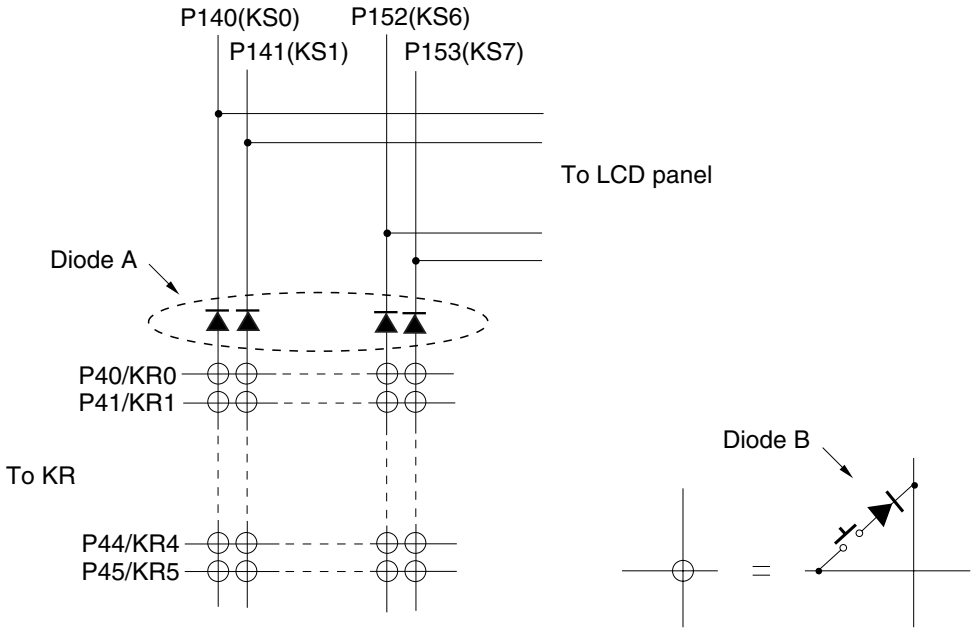
When the segment key scan function is used (KSON = 1), set KRMn to 1 or 0 to use or not use the KRn pin as a segment key scan input pin.

(5) Circuit configuration

When using the segment key scan function, at least diode A or diode B shown in Figure 18-35 is required.

The following problems will occur when diodes A and B are missing.

Figure 18-35. Key Matrix Configuration Example



(a) When both diodes A and B are missing

When both diodes A and B are missing, the segment key scan function cannot be used, because of the following.

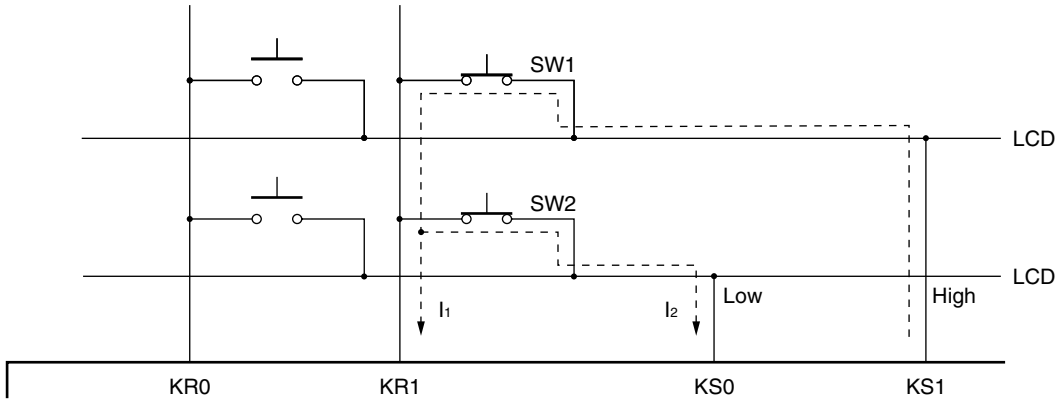
The following figure shows a circuit example when both diodes A and B are missing.

Assume, as shown in the figure below, that switches SW1 and SW2 are turned on, and a high level and a low level are output from the KS1 pin and KS0 pin, respectively.

When diode A is missing at this time, currents I_1 and I_2, shown as broken lines, will flow.

Consequently, the high level of KS1 and the low level of KS0 will not be output normally due to I_2, and the key input data of KR1 will become undefined.

Furthermore, the LCD display will not be turned on or off normally.



(b) When only diode A exists

When only diode A exists, whether switches are pressed simultaneously cannot be identified, due to the following.

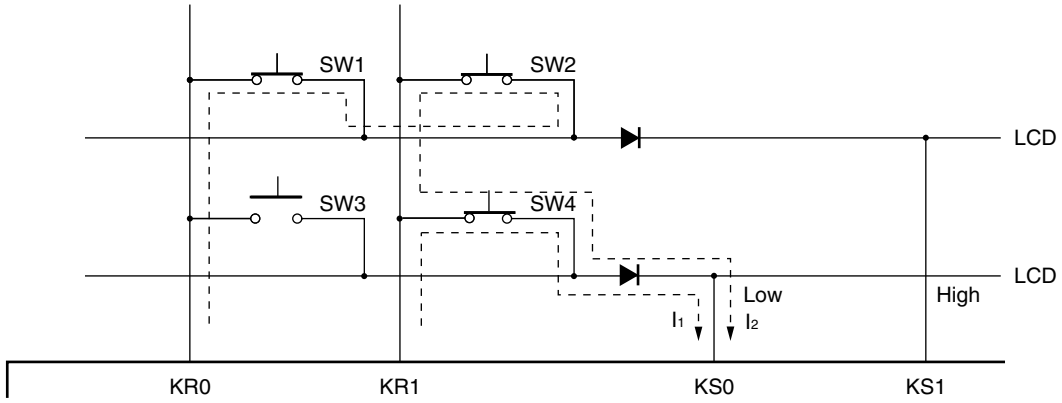
The following figure shows a circuit example when only diode A exists.

Assume, as shown in the figure below, that switches SW1, SW2, and SW4 are turned on, and a high level and a low level are output from the KS1 pin and KS0 pin, respectively.

At this time currents I_1 and I_2, shown as broken lines, will flow.

Consequently, even though SW3 is turned off, SW3 is identified to be turned on, because a low level is input to KR0 due to I_2.

There is no interference with the LCD display.



(c) When only diode B exists

Identification of at least three switches being pressed simultaneously can be performed.

There is no interference with the LCD display.

18.10 Supplying LCD Drive Voltages V_{LC0}, V_{LC1}, and V_{LC2}

With the 78K0/Lx3-M microcontrollers, a LCD drive power supply can be generated using either of two types of methods: internal resistance division method or external resistance division method.

18.10.1 Internal resistance division method

The 78K0/Lx3-M microcontrollers incorporate voltage divider resistors for generating LCD drive power supplies. Using internal voltage divider resistors, a LCD drive power supply that meet each bias method listed in Table 18-10 can be generated, without using external voltage divider resistors.

Table 18-10. LCD Drive Voltages (with On-Chip Voltage Divider Resistors)

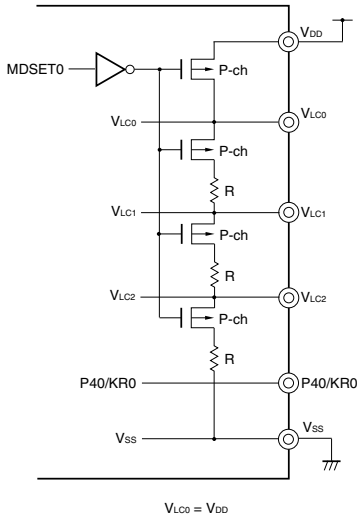
Bias Method / LCD Drive Voltage Pin	No Bias (Static)	1/2 Bias Method	1/3 Bias Method
V_{LC0}	V_{LCD}	V_{LCD}	V_{LCD}
V_{LC1}	$\frac{2}{3}$ V_{LCD}	$\frac{1}{2}$ V_{LCD} Note	$\frac{2}{3}$ V_{LCD}
V_{LC2}	$\frac{1}{3}$ V_{LCD}		$\frac{1}{3}$ V_{LCD}

Note For the 1/2 bias method, it is necessary to connect the V_{LC1} and V_{LC2} pins externally.

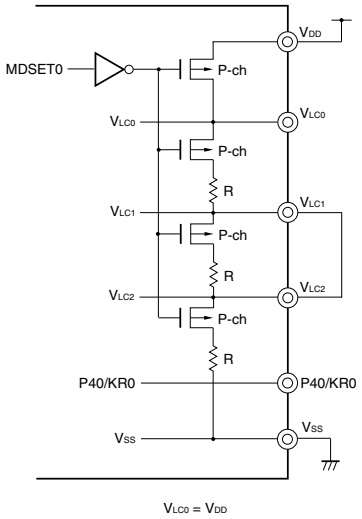
Figure 18-36 shows examples of generating LCD drive voltages internally according to Table 18-10.

Figure 18-36. Examples of LCD Drive Power Connections (Internal Resistance Division Method)

(a) 1/3 bias method and static display mode (MDSET1, MDSET0 = 0, 1) (example of V_{DD} = 3 V, V_{LC0} = 3 V)



(b) 1/2 bias method (MDSET1, MDSET0 = 0, 1) (example of V_{DD} = 3 V, V_{LC0} = 3 V)



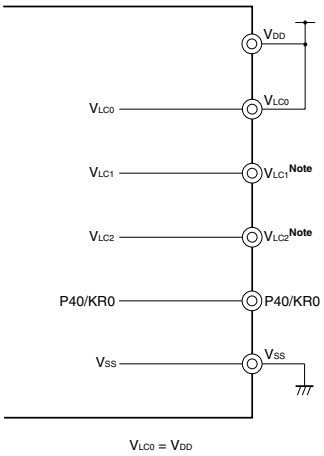
Remark It is recommended to use the external resistance division method when using the static display mode, in order to reduce power consumed by the voltage divider resistor.

18.10.2 External resistance division method

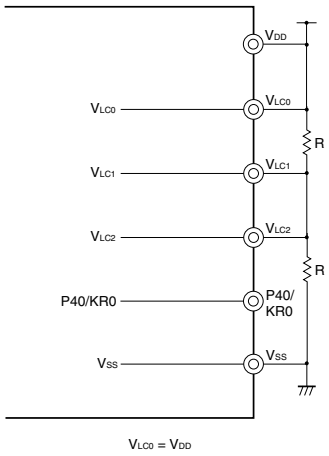
The 78K0/Lx3-M microcontrollers can also use external voltage divider resistors for generating LCD drive power supplies, without using internal resistors. Figure 18-37 shows examples of LCD drive voltage connection, corresponding to each bias method.

Figure 18-37. Examples of LCD Drive Power Connections (External Resistance Division Method)

(a) Static display mode (MDSET1, MDSET0 = 0, 0) (example of V_{DD} = 3 V, V_{LC0} = 3 V)

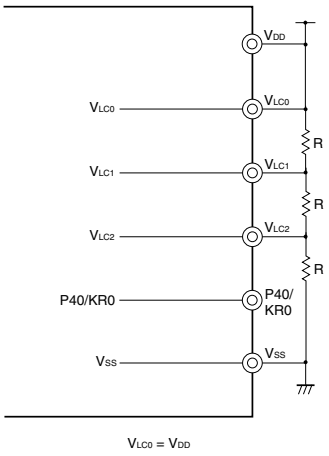


(b) 1/2 bias method (MDSET1, MDSET0 = 0, 0) (example of V_{DD} = 3 V, V_{LC0} = 3 V)



Note Connect V_{LC1} and V_{LC2} directly to GND or V_{LC0}.

(c) 1/3 bias method (MDSET1, MDSET0 = 0, 0) (example of V_{DD} = 3 V, V_{LC0} = 3 V)



CHAPTER 19 REMOTE CONTROLLER TRANSMITTER

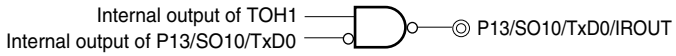
19.1 Functions of Remote Controller Transmitter

Remote controller transmitter is mounted onto all 78K0/Lx3-M microcontroller products.

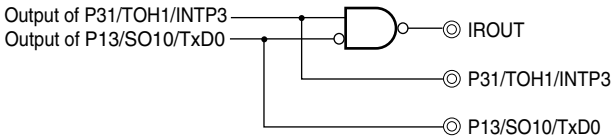
The remote control transmission circuit uses timer H1 output and UART0 output to generate a remote control transmission signal.

Figure 19-1. Block Diagram of Remote Controller Transmitter

(a) 78K0/LE3-M



(b) 78K0/LG3-M



Cautions 1. For the 78K0/LG3-M, the IROUT pin cannot be used at the same time as the P31/TOH1/INTP3 or P13/SO10/TxD0 pin.

2. Table 19-1 shows the setting of P31/TOH1/INTP3, P13/SO10/TxD0, and IROUT pins when using function.

Table 19-1. Setting of P31/TOH1/INTP3, P13/SO10/TxD0, and IROUT pins

(a) 78K0/LE3-M

P13/SO10/TxD0/IROUT pin	
Using IROUT	Using P13/SO10/TxD0
Clear PM31 to “0”. Clear PM13 to “0”.	Clear PM31 to “0” and set P31 to 1. Clear PM13 to “0”.

(b) 78K0/LG3-M

P31/TOH1/INTP3 and P13/SO10/TxD0/IROUT pins		Using IROUT
Input	Output	
Set PM13 and PM31 to 1. Be sure to pull-up.	Clear PM13 and PM31 to “0”.	Clear PM13 and PM31 to “0”.

CHAPTER 20 INTERRUPT FUNCTIONS

		78K0/LE3-M	78K0/LG3-M
Maskable interrupts	External	4	5
	internal	17	

20.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into a high interrupt priority group and a low interrupt priority group by setting the priority specification flag registers (PR0L, PR0H, PR1L, PR1H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 20-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

20.2 Interrupt Sources and Configuration

The interrupt sources consist of maskable interrupts and software interrupts. In addition, they also have up to four reset sources (see **Table 20-1**).

Table 20-1. Interrupt Source List

Interrupt Type	Internal/ External	Basic Configuration Type[Note 1]	Default Priority[Note 2]	Interrupt Source		Vector Table Address	78K0/ LE3-M	78K0/ LG3-M
				Name	Trigger			
Maskable	Internal	(A)	0	INTLVI	Low-voltage detection[Note 3]	0004H	√	√
	External	(B)	1	INTP0	Pin input edge detection	0006H	√	√
	Internal	(A)	2	INTP1	Interrupt request from extended SFR	0008H	√	√
	External	(B)	3	INTP2	Pin input edge detection	000AH	√	√
			4	INTP3		000CH	–	√
			5	INTP5		0010H	√	√
	Internal	(A)	6	INTSRE6	UART6 reception error generation	0012H	√	√
			7	INTSR6	End of UART6 reception	0014H	√	√
			8	INTST6	End of UART6 transmission	0016H	√	√
			9	INTCSI10/ INTST0	End of CSI10 communication/end of UART0 transmission	0018H	√	√
			10	INTTMH1	Match between TMH1 and CMP01 (when compare register is specified)	001AH	√	√
			11	INTTMH0	Match between TMH0 and CMP00 (when compare register is specified)	001CH	√	√
			12	INTTM50	Match between TM50 and CR50 (when compare register is specified)	001EH	√	√
			13	INTTM000	Match between TM00 and CR000 (when compare register is specified)	0020H	√	√
			14	INTTM010	Match between TM00 and CR010 (when compare register is specified), TI000 pin valid edge detection (when capture register is specified)	0022H	√	√
			15	INTAD	End of 10-bit successive approximation type A/D conversion	0024H	√	√
			16	INTSR0	End of UART0 reception or reception error generation	0026H	√	√
			17	INTTM51 [Note 4]	Match between TM51 and CR51 (when compare register is specified)	002AH	√	√
	External	(C)	18	INTKR	Key interrupt detection	002CH	√	√
	Internal	(A)	19	INTTM52	Match between TM52 and CR52 (when compare register is specified)	0032H	√	√
			20	INTTMH2	Match between TMH2 and CRH2 (when compare register is specified)	0034H	√	√
			21	INTACSI	Interrupt request from extended SFR interface	003CH	√	√
Software	–	(D)	–	BRK	BRK instruction execution	003EH	√	√
Reset	–	–	–	RESET	Reset input	0000H	√	√
				POC	Power-on clear		√	√
				LVI	Low-voltage detection [Note 5]		√	√
				WDT	WDT overflow		√	√

(**Note** is listed on the next page.)

Notes 1. Basic configuration types (A) to (D) correspond to (A) to (D) in **Figure 20-1**.

2. The default priority determines the sequence of processing vectored interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 21 indicates the lowest priority.

3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

4. When 8-bit timer/event counter 51 and 8-bit timer H1 are used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (see **Figure 8-15 Transfer Timing**).

5. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

If an interrupt is generated by any circuit controlled using an extended SFR (the real-time counter, ΔΣ-type A/D converter, power calculation circuit, power quality measurement circuit, or digital frequency conversion circuit), the interrupt is input to the interrupt controller as an INTP1 interrupt. Check the interrupt source in the interrupt handler, and then perform the appropriate processing.

Table 20-2. Interrupt Source List of Extended SFR (1/2)

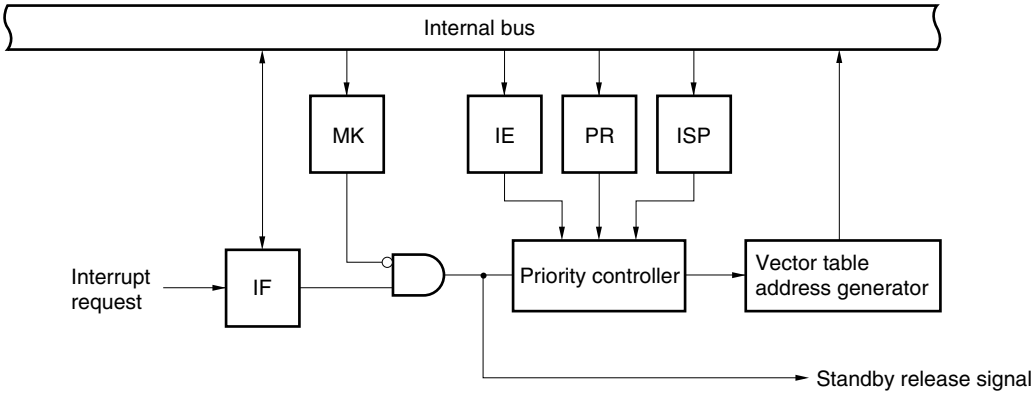
Interrupt Type	Internal/ External	Interrupt Source		Circuit
		Name	Trigger	
Maskable	Internal (extended SFR)	INTRTC0	RTC alarm and constant-period interrupt	Real-time counter
		INTRTC2	RTC interval interrupt	Real-time counter
		INTAD2	ΔΣ ADC conversion end interrupt	ΔΣ-type A/D converter
		INTFAULTSIGN	Fault detection interrupt	Power quality measurement circuit
		INTREASIGN	Reactive power sign change interrupt	Power calculation circuit
		INTACTSIGN	Active power sign change interrupt	Power calculation circuit
		INTAPPNOLD	Apparent power no-load interrupt	Power calculation circuit
		INTREANOLD	Reactive power no-load interrupt	Power calculation circuit
		INTACTNOLD	Active power no-load interrupt	Power calculation circuit
		INTCF	CF output interrupt	Digital frequency conversion circuit
		INTAPPEOF	APPHR register overflow interrupt	Power calculation circuit
		INTREAEOF	REAHR register overflow interrupt	Power calculation circuit
		INTACTEOF	ACTHR register overflow interrupt	Power calculation circuit
		INTAPPEHF	APPHR register half full interrupt	Power calculation circuit
		INTREAEHF	REAHR register half full interrupt	Power calculation circuit
		INTACTEHF	ACTHR register half full interrupt	Power calculation circuit
		INTWFSM	WAVE form register update interrupt	Power calculation circuit
		INTPKI1	Peak detection interrupt for current channel	Power quality measurement circuit
		INTPKV1	Peak detection interrupt for voltage channel	Power quality measurement circuit
		INTCYCEND	Synchronous reading interrupt (accumulation completion interrupt of LINNUM)	Power calculation circuit

Table 20-2. Interrupt Source List of Extended SFR (2/2)

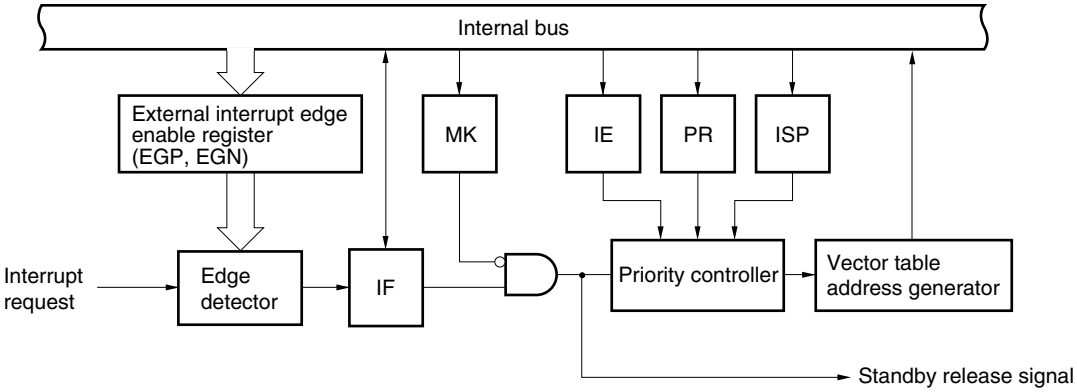
Interrupt Type	Internal/ External	Interrupt Source		Circuit
		Name	Trigger	
Maskable	Internal (extended SFR)	INTZXTO1	Zero-crossing timeout interrupt (voltage channel 1)	Power quality measurement circuit
		INTZXTO2	Zero-crossing timeout interrupt (voltage channel 2)	Power quality measurement circuit
		INTZX1	Zero-crossing detection interrupt (voltage channel 1)	Power quality measurement circuit
		INTZX2	Zero-crossing detection interrupt (voltage channel 2)	Power quality measurement circuit
		INTSAG1	SAG detection interrupt (voltage channel 1)	Power quality measurement circuit
		INTSAG2	SAG detection interrupt (voltage channel 2)	Power quality measurement circuit
		INTRQFLG	Interrupt from extended SFR space	–

Figure 20-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal maskable interrupt



(B) External maskable interrupt (INTPn)

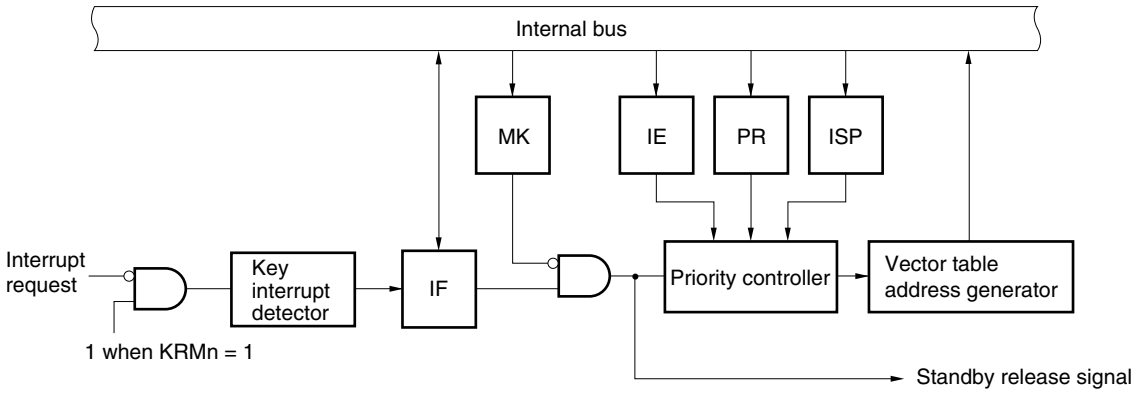


Remark n = 0 to 2, 5: 78K0/LE3-M
n = 0 to 3, 5: 78K0/LG3-M

IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

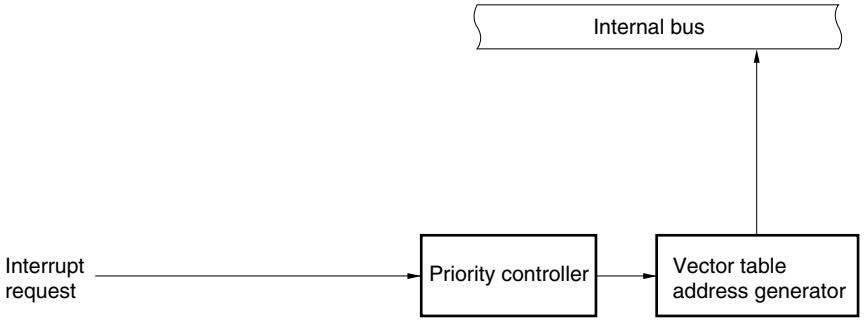
Figure 20-1. Basic Configuration of Interrupt Function (2/2)

(C) External maskable interrupt (INTKR)



Remark n = 0, 1: 78K0/LE3-M
n = 0 to 5: 78K0/LG3-M

(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag
KRM: Key return mode register

20.3 Registers Controlling Interrupt Functions

The following eight types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L, IF0H, IF1L, IF1H)
- Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H)
- Extended SFR interrupt request flag register (IF20, IF21, IF22, IF23)
- Extended SFR Interrupt mask flag register (MK20, MK21, MK22, MK23)
- Priority specification flag register (PR0L, PR0H, PR1L, PR1H)
- External interrupt rising edge enable register (EGP)
- External interrupt falling edge enable register (EGN)
- Program status word (PSW)

Table 20-3 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 20-3. Flags Corresponding to Interrupt Request Sources

78K0/ LE3-M	78K0/ LG3-M	Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
				Register		Register		Register
√	√	INTLVI	LVIIF	IF0L	LVIMK	MK0L	LVIPR	PR0L
√	√	INTP0	PIF0		PMK0		PPR0	
√	√	INTP1	PIF1		PMK1		PPR1	
√	√	INTP2	PIF2		PMK2		PPR2	
–	√	INTP3	PIF3		PMK3		PPR3	
√	√	INTP5	PIF5		PMK5		PPR5	
√	√	INTSRE6	SREIF6		SREMK6		SREPR6	
√	√	INTSR6	SRIF6	IF0H	SRMK6	MK0H	SRPR6	PR0H
√	√	INTST6	STIF6		STMK6		STPR6	
√	√	INTCSI10	CSIIF10[Note 1]		CSIMK10[Note 2]		CSIPR10[Note 3]	
		INTST0	STIF0[Note 1]		STMK0[Note 2]		STPR0[Note 3]	
√	√	INTTMH1	TMIFH1		TMMKH1		TMPRH1	
√	√	INTTMH0	TMIFH0		TMMKH0		TMPRH0	
√	√	INTTM50	TMIF50		TMMK50		TMPR50	
√	√	INTTM000	TMIF000		TMMK000		TMPR000	
√	√	INTTM010	TMIF010		TMMK010		TMPR010	
√	√	INTAD	ADIF	IF1L	ADMK	MK1L	ADPR	PR1L
√	√	INTSR0	SRIF0		SRMK0		SRPR0	
√	√	INTTM51[Note 4]	TMIF51		TMMK51		TMPR51	
√	√	INTKR	KRIF		KRMK		KRPR	
√	√	INTTM52	TMIF52		TMMK52		TMPR52	
√	√	INTTMH2	TMHIF2	IF1H	TMHMK2	MK1H	TMHPR2	PR1H
√	√	INTACSI	ACSIIF		ACSIMK		ACSIPR	

(**Note** is listed on the next page.)

Notes 1. If either interrupt source INTCSI10 or INTST0 is generated, bit 2 of IF0H is set (1).

2. Bit 2 of MK0H supports both interrupt sources INTCSI10 and INTST0.

3. Bit 2 of PR0H supports both interrupt sources INTCSI10 and INTST0.

4. When 8-bit timer/event counter 51 and 8-bit timer H1 are used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (see **Figure 8-15 Transfer Timing**).

Table 20-4. Flags Corresponding to Extended SFR Interrupt Request Sources

78K0/ LE3-M	78K0/ LG3-M	Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag	
				Register		Register
√	√	INTRTC0	RTC0IF	IF20	RTC0MK	MK20
√	√	INTRTC2	RTC2IF		RTC2MK	
√	√	INTAD2	ADIF2		ADMK2	
√	√	INTFAULTSIGN	FAULTSIGNIF		FAULTSIGNMK	
√	√	INTREASIGN	REASIGNIF		REASIGNMK	
√	√	INTACTSIGN	ACTSIGNIF		ACTSIGNMK	
√	√	INTAPPNOLD	APPNOLDIF		APPNOLDMK	
√	√	INTREANOLD	REANOLDIF		REANOLDMK	
√	√	INTACTNOLD	ACTNOLDIF	IF21	ACTNOLDMK	MK21
√	√	INTCF	CFIF		CFMK	
√	√	INTAPPEOF	APPEOFIF		APPEOFMK	
√	√	INTREAEOF	REAEOFIF		REAEOFMK	
√	√	INTACTEOF	ACTEOFIF		ACTEOFMK	
√	√	INTAPPEHF	APPEHFIF		APPEHFMK	
√	√	INTREAEHF	REAEHFIF		REAEHFMK	
√	√	INTACTEHF	ACTEHFIF	IF22	ACTEHFMK	MK22
√	√	INTWFSM	WFSMIF		WFSMMK	
√	√	INTPKI1	PKI1IF		PKI1MK	
√	√	INTPKV1	PKV1IF		PKV1MK	
√	√	INTCYCEND	CYCENDIF		CYCENDMK	
√	√	INTZXTO1	ZXTO1IF		ZXTO1MK	
√	√	INTZXTO2	ZXTO2IF	IF23	ZXTO2MK	MK23
√	√	INTZX1	ZX1IF		ZX1MK	
√	√	INTZX2	ZX2IF		ZX2MK	
√	√	INTSAG1	SAG1IF		SAG1MK	
√	√	INTSAG2	SAG2IF		SAG2MK	
<R> √	√	INTRQFLG	–		–	

(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

IF0L, IF0H, IF1L, and IF1H are set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H, and IF1L and IF1H are combined to form 16-bit registers IF0 and IF1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Cautions 1. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

Figure 20-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	0	PIF3[Note]	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	2	<1>	<0>
IF1L	TMIF52	0	0	KRIF	TMIF51	0	SIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	3	2	1	<0>
IF1H	0	0	0	ACSIIF	0	0	0	TMHIF2

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note 78K0/LG3-M only.

Caution Be sure to clear bit 5 of IF0L, bits 2, 5, and 6 of IF1L, and bit 1 to 3 and 5 to 7 of IF1H to 0.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

MK0L, MK0H, MK1L, and MK1H are set by a 1-bit or 8-bit memory manipulation instruction. When MK0L and MK0H, and MK1L and MK1H are combined to form 16-bit registers MK0 and MK1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 20-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	1	PMK3[Note]	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK52	1	1	KRMK	TMMK51	1	SRMK0	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	<4>	3	2	1	<0>
MK1H	1	1	1	ACSIMK	1	1	1	TMHMK2

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note 78K0/LG3-M only.

Caution Be sure to set bits 5 of MK0L, bits 2, 5, and 6 of MK1L, and bits 1 to 3 and 5 to 7 of MK1H to 1.

(3) Extended SFR interrupt request flag registers (IF20, IF21, IF22, IF23)

The extended SFR interrupt request flags are set to 1 when the corresponding interrupt request is generated. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is not automatically cleared.

IF20, IF21, IF22, and IF23 are allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears these registers to 00H.

<R> **Caution If clearing the extended SFR interrupt request flag before the extended SFR interrupt mask flag, clear the extended SFR interrupt request flag twice.**

Figure 20-4. Format of Extended SFR Interrupt Request Flag Registers (IF20, IF21, IF22, IF23)

Address: 80H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF20	REANOLDIF	APPNOLDIF	ACTSIGNIF	REASIGNIF	FAULTSIGNIF	ADIF2	RTC2IF	RTC0IF

Address: 81H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF21	REAEHFIF	APPEHFIF	ACTEOFIF	REAEOFIF	APPEOFIF	0	CFIF	ACTNOLDIF

Address: 82H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF22	ZXTO1IF	CYCENDIF	0	PKV1IF	0	PKI1IF	WFSMIF	ACTEHFIF

Address: 83H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
<R> IF23	0	0	0	SAG2IF	SAG1IF	ZX2IF	ZX1IF	ZXTO2IF

XXIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

(4) Extended SFR Interrupt mask flag registers (MK20, MK21, MK22, MK23)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

MK20, MK21, MK22, and MK23 are allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears these registers to FFH.

Figure 20-5. Format of Extended SFR Interrupt Mask Flag Registers (MK20, MK21, MK22, MK23)

Address: 84H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK20	REANOLDMK	APPNOLDMK	ACTSIGNMK	REASIGNMK	FAULTSIGNMK	ADMK2	RTC2MK	RTC0MK

Address: 85H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK21	REAEHFMK	APPEHFMK	ACTEOFMK	REAEOFMK	APPEOFMK	1	CFMK	ACTNOLDMK

Address: 86H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK22	ZXTO1MK	CYCENDMK	1	PKV1MK	1	PKI1MK	WFSMMK	ACTEHFMK

Address: 87H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK23	1	1	1	SAG2MK	SAG1MK	ZX2MK	ZX1MK	ZXTO2MK

XXMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

(5) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority order.

PR0L, PR0H, PR1L, and PR1H are set by a 1-bit or 8-bit memory manipulation instruction. If PR0L and PR0H, and PR1L and PR1H are combined to form 16-bit registers PR0 and PR1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 20-6. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	1	PPR3[Note]	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	<7>	6	5	<4>	<3>	2	<1>	<0>
PR1L	TMPR52	1	1	KRPR	TMPR51	1	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	<4>	3	2	1	<0>
PR1H	1	1	1	ACSIPR	1	1	1	TMHPR2

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Note 78K0/LG3-M only.

Caution Be sure to set bits 5 of PR0L, bits 2, 5, and 6 of PR1L, and bits 1 to 3 and 5 to 7 of PR1H to 1.

(6) External interrupt rising edge enable register (EGP), external interrupt falling edge enable register (EGN)

These registers specify the valid edge for INTP0 to INTP3 and INTP5.

EGP and EGN are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 20-7. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN)

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	0	EGP3 Note	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGN5	0	EGN3 Note	EGN2	EGN1	EGN0

(a) EGPn, EGNn (n = 0, 2, 3, and 5)

EGPn	EGNn	INTPn pin valid edge selection (n = 0, 2, 3, and 5)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

(b) EGP1, EGN1

EGP1	EGN1	INTP1 signal valid edge selection
0	0	Edge detection disabled
0	1	Setting prohibited
1	0	Rising edge
1	1	Setting prohibited

Note 78K0/LG3-M only.

Table 20-5 shows the ports corresponding to EGPn and EGNn.

Table 20-5. Ports Corresponding to EGPn and EGNn

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120/EXLVI	INTP0
EGP1	EGN1	–	INTP1
EGP2	EGN2	P33/TI000/BUZ	INTP2
EGP3 Note	EGN3 Note	P31 Note /TOH1	INTP3 Note
EGP5	EGN5	P30	INTP5

Note 78K0/LG3-M only.

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 2 and 5: 78K0/LE3-M
n = 0 to 3 and 5: 78K0/LG3-M

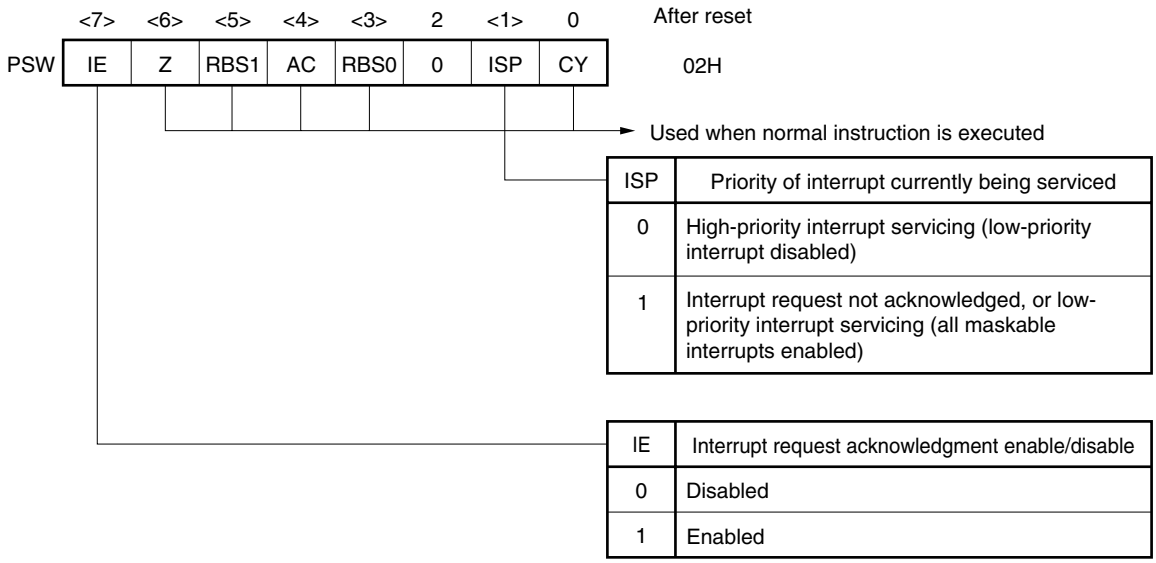
(7) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP flag that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 20-8. Format of Program Status Word



ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (low-priority interrupt disabled)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (all maskable interrupts enabled)

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

20.4 Interrupt Servicing Operations

20.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 20-6 below.

For the interrupt request acknowledgment timing, see **Figure 20-9** and **Figure 20-10**.

Table 20-6. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

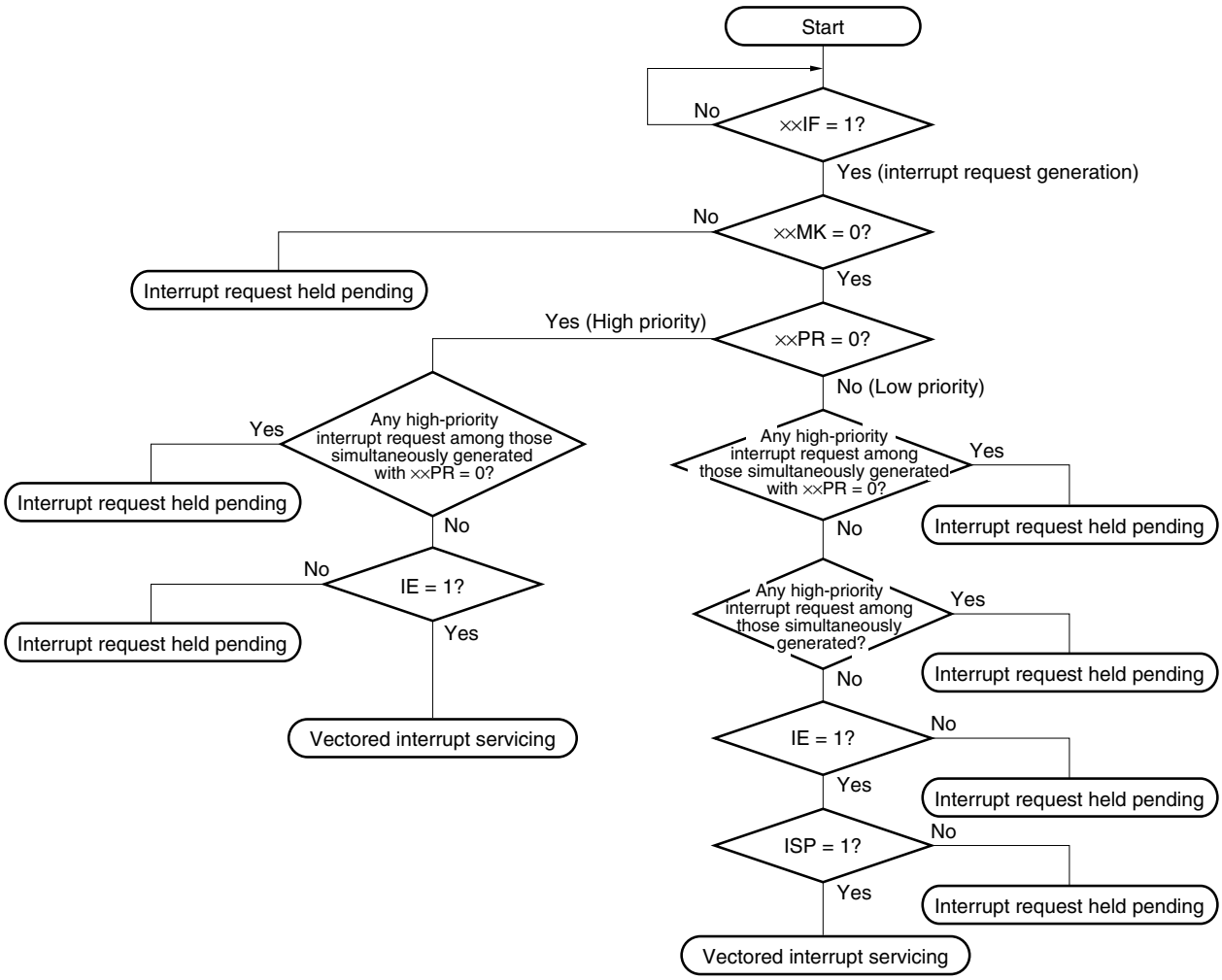
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 20-9 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

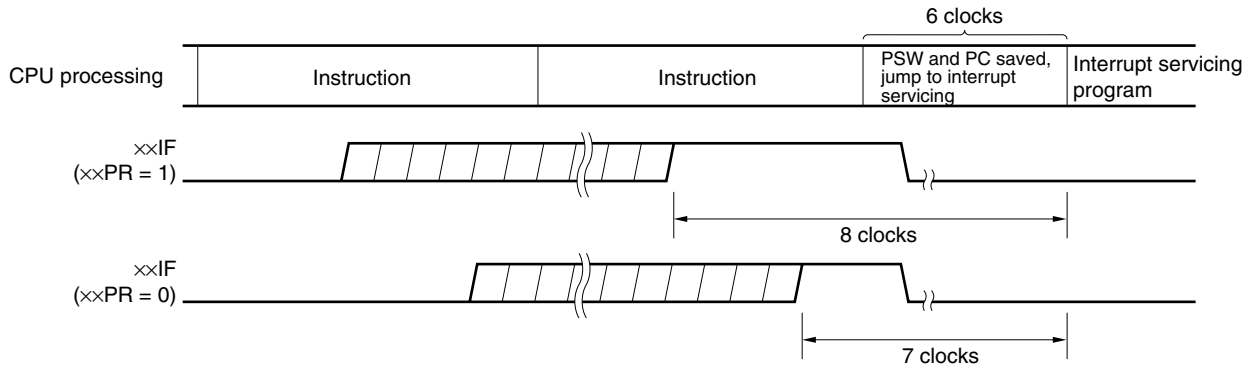
Restoring from an interrupt is possible by using the RETI instruction.

Figure 20-9. Interrupt Request Acknowledgment Processing Algorithm



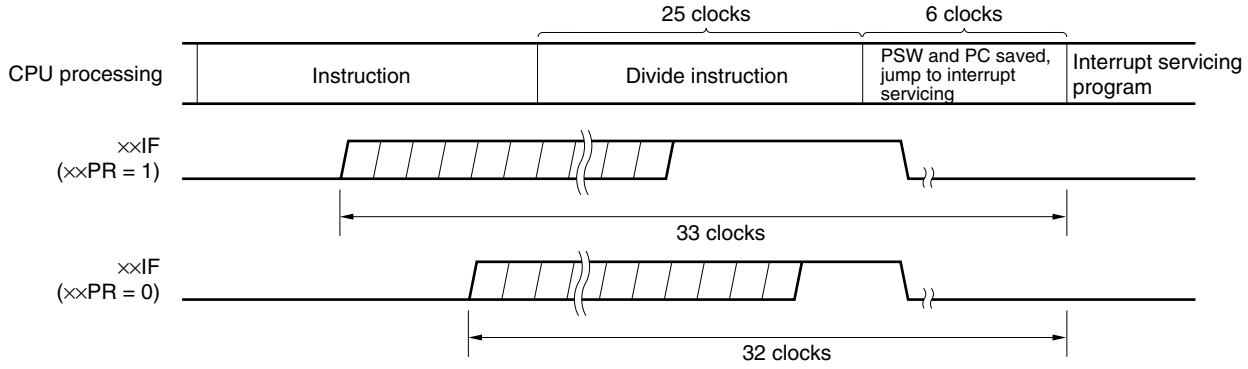
××IF: Interrupt request flag
××MK: Interrupt mask flag
××PR: Priority specification flag
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP: Flag that indicates the priority level of the interrupt currently being serviced (0 = high-priority interrupt servicing, 1 = No interrupt request acknowledged, or low-priority interrupt servicing)

Figure 20-10. Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock: 1/f_{CPU} (f_{CPU}: CPU clock)

Figure 20-11. Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: 1/f_{CPU} (f_{CPU}: CPU clock)

20.4.2 Software interrupt request acknowledgment

A software interrupt acknowledge is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (003EH, 003FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

Caution Do not use the RETI instruction for restoring from the software interrupt.

20.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 20-7 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 20-12 shows multiple interrupt servicing examples.

Table 20-7. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request				Software Interrupt Request
		PR = 0		PR = 1		
		IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP = 0	○	×	×	×	○
	ISP = 1	○	×	○	×	○
Software interrupt		○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP and IE are flags contained in the PSW.

ISP = 0: An interrupt with higher priority is being serviced.

ISP = 1: No interrupt request has been acknowledged, or an interrupt with a lower priority is being serviced.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

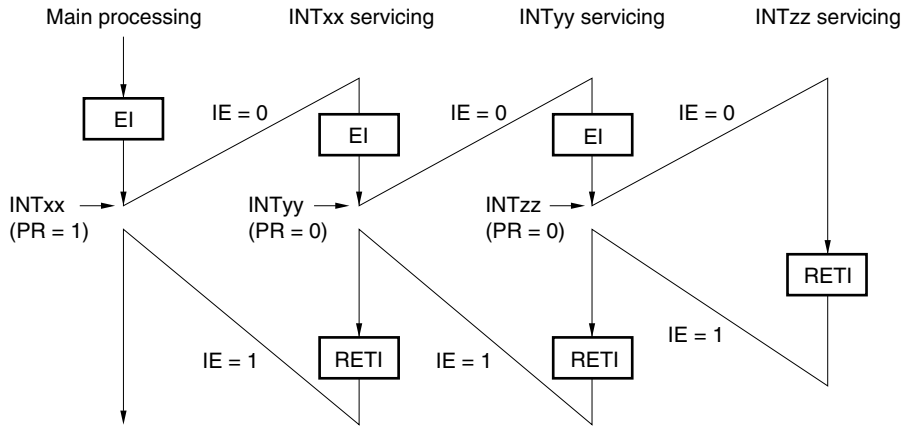
4. PR is a flag contained in PR0L, PR0H, PR1L, and PR1H.

PR = 0: Higher priority level

PR = 1: Lower priority level

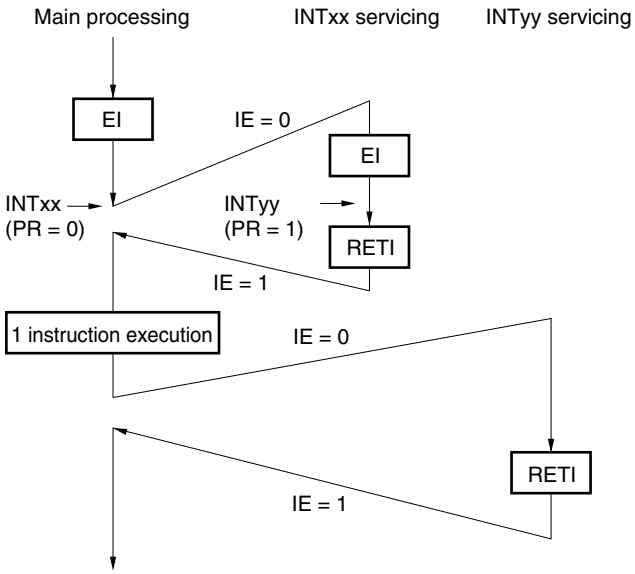
Figure 20-12. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

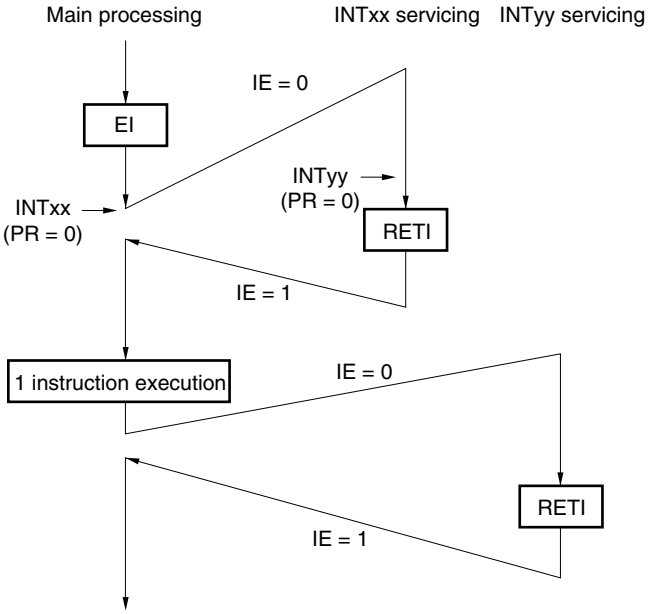


Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
PR = 1: Lower priority level
IE = 0: Interrupt request acknowledgment disabled

Figure 20-12. Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
IE = 0: Interrupt request acknowledgment disabled

20.4.4 Interrupt request hold

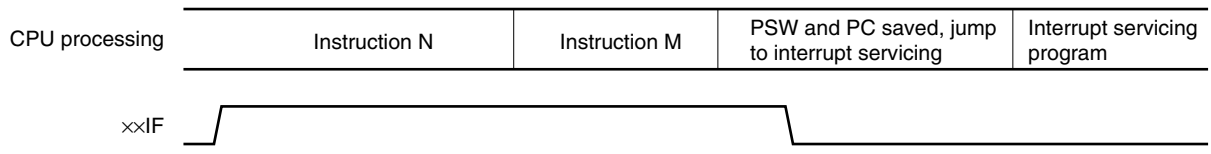
There are instructions where, even if an interrupt request is issued for them while another instruction is being executed, request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV A, PSW
- MOV PSW, A
- MOV1 PSW. bit, CY
- MOV1 CY, PSW. bit
- AND1 CY, PSW. bit
- OR1 CY, PSW. bit
- XOR1 CY, PSW. bit
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- PUSH PSW
- POP PSW
- BT PSW. bit, $addr16
- BF PSW. bit, $addr16
- BTCLR PSW. bit, $addr16
- EI
- DI
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, MK0L, MK0H, MK1L, MK1H, PR0L, PR0H, PR1L, and PR1H registers.

Caution The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.

Figure 20-13 shows the timing at which interrupt requests are held pending.

Figure 20-13. Interrupt Request Hold



Remarks 1. Instruction N: Interrupt request hold instruction

2. Instruction M: Instruction other than interrupt request hold instruction

3. The ××PR (priority level) values do not affect the operation of ××IF (interrupt request).

CHAPTER 21 KEY INTERRUPT FUNCTION

	78K0/LE3-M	78K0/LG3-M
Key interrupt	2 ch	6 ch

21.1 Functions of Key Interrupt

A key interrupt (INTKR) can be generated by setting the key return mode register (KRM) and inputting a falling edge to the key interrupt input pins (KRn).

Table 21-1. Assignment of Key Interrupt Detection Pins

Flag	Description
KRMn	Controls KRn signal in 1-bit units.

Remark n = 0, 1: 78K0/LE3-M
n = 0 to 5: 78K0/LG3-M

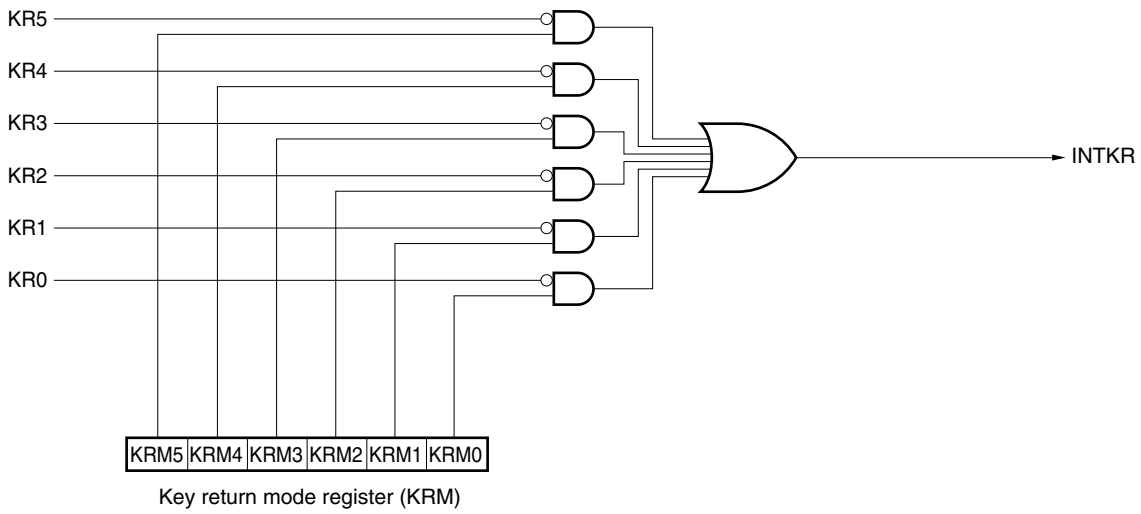
21.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

Table 21-2. Configuration of Key Interrupt

Item	Configuration
Control register	Key return mode register (KRM)

Figure 21-1. Block Diagram of Key Interrupt



Remark KR0, KR1: 78K0/LE3-M
KR0 to KR5: 78K0/LG3-M

21.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register is used to set whether to detect a key interrupt (INTKR) when a falling edge of the key interrupt input pins (KRn) is generated.

KRM is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears KRM to 00H.

Remark n = 0, 1: 78K0/LE3-M
n = 0 to 5: 78K0/LG3-M

Figure 21-2. Format of Key Return Mode Register (KRM)

(a) 78K0/LE3-M

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	0	0	KRM1	KRM0

(b) 78K0/LG3-M

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. When setting the KRMn bit to 1 in order to use the key interrupt function, set the bit of the corresponding pull-up resistor option register (PU4) to 1.

2. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

3. If detection of key interrupt signals is disabled (KRMn = 0), the corresponding Pxx pins can be used as a normal port.

4. When using the KRn pin as a segment key scan input pin while using the segment key scan function (KSON = 1), set KRMn to 1. When not using the KRn pin as a segment key scan input pin, set KRMn to 0 (see Figure 18-8).

Remark n = 0, 1: 78K0/LE3-M
n = 0 to 5: 78K0/LG3-M

CHAPTER 22 POWER CALCULATION CIRCUIT

22.1 Power Calculation Circuit Functions

This circuit measures the power and amount of power (energy) through linkage with the ΔΣ-type A/D converter, the digital filter for the A/D converter, and other functions (such as zero crossing, period and frequency measurement, SAG detection, and peak detection). The measurement functions include active power and energy calculation, reactive power and energy calculation, apparent power and energy calculation, and current and voltage RMS calculation.

The power calculation circuit can be used in both the single-phase two-wire and single-phase three-wire modes.

The power calculation circuit has the following functions:

- Integrator (for a di/dt current sensor (Rogowski coil))
- 90° phase shift (for reactive power calculation)
- Current and voltage RMS calculation
- Active power and energy calculation
- Reactive power and energy calculation
- Apparent power and energy calculation
- Ampere-hour accumulation
- Waveform sampling function

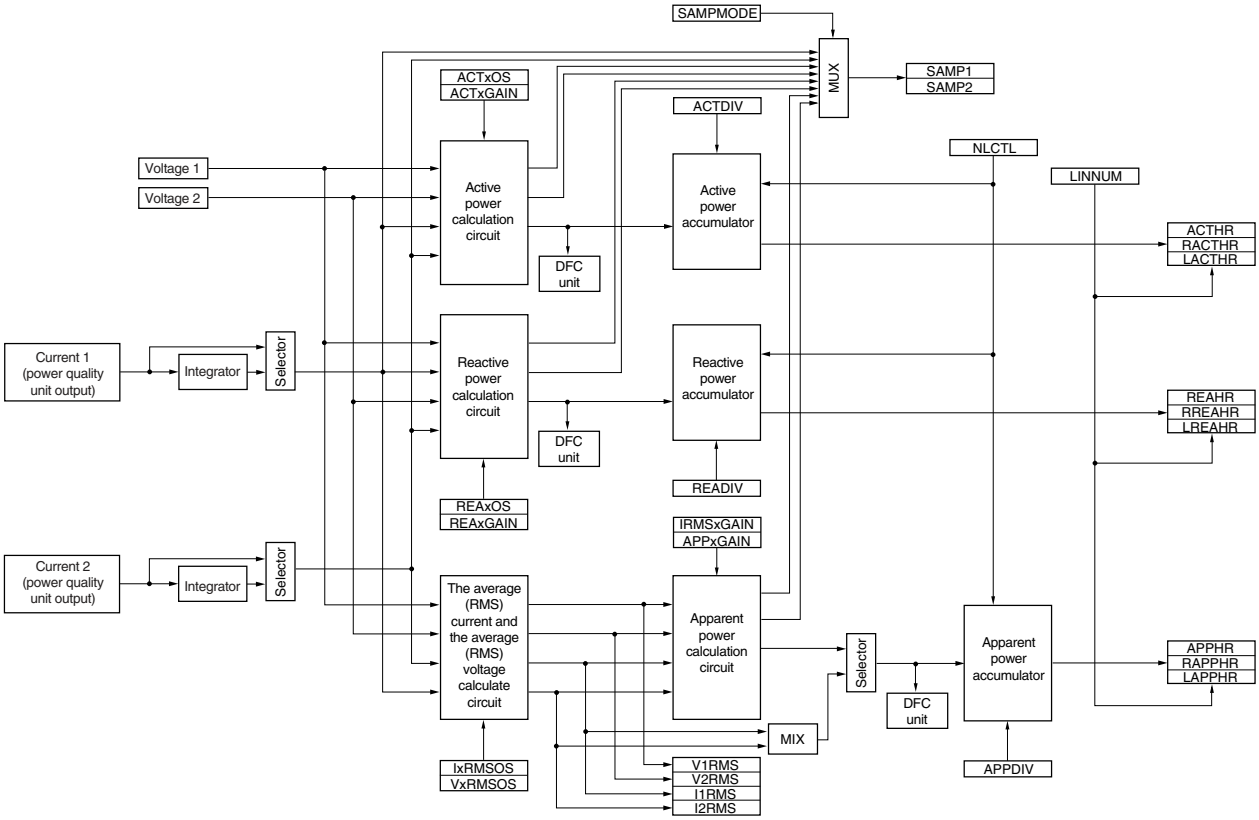
22.2 Configuration of Power Calculation Circuit

The power calculation circuit includes the following hardware.

Table 22-1. Configuration of Power Calculation Circuit

Item	Configuration
Controller	Current integrator circuit
	90° phase shifter circuit
	Current and voltage RMS calculation circuit
	Active power and energy calculation circuit
	Reactive power and energy calculation circuit
	Apparent power and energy calculation circuit
	Ampere-hour calculation circuit
	Waveform sampling circuit
Registers	RMS registers for voltage channels 1 and 2 (V1RMS, V2RMS)
	RMS registers for current channels 1 and 2 (I1RMS, I2RMS)
	Active power accumulation reading register (ACTHR)
	Active power accumulation reading and resetting register (RACTHR)
	Active power accumulation synchronous reading register (LACTHR)
	Reactive power accumulation reading register (REAHR)
	Reactive power accumulation reading and resetting register (RREAHR)
	Reactive power accumulation synchronous reading register (LREAHR)
	Apparent power accumulation reading register (APPHR)
	Apparent power accumulation reading and resetting register (RAPPHR)
	Apparent power accumulation synchronous reading register (LAPPHR)
	Sampling result registers 1 and 2 (SAMP1, SAMP2)
Control registers	Power calculation mode control register 1 (PWCTL1)
	Power calculation mode control register 2 (PWCTL2)
	No-load level control register (NLCTL)
	Active power scaling specification register (ACTDIV)
	Reactive power scaling specification register (READIV)
	Apparent power scaling specification register (APPDIV)
	Line cycle number specification register (LINNUM)
	Active power gain specification registers 1 and 2 (ACT1GAIN, ACT2GAIN)
	Reactive power gain specification registers 1 and 2 (REA1GAIN, REA2GAIN)
	Apparent power gain specification registers 1 and 2 (APP1GAIN, APP2GAIN)
	RMS gain specification registers for current channels 1 and 2 (IRMS1GAIN, IRMS2GAIN)
	Active power offset specification registers 1 and 2 (ACT1OS, ACT2OS)
	Reactive power offset specification registers 1 and 2 (REA1OS, REA2OS)
	RMS offset specification registers for current channels 1 and 2 (I1RMSOS, I2RMSOS)
	RMS offset specification registers for voltage channels 1 and 2 (V1RMSOS, V2RMSOS)
	Sampling mode selection register (SAMPMODE)

Figure 22-1. Block Diagram of Power Calculation Circuit



(1) Current integrator circuit

If a di/dt current sensor (such as a Rogowski coil) is connected, this circuit is used to integrate the current value.

(2) 90° phase shifter circuit

This circuit shifts the phase of the voltage channel 90° to calculate the reactive power.

(3) Current and voltage RMS calculation circuit

This circuit calculates the average (RMS) current and the average (RMS) voltage.

(4) Active power and energy calculation circuit

This circuit is used to calculate the active power and energy.

(5) Reactive power and energy calculation circuit

This circuit is used to calculate the reactive power and energy.

(6) Apparent power and energy calculation circuit

This circuit is used to calculate the apparent power and energy. Because the same circuit is used for this circuit and the ampere-hour calculation circuit, select and use one.

(7) Ampere-hour calculation circuit

This circuit is used to calculate the ampere-hour charge. Because the same circuit is used for this circuit and the apparent power and energy calculation circuit, select and use one.

(8) Waveform sampling circuit

This circuit is used to read the calculation results each time A/D converter sampling is performed (including the current value, voltage value, active power, reactive power, and apparent power). Of these results, two can be selected using the SAMMODE register and read. For details, see **22.4.8 Waveform sampling function**.

22.3 Power Calculation Circuit

The power calculation circuit uses the following registers.
These registers are all allocated to the extended SFR space.
For details about how to access the extended SFR space, see **CHAPTER 17 EXTENDED SFR INTERFACE**.

- Power calculation mode control register 1 (PWCTL1)
- Power calculation mode control register 2 (PWCTL2)
- No-load level control register (NLCTL)
- Active power scaling specification register (ACTDIV)
- Reactive power scaling specification register (READIV)
- Apparent power scaling specification register (APPDIV)
- RMS registers for voltage channels 1 and 2 (V1RMS, V2RMS)
- RMS registers for current channels 1 and 2 (I1RMS, I2RMS)
- Active power accumulation reading register (ACTHR)
- Active power accumulation reading and resetting register (RACTHR)
- Active power accumulation synchronous reading register (LACTHR)
- Reactive power accumulation reading register (REAHR)
- Reactive power accumulation reading and resetting register (RREAHR)
- Reactive power accumulation synchronous reading register (LREAHR)
- Apparent power accumulation reading register (APPHR)
- Apparent power accumulation reading and resetting register (RAPPHR)
- Apparent power accumulation synchronous reading register (LAPPHR)
- Line cycle number specification register (LINNUM)
- Active power gain specification registers 1 and 2 (ACT1GAIN, ACT2GAIN)
- Reactive power gain specification registers 1 and 2 (REA1GAIN, REA2GAIN)
- Apparent power gain specification registers 1 and 2 (APP1GAIN, APP2GAIN)
- RMS gain specification registers for current channels 1 and 2 (IRMS1GAIN, IRMS2GAIN)
- Active power offset specification registers 1 and 2 (ACT1OS, ACT2OS)
- Reactive power offset specification registers 1 and 2 (REA1OS, REA2OS)
- RMS offset specification registers for current channels 1 and 2 (I1RMSOS, I2RMSOS)
- RMS offset specification registers for voltage channels 1 and 2 (V1RMSOS, V2RMSOS)
- Sampling mode selection register (SAMPMODE)
- Sampling result registers 1 and 2 (SAMP1, SAMP2)

(1) Power calculation mode control register 1 (PWCTL1)

The PWCTL1 register is used to control the power calculation, power quality measurement, and digital frequency conversion.

PWCTL1 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-2. Format of Power Calculation Mode Control Register 1 (PWCTL1) (1/2)

Address: 180H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PWCTL1	PWREN	READIS	APPDIS	CYCDIS	SAMPEN	APPRMS CFCON	INTE2	INTE1

PWREN[Note 1]	Control power calculation, power quality measurement, and digital frequency conversion
0	Disables operation of the power calculation circuit.
1	Enables operation of the power calculation circuit.

READIS	Control reactive power measurement
0	Enables reactive power measurement.
1	Disables reactive power measurement.

APPDIS	Control apparent power measurement
0	Enables apparent power measurement.
1	Disables apparent power measurement.

CYCDIS	Control synchronous reading interrupt (CYCEND) detection
0	Enables synchronous reading interrupt (CYCEND) detection.
1	Disables synchronous reading interrupt (CYCEND) detection[Note 2].

Notes 1. By setting ADCE2 bit of ADM2 register and PWREN bit of PWCTL1 register, the operation is controlled as follows.

ADCE2	PWREN	ΔΣ-type A/D converter (analog block and digital block)	power calculation, power quality measurement, and digital frequency conversion
0	0	Cannot operate	Cannot operate
0	1	Cannot operate	Cannot operate
1	0	Operable	Cannot operate
1	1	Operable	Operable

2. If CYCDIS is 1, the CYCEND interrupt is not generated when the number of half-line cycles reaches the value specified for the LINNUM register. In addition, the accumulation register is not cleared when the LINNUM register is written to.

Figure 22-2. Format of Power Calculation Mode Control Register 1 (PWCTL1) (2/2)

Address: 180H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PWCTL1	PWREN	READIS	APPDIS	CYCDIS	SAMPEN	APPRMS CFCON	INTE2	INTE1

SAMPEN	Control waveform sample mode
0	Disables waveform sample mode.
1	Enables waveform sample mode.

APPRMS CFCON	Select apparent power or the average (RMS) current Irms for the apparent power accumulation register and CF pulse output
0	If this is specified, the apparent power accumulation register accumulates the apparent power. If the CFSEL1 bit of the CFCTL register is set to 1, the apparent power is output as CF pulses. CHMD = 0 (two-wire mode): Apparent power 1 is output as CF pulses. CHMD = 1 (three-wire mode): Apparent power 1 and apparent power 2 are output as CF pulses. If this is specified, the apparent power accumulation register accumulates the average (RMS) current Irms. If the CFSEL1 bit of the CFCTL register is set to 1, the Irms is output as CF pulses. CHMD = 0 (two-wire mode): I1rms is output as CF pulses. CHMD = 1 (three-wire mode): I1rms and I2rms are output as CF pulses.
1	If this is specified, the apparent power accumulation register accumulates the average (RMS) current Irms. If the CFSEL1 bit of the CFCTL register is set to 1, the Irms is output as CF pulses. CHMD = 0 (two-wire mode): I1rms is output as CF pulses. CHMD = 1 (three-wire mode): I1rms and I2rms are output as CF pulses.

INTE2	Control integrator 2 (for current channel 2)
0	Disables operation of the integrator 2.
1	Enables operation of the integrator 2.

INTE1	Control integrator 1 (for current channel 1)
0	Disables operation of the integrator 1.
1	Enables operation of the integrator 1.

(2) Power calculation mode control register 2 (PWCTL2)

The PWCTL2 register is used to control the power calculation, power quality measurement, and digital frequency conversion.

PWCTL2 is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-3. Format of Power Calculation Mode Control Register 2 (PWCTL2) (1/2)

Address: 181H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PWCTL2	ACTDIS	0	REASIGN	ACTSIGN	ABSVARM	SAVARM	POAM	ABSAM

ACTDIS	Control active power measurement
0	Enables active power measurement.
1	Disables active power measurement.

REASIGN	Specify the trigger for generating a reactive power sign change interrupt (INTREASIGN)
0	Generates an interrupt when the reactive power sign changes from positive to negative.
1	Generates an interrupt when the reactive power sign changes from negative to positive.

ACTSIGN	Specify the trigger for generating a active power sign change interrupt (INTACTSIGN)
0	Generates an interrupt when the active power sign changes from positive to negative.
1	Generates an interrupt when the active power sign changes from negative to positive.

ABSVARM Note 1	Control accumulation of the absolute value of the reactive power and pulse output
0	Disables the reactive-power absolute-value accumulation mode.
1	Enables the reactive-power absolute-value accumulation mode.

SAVARM Note 1	Specify the sign for the reactive power accumulation mode
0	Specifies that the sign does not depend on the active power sign.
1	Specifies that the sign depends on the active power sign

Caution Be sure to clear bit 6 to 0.

Notes 1. The integration method for the reactive power signal can be selected by specifying values for the SAVARM and ABSVARM bits.

SAVARM	ABSVARM	Reactive Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Anti-tamper accumulation mode Note 2
1	1	Absolute value accumulation mode

2. If the active power is positive, the reactive power is added to the reactive energy accumulator. If the active power is negative, the reactive power is subtracted from the reactive energy accumulator. This setting affects both the reactive power registers and pulse output.

Figure 22-3. Format of Power Calculation Mode Control Register 2 (PWCTL2) (2/2)

Address: 181H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PWCTL2	ACTDIS	0	REASIGN	ACTSIGN	ABSVARM	SAVARM	POAM	ABSAM

POAM Note	Control accumulation of the positive value of the active power and pulse output
0	Disables the active-power positive value accumulation mode.
1	Enables the active-power positive value accumulation mode.

ABSAM Note	Control accumulation of the absolute value of the active power and pulse output
0	Disables the active-power absolute-value accumulation mode.
1	Enables the active-power absolute-value accumulation mode.

Caution Be sure to clear bit 6 to 0.

Note The integration method for the active power signal can be selected by specifying values for the POAM and ABSAM bits.

POAM	ABSAM	Reactive Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Positive value accumulation mode
1	1	Absolute value accumulation mode

(3) No-load level control register (NLCTL)

The NLCTL register is used to set the no-load detection.

NLCTL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-4. Format of No-load Level Control Register (NLCTL)

Address: 182H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NLCTL	DISREACMP	ZXRMS	APPNO LOAD1	APPNO LOAD0	REANO LOAD1	REANO LOAD0	ACTNO LOAD1	ACTNO LOAD0

DISREACMP	Specify whether to enable reactive power gain compensation according to the line frequency
0	Enables gain compensation.
1	Disables gain compensation.

ZXRMS	Specify whether to synchronize with the line frequency when storing the rms value
0	Does not synchronize with the line frequency.
1	Synchronizes with the line frequency.

APPNO LOAD1	APPNO LOAD0	Specify the no-load threshold value for the apparent power and IRMS
0	0	Disables no-load detection for the apparent power and IRMS.
0	1	Enables no-load detection for the apparent power and IRMS. Threshold value = 0.03% of full scale
1	0	Enables no-load detection for the apparent power and IRMS. Threshold value = 0.015% of full scale
1	1	Enables no-load detection for the apparent power and IRMS. Threshold value = 0.0075% of full scale

REANO LOAD1	REANO LOAD0	Specify the no-load threshold value for the reactive power
0	0	Disables no-load detection for the reactive power.
0	1	Enables no-load detection for the reactive power. Threshold value = 0.015% of full scale
1	0	Enables no-load detection for the reactive power. Threshold value = 0.0075% of full scale
1	1	Enables no-load detection for the reactive power. Threshold value = 0.0037% of full scale

ACTNO LOAD1	ACTNO LOAD0	Specify the no-load threshold value for the active power
0	0	Disables no-load detection for the active power.
0	1	Enables no-load detection for the active power. Threshold value = 0.015% of full scale
1	0	Enables no-load detection for the active power. Threshold value = 0.0075% of full scale
1	1	Enables no-load detection for the active power. Threshold value = 0.0037% of full scale

(4) Active power scaling specification register (ACTDIV)

The ACTDIV register is used to set the active power scaling specification.

ACTDIV is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-5. Format of Active Power Scaling Specification Register (ACTDIV)

Address: 183H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACTDIV	ACTDIV7	ACTDIV6	ACTDIV5	ACTDIV4	ACTDIV3	ACTDIV2	ACTDIV1	ACTDIV0

ACTDIV7 to 0	Specify the value of active power scaling
00H to FFH	Active power scaling Value

(5) Reactive power scaling specification register (READIV)

The READIV register is used to set the reactive power scaling specification.

READIV is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-6. Format of Reactive Power Scaling Specification Register (READIV)

Address: 184H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
READIV	READIV7	READIV6	READIV5	READIV4	READIV3	READIV2	READIV1	READIV0

READIV7 to 0	Specify the value of reactive power scaling
00H to FFH	Reactive power scaling value

(6) Apparent power scaling specification register (APPDIV)

The APPDIV register is used to set the apparent power scaling specification.

APPDIV is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-7. Format of Apparent Power Scaling Specification Register (APPDIV)

Address: 185H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
APPDIV	APPDIV7	APPDIV6	APPDIV5	APPDIV4	APPDIV3	APPDIV2	APPDIV1	APPDIV0

APPDIV7 to 0	Specify the value of apparent power scaling
00H to FFH	Apparent power scaling value

(7) RMS registers for voltage channels 1 and 2 (V1RMS, V2RMS)

These registers are used to store the RMS measured value of voltage channels 1 and 2.

V1RMS and V2RMS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 000000H.

Figure 22-8. Format of RMS Registers for Voltage Channels 1 and 2 (V1RMS, V2RMS)

(a) V1RMS

Address: 186H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V1RMSL	V1RMS7	V1RMS6	V1RMS5	V1RMS4	V1RMS3	V1RMS2	V1RMS1	V1RMS0

Address: 187H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V1RMSM	V1RMS15	V1RMS14	V1RMS13	V1RMS12	V1RMS11	V1RMS10	V1RMS9	V1RMS8

Address: 188H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V1RMSH	V1RMS23	V1RMS22	V1RMS21	V1RMS20	V1RMS19	V1RMS18	V1RMS17	V1RMS16

(b) V2RMS

Address: 189H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V2RMSL	V2RMS7	V2RMS6	V2RMS5	V2RMS4	V2RMS3	V2RMS2	V2RMS1	V2RMS0

Address: 18AH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V2RMSM	V2RMS15	V2RMS14	V2RMS13	V2RMS12	V2RMS11	V2RMS10	V2RMS9	V2RMS8

Address: 18BH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
V2RMSH	V2RMS23	V2RMS22	V2RMS21	V2RMS20	V2RMS19	V2RMS18	V2RMS17	V2RMS16

VnRMS23 to 0	Used to store the RMS measured value of voltage channels n (n = 1, 2)
000000H to FFFFFFH	RMS measured value of voltage channels n

(8) RMS registers for current channels 1 and 2 (I1RMS, I2RMS)

These registers are used to store the RMS measured value of current channels 1 and 2.

I1RMS and I2RMS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 000000H.

Figure 22-9. Format of RMS Registers for Current Channels 1 and 2 (I1RMS, I2RMS)

(a) I1RMS

Address: 18CH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I1RMSL	I1RMS7	I1RMS6	I1RMS5	I1RMS4	I1RMS3	I1RMS2	I1RMS1	I1RMS0

Address: 18DH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I1RMSM	I1RMS15	I1RMS14	I1RMS13	I1RMS12	I1RMS11	I1RMS10	I1RMS9	I1RMS8

Address: 18EH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I1RMSH	I1RMS23	I1RMS22	I1RMS21	I1RMS20	I1RMS19	I1RMS18	I1RMS17	I1RMS16

(b) I2RMS

Address: 18FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I2RMSL	I2RMS7	I2RMS6	I2RMS5	I2RMS4	I2RMS3	I2RMS2	I2RMS1	I2RMS0

Address: 190H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I2RMSM	I2RMS15	I2RMS14	I2RMS13	I2RMS12	I2RMS11	I2RMS10	I2RMS9	I2RMS8

Address: 191H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
I2RMSH	I2RMS23	I2RMS22	I2RMS21	I2RMS20	I2RMS19	I2RMS18	I2RMS17	I2RMS16

InRMS23 to 0	Used to store the RMS measured value of current channels n (n = 1, 2)
000000H to FFFFFFH	RMS measured value of current channels n

(9) Active power accumulation reading register (ACTHR)

This register is used to store the active power accumulation value.
This register value is not cleared after being read.
ACTHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-10. Format of Active Power Accumulation Reading Register (ACTHR)

Address: 192H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ACTHRL	ACTHR7	ACTHR6	ACTHR5	ACTHR4	ACTHR3	ACTHR2	ACTHR1	ACTHR0

Address: 193H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ACTHRM	ACTHR15	ACTHR14	ACTHR13	ACTHR12	ACTHR11	ACTHR10	ACTHR9	ACTHR8

Address: 194H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ACTHRH	ACTHR23	ACTHR22	ACTHR21	ACTHR20	ACTHR19	ACTHR18	ACTHR17	ACTHR16

ACTHR23 to 0	Used to store the accumulator value of the active power
000000H to FFFFFFH	Accumulator value of the active power (this register value is not cleared after being read)

(10) Active power accumulation reading and resetting register (RACTHR)

The active power accumulation value is stored in this register.
This register value is cleared after being read.
RACTHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-11. Format of Active Power Accumulation Reading and Resetting Register (RACTHR)

Address: 196H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RACTHRL	RACTHR7	RACTHR6	RACTHR5	RACTHR4	RACTHR3	RACTHR2	RACTHR1	RACTHR0

Address: 197H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RACTHRM	RACTHR15	RACTHR14	RACTHR13	RACTHR12	RACTHR11	RACTHR10	RACTHR9	RACTHR8

Address: 198H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RACTHRH	RACTHR23	RACTHR22	RACTHR21	RACTHR20	RACTHR19	RACTHR18	RACTHR17	RACTHR16

RACTHR23 to 0	Used to store the accumulator value of the active power
000000H to FFFFFFH	Accumulator value of the active power (this register value is cleared after being read)

(11) Active power accumulation synchronous reading register (LACTHR)

This register synchronizes the accumulator value of the active power with the line frequency and is used to store the value.

LACTHR is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 22-12. Format of Active Power Accumulation Synchronous Reading Register (LACTHR)

Address: 199H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LACTHRL	LACTHR7	LACTHR6	LACTHR5	LACTHR4	LACTHR3	LACTHR2	LACTHR1	LACTHR0

Address: 19AH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LACTHRM	LACTHR15	LACTHR14	LACTHR13	LACTHR12	LACTHR11	LACTHR10	LACTHR9	LACTHR8

Address: 19BH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LACTHRH	LACTHR23	LACTHR22	LACTHR21	LACTHR20	LACTHR19	LACTHR18	LACTHR17	LACTHR16

LACTHR23 to 0	Used to store the accumulator value of the active power
000000H to FFFFFFH	Accumulator value of the active power (stored in the register after synchronization with the line frequency)

(12) Reactive power accumulation reading register (REAHR)

The reactive power accumulation value is stored in this register.

This register value is not cleared after being read.

REAHR is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 22-13. Format of Reactive Power Accumulation Reading Register (REAHR)

Address: 19CH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
REAHRL	REAHR7	REAHR6	REAHR5	REAHR4	REAHR3	REAHR2	REAHR1	REAHR0

Address: 19DH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
REAHRM	REAHR15	REAHR14	REAHR13	REAHR12	REAHR11	REAHR10	REAHR9	REAHR8

Address: 19EH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
REAHRH	REAHR23	REAHR22	REAHR21	REAHR20	REAHR19	REAHR18	REAHR17	REAHR16

REAHR23 to 0	Used to store the accumulator value of the reactive power
000000H to FFFFFFH	Accumulator value of the reactive power (this register value is not cleared after being read)

(13) Reactive power accumulation reading and resetting register (RREAHR)

The reactive power accumulation value is stored in this register.
This register value is cleared after being read.
RREAHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-14. Format of Reactive Power Accumulation Reading and Resetting Register (RREAHR)

Address: 1A0H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RREAHRL	RREAHR7	RREAHR6	RREAHR5	RREAHR4	RREAHR3	RREAHR2	RREAHR1	RREAHR0

Address: 1A1H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RREAHRM	RREAHR15	RREAHR14	RREAHR13	RREAHR12	RREAHR11	RREAHR10	RREAHR9	RREAHR8

Address: 1A2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RREAHRH	RREAHR23	RREAHR22	RREAHR21	RREAHR20	RREAHR19	RREAHR18	RREAHR17	RREAHR16

RREAHR23 to 0	Used to store the accumulator value of the reactive power
000000H to FFFFFFH	Accumulator value of the reactive power (this register value is cleared after being read)

(14) Reactive power accumulation synchronous reading register (LREAHR)

This register synchronizes the accumulator value of the reactive power with the line frequency and is used to store the value.
LREAHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-15. Format of Reactive Power Accumulation Synchronous Reading Register (LREAHR)

Address: 1A3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LREAHRL	LREAHR7	LREAHR6	LREAHR5	LREAHR4	LREAHR3	LREAHR2	LREAHR1	LREAHR0

Address: 1A4H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LREAHRM	LREAHR15	LREAHR14	LREAHR13	LREAHR12	LREAHR11	LREAHR10	LREAHR9	LREAHR8

Address: 1A5H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LREAHRH	LREAHR23	LREAHR22	LREAHR21	LREAHR20	LREAHR19	LREAHR18	LREAHR17	LREAHR16

LREAHR23 to 0	Used to store the accumulator value of the reactive power
000000H to FFFFFFH	Accumulator value of the reactive power (stored in the register after synchronization with the line frequency)

(15) Apparent power accumulation reading register (APPHR)

The apparent power accumulation value is stored in this register.
This register value is not cleared after being read.
APPHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-16. Format of Apparent Power Accumulation Reading Register (APPHR)

Address: 1A6H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
APPHRL	APPHR7	APPHR6	APPHR5	APPHR4	APPHR3	APPHR2	APPHR1	APPHR0

Address: 1A7H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
APPHRM	APPHR15	APPHR14	APPHR13	APPHR12	APPHR11	APPHR10	APPHR9	APPHR8

Address: 1A8H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
APPHRH	APPHR23	APPHR22	APPHR21	APPHR20	APPHR19	APPHR18	APPHR17	APPHR16

APPHR23 to 0	Used to store the accumulator value of the apparent power
000000H to FFFFFFH	Accumulator value of the apparent power (this register value is not cleared after being read)

(16) Apparent power accumulation reading and resetting register (RAPPHR)

The reactive power accumulation value is stored in this register.
This register value is cleared after being read.
RAPPHR is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 000000H.

Figure 22-17. Format of Apparent Power Accumulation Reading and Resetting Register (RAPPHR)

Address: 1AAH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RAPPHRL	RAPPHR7	RAPPHR6	RAPPHR5	RAPPHR4	RAPPHR3	RAPPHR2	RAPPHR1	RAPPHR0

Address: 1ABH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RAPPHRM	RAPPHR15	RAPPHR14	RAPPHR13	RAPPHR12	RAPPHR11	RAPPHR10	RAPPHR9	RAPPHR8

Address: 1ACH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RAPPHRH	RAPPHR23	RAPPHR22	RAPPHR21	RAPPHR20	RAPPHR19	RAPPHR18	RAPPHR17	RAPPHR16

RAPPHR23 to 0	Used to store the accumulator value of the apparent power
000000H to FFFFFFH	Accumulator value of the apparent power (this register value is cleared after being read)

(17) Apparent power accumulation synchronous reading register (LAPPHR)

This register synchronizes the accumulator value of the apparent power with the line frequency and is used to store the value.

LAPPH is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 22-18. Format of Apparent Power Accumulation Synchronous Reading Register (LAPPHR)

Address: 1ADH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LAPPHRL	LAPPHR7	LAPPHR6	LAPPHR5	LAPPHR4	LAPPHR3	LAPPHR2	LAPPHR1	LAPPHR0

Address: 1AEH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LAPPHRM	LAPPHR15	LAPPHR14	LAPPHR13	LAPPHR12	LAPPHR11	LAPPHR10	LAPPHR9	LAPPHR8

Address: 1AFH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
LAPPHRH	LAPPHR23	LAPPHR22	LAPPHR21	LAPPHR20	LAPPHR19	LAPPHR18	LAPPHR17	LAPPHR16

LAPPHR23 to 0	Used to store the accumulator value of the apparent power
000000H to FFFFFFH	Accumulator value of the apparent power (stored in the register after synchronization with the line frequency)

(18) Line cycle number specification register (LINNUM)

The LINNUM register is used to set the line cycle number of accumulator in synchronous reading mode.

This register can be set by a half line unit.

LINNUM is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to FFFFH.

Figure 22-19. Format of Line Cycle Number Specification Register (LINNUM)

Address: 1B0H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
LINNUML	LINNUM7	LINNUM6	LINNUM5	LINNUM4	LINNUM3	LINNUM2	LINNUM1	LINNUM0

Address: 1B1H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
LINNUMH	LINNUM15	LINNUM14	LINNUM13	LINNUM12	LINNUM11	LINNUM10	LINNUM9	LINNUM8

LINNUM15 to 0	Specify the half line cycle number of accumulator
0000H to FFFFH	Half line cycle number

(19) Active power gain specification registers 1 and 2 (ACT1GAIN, ACT2GAIN)

The ACT1GAIN and ACT2GAIN registers are used to set the gain value of the active power.

ACT1GAIN and ACT2GAIN are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-20. Format of Active Power Gain Specification Registers 1 and 2 (ACT1GAIN, ACT2GAIN)

(a) ACT1GAIN

Address: 1B2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT1GAINL	ACT1GAIN7	ACT1GAIN6	ACT1GAIN5	ACT1GAIN4	ACT1GAIN3	ACT1GAIN2	ACT1GAIN1	ACT1GAIN0

Address: 1B3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT1GAINH	0	0	0	0	ACT1GAIN11	ACT1GAIN10	ACT1GAIN9	ACT1GAIN8

(b) ACT2GAIN

Address: 1B4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT2GAINL	ACT2GAIN7	ACT2GAIN6	ACT2GAIN5	ACT2GAIN4	ACT2GAIN3	ACT2GAIN2	ACT2GAIN1	ACT2GAIN0

Address: 1B5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT2GAINH	0	0	0	0	ACT2GAIN11	ACT2GAIN10	ACT2GAIN9	ACT2GAIN8

ACTnGAIN11 to 0	Specify the gain value of the active power (n = 1, 2)
0000H to 0FFFH	Gain value of active power

Caution Be sure to clear bits 4 to 7 of the ACT1GAINH and ACT2GAINH to 0.

(20) Reactive power gain specification registers 1 and 2 (REA1GAIN, REA2GAIN)

The REA1GAIN and REA2GAIN registers are used to set the gain value of the reactive power.

REA1GAIN and REA2GAIN are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-21. Format of Reactive Power Gain Specification Registers 1 and 2 (REA1GAIN, REA2GAIN)

(a) REA1GAIN

Address: 1B6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA1GAINL	REA1GAIN7	REA1GAIN6	REA1GAIN5	REA1GAIN4	REA1GAIN3	REA1GAIN2	REA1GAIN1	REA1GAIN0

Address: 1B7H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA1GAINH	0	0	0	0	REA1GAIN11	REA1GAIN10	REA1GAIN9	REA1GAIN8

(b) REA2GAIN

Address: 1B8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA2GAINL	REA2GAIN7	REA2GAIN6	REA2GAIN5	REA2GAIN4	REA2GAIN3	REA2GAIN2	REA2GAIN1	REA2GAIN0

Address: 1B9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA2GAINH	0	0	0	0	REA2GAIN11	REA2GAIN10	REA2GAIN9	REA2GAIN8

REAnGAIN11 to 0	Specify the gain value of the reactive power (n = 1, 2)
0000H to 0FFFH	Gain value of reactive power

Caution Be sure to clear bits 4 to 7 of the REA1GAINH and REA2GAINH to 0.

(21) Apparent power gain specification registers 1 and 2 (APP1GAIN, APP2GAIN)

The APP1GAIN and APP2GAIN registers are used to set the gain value of apparent power.

APP1GAIN and APP2GAIN are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-22. Format of Apparent Power Gain Specification Registers 1 and 2 (APP1GAIN, APP2GAIN)

(a) APP1GAIN

Address: 1BAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
APP1GAINL	APP1GAIN7	APP1GAIN6	APP1GAIN5	APP1GAIN4	APP1GAIN3	APP1GAIN2	APP1GAIN1	APP1GAIN0

Address: 1BBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
APP1GAINH	0	0	0	0	APP1GAIN11	APP1GAIN10	APP1GAIN9	APP1GAIN8

(b) APP2GAIN

Address: 1BCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
APP2GAINL	APP2GAIN7	APP2GAIN6	APP2GAIN5	APP2GAIN4	APP2GAIN3	APP2GAIN2	APP2GAIN1	APP2GAIN0

Address: 1BDH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
APP2GAINH	0	0	0	0	APP2GAIN11	APP2GAIN10	APP2GAIN9	APP2GAIN8

APPnGAIN11 to 0	Specify the gain value of the apparent power (n = 1, 2)
0000H to 0FFFH	Gain value of apparent power

Caution Be sure to clear bits 4 to 7 of the APP1GAINH and APP2GAINH to 0.

(22) RMS gain specification registers for current channels 1 and 2 (IRMS1GAIN, IRMS2GAIN)

The IRMS1GAIN and IRMS2GAIN registers are used to set the gain value of the current power.

IRMS1GAIN and IRMS2GAIN are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-23. Format of RMS gain Specification Registers for Current Channels 1 and 2 (IRMS1GAIN, IRMS2GAIN)

(a) IRMS1GAIN

Address: 1BEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IRMS1GAINL	IRMS1 GAIN7	IRMS1 GAIN6	IRMS1 GAIN5	IRMS1 GAIN4	IRMS1 GAIN3	IRMS1 GAIN2	IRMS1 GAIN1	IRMS1 GAIN0

Address: 1BFH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IRMS1GAINH	0	0	0	0	IRMS1 GAIN11	IRMS1 GAIN10	IRMS1 GAIN9	IRMS1 GAINN8

(b) IRMS2GAIN

Address: 1C0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IRMS2GAINL	IRMS2 GAIN7	IRMS2 GAIN6	IRMS2 GAIN5	IRMS2 GAIN4	IRMS2 GAIN3	IRMS2 GAIN2	IRMS2 GAIN1	IRMS2 GAIN0

Address: 1C1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IRMS2GAINH	0	0	0	0	IRMS2 GAIN11	IRMS2 GAIN10	IRMS2 GAIN9	IRMS2 GAIN8

IRMSnGAIN11 to 0	Specify the RMS gain value of the current power (n = 1, 2)
0000H to 0FFFH	RMS gain value of apparent power

Caution Be sure to clear bits 4 to 7 of the IRMS1GAINH and IRMS2GAINH to 0.

(23) Active power offset specification registers 1 and 2 (ACT1OS, ACT2OS)

The ACT1OS and ACT2OS registers are used to set the offset value of the active power.

ACT1OS and ACT2OS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-24. Format of Active Power Offset Specification Registers 1 and 2 (ACT1OS, ACT2OS)

(a) ACT1OS

Address: 1C2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT1OSL	ACT1OS7	ACT1OS6	ACT1OS5	ACT1OS4	ACT1OS3	ACT1OS2	ACT1OS1	ACT1OS0

Address: 1C3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT1OSH	ACT1OS15	ACT1OS14	ACT1OS13	ACT1OS12	ACT1OS11	ACT1OS10	ACT1OS9	ACT1OS8

(b) ACT2OS

Address: 1C4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT2OSL	ACT2OS7	ACT2OS6	ACT2OS5	ACT2OS4	ACT2OS3	ACT2OS2	ACT2OS1	ACT2OS0

Address: 1C5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ACT2OSH	ACT2OS15	ACT2OS14	ACT2OS13	ACT2OS12	ACT2OS11	ACT2OS10	ACT2OS9	ACT2OS8

ACTnOS15 to 0	Specify the offset value of the active power (n = 1, 2)
0000H to FFFFH	Offset value of active power

(24) Reactive power offset specification registers 1 and 2 (REA1OS, REA2OS)

The REA1OS and REA1OS registers are used to set the offset value of the reactive power.

REA1OS and REA1OS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-25. Format of Reactive power offset specification registers 1 and 2 (REA1OS, REA2OS)

(a) REA1OS

Address: 1C6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA1OSL	REA1OS7	REA1OS6	REA1OS5	REA1OS4	REA1OS3	REA1OS2	REA1OS1	REA1OS0

Address: 1C7H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA1OSH	REA1OS15	REA1OS14	REA1OS13	REA1OS12	REA1OS11	REA1OS10	REA1OS9	REA1OS8

(b) REA2OS

Address: 1C8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA2OSL	REA2OS7	REA2OS6	REA2OS5	REA2OS4	REA2OS3	REA2OS2	REA2OS1	REA2OS0

Address: 1C9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
REA2OSH	REA2OS15	REA2OS14	REA2OS13	REA2OS12	REA2OS11	REA2OS10	REA2OS9	REA2OS8

REAnOS15 to 0	Specify the offset value of the reactive power (n = 1, 2)
0000H to FFFFH	Offset value of reactive power

(25) RMS offset specification registers for current channels 1 and 2 (I1RMSOS, I2RMSOS)

The I1RMSOS and I2RMSOS registers are used to set the offset value of current channels 1 and 2.

I1RMSOS and I2RMSOS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-26. Format of RMS Offset Specification Registers for Current Channels 1 and 2 (I1RMSOS, I2RMSOS)

(a) I1RMSOS

Address: 1CAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
I1RMSOSL	I1RMSOS7	I1RMSOS6	I1RMSOS5	I1RMSOS4	I1RMSOS3	I1RMSOS2	I1RMSOS1	I1RMSOS0

Address: 1CBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
I1RMSOSH	0	0	0	0	I1RMSOS11	I1RMSOS10	I1RMSOS9	I1RMSOS8

(b) I2RMSOS

Address: 1CEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
I2RMSOSL	I2RMSOS7	I2RMSOS6	I2RMSOS5	I2RMSOS4	I2RMSOS3	I2RMSOS2	I2RMSOS1	I2RMSOS0

Address: 1CFH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
I2RMSOSH	0	0	0	0	I2RMSOS11	I2RMSOS10	I2RMSOS9	I2RMSOS8

InRMSOS11 to 0	Specify the RMS offset value of the current channel n (n = 1, 2)
0000H to 0FFFH	RMS offset value of current channel n

Caution Be sure to clear bits 4 to 7 of the I1RMSOSH and I2RMSOSH to 0.

(26) RMS offset specification registers for voltage channels 1 and 2 (V1RMSOS, V2RMSOS)

The V1RMSOS and V2RMSOS registers are used to set the offset value of voltage channels 1 and 2.

V1RMSOS and V2RMSOS are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 0000H.

Figure 22-27. Format of RMS Offset Specification Registers for Voltage Channels 1 and 2 (V1RMSOS, V2RMSOS)

(a) V1RMSOS

Address: 1CCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
V1RMSOSL	V1RMSOS7	V1RMSOS6	V1RMSOS5	V1RMSOS4	V1RMSOS3	V1RMSOS2	V1RMSOS1	V1RMSOS0

Address: 1CDH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
V1RMSOSH	0	0	0	0	V1RMSOS11	V1RMSOS10	V1RMSOS9	V1RMSOS8

(b) V2RMSOS

Address: 1D0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
V2RMSOSL	V2RMSOS7	V2RMSOS6	V2RMSOS5	V2RMSOS4	V2RMSOS3	V2RMSOS2	V2RMSOS1	V2RMSOS0

Address: 1D1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
V2RMSOSH	0	0	0	0	V2RMSOS11	V2RMSOS10	V2RMSOS9	V2RMSOS8

VnRMSOS11 to 0	Specify the RMS offset value of voltage channel n (n = 1, 2)
0000H to 0FFFH	RMS offset value of voltage channel n

Caution Be sure to clear bits 4 to 7 of the V1RMSOSH and V2RMSOSH to 0.

(27) Sampling mode selection register (SAMPMODE)

The SAMPMODE register is used to select the sampling waveform.

SAMPMODE is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 22-28. Format of Sampling Mode Selection Register (SAMPMODE)

Address: 1D2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAMPMODE	0	SAMP2SEL2	SAMP2SEL1	SAMP2SEL0	0	SAMP1SEL2	SAMP1SEL1	SAMP1SEL0

SAMPnSEL2	SAMPnSEL1	SAMPnSEL0	Select the waveform n for sample mode (n = 1, 2)
0	0	0	I1 output from integrator
0	0	1	I2 output from integrator
0	1	0	Active power 1 (output of ACT1GAIN after multiplication)
0	1	1	Active power 2 (output of ACT2GAIN after multiplication)
1	0	0	Reactive power 1 (output of REA1GAIN after multiplication)
1	0	1	Reactive power 2 (output of REA2GAIN after multiplication)
1	1	0	Apparent power 1 (output of APP1GAIN after multiplication)
1	1	1	Apparent power 2 (output of APP2GAIN after multiplication)

Caution Be sure to clear bits 3 and 7 to 0.

(28) Sampling result registers 1 and 2 (SAMP1, SAMP2)

The calculation result by sampling is stored in these registers.

SAMP1 and SAMP2 are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 000000H.

Figure 22-29. Format of Sampling Result Registers 1 and 2 (SAMP1, SAMP2)

(a) SAMP1

Address: 1D3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP1L	SAMP17	SAMP16	SAMP15	SAMP14	SAMP13	SAMP12	SAMP11	SAMP10

Address: 1D4H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP1M	SAMP115	SAMP114	SAMP113	SAMP112	SAMP111	SAMP110	SAMP19	SAMP18

Address: 1D5H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP1H	SAMP123	SAMP122	SAMP121	SAMP120	SAMP119	SAMP118	SAMP117	SAMP116

(b) SAMP2

Address: 1D6H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP2L	SAMP27	SAMP26	SAMP25	SAMP24	SAMP23	SAMP22	SAMP21	SAMP20

Address: 1D7H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP2M	SAMP215	SAMP214	SAMP213	SAMP212	SAMP211	SAMP210	SAMP29	SAMP28

Address: 1D8H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
SAMP2H	SAMP223	SAMP222	SAMP221	SAMP220	SAMP219	SAMP218	SAMP217	SAMP216

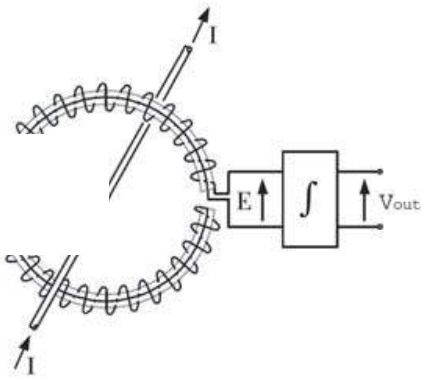
SAMPn23 to n0	Used to store the calculation result by sampling (n = 1, 2)
000000H to FFFFFFH	Calculation result by sampling

22.4 Power and Energy Calculation

22.4.1 Current integrator

If using a di/dt sensor, the current integrator is used to integrate the current. di/dt sensors, such as Rogowski coils, are systems that measure the primary circuit current and secondary circuit current (induced electromotive force) by using mutual inductance. When the primary circuit current flows, a magnetic field is generated around it, and this field is converted to current by the coil. This secondary circuit current shows how much the primary circuit current changes (di/dt).

Figure 22-30. Rogowski Coils



If using a Rogowski coil as a current sensor, the input current signal is a di/dt signal, and, because the current signal must be restored before the power can be calculated, an integrator is included.

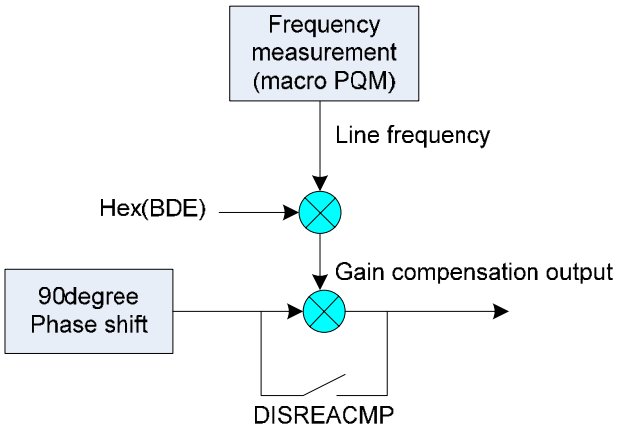
There are two integrators, integrator 1 for current channel 1 and integrator 2 for current channel 2. During a reset, the integrators for the current channels are turned off. To turn the integrators on, set the INTE1 and INTE2 bits of the PWCTL1 register to 1.

22.4.2 90° phase shifter

During reactive power or energy calculation, a 90° phase shift is needed between the current and voltage channel. The phase-shifting filter is a single-pole low-pass filter that performs a 90° phase shift over the relevant frequency (50 Hz or 60 Hz) and performs attenuation of 20 dB/dec.

A gain compensator is placed after the 90° phase shift. For a 90° phase shift, the frequency changes –20 dB/dec, so gain compensation is performed by multiplying the line frequency with the 90° phase shift output. However, gain compensation is only effective at the line frequency. The line frequency is measured by using the power quality measurement circuit. Gain compensation can be disabled using the DISREACMP bit of the NLCTL register.

Figure 22-31. 90° phase Shifter



22.4.3 Current and voltage RMS calculation

(1) RMS calculation method

The root mean square (rms) value of a signal V (t) is defined as:

$$Vrms = \sqrt{\frac{1}{T} * \int_0^T V^2(t)dt}$$

For sampled signals, RMS calculation involves squaring the signal, obtaining the average, and calculating the square root. This average is calculated by implementing a low-pass filter (LPF3). This low-pass filter has a –3 dB cutoff frequency of about 1.3 Hz when the sampling frequency is 4.34 kHz.

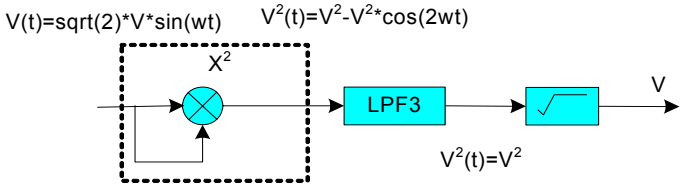
$$V(t) = \sqrt{2} \times V \sin(\omega t)$$

Here, V is the RMS voltage.

$$V^2(t) = V^2 - V^2 \cos(2\omega t)$$

When this signal goes through LPF3, the cos (2wt) term is attenuated and only the DC term $Vrms^2$ goes through.

Figure 22-32. Low-pass Filter (LPF3)



Four RMS values must be calculated: I1rms, I2rms, V1rms, and V2rms.

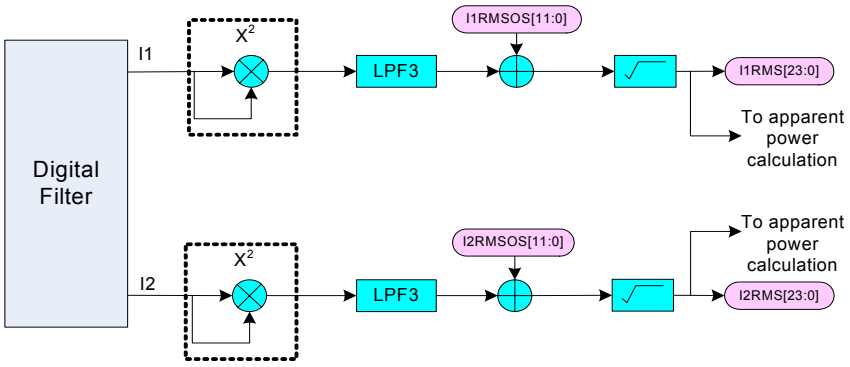
The RMS values can be read from the 24-bit registers I1RMS, I2RMS, V1RMS, and V2RMS, respectively.

(2) Current channel RMS calculation

This circuit calculates the RMS values for the two input current channels (I1 and I2). The methods for calculating the RMS values of the I1 channel and I2 channel are the same.

The RMS value calculated for each current channel is stored in the unsigned 24-bit register I1RMS or I2RMS.

Figure 22-33. Current Channel RMS Calculation



The measured current channel RMS value is stored in the relevant register every 4.34 kHz. Note that, by setting the ZXRMS bit of the NLCTL register to 1, the measurement result can be stored in the register in sync with the line frequency (in sync with the zero-crossing of the input voltage). If the ZXRMS bit is set, the operation is as follows.

- If CHMD = 0:
  The system enters the two-wire mode, and the I1RMS and I2RMS registers are updated in sync with the zero-crossing of the input voltage V1 (INTZX1).

- If CHMD = 1:
  The system enters the three-wire mode, the I1RMS register is updated in sync with the zero-crossing of the input voltage V1 (INTZX1), and the I2RMS register is updated in sync with the zero-crossing of the input voltage V2 (INTZX2).

For details about INTZX1 and INTZX2, see **CHAPTER 23 POWER QUALITY MEASUREMENT CIRCUIT**.

For full-scale input, the ΔΣ-type A/D converter outputs the 23-bit conversion result 2^{20} = 0d1048576 = 0x100000. The relationship between the maximum ΔΣ-type A/D converter conversion result, the PGA (preamplifier gain), and the input voltage range is as follows:

- If PGA = 1: maximum input = 0.375 V
- If PGA = 2: maximum input = 0.1875 V
- If PGA = 16: maximum input = 0.0234375 V

The equivalent RMS (24-bit) value of a full-scale AC signal is:

$$Irms\_FS = \frac{2^{20}}{\sqrt{2}} = 0d741455 = 0xB504F$$

The current RMS measurement is accurate to within 0.5% for signal input between full scale and full scale/500.

Note that the calculated register value must be converted to amps by using the CPU.

(3) Current channel RMS offset compensation

To remove current channel offset during current channel RMS value calculation, current channel RMS offset specification registers (I1RMSOS and I2RMSOS) are provided. These are signed 12-bit registers.

One LSB of the current channel RMS offset specification register is equivalent to 2,048 LSBs of the square of the current channel RMS register value.

The offset specified for the current channel RMS offset specification register is adjusted by multiplying the offset by 2,048 and adding the square of the pre-correction RMS value. For full-scale AC input, the maximum value from the current channel RMS calculation is 0d741455. For –60 dB input (1,000: equivalent to one dynamic range), the adjustment precision of the current channel RMS offset specification register is 0.186%/LSB. For –54 dB input (500: equivalent to one dynamic range), the adjustment precision of the current channel RMS offset specification register is 0.046%/LSB.

$$Irms = \sqrt{Irms0^2 + IRMSOS \times 2048}$$

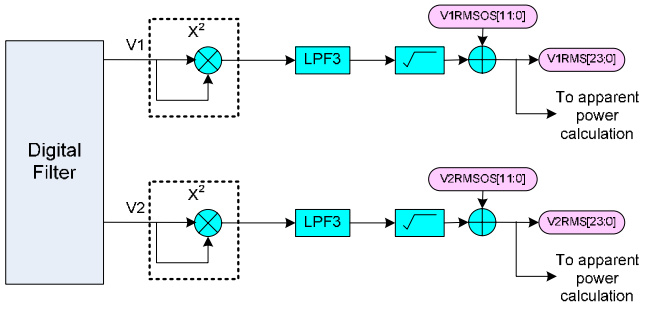
Here, Irms0 is the RMS measurement result without offset correction.

(4) Current channel RMS calculation

This circuit calculates the RMS values for the two input current channels (V1 and V2). The methods for calculating the RMS values of the V1 channel and V2 channel are the same.

The RMS value calculated for each current channel is stored in the unsigned 24-bit register V1RMS or V2RMS.

Figure 22-34. Current Channel RMS Calculation



The measured current channel RMS value is stored in the relevant register every 4.34 kHz. Note that, by setting the ZXRMS bit of the NLCTL register to 1, the measurement result can be stored in the register in sync with the line frequency (in sync with the zero-crossing of the input voltage). If the ZXRMS bit is set, the operation is as follows.

- If CHMD = 0:

  The system enters the two-wire mode, and the V1RMS and V2RMS registers are updated in sync with the zero-crossing of the input voltage V1 (INTZX1).

- If CHMD = 1:

  The system enters the three-wire mode, the V1RMS register is updated in sync with the zero-crossing of the input voltage V1 (INTZX1), and the V2RMS register is updated in sync with the zero-crossing of the input voltage V2 (INTZX2).

For details about INTZX1 and INTZX2, see **CHAPTER 23 POWER QUALITY MEASUREMENT CIRCUIT**.

The equivalent rms (24-bit) value of a full-scale AC signal is 0d741455 (0xB504F), which represents an analog input of 0.375 V x sin (ωt).
The current RMS measurement is accurate to within 0.5% for signal input between full scale and full scale/100.
Note that the calculated register value must be converted to bolts by using the CPU.

(5) Voltage channel RMS offset compensation

To remove voltage channel offset during voltage channel RMS value calculation, voltage channel RMS offset specification registers (V1RMSOS and V2RMSOS) are provided. These are signed 12-bit registers.
One LSB of the voltage channel RMS offset specification register is equivalent to 16 LSBs of the voltage channel RMS register value.
The offset specified for the voltage channel RMS offset specification register is adjusted by multiplying the offset by 16 and adding of the pre-correction RMS value. For full-scale AC input, the maximum value from the voltage channel
<R> RMS calculation is 0d741455. For –60 dB input (1,000: equivalent to one dynamic range), the adjustment precision of the voltage channel RMS offset specification register is 2.15 %/LSB. For –40 dB input (100: equivalent to one dynamic range), the adjustment precision of the voltage channel RMS offset specification register is 0.215%/LSB.

$$Vrms = Vrms0 + 16 \times VRMSOS$$

Here, Vrms0 is the RMS measurement result without offset correction.

22.4.4 Active power and energy calculation

(1) Active power calculation

(a) Active power calculation method

Active power is defined as the rate of energy flow from the power supply to the load and is the product of the voltage and current signal. The product is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is the watt. The following equations are used to calculate the instantaneous power signal in an AC system:

$$i(t) = \sqrt{2} \times I \sin(wt)$$

$$v(t) = \sqrt{2} \times V \sin(wt)$$

Here, V is the RMS voltage, I is the RMS current, and w is the frequency in radians.

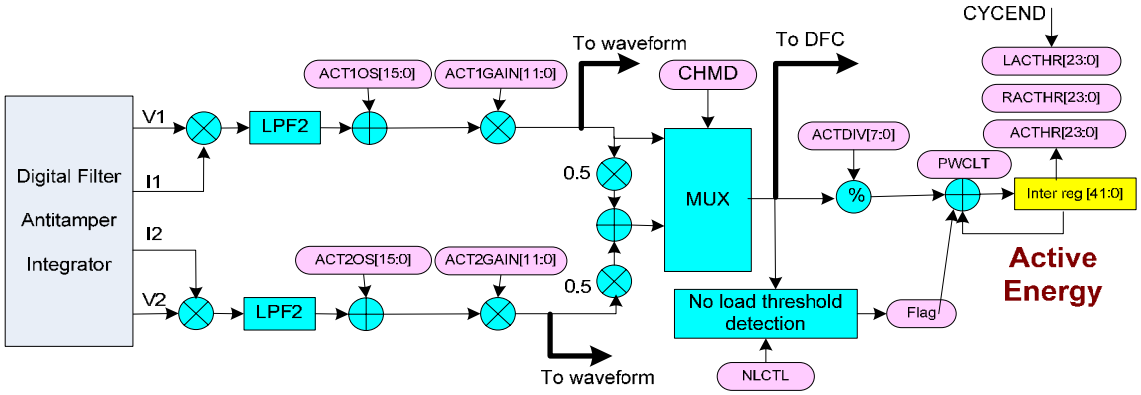
$$p(t) = v(t) \times i(t) = V \times I - V \times I \cos(2wt)$$

The average power over a specific number of line cycles (n) is calculated using the following equation:

$$P = \frac{1}{nT}\int_{0}^{nT} p(t)dt = V \times I$$

Here, T is the line cycle period, and P is the active or real power.
Note that the active power is equal to the DC component of the instantaneous power signal p (t), or V x I. This relationship is used to calculate the active power. The instantaneous power signal p (t) is generated by multiplying the current and voltage signals. The DC component of the instantaneous power signal is extracted by LPF2 (a low-pass filter).
This process is shown in the following figure:

Figure 22-35. Active Power Calculation



- If CHMD = 0 (the single-phase two-wire mode): active power = V1 × I1
- If CHMD = 1: (the single-phase three-wire mode): active power = 0.5 × (V1 × I1 + V2 × I2)

The low-pass filter LPF2 is used to extract the DC component of the instantaneous power, which has a frequency of f – 3 db = 5.4 Hz.

For LPF2, a certain amount of ripple occurs due to the instantaneous power signal, but this ripple is sinusoidal and has a frequency equal to twice the line frequency. For example, if the line frequency is 50 Hz, the ripple frequency is 100 Hz, and, if the line frequency is 60 Hz, the ripple frequency is 120 Hz. Because the ripple is sinusoidal, it is removed when the active power signal is integrated to calculate the energy. (For details, see **22.4.4 (2) Active energy calculation**.)
The active power signal can be read from the waveform register by setting up the SAMPMODE register and clearing the WFSMMK bit in the extended SFR interrupt mask flag register 22 (MK22). For the recommended flow, see **22.4.9 (5) Waveform-related interrupt (INTWFSM)**.

(b) Active power gain calibration

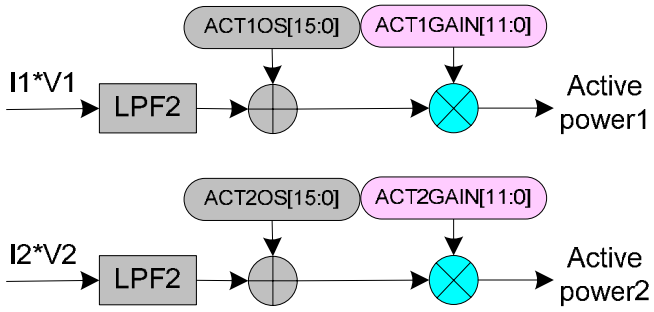
The active power is calculated by filtering the multiplier output by using a low-pass filter (LPF2). No gain calibration is performed on the current channel or voltage channel. Gain calibration is performed on active power by using the active power gain specification registers (ACT1GAIN and ACT2GAIN). The gain is adjusted by writing to the signed 12-bit registers ACT1GAIN and ACT2GAIN.

There are two active power channels in the three-wire mode:

- power1 = I1 x V1
- power2 = I2 x V2

Therefore, there are two registers called ACT1GAIN and ACT2GAIN for power1 and power2, respectively.

Figure 22-36. Active Power Gain Calibration



The following equations show how the gain is related to the ACT1GAIN and ACT2GAIN register settings:

$$OutputACT1GAIN = \{ActivePower1 \times [1 + \frac{ACT1GAIN}{2^{12}}]\}$$

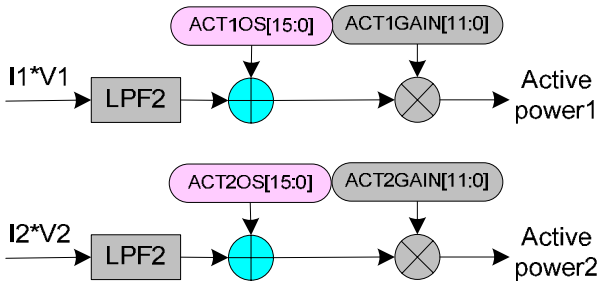
$$OutputACT2GAIN = \{ActivePower2 \times [1 + \frac{ACT2GAIN}{2^{12}}]\}$$

For example, if 0x7FF is written to the active power gain specification registers (ACT1GAIN and ACT2GAIN), the power output increases by 50% (0x7FF = 2047d, $2047/2^{12} = 0.5$). Similarly, if 0x800 = –2048d (signed, two's complement), the power output decreases by 50%. Each LSB increases or decreases the power output by 0.0244% ($1/2^{12} = 0.0244\%$). The output range is minimized when the ACT1GAIN or ACT2GAIN register setting is equal to 0x800, and the output range is maximized by writing 0x7ff to the ACT1GAIN or ACT2GAIN register. This can be used to calibrate the active power (or energy) calculation.

(c) Active power offset calibration

The active power offset can be calibrated using the active power offset specification registers (ACT1OS and ACT2OS). These signed 16-bit registers can be used to remove offset during active power calculation. Using offset calibration keeps the active power register value at 0 when no power is being consumed.

Figure 22-37. Active Power Offset Calibration



128 LSBs (ACT1OS = 0x080 or ACT2OS = 0x080) written to the active power offset specification register are equivalent to one LSB of the LPF2 output. If the input of the voltage and current channels is at full scale , the value output by LPF2 is 0x200000 = 0d2097152. However, if the current channel input is at –60 dB (1/1000th of the full-scale current channel input), the value output by LPF2 is 0d2097.152. This means that, when a –60 dB signal is input, one LSB in the LPF2 output has a maximum measurement error of 0.0477%. One LSB of the active power offset specification register is equivalent to 1/128 LSB of LPF2 output. Therefore, when performing offset calibration, the measurement error is 0.000372%/LSB (0.0477%/128) at –60 dB.

(d) Active power sign detection

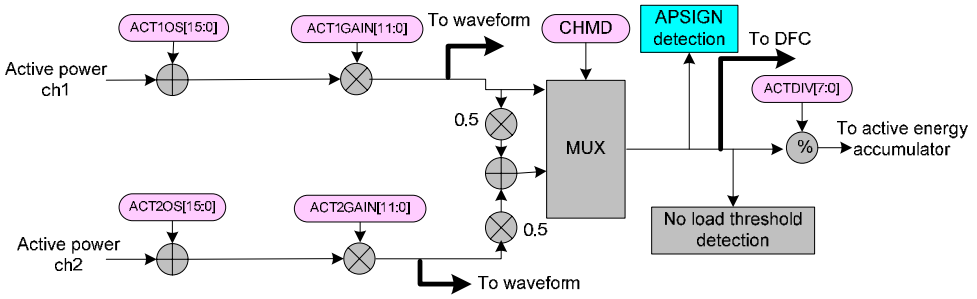
Active power sign detection detects a change of the active power sign.
The following three bits are used for this detection.

- The ACTSIGN bit in the PWCTL2 register:
  This bit selects the event that triggers an active power sign interrupt.
  If ACTSIGN = 0: An INTACTSIGN interrupt occurs when the active power changes from positive to negative.
  If ACTSIGN = 1: An INTACTSIGN interrupt occurs when the active power changes from negative to positive.

- The ACTSIGNIF bit in the extended SFR interrupt request flag register 20 (IF20)
  If this bit is 1, the trigger condition specified by ACTSIGN has been satisfied. Once the ACTSIGNIF interrupt status is set to 1, it remains 1 until this status bit is cleared. The ACTSIGNIF status is cleared when a zero is written to this bit.

- The ACTSIGNMK bit in the extended SFR interrupt mask flag register 20 (MK20)
  When this bit is cleared, the ACTSIGNIF flag is set and an interrupt occurs.

Figure 22-38. Active Power Offset Calibration



(e) Active-power no-load detection

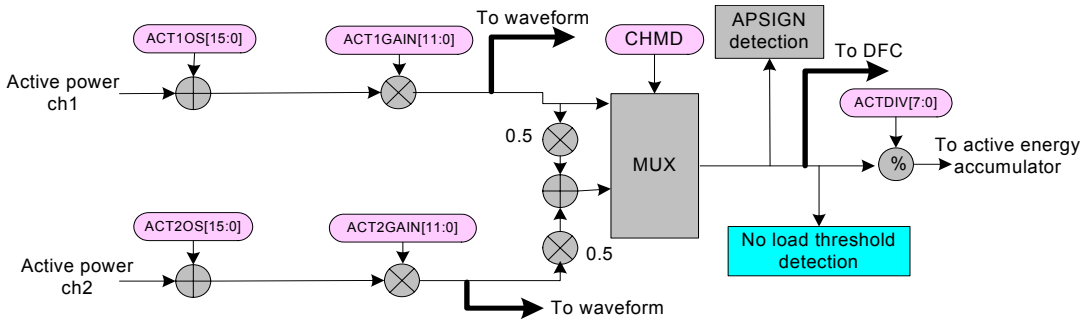
A no-load detection function is included for the active energy that eliminates any creep effects on the meter. When this function is used, active energy is not accumulated if the active power is below the no-load threshold. The following three bits are used for active-power no-load detection.

- The ACTNOLOAD1 and ACTNOLOAD0 bits in the NLCTL register:
  These two bits specify the active-power no-load threshold.
  00: Disables active-power no-load detection.
  01: Enables active-power no-load detection with a threshold of 0.015% of the full scale.
  10: Enables active-power no-load detection with a threshold of 0.0075% of the full scale.
  11: Enables active-power no-load detection with a threshold of 0.0037% of the full scale.

- The ACTNOLDIF flag in the extended SFR interrupt request flag register 21 (IF21):
  The ACTNOLDIF flag is set when the active power falls below the no-load threshold specified by the ACTNOLOAD1 and ACTNOLOAD0 bits in the NLCTL register.

- The ACTNOLDMK bit in the extended SFR interrupt mask flag register 21 (MK21):
  If the ACTNOLDMK bit is cleared in the extended SFR interrupt mask flag register 21 (MK21), an interrupt occurs. This interrupt stays active until the ACTNOLDIF status bit is cleared.

Figure 22-39. Active-power no-load detection



(2) Active energy calculation

(a) Active energy calculation method

As stated in the active power calculation section, power is defined as the rate of energy flow. The energy can be calculated using the following equation:

$$E = \int P(t)dt$$

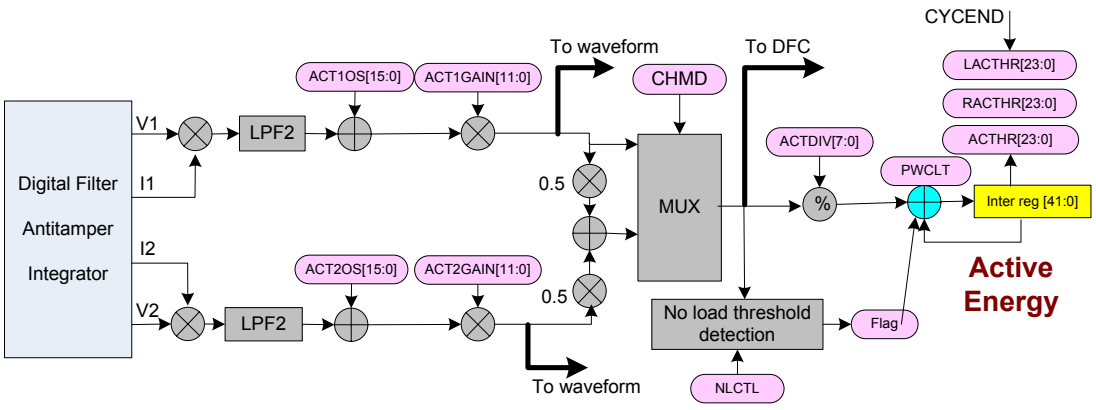
The active power signal is integrated by accumulating the active power signal in an internal 42-bit energy register. The higher 24 bits of this internal register can be read by the ACTHR register. This accumulation processing is equivalent to integration over a continuous period of time.

$$E = \int p(t)dt = \lim_{t->0}\{\sum_{n=1}^{\infty} p(nt) \times T\}$$

In the above equation, n is the discrete time sample number and T is the sample period.

The discrete time sample period (T) for the accumulation register is 230.4 μs (18 x 128/MCLK_10M). In addition to calculating the energy, this integration removes sinusoidal components from the active power signal.

Figure 22-40. Active Energy Calculation



The active energy accumulation method can be selected by specifying values for the POAM and ABSAM bits in the PWCTL2 register. For details about the accumulation method, see **22.4.4 (2) (c) Active energy accumulation modes**.

Table 22-2. Setting of Active Power Accumulation Mode

POAM	ABSAM	Active Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Positive value accumulation mode
1	1	Absolute value accumulation mode

The active power is scaled by the value of the ACTDIV register and is then accumulated in an internal energy accumulator. ACTDIV is an 8-bit unsigned register, and the scaling processing is as follows:

Amount of energy after scaling = power before scaling/ACTDIV

Note that clearing ACTDIV to 0 is prohibited. If 0 is specified, processing is performed as though 1 is specified.

After scaling, the active power is accumulated in an internal 42-bit active energy accumulator. The higher 24 bits of the internal accumulator can be read by a register. There are three methods for reading the accumulator value, and a reading register is prepared for each.

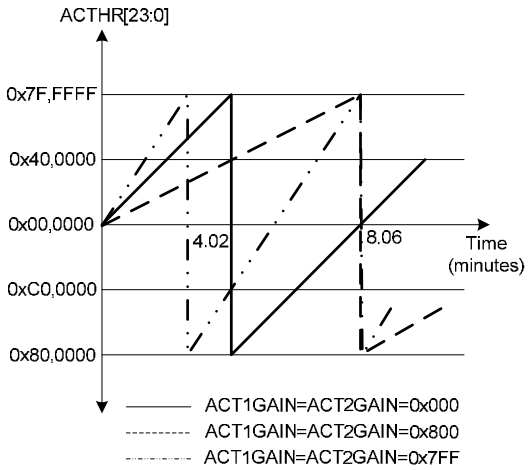
- If reading the value by using the ACTHR register:
  The value of the higher 24 bits of the accumulator at the time of reading is read.

- If reading the value by using the RACTHER register:
  The value of the higher 24 bits of the accumulator at the time of reading is read. After reading, the higher 24 bits of the accumulator are cleared.

- If reading the value by using the LACTHR register:
  The value is read in sync with the line frequency. For details, see **22.4.4 (2) (e) Line cycle active energy accumulation mode**.

The figure below shows this energy accumulation for full-scale analog-input signals (sinusoidal). The three displayed curves show the minimum period of time it takes the energy register to overflow or underflow when the active power gain specification register contents (ACT1GAIN and ACT2GAIN) are 0x7FF, 0x000, and 0x800. As shown, the fastest integration time occurs when the active power gain specification register is set to maximum full scale, which is 0x7FF.

Figure 22-41. Active Energy Accumulation for Full-scale signals



Note that, if an overflow occurs while the power or energy flow is positive, the energy register contents invert to the maximum negative value (0x800000) and then continuously increase in value. Conversely, if the power is negative, after an underflow, the energy register contents switch to the maximum positive value (0x7FFFFF) and then continuously decrease in value.

If the active energy register is half full (positive or negative) or an overflow or underflow occurs, the interrupt flag bit ACTEHFIF or ACTEOFIF is set. By clearing the ACTEHFMK and ACTEOFMK bits in the extended SFR interrupt mask flag registers 21 and 22 (MK21 and MK22), it is possible to specify that interrupts be generated when the active energy register is half full or when an overflow occurs.

(b) Integration time under a steady load

As mentioned in the active energy calculation section, the discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz). If the analog input is a full-scale sinusoidal signal and the ACT1GAIN and ACT2GAIN registers are set to 0x000, the average word value from each GAIN is 2^{21} (or 0x1F, FFFF). The maximum positive value that can be stored in the internal 42-bit register before it overflows is 2^{41} (or 0x1FF, FFFF, FFFF). The integration time under these conditions when ACTDIV = 0 is calculated using the following equation:

$$Time = \frac{0x1FF,FFFF,FFFF}{0x1F,FFFF} \times 230.4us = 241.59\,\mathrm{sec} = 4.02\,\mathrm{min}$$

If ACTDIV is set to a value other than 0, the integration time varies as follows:

$$Time = Time_{ACTDIV=0} \times ACTDIV$$

(c) Active energy accumulation modes

There are three accumulation modes for active energy calculation. The mode is determined using the POAM and ABSAM bits in the PWCTL2 register.

Table 22-3. Setting of Active Power Accumulation Mode

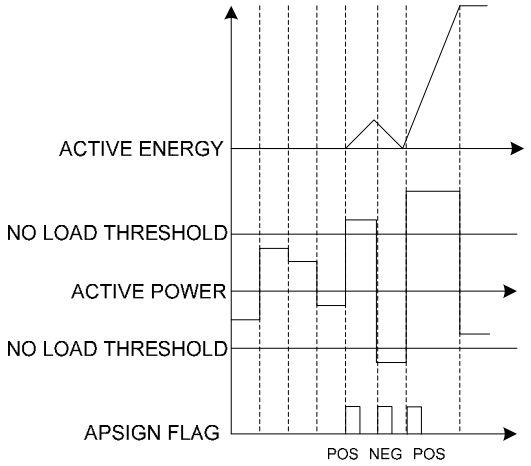
POAM	ABSAM	Active Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Positive value accumulation mode
1	1	Absolute value accumulation mode

<1> Signed accumulation mode

In the signed accumulation mode, the signed active power is accumulated. If the active power is positive, it is added to the active energy accumulator. If the active power is negative, it is subtracted from the accumulator. This mode returns to the default mode after a reset.

If the active power is below the no-load threshold, it is not accumulated.

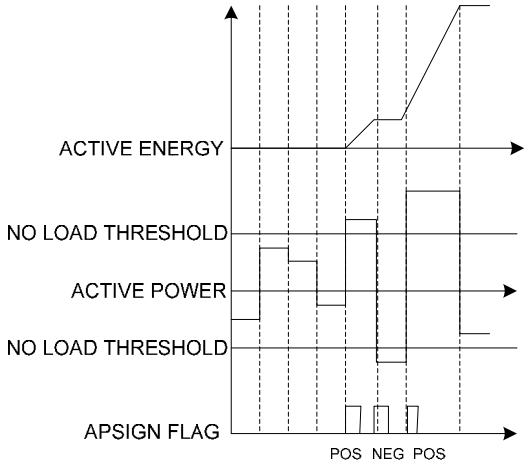
Figure 22-42. Signed Accumulation Mode (active power)



<2> Positive value accumulation mode:

This mode can be specified by setting the POAM bit in the PWCTL2 register to 1 and clearing the ABSAM bit in the same register to 0. In this mode, only positive power values are accumulated and negative power values are ignored. Negative power values and values below the no-load threshold are not accumulated.

Figure 22-43. Positive Value Accumulation Mode (active power)

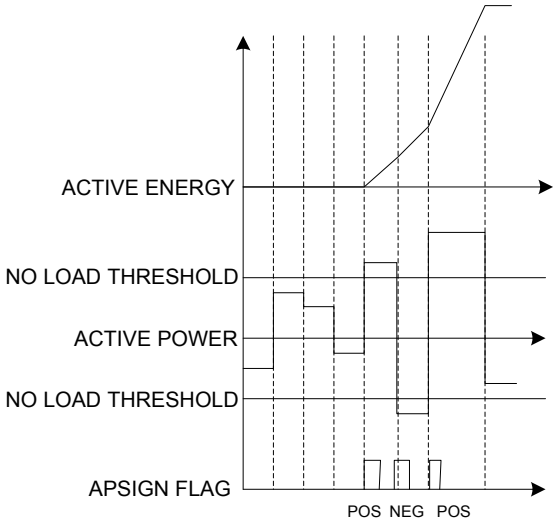


This mode also applies to CF pulse output. The default setting for this mode is off. Detection of transitions in the direction of power flow and detection of the no-load threshold are enabled in this mode.

<3> Absolute value accumulation mode:

This mode can be specified by setting the ABSAM bit in the PWCTL2 register to 1. In this mode, energy accumulation is performed using the absolute active power, ignoring active power below the no-load threshold.

Figure 22-44. Absolute Value Accumulation Mode (active power)

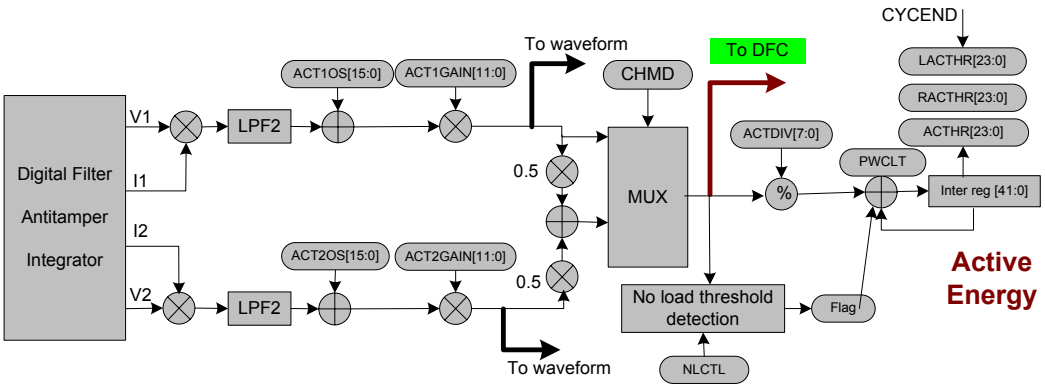


This mode also applies to CF pulse output. The default setting for this mode is off. Detection of transitions in the direction of power flow and detection of the no-load threshold are enabled in this mode.

(d) Active energy pulse output

A pulse whose frequency is proportional to the active energy is output. Outputting a pulse of this frequency uses the active power signal output by the ACT1GAIN and ACT2GAIN registers, and operation is performed in accordance with the setting of the active energy accumulation mode in the PWCTL2 register. For details about pulse output, see **CHAPTER 24 DIGITAL FREQUENCY CONVERSION CIRCUIT**.

Figure 22-45. Active Energy Pulse Output



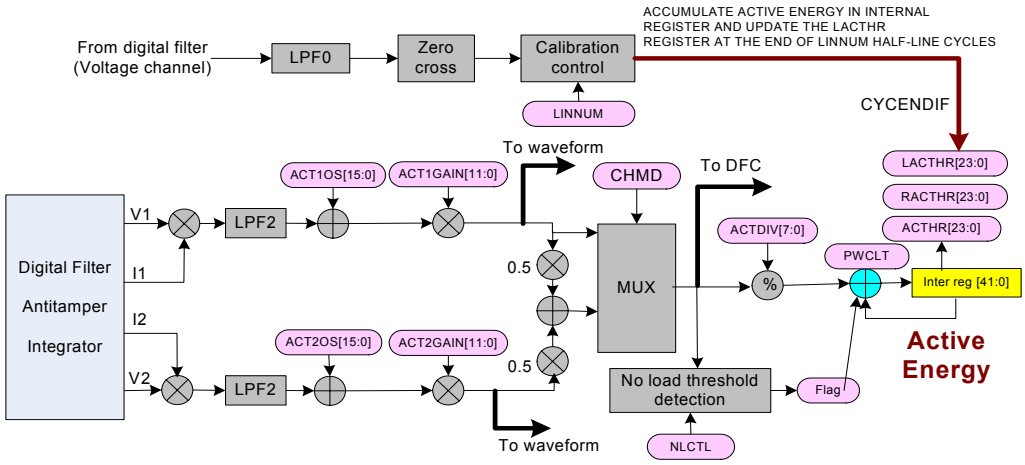
(e) Line cycle active energy accumulation mode

In the line cycle active energy accumulation mode, the error due to the sinusoidal component of the active energy is eliminated, so the active power is accumulated in units equal to twice the line frequency. This mode is implemented by synchronizing the energy accumulation with the voltage-channel zero crossing.

Active power has a ripple of 100 Hz or 120 Hz when the line frequency is 50 Hz or 60 Hz, respectively. This ripple causes calibration error when a non-integer period is accumulated during energy accumulation. This ripple has very little effect on the CF frequency because this frequency is normally very low. (For example, at 1 Hz, the accumulation time is 1 second.) However, during calibration, a short calibration time is required, and the error caused by ripple can have a large effect. If the accumulation time is equal to the integer period of the line frequency, the error caused by ripple can be eliminated. Therefore, the energy is calculated more accurately in the line cycle active energy accumulation mode.

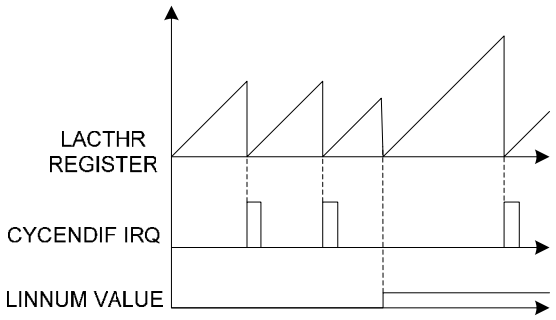
By using this mode, energy calibration can be greatly simplified, and the time necessary for calibration can be significantly reduced. In the line cycle active energy accumulation mode, the active power signal is accumulated in the LACTHR register for the specified line cycle period. The number of half-line cycles is specified in the LINNUM register, and the active energy can be accumulated for up to 65,535 half-line cycles. The active power is integrated over the specified number of line cycles, and the CYCENDIF flag in the extended SFR interrupt request flag register 22 (IF22) is set at the end of an active energy accumulation line cycle. If the CYCENDMK mask bit in the extended SFR interrupt mask flag register 22 (MK22) is cleared to 0, an interrupt occurs. This interrupt stays active until the CYCENDIF status bit is cleared. Another calibration cycle starts as soon as the CYCENDIF flag is set. If the LACTHR register is not read before a new CYCENDIF flag is set, the LACTHR register is overwritten by a new value.

Figure 22-46. Line Cycle Active Energy Accumulation Mode



When a new half-line cycle is written to the LINNUM register, the LACTHR register is reset, and a new accumulation starts at the next zero crossing. The number of half-line cycles is then counted until the LINNUM register value is reached. In this way, valid measurement is performed at the first CYCEND interrupt after writing to the LINNUM register. Line active energy accumulation uses the same signal path as active energy accumulation. The LSB size of these two registers is equivalent.

Figure 22-47. Accumulation Timing of Active Power



The CYCDIS bit in the PWCTL1 register can disable CYCEND detection. If the CYCDIS bit is set to 1, the CYCEND interrupt will not occur when the number of half-line cycles reaches the value specified for the LINNUM register. Also, if the CYCDIS bit is set to 1, the LACTHR register and inner accumulation register will not reset to 0 when a new half-line cycle is written to the LINNUM register.

Note that, in this mode, the 16-bit LINNUM register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration of 65,535 half-line cycles. At a 60 Hz line frequency, this results in a total duration of 65,535/120 Hz = 546 sec.

22.4.5 Reactive power and energy calculation

(1) Reactive power calculation

(a) Reactive power calculation method

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase-shifted by 90°. The resulting waveform is called the instantaneous reactive power signal. The instantaneous reactive power signal when the phase of the current channel is shifted by 90° is calculated using the following equations:

$$v(t) = \sqrt{2}V\sin(\omega t + \theta) \qquad i(t) = \sqrt{2}I\sin(\omega t) \qquad i'(t) = \sqrt{2}I\sin(\omega t + \frac{\pi}{2})$$

Here, θ is the phase difference between the voltage and current channel, V is the RMS voltage, and I is the RMS current.

$$q(t) = V(t) \times i'(t) = VI\sin(\theta) + VI\sin(2\omega t + \theta)$$

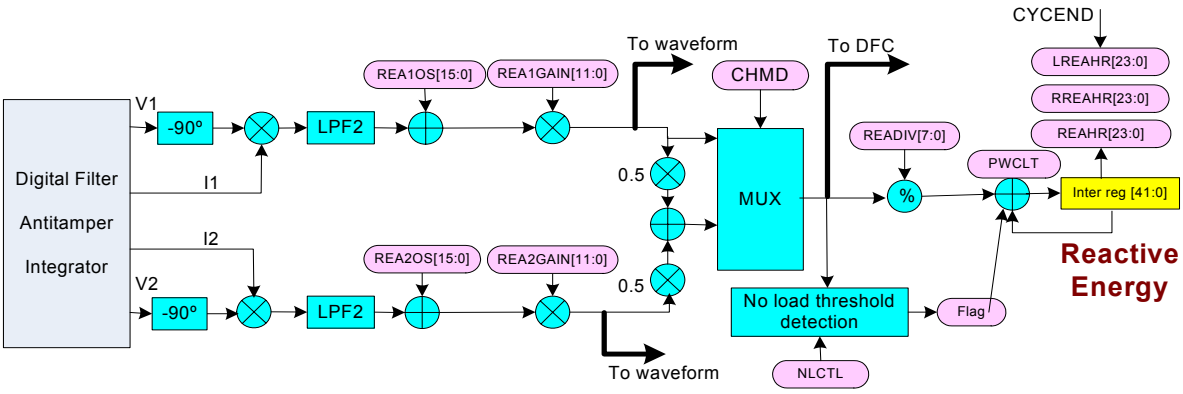
The average reactive power for the number of line cycles (n) is calculated using the following equation:

$$Q = \frac{1}{nT}\int_0^{nT} q(t)dt = VI\sin\theta$$

Here, T is the line cycle period and Q is the reactive power.

Figure 22-48 shows the reactive power calculation process.

Figure 22-48. Reactive Power Calculation



- If CHMD = 0 (the single-phase two-wire mode): reactive power = V1_ phase-shifted × I1
- If CHMD = 1 (the single-phase three-wire mode): reactive power = 0.5 × (V1_ phase-shifted × I1 + V2_ phase-shifted × I2)

Phase shifting (a –90° phase shift) is realized using a low-pass filter (LPF) for which the high frequency component is attenuated. However, because the reactive power is calculated in the line frequency band, there are almost no harmonic effects. Gain compensation for the attenuated portion of the signal line is performed in the line frequency band. This gain compensation can be disabled using the DISREACMP bit of the NLCTL register. For details, see **22.4.2 90° phase shifter**.

The frequency response of the LPF on the reactive signal path is the same as the one used for LPF2 during average active power calculation.

For LPF2, a certain amount of ripple occurs due to the instantaneous power signal, but this ripple is sinusoidal and has a frequency equal to twice the line frequency. For example, if the line frequency is 50 Hz, the ripple frequency is 100 Hz, and, if the line frequency is 60 Hz, the ripple frequency is 120 Hz. Because the ripple is sinusoidal, it is removed when the reactive power signal is integrated to calculate the energy.

The reactive power signal can be read from the waveform register by setting up the SAMPMODE register and clearing the WFSMMK bit in the extended SFR interrupt mask flag register 22 (MK22). For the recommended flow, see **22.4.9 (5) Waveform-related interrupt (INTWFSM**).

(b) Reactive power gain calibration

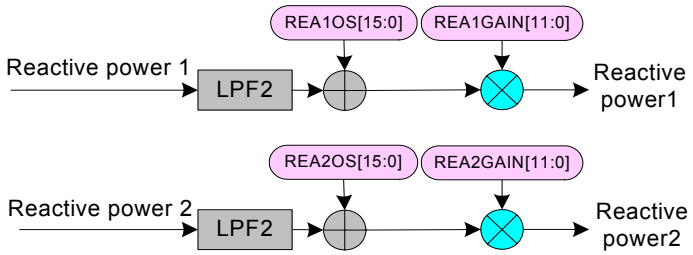
The reactive power is calculated by filtering the multiplier output by using a low-pass filter (LPF2). No gain calibration is performed on the current channel or voltage channel. Gain calibration is performed on reactive power by using the reactive power gain specification registers (REA1GAIN and REA2GAIN). The gain is adjusted by writing to the signed 12-bit registers REA1GAIN and REA2GAIN.

There are two reactive power channels in the three-wire mode:

- power1 = I1 x V1 x sinθ1
- power2 = I2 x V2 x sinθ2

Therefore, there are two registers called REA1GAIN and REA2GAIN for power1 and power2, respectively.

Figure 22-49. Reactive Power Gain Calibration



The following equations show how the gain is related to the REA1GAIN and REA2GAIN register settings:

$$OutputREA1GAIN = \{\mathrm{Re}\, activePower1 \times [1 + \frac{REA1GAIN}{2^{12}}]\}$$

$$OutputREA2GAIN = \{\mathrm{Re}\, activePower2 \times [1 + \frac{REA2GAIN}{2^{12}}]\}$$

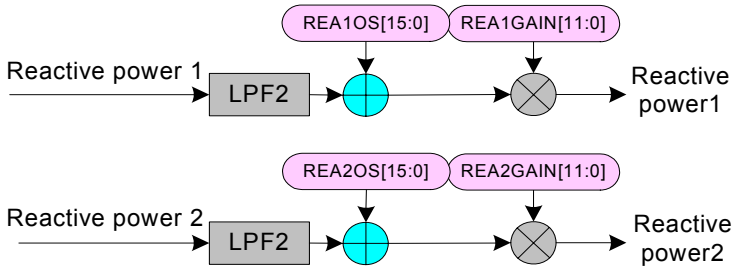
The resolution of the REA1GAIN and REA2GAIN registers is the same as the ACT1GAIN and ACT2GAIN registers (see **22.4.4 (1) (b) Active power gain calibration**).

Each LSB increases or decreases the power output by 0.0244% ($1/2^{12}$ = 0.0244%).The REA1GAIN and REA2GAIN registers can be used to adjust the reactive power (or energy) calculation.

(c) Reactive power offset calibration

The reactive power offset can be calibrated using the reactive power offset specification registers (REA1OS and REA2OS). These signed 16-bit registers can be used to remove offset during reactive power calculation. Using offset calibration keeps the reactive power register value at 0 when no power is being consumed.

Figure 22-50. Reactive Power Offset Calibration

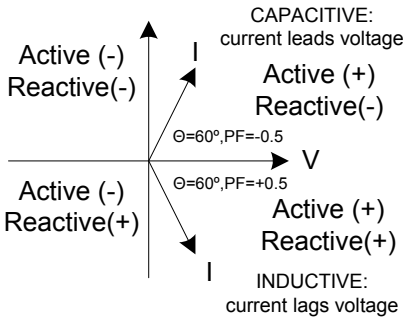


128 LSBs (REA1OS = 0x080 or REA2OS = 0x080) written to the reactive power offset specification register are equivalent to one LSB of the LPF2 output. If the input of the voltage and current channels is at full scale and the phase between the voltage and current is exactly 90 degrees, the value output by LPF2 is 0x200000 = 0d2097152. However, if the current channel input is at –60 dB (1/1000th of the full-scale current channel input), the value output by LPF2 is 0d2097.152. This means that, when a –60 dB signal is input, one LSB in the LPF2 output has a maximum measurement error of 0.0477%. One LSB of the reactive power offset specification register is equivalent to 1/128 LSB of LPF2 output. Therefore, when performing offset calibration, the measurement error is 0.000372%/LSB (0.0477%/128) at –60 dB.

(d) Reactive power sign calculation and detection

Figure 22-51 shows the signs for active power and reactive power.

Figure 22-51. Signs for Active Power and Reactive Power



Note that the average reactive power is calculated using signs. The phase shift filter performs a –90° phase shift. The following table shows the relationship of the phase difference between the voltage and the current and the sign of the reactive power calculation result.

Table 22-4. Relationship Between Phase Difference and Sign

Angle	Integrator	Sign
0° to +90°	Off	Positive
–90° to 0°	Off	Negative
0° to +90°	On	Positive
–90° to 0°	On	Negative

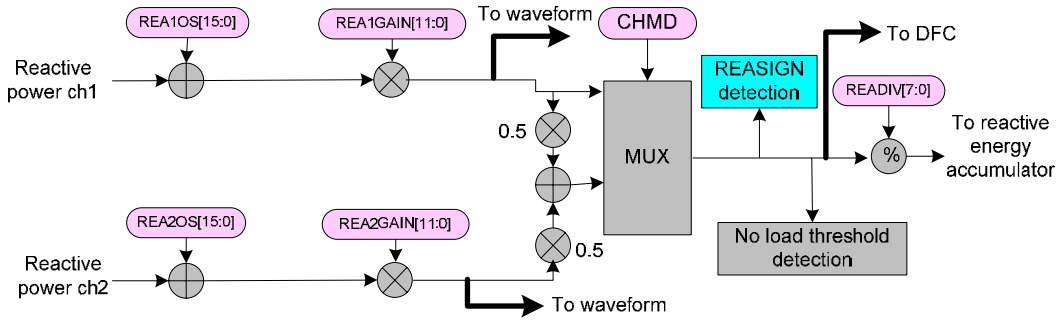
Reactive power sign detection detects a change of the active power sign.
The following three bits are used for this detection.

- The REASIGN bit in the PWCTL2 register:
  This bit selects the event that triggers an reactive power sign interrupt.
  If REASIGN = 0: An INTREASIGN interrupt occurs when the reactive power changes from positive to negative.
  If REASIGN = 1: An INTREASIGN interrupt occurs when the reactive power changes from negative to positive.

- The REASIGNIF bit in the extended SFR interrupt request flag register 20 (IF20)
  If this bit is 1, the trigger condition specified by REASIGN has been satisfied. Once the REASIGNIF interrupt status is set to 1, it remains 1 until this status bit is cleared. The REASIGNIF status is cleared when a zero is written to this bit.

- The REASIGNMK bit in the extended SFR interrupt mask flag register 20 (MK20)
  When this bit is cleared, the REASIGNIF flag is set and an interrupt occurs.

Figure 22-52. Reactive Power Offset Calibration



(e) Reactive-power no-load detection

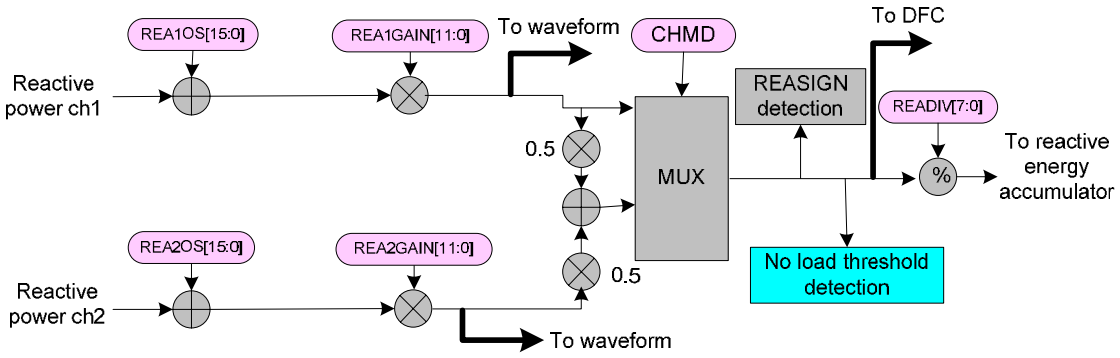
A no-load detection function is provided for the reactive power measurement. When this function is used, reactive energy is not accumulated if the reactive power is below the no-load threshold. The following three bits are used for reactive-power no-load detection.

- The REANOLOAD1 and REANOLOAD0 bits in the NLCTL register:
  These two bits specify the reactive-power no-load threshold.
  00: Disables reactive-power no-load detection.
  01: Enables reactive-power no-load detection with a threshold of 0.015% of the full scale.
  10: Enables reactive-power no-load detection with a threshold of 0.0075% of the full scale.
  11: Enables reactive-power no-load detection with a threshold of 0.0037% of the full scale.

- The REANOLDIF flag in the extended SFR interrupt request flag register 21 (IF21):
  The REANOLDIF flag is set when the reactive power falls below the no-load threshold specified by the REANOLOAD1 and REANOLOAD0 bits in the NLCTL register.

- The REANOLDMK bit in the extended SFR interrupt mask flag register 20 (MK20):
  If the REANOLDMK bit is cleared in the extended SFR interrupt mask flag register 20 (MK20), an interrupt occurs. This interrupt stays active until the REANOLDIF status bit is cleared.

Figure 22-53. Reactive-power no-load detection

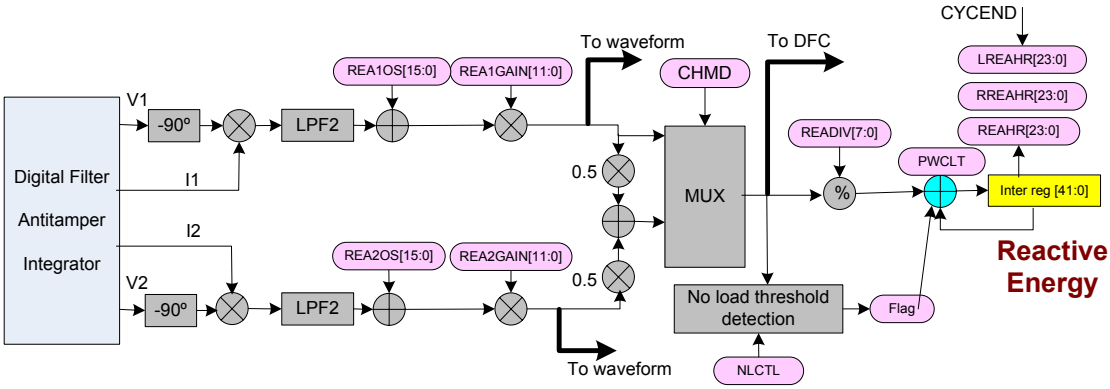


(2) Reactive energy calculation

(a) Reactive energy calculation method

As stated in the active power calculation section, reactive energy calculation is integrated by accumulating the reactive power signal in an internal 42-bit energy register. The higher 24 bits of this internal register can be read by the REAHR register. The discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz). In addition to calculating the energy, this integration removes sinusoidal components from the reactive power signal.

Figure 22-54. Reactive Energy Calculation



The reactive energy accumulation method can be selected by specifying values for the SAVARM and ABSVARM bits in the PWCTL2 register. For details about the accumulation method, see **22.4.5 (2) (c) Reactive energy accumulation modes**.

Table 22-5. Setting of Reactive Power Accumulation Mode

SAVARM	ABSVARM	Reactive Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Positive value accumulation mode
1	1	Absolute value accumulation mode

The reactive power is scaled by the value of the READIV register and is then accumulated in an internal energy accumulator. READIV is an 8-bit unsigned register, and the scaling processing is as follows:

Amount of energy after scaling = power before scaling/READIV

Note that clearing READIV to 0 is prohibited. If 0 is specified, processing is performed as though 1 is specified.

After scaling, the active power is accumulated in an internal 42-bit reactive energy accumulator. The higher 24 bits of the internal accumulator can be read by a register. There are three methods for reading the accumulator value, and a reading register is prepared for each.

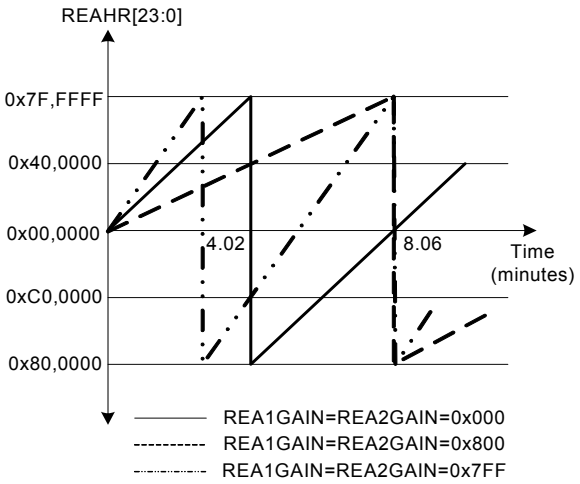
- If reading the value by using the REAHR register:
  The value of the higher 24 bits of the accumulator at the time of reading is read.

- If reading the value by using the REATHER register:
  The value of the higher 24 bits of the accumulator at the time of reading is read. After reading, the higher 24 bits of the accumulator are cleared.

- If reading the value by using the LREAHR register:
  The value is read in sync with the line frequency. For details, see **22.4.5 (2) (e) Line cycle reactive energy accumulation mode**.

The figure below shows this energy accumulation for full-scale analog-input signals (sinusoidal). The three displayed curves show the minimum period of time it takes the energy register to overflow or underflow when the reactive power gain specification register contents (REA1GAIN and REA2GAIN) are 0x7FF, 0x000, and 0x800. As shown, the fastest integration time occurs when the reactive power gain specification register is set to maximum full scale, which is 0x7FF.

Figure 22-55. Reactive Energy Accumulation for Full-scale signals



Note that, if an overflow occurs while the power or energy flow is positive, the energy register contents invert to the maximum negative value (0x800000) and then continuously increase in value. Conversely, if the power is negative, after an underflow, the energy register contents switch to the maximum positive value (0x7FFFFF) and then continuously decrease in value.

If the reactive energy register is half full (positive or negative) or an overflow or underflow occurs, the interrupt flag bit REAHFIF or REAOFIF is set. By clearing the REAHFMK and REAOFMK bits in the extended SFR interrupt mask flag register 21 (MK21), it is possible to specify that interrupts be generated when the reactive energy register is half full or when an overflow occurs.

(b) Integration time under a steady load

As mentioned in the reactive energy calculation section, the discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz). If the analog input is a full-scale sinusoidal signal and the REA1GAIN and REA2GAIN registers are set to 0x000, the average word value from each GAIN is 2^{21} (or 0x1F, FFFF). The maximum positive value that can be stored in the internal 42-bit register before it overflows is 2^{41} (or 0x1FF, FFFF, FFFF). The integration time under these conditions when READIV = 0 is calculated using the following equation:

$$Time = \frac{0x1FF,FFFF,FFFF}{0x1F,FFFF} \times 230.4us = 241.59\,\text{sec} = 4.02\,\text{min}$$

If READIV is set to a value other than 0, the integration time varies as follows:

$$Time = Time_{READIV=0} \times READIV$$

(c) Reactive energy accumulation modes

There are three accumulation modes for reactive energy calculation. The mode is determined using the SAVARM and ABSVARM bits in the PWCTL2 register.

Table 22-6. Setting of Reactive Power Accumulation Mode

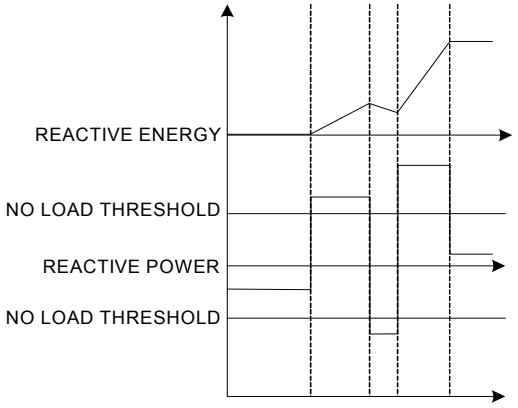
SAVARM	ABSVARM	Reactive Power Accumulation Mode
0	0	Signed value accumulation mode
0	1	Absolute value accumulation mode
1	0	Anti-tamper accumulation mode
1	1	Absolute value accumulation mode

<1> Signed accumulation mode

In the signed accumulation mode, the signed reactive power is accumulated. If the reactive power is positive, it is added to the reactive energy accumulator. If the reactive power is negative, it is subtracted from the accumulator. This mode returns to the default mode after a reset.

If the reactive power is below the no-load threshold, it is not accumulated.

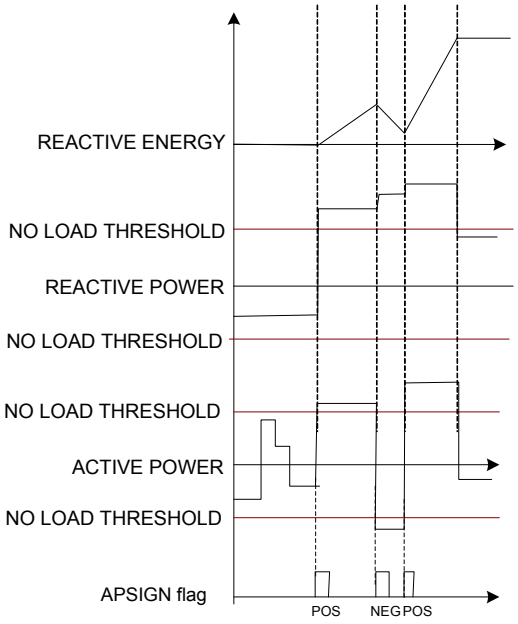
Figure 22-56. Signed Accumulation Mode (reactive power)



<2> Anti-tamper accumulation mode:

The anti-tamper accumulation mode can be specified by setting the SAVARM bit in the PWCTL2 register to 1. In this mode, the reactive power is accumulated in accordance with the sign of the active power. If the active power is positive, the reactive power is added as is to the reactive energy accumulator. If the active power is negative, the reactive power is subtracted from the reactive energy accumulator.

Figure 22-57. Anti-tamper Accumulation Mode (reactive power)

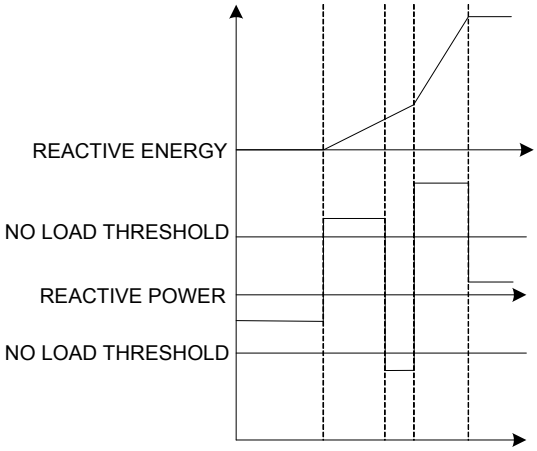


This mode also applies to CF pulse output. The default setting for this mode is off. Detection of transitions in the direction of power flow and detection of the no-load threshold are enabled in this mode.

<3> Absolute value accumulation mode:

This mode can be specified by setting the ABSVARM bit in the PWCTL2 register to 1. In this mode, energy accumulation is performed using the absolute reactive power, ignoring reactive power below the no-load threshold.

Figure 22-58. Absolute Value Accumulation Mode (reactive power)

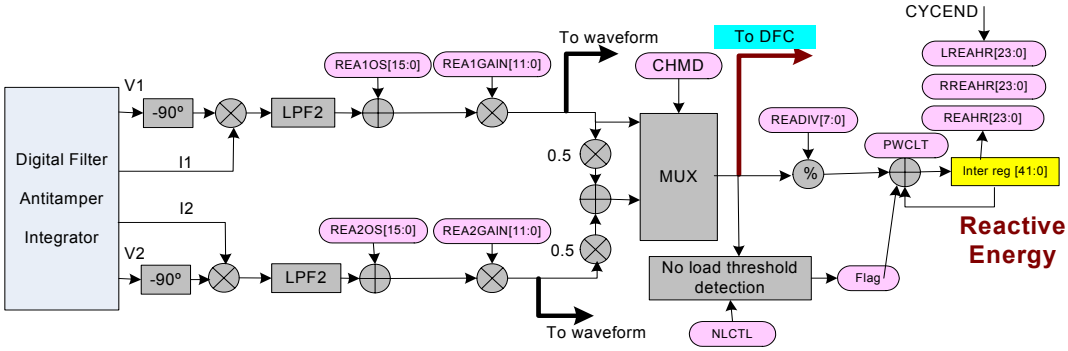


This mode also applies to CF pulse output. The default setting for this mode is off. Detection of transitions in the direction of power flow and detection of the no-load threshold are enabled in this mode.

(d) Reactive energy pulse output

A pulse whose frequency is proportional to the reactive energy is output. Outputting a pulse of this frequency uses the reactive power signal output by the REA1GAIN and REA2GAIN registers, and operation is performed in accordance with the setting of the reactive energy accumulation mode in the PWCTL2 register. For details about pulse output, see **CHAPTER 24 DIGITAL FREQUENCY CONVERSION CIRCUIT**.

Figure 22-59. Reactive Energy Pulse Output



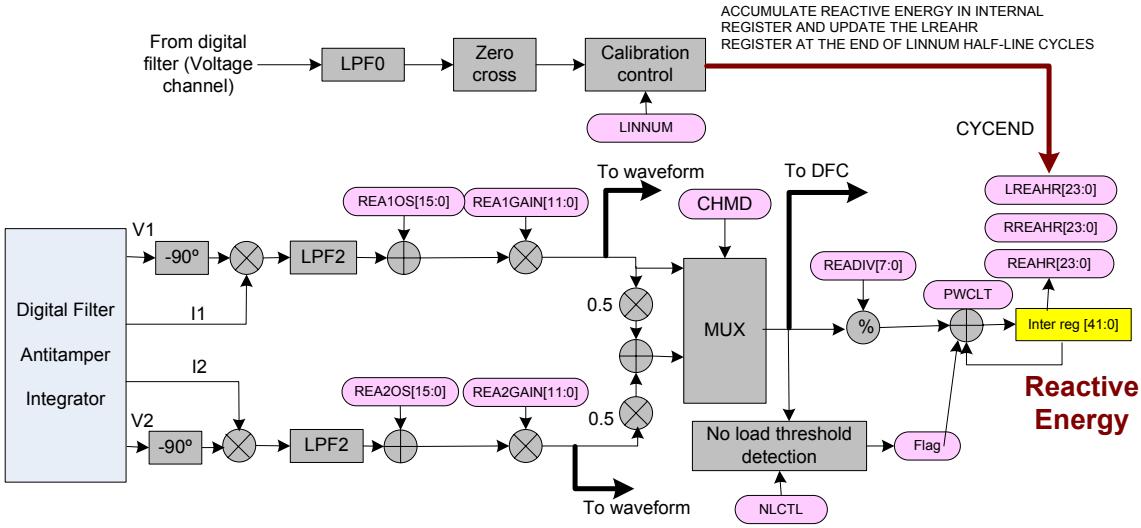
(e) Line cycle reactive energy accumulation mode

In the line cycle reactive energy accumulation mode, the error due to the sinusoidal component of the reactive energy is eliminated, so the reactive power is accumulated in units equal to twice the line frequency. This mode is implemented by synchronizing the energy accumulation with the voltage-channel zero crossing.

Reactive power has a ripple of 100 Hz or 120 Hz when the line frequency is 50 Hz or 60 Hz, respectively. This ripple causes calibration error when a non-integer period is accumulated during energy accumulation. This ripple has very little effect on the CF frequency because this frequency is normally very low. (For example, at 1 Hz, the accumulation time is 1 second.) However, during calibration, a short calibration time is required, and the error caused by ripple can have a large effect. If the accumulation time is equal to the integer period of the line frequency, the error caused by ripple can be eliminated. Therefore, the energy is calculated more accurately in the line cycle reactive energy accumulation mode.

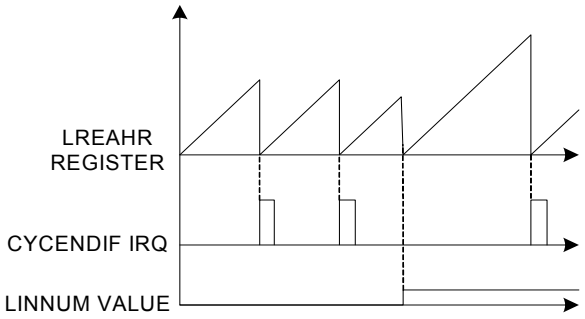
By using this mode, energy calibration can be greatly simplified, and the time necessary for calibration can be significantly reduced. In the line cycle reactive energy accumulation mode, the reactive power signal is accumulated in the LREAHR register for the specified line cycle period. The number of half-line cycles is specified in the LINNUM register, and the reactive energy can be accumulated for up to 65,535 half-line cycles. The reactive power is integrated over the specified number of line cycles, and the CYCENDIF flag in the extended SFR interrupt request flag register 22 (IF22) is set at the end of an reactive energy accumulation line cycle. If the CYCENDMK mask bit in the extended SFR interrupt mask flag register 22 (MK22) is cleared to 0, an interrupt occurs. This interrupt stays active until the CYCENDIF status bit is cleared. Another calibration cycle starts as soon as the CYCENDIF flag is set. If the LREAHR register is not read before a new CYCENDIF flag is set, the LREAHR register is overwritten by a new value.

Figure 22-60. Line Cycle Reactive Energy Accumulation Mode



When a new half-line cycle is written to the LINNUM register, the LREAHR register is reset, and a new accumulation starts at the next zero crossing. The number of half-line cycles is then counted until the LINNUM register value is reached. In this way, valid measurement is performed at the first CYCEND interrupt after writing to the LINNUM register. Line reactive energy accumulation uses the same signal path as reactive energy accumulation. The LSB size of these two registers is equivalent.

Figure 22-61. Accumulation Timing of Reactive Power



The CYCDIS bit in the PWCTL1 register can disable CYCEND detection. If the CYCDIS bit is set to 1, the CYCEND interrupt will not occur when the number of half-line cycles reaches the value specified for the LINNUM register. Also, if the CYCDIS bit is set to 1, the LREAHR register and inner accumulation register will not reset to 0 when a new half-line cycle is written to the LINNUM register.

Note that, in this mode, the 16-bit LINNUM register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate reactive energy for a maximum duration of 65,535 half-line cycles. At a 60 Hz line frequency, this results in a total duration of 65,535/120 Hz = 546 sec.

22.4.6 Apparent power and energy calculation

(1) Apparent power calculation

(a) Apparent power calculation method

Apparent power is defined as the maximum power that can be delivered to a load. Vrms and Irms are the effective voltage and current delivered to the load, respectively. Therefore, for the single-phase two-wire mode, the apparent power (AP) = V1RMS x I1RMS, and, for the single-phase three-wire mode, (AP) = 0.5 x (V1RMS x I1RMS + V2RMS x I2RMS). These equations are independent of the phase angle between the current and the voltage. The following equations are used to calculate the instantaneous power signal:

$$i(t) = \sqrt{2} \times Irms \sin(wt)$$

$$v(t) = \sqrt{2} \times Vrms \sin(wt + \theta)$$

$$p(t) = v(t) \times i(t) = VrmsIrms \cos(\theta) - Vrms \times Irms \cos(2wt + \theta)$$

- If CHMD = 0 (the single-phase two-wire mode):

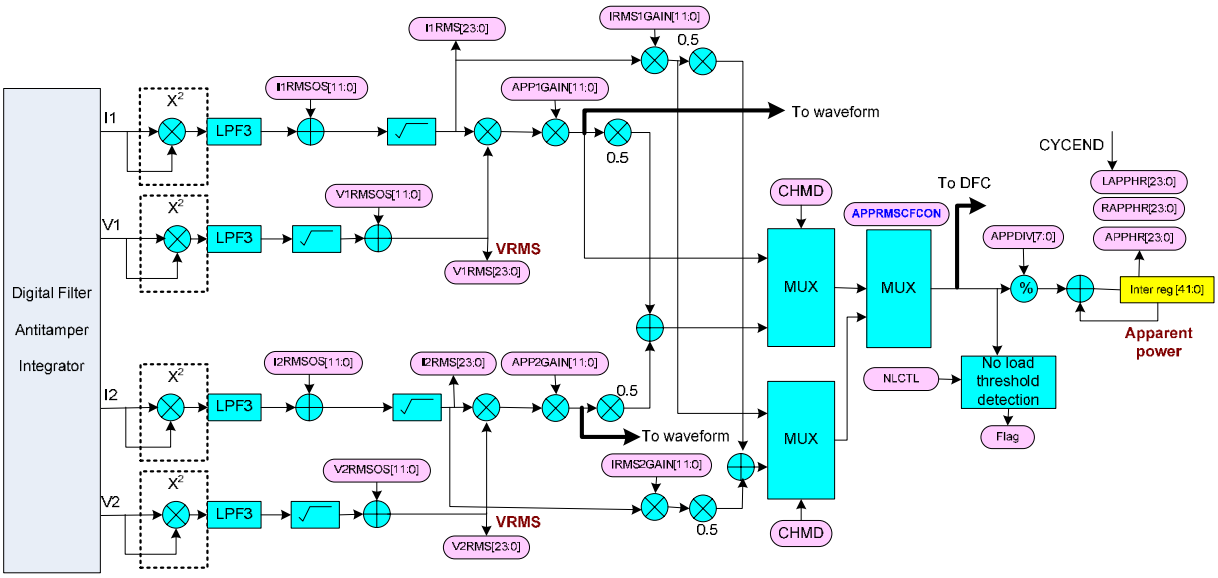
$$Apparen\_power = V1rms \times I1rms$$

- If CHMD = 1: (the single-phase three-wire mode):

$$Apparen\_power = 0.5 * (V1rms \times I1rms + V2rms \times I2rms)$$

Figure 22-62 shows the signal processing for calculating the apparent power.

Figure 22-62. Calculating the Apparent Power

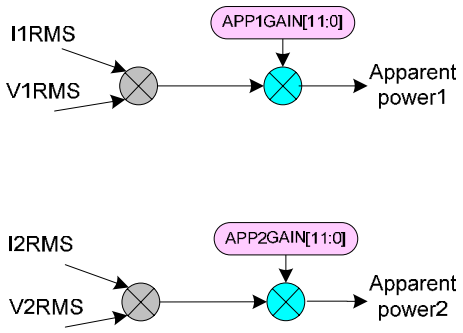


The apparent power signal can be read from the waveform register by setting up the SAMPMODE register and clearing the WFSMMK bit in the extended SFR interrupt mask flag register 22 (MK22). For the recommended flow, see **22.4.9 (5) Waveform-related interrupt (INTWFSM)**.

(b) Apparent power gain calibration

The signed 12-bit registers APP1GAIN and APP2GAIN are used to adjust the apparent energy gain.

Figure 22-63. Apparent Power Gain Calibration



The following equations show how the gain is related to the APP1GAIN and APP2GAIN register settings:

$$Output\_APP1GAIN = \{ApparentPower1 \times [1 + \frac{APP1GAIN}{2^{12}}]\}$$

$$Output\_APP2GAIN = \{ApparentPower2 \times [1 + \frac{APP2GAIN}{2^{12}}]\}$$

For example, if 0x7FF is written to the APP1GAIN register, the apparent power 1 output increases by 50% (0x7FF = 2047d, $2047/2^{12} = 0.5$). Similarly, if 0x800 = –2047d (signed, two's complement), the power output decreases by 50%. Each LSB represents 0.0244% of the power output. The apparent power is calculated using the current and voltage RMS values obtained in the RMS blocks.

(c) Apparent power offset calibration

The apparent power is the product of multiplying the average current (I1RMS, I2RMS) and average voltage (V1RMS, V2RMS). To calibrate the offset of the apparent power, use the I1RMS, I2RMS, V1RMS, and V2RMS offset specification registers. For details about offset calibration, see **22.3 (25) RMS offset specification registers for current channels 1 and 2 (I1RMSOS, I2RMSOS) and (26) RMS offset specification registers for voltage channels 1 and 2 (V1RMSOS, V2RMSOS)**.

(d) Apparent power no-load detection

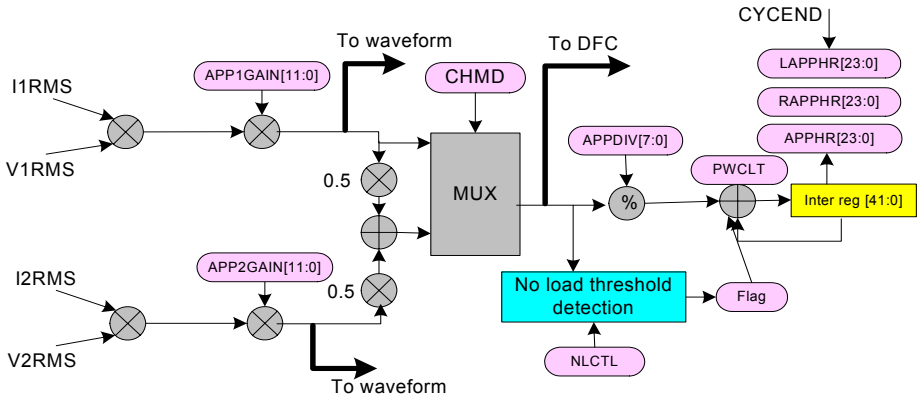
A no-load detection function is provided for the apparent power measurement. When this function is used, apparent energy is not accumulated if the apparent power is below the no-load threshold. The following three bits are used for apparent power no-load detection.

- The APPNOLOAD1 and APPNOLOAD0 bits in the NLCTL register:
  These two bits specify the apparent power no-load threshold.
  00: Disables apparent power no-load detection.
  01: Enables apparent power no-load detection with a threshold of 0.03% of the full scale.
  10: Enables apparent power no-load detection with a threshold of 0.015% of the full scale.
  11: Enables apparent power no-load detection with a threshold of 0.0075% of the full scale.

- The APPNOLDIF flag in extended SFR interrupt request flag register 21 (IF21):
  The APPNOLDIF flag is set when the apparent power falls below the no-load threshold specified by the APPNOLOAD1 and APPNOLOAD0 bits in the NLCTL register.

- The APPNOLDMK bit in the extended SFR interrupt mask flag register 20 (MK20):
  If the APPNOLDMK bit is cleared in the extended SFR interrupt mask flag register 20 (MK20), an interrupt occurs. This interrupt stays active until the APPNOLDIF status bit is cleared.

Figure 22-64. Apparent power No-load Detection



This no-load threshold can also be applied to the CF pulse output. In this case, the no-load threshold level is the same as that for the apparent energy.

(2) Apparent energy calculation

(a) apparent energy calculation method

The apparent energy is defined as integration of apparent power.

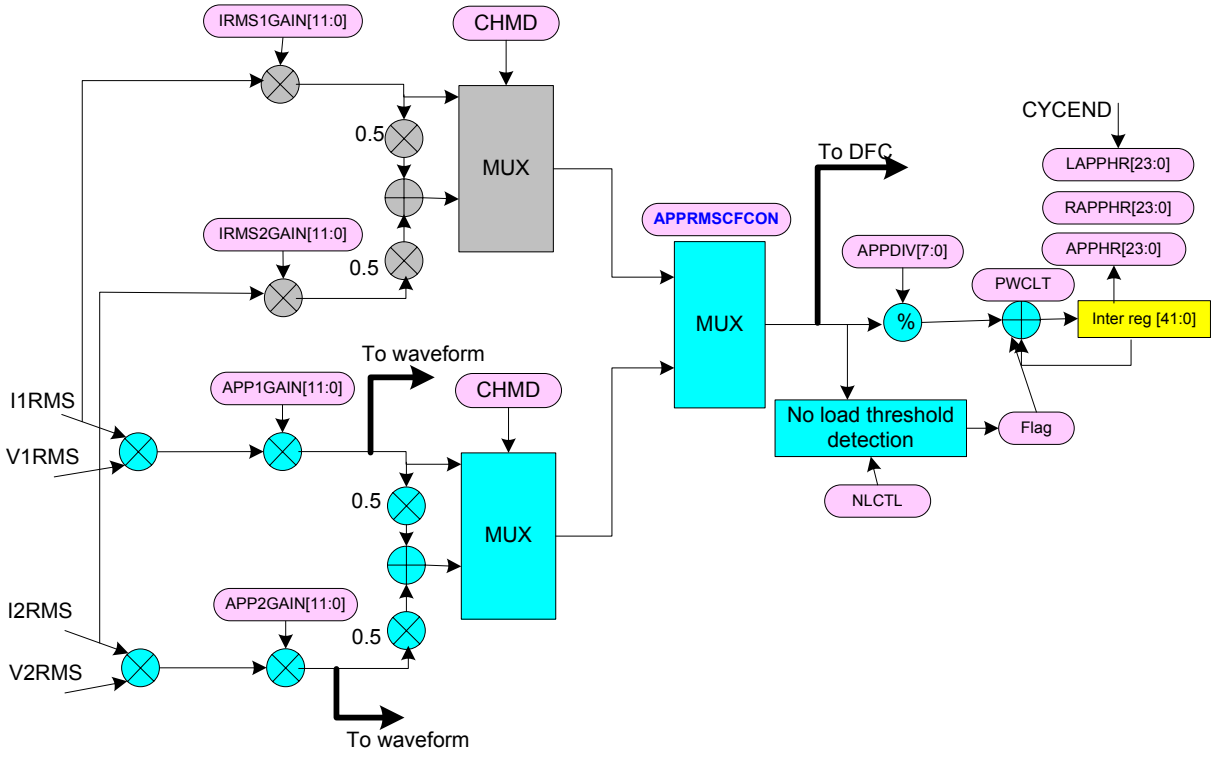
$$Apparen\_energy = \int apparent\_power(t)dt$$

The apparent power signal is integrated by accumulating the apparent power signal in an internal 42-bit energy register. The higher 24 bits of this internal register can be read by the ACTHR register.

$$Apparen\_energy = \lim_{T->0}\{\sum_{n=0}^{\infty} Apparent\_power(nT)\times T$$

In the above equation, n is the discrete time sample number and T is the sample period.
The discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz).

Figure 22-65. Apparent Energy Calculation



The apparent power signal is continuously added to the internal register by performing signed addition. The apparent power is scaled by the value of the APPDIV register and is then accumulated in an internal energy accumulator. APPDIV is an 8-bit unsigned register, and the scaling processing is as follows:

Amount of energy after scaling = power before scaling/APPDIV

Note that clearing APPIV to 0 is prohibited. If 0 is specified, processing is performed as though 1 is specified.
After scaling, the apparent power is accumulated in an internal 42-bit apparent energy accumulator. The higher 24 bits of the internal accumulator can be read by a register. There are three methods for reading the accumulator value, and a reading register is prepared for each.

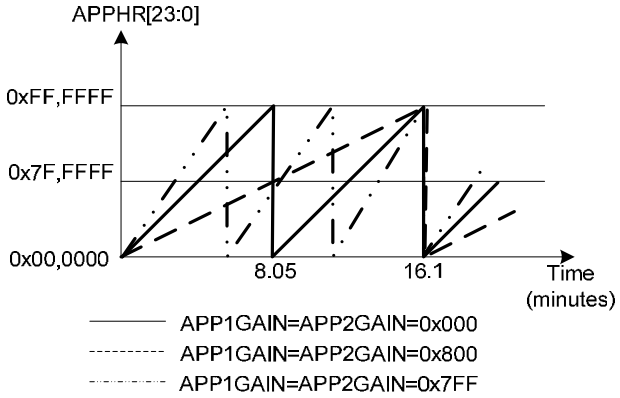
- If reading the value by using the APPHR register:
  The value of the higher 24 bits of the accumulator at the time of reading is read.

- If reading the value by using the RAPPHR register:
  The value of the higher 24 bits of the accumulator at the time of reading is read. After reading, the higher 24 bits of the accumulator are cleared.

- If reading the value by using the LAPPHR register:
  The value is read in sync with the line frequency. For details, see **22.4.6 (2) (d) Line cycle apparent energy accumulation mode**.

Because the apparent energy is always a positive value, the accumulator is always added to.

Figure 22-66. Apparent Energy Accumulation for Full-scale signals



If the apparent energy register is half full (positive or negative) or an overflow or underflow occurs, the interrupt flag bit APPHFIF or APPOFIF is set. By clearing the APPEHFMK and APPEOFMK bits in the extended SFR interrupt mask flag register 21 (MK21), it is possible to specify that interrupts be generated when the apparent energy register is half full or when an overflow occurs. Note that, because the apparent energy register is unsigned, half-full interrupts are generated using 24 bits instead of using 23 bits as they are for the signed active energy register.

(b) Integration time under a steady load

As mentioned in the apparent energy calculation section, the discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz). If the analog input is a full-scale sinusoidal signal and the APP1GAIN and APP2GAIN registers are set to 0x000, the average word value from each GAIN is 2^{21} (or 0x1F, FFFF). The maximum positive value that can be stored in the internal 42-bit register before it overflows is 2^{42} (or 0x3FF, FFFF, FFFF). The integration time under these conditions when APPDIV = 0 is calculated using the following equation:

$$Time = \frac{0x3FF,FFFF,FFFF}{0x1F,FFFF} \times 230.4us = 483.13\,\text{sec} = 8.05\,\text{min}$$

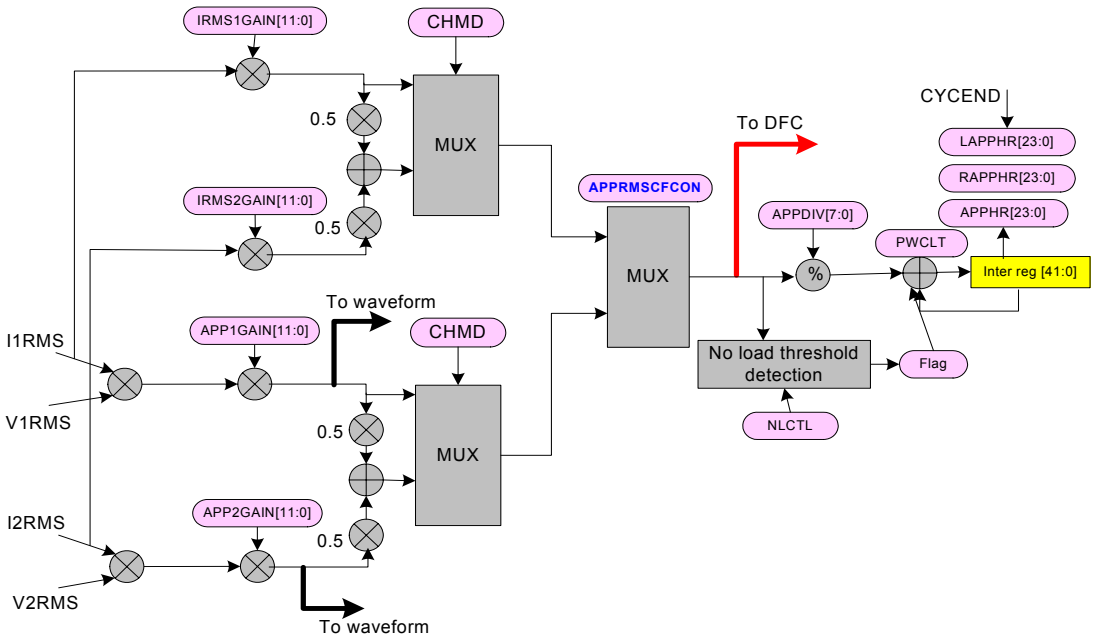
If APPDIV is set to a value other than 0, the integration time varies as follows:

$$Time = Time_{APPDIV=0} \times APPDIV$$

(c) Apparent energy pulse output

A pulse whose frequency is proportional to the apparent energy is output. Outputting a pulse of this frequency uses the apparent energy signal output by the APP1GAIN and APP2GAIN registers. This output can also be used to output a pulse whose frequency is proportional to I1rms or I2rms. For details about pulse output, see **CHAPTER 24 DIGITAL FREQUENCY CONVERSION CIRCUIT**.

Figure 22-67. Apparent Energy Pulse Output



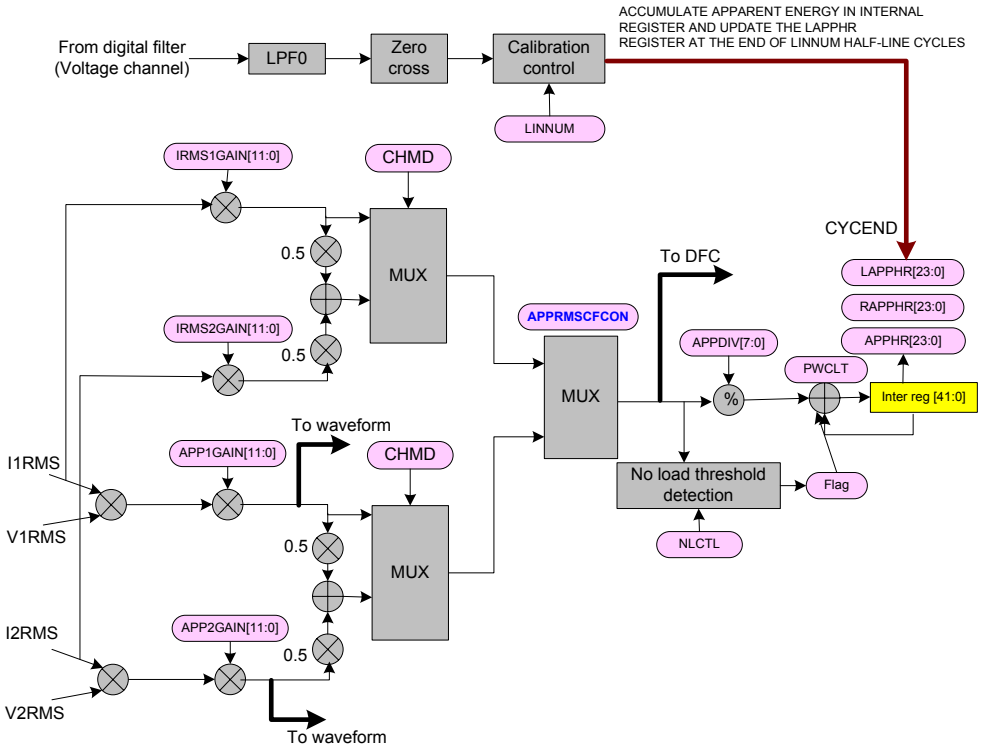
(d) Line cycle apparent energy accumulation mode

In the line cycle apparent energy accumulation mode, the error due to the sinusoidal component of the apparent energy is eliminated, so the apparent power is accumulated in units equal to twice the line frequency. This mode is implemented by synchronizing the energy accumulation with the voltage-channel zero crossing.

Apparent power has a ripple of 100 Hz or 120 Hz when the line frequency is 50 Hz or 60 Hz, respectively. This ripple causes calibration error when a non-integer period is accumulated during energy accumulation. This ripple has very little effect on the CF frequency because this frequency is normally very low. (For example, at 1 Hz, the accumulation time is 1 second.) However, during calibration, a short calibration time is required, and the error caused by ripple can have a large effect. If the accumulation time is equal to the integer period of the line frequency, the error caused by ripple can be eliminated. Therefore, the energy is calculated more accurately in the line cycle apparent energy accumulation mode.

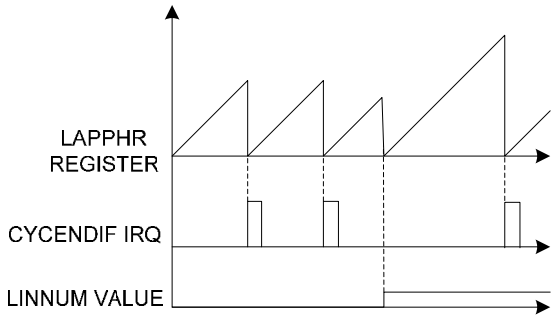
By using this mode, energy calibration can be greatly simplified, and the time necessary for calibration can be significantly reduced. In the line cycle apparent energy accumulation mode, the reactive power signal is accumulated in the LAPPHR register for the specified line cycle period. The number of half-line cycles is specified in the LINNUM register, and the apparent energy can be accumulated for up to 65,535 half-line cycles. The apparent power is integrated over the specified number of line cycles, and the CYCENDIF flag in the extended SFR interrupt request flag register 22 (IF22) is set at the end of an apparent energy accumulation line cycle. If the CYCENDMK mask bit in the extended SFR interrupt mask flag register 22 (MK22) is cleared to 0, an interrupt occurs. This interrupt stays active until the CYCENDIF status bit is cleared. Another calibration cycle starts as soon as the CYCENDIF flag is set. If the LAPPHR register is not read before a new CYCENDIF flag is set, the LAPPHR register is overwritten by a new value.

Figure 22-68. Line Cycle Apparent Energy Accumulation Mode



When a new half-line cycle is written to the LINNUM register, the LAPPHR register is reset, and a new accumulation starts at the next zero-crossing. The number of half-line cycles is then counted until the LINNUM register value is reached. In this way, valid measurement is performed at the first CYCEND interrupt after writing to the LINNUM register. Line apparent energy accumulation uses the same signal path as apparent energy accumulation. The LSB size of these two registers is equivalent.

Figure 22-69. Accumulation Timing of Apparent Power



The CYCDIS bit in the PWCTL1 register can disable CYCEND detection. If the CYCDIS bit is set to 1, the CYCEND interrupt will not occur when the number of half-line cycles reaches the value specified for the LINNUM register. Also, if the CYCDIS bit is set to 1, the LAPPHR register and inner accumulation register will not reset to 0 when a new half-line cycle is written to the LINNUM register.

Note that, in this mode, the 16-bit LINNUM register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate apparent energy for a maximum duration of 65,535 half-line cycles. At a 60 Hz line frequency, this results in a total duration of 65,535/120 Hz = 546 sec.

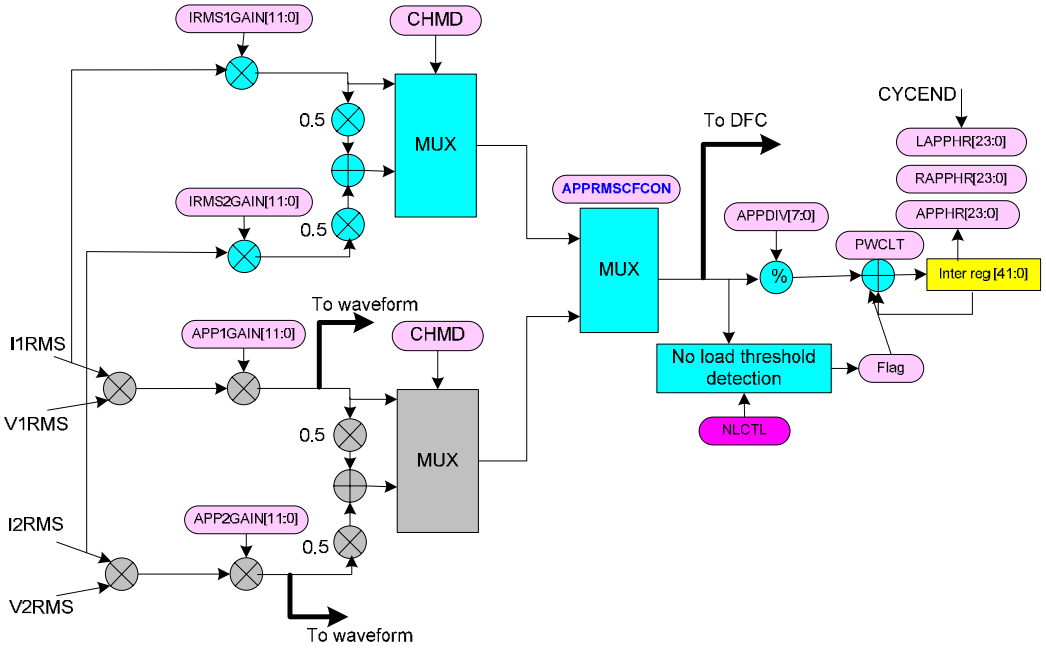
22.4.7 Ampere-hour accumulation

(1) Ampere-hour accumulation selection

Ampere-hour values can be accumulated instead of apparent power. The results of ampere-hour measurement are read using the APPHR, RAPPHR, and LAPPHR registers. Ampere-hour accumulation can be specified by setting the APPRMSCFCON bit to 1. If such accumulation is specified, digital frequency conversion also uses I1rms or 0.5 x (I1rms + I2rms) instead of the apparent power.

Note that, because apparent power accumulation and ampere-hour accumulation use the same circuits, select and use one.

Figure 22-70. Ampere-hour Accumulation



- If CHMD = 0 (the single-phase two-wire mode) : IRMS_accumulation = I1RMS
- If CHMD = 1 (the single-phase three-wire mode) : IRMS_accumulation = 0.5 x (I1RMS + I2RMS)

In this case, the IRMS_accumulation signal is used for the following accumulation and digital frequency conversion.

No-load threshold detection can be enabled by setting the APPRMSCFCON bit to 1. Specify the threshold level by using the APPNOLOAD1 and APPNOLOAD0 bits.

(2) Integration time under a steady load

The discrete time sample period (T) for the accumulation register is 230.4 μs (4.34 kHz). If the analog input is a full-scale sinusoidal signal and the RMS1GAIN and RMS2GAIN registers are set to 0x000, the average value of Irms is:

$$Irms\_FS = \frac{2^{20}}{\sqrt{2}} = 0d741455 = 0xB504F$$

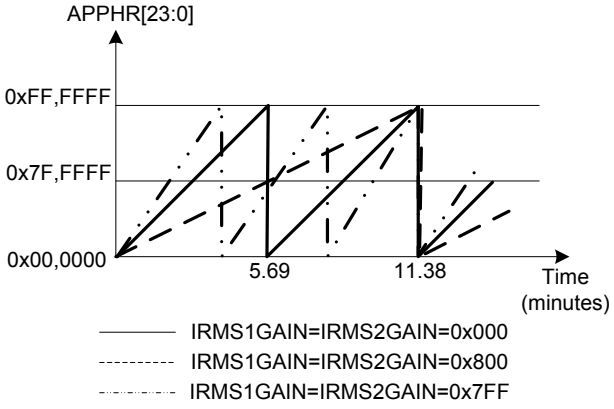
Before IRMS is accumulated in the energy accumulator, 2 LSBs of "0" are added to IRMS.

$$Irms\_acc\_FS = \frac{2^{22}}{\sqrt{2}} = 0d2965820 = 0x2D413C$$

IRMS accumulation is unsigned just like apparent power accumulation. The maximum positive value that can be stored in the internal 42-bit register is 2^{42} (or 0x3FF, FFFF, FFFF). The integration time under these conditions when APPDIV = 0 is calculated using the following equation:

$$Time = \frac{0x3FF,FFFF,FFFF}{0x2D413C} \times 230.4us = 341.66\sec = 5.69\min$$

Figure 22-71. Full-Scale Signal Ampere-Hour Accumulation



When APPDIV is set to a value other than 0, the integration time varies, as shown by the following equation:

$$Time = Time_{APPDIV=0} \times APPDIV$$

22.4.8 Waveform sampling function

There are two registers (SAMP1 and SAMP2) used to read the intermediate data for power calculation. The data to read is selected using the SAMPMODE register, and up to two signals can be read at the same time. The specified data is read at a rate of 4.34 kHz and is latched to the SAMP1 and SAMP2 registers.

Figure 22-72. Waveform Sampling Function

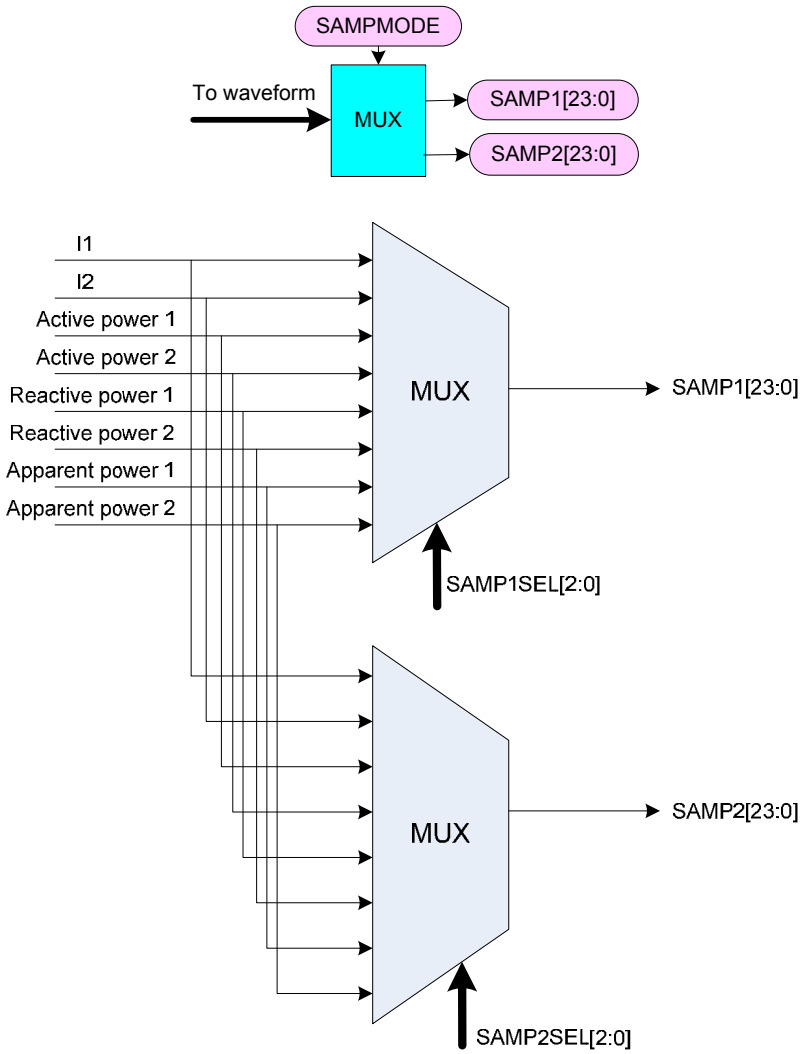


Table 22-7. Select the Waveform for Sample Mode by SAMPMODE Register

SAMPnSEL2	SAMPnSEL1	SAMPnSEL0	Select the waveform n for sample mode by SAMPMODE register (n = 1, 2)	Fs_code
0	0	0	I1 output from integrator	2^{20}
0	0	1	I2 output from integrator	2^{20}
0	1	0	Active power 1 (output of ACT1GAIN after multiplication)	2^{21}
0	1	1	Active power 2 (output of ACT2GAIN after multiplication)	2^{21}
1	0	0	Reactive power 1 (output of REA1GAIN after multiplication)	2^{21}
1	0	1	Reactive power 2 (output of REA2GAIN after multiplication)	2^{21}
1	1	0	Apparent power 1 (output of APP1GAIN after multiplication)	2^{21}
1	1	1	Apparent power 2 (output of APP2GAIN after multiplication)	2^{21}

22.4.9 Interrupt

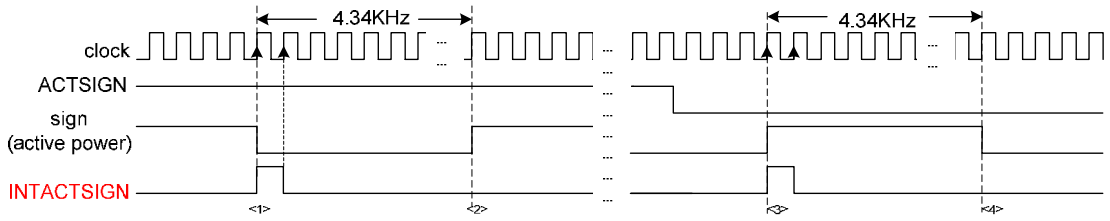
There are 13 interrupts in the power calculation circuit.

(1) Active power and energy-related interrupts

(a) INTACTSIGN

If ACTSIGN = 0, an INTACTSIGN interrupt occurs when the active power changes from positive to negative.
If ACTSIGN = 1, an INTACTSIGN interrupt occurs when the active power changes from negative to positive.

Figure 22-73. INTACTSIGN Interrupt (active power)



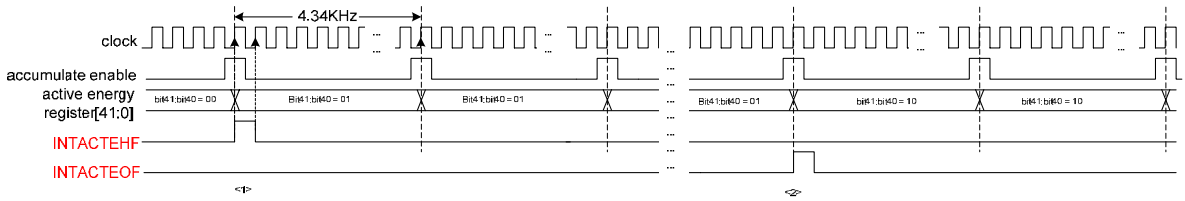
<1> If ACTSIGN = 1 and the active power changes from negative to positive, an INTACTSIGN interrupt occurs.
<2> If ACTSIGN = 1 and the active power changes from positive to negative, no INTACTSIGN interrupt occurs.
<3> If ACTSIGN = 0 and the active power changes from positive to negative, an INTACTSIGN interrupt occurs.
<4> If ACTSIGN = 0 and the active power changes from negative to positive, no INTACTSIGN interrupt occurs.

(b) INTACTEHF, INTACTEOF

An INTACTEHF interrupt occurs when the active energy register is half full (positive or negative).

An INTACTEOF interrupt occurs when the active energy register overflows or underflows (positive or negative).

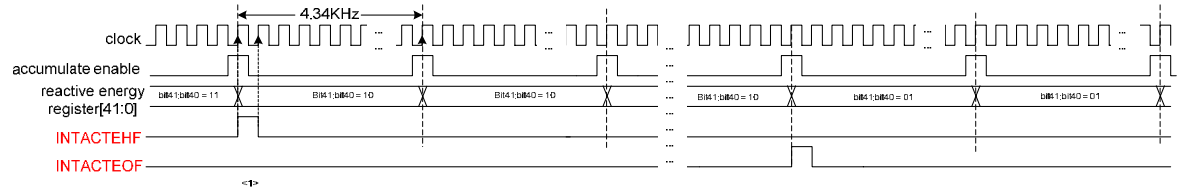
Figure 22-74. INTACTEHF and INTACTEOF Interrupts (When Active Energy Is Positive)



<1> If the active energy is half full, an INTACTEHF interrupt occurs.

<2> If the active energy overflows, an INTACTEOF interrupt occurs.

Figure 22-75. INTACTEHF and INTACTEOF Interrupts (When Active Energy Is Negative)



<1> If the active energy is half full, an INTACTEHF interrupt occurs.

<2> If the active energy overflows, an INTACTEOF interrupt occurs.

(c) INTACTNOLD

An INTACTNOLD interrupt occurs when the active power falls below the no-load threshold.

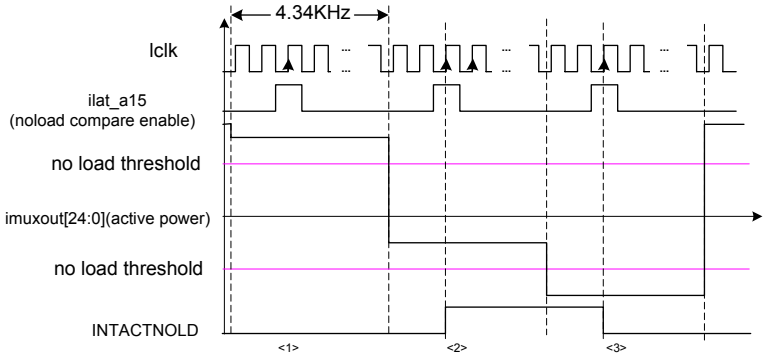
The threshold is specified by using the ACTNOLOAD1 and ACTNOLOAD0 bits in the NLCTL register. (For details, see **22.3 (3) No-load level control register (NLCTL)**).

The full-scale active power is 2^{21} = 1FFFFFH. Table 22-8 shows the threshold values for each combination of bit settings.

Table 22-8 No-load threshold of active power

ACTNOLOAD1, 0	No-load threshold
00	0
01	25'h013A (0.015% of the full scale)
10	25'h009D (0.0075% of the full scale)
11	25'h004D (0.0037% of the full scale)

Figure 22-76. INTACTNOLD Interrupt (Active Power)



<1> If the active power rises above the no-load threshold, no INTACTNOLD interrupt occurs.

<2> If the active power falls below the no-load threshold, an INTACTNOLD interrupt occurs.

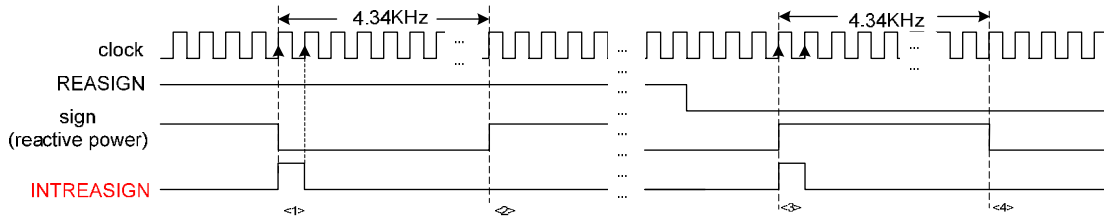
<3> If the absolute value of the active power rises above the no-load threshold, no INTACTNOLD interrupt occurs.

(2) Reactive power and energy-related interrupts

(a) INTREASIGN

If REASIGN = 0, an INTREASIGN interrupt occurs when the reactive power changes from positive to negative.
If REASIGN = 1, an INTREASIGN interrupt occurs when the reactive power changes from negative to positive.

Figure 22-77. INTREASIGN Interrupt (Reactive Power)



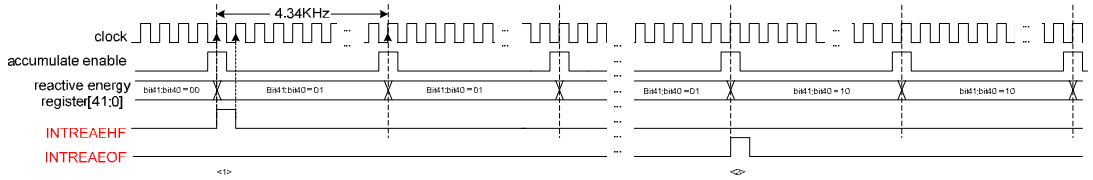
<1> If REASIGN = 1 and the reactive power changes from negative to positive, an INTREASIGN interrupt occurs.
<2> If REASIGN = 1 and the reactive power changes from positive to negative, no INTREASIGN interrupt occurs.
<3> If REASIGN = 0 and the reactive power changes from positive to negative, an INTREASIGN interrupt occurs.
<4> If REASIGN = 0 and the reactive power changes from negative to positive, no INTREASIGN interrupt occurs.

(b) INTREAEHF, INTREAEOF

An INTREAEHF interrupt occurs when the reactive energy register is half full (positive or negative).

An INTREAEOF interrupt occurs when the reactive energy register overflows or underflows (positive or negative).

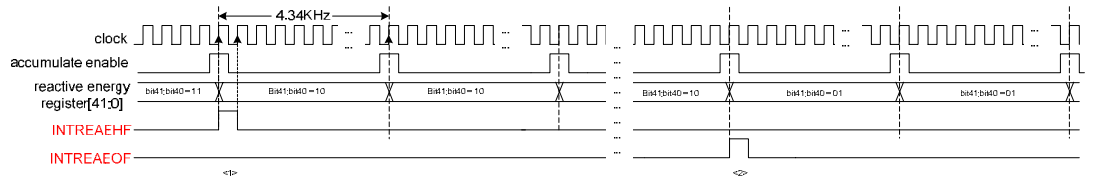
Figure 22-78. INTREAEHF and INTREAEOF Interrupts (When Reactive Energy Is Positive)



<1> If the reactive energy is half full, an INTREAEHF interrupt occurs.

<2> If the reactive energy overflows, an INTREAEOF interrupt occurs.

Figure 22-79. INTREAEHF and INTREAEOF Interrupts (When Reactive Energy Is Negative)



<1> If the reactive energy is half full, an INTREAEHF interrupt occurs.

<2> If the reactive energy overflows, an INTREAEOF interrupt occurs.

(c) INTREANOLD

An INTREANOLD interrupt occurs when the reactive power falls below the no-load threshold.

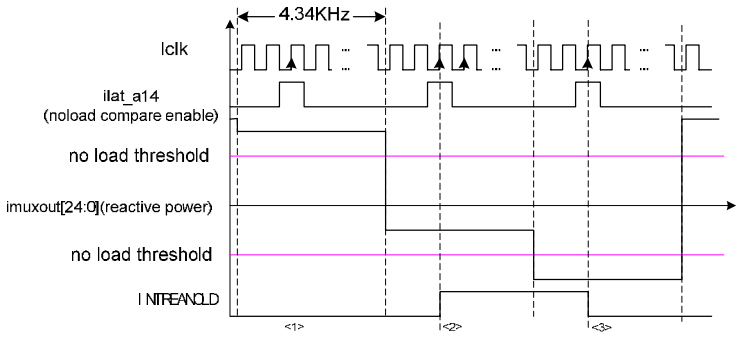
The threshold is specified by using the REANOLOAD1 and REANOLOAD0 bits in the NLCTL register. (For details, see **22.3 (3) No-load level control register (NLCTL)**.)

The full-scale reactive power is 2^{21} = 1FFFFFH. Table 22-9 shows the threshold values for each combination of bit settings.

Table 22-9 No-load threshold of reactive power

REANOLOAD1, 0	No-load threshold
00	0
01	25'h013A (0.015% of the full scale)
10	25'h009D (0.0075% of the full scale)
11	25'h004D (0.0037% of the full scale)

Figure 22-80. INTREANOLD Interrupt (Reactive Power)



<1> If the reactive power rises above the no-load threshold, no INTREANOLD interrupt occurs.

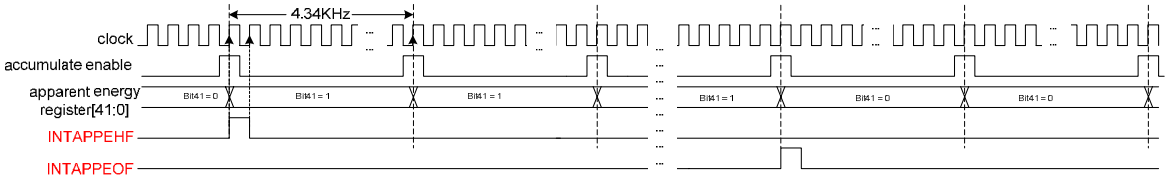
<2> If the reactive power falls below the no-load threshold, an INTREANOLD interrupt occurs.

<3> If the absolute value of the reactive power rises above the no-load threshold, no INTREANOLD interrupt occurs.

(3) Apparent power and energy-related interrupts

(a) INTAPPEHF, INTAPPEOF

Figure 22-81. INTAPPEHF and INTAPPEOF Interrupts



(b) INTAPPNOLD

An INTAPPNOLD interrupt occurs when the apparent power falls below the no-load threshold.

The threshold is specified by using the APPNOLOAD1 and APPNOLOAD0 bits in the NLCTL register. (For details, see **22.3 (3) No-load level control register (NLCTL)**.)

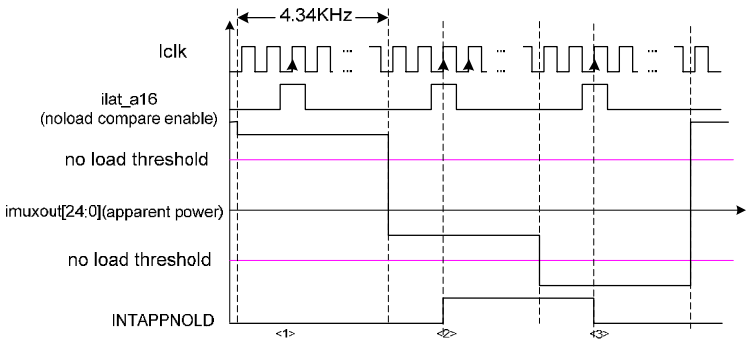
The full-scale apparent power is 2^{21} = 1FFFFFH. Table 22-10 shows the threshold values for each combination of bit settings.

Note that this no-load threshold also applies to the Irms pulse output if the APPRMSCFCON bit is set. In this case, if APPRMSCFCON = 1, IRMS no-load threshold detection is enabled, and the level of the no-load threshold is the same as for the apparent energy. The full-scale IRMS value is $2^{19.5}$. This is because, due to the fact that IRMS is 23 bits and the power is 25 bits, IRMS is expanded by two bits. The IRMS threshold is $2^{(19.5+2)}$ = $2^{21.5}$ = 2D413D H.

Table 22-10 No-load Threshold of Apparent Power

APPRMSCFCON	APPNOLOAD1, 0	No-load threshold
0	00	0
0	01	25'h0275 (0.03% of the apparent power full scale)
0	10	25'h013A (0.015% of the apparent power full scale)
0	11	25'h009D (0.0075% of the apparent power full scale)
1	00	0
1	01	25'h0379 (0.03% of the IRMS full scale)
1	10	25'h01BC (0.015% of the IRMS full scale)
1	11	25'h00DE (0.0075% of the IRMS full scale)

Figure 22-82. INTAPPNOLD Interrupt



<1> If the apparent power rises above the no-load threshold, no INTAPPNOLD interrupt occurs.

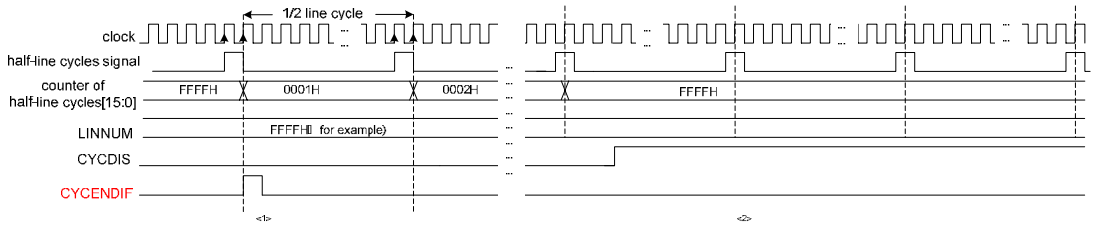
<2> If the apparent power falls below the no-load threshold, an INTAPPNOLD interrupt occurs.

<3> If the absolute value of the apparent power rises above the no-load threshold, no INTAPPNOLD interrupt occurs.

(4) Cycend-related interrupt (INTCYCED)

An INTCYCED interrupt occurs when the number of half-line cycles becomes equal to the LINNUM register value. The CYCDIS bit in the PWCTL1 register can be used to disable INTCYCED detection. If the CYCDIS bit is set to 1, no INTCYCED interrupt occurs when the number of half-line cycles reaches the value specified for the LINNUM register.

Figure 22-83. INTCYCED Interrupt



<1> If CYCDIS = 0 and the number of half-line cycles = the LINNUM value, an INTCYCED interrupt occurs.

<2> If CYCDIS = 1 and the number of half-line cycles = the LINNUM value, no INTCYCED interrupt occurs.

(5) Waveform-related interrupt (INTWFSM)

INTWFSM interrupts occur according to the settings for SAMPnSEL2, SAMPnSEL1, and SAMPnSEL0 (For details, see **22.3 (27) Sampling mode selection register (SAMPMODE)**).

When the signal assigned to SAMPnSEL changes, the corresponding interrupt occurs.

The SAMP1 and SAMP2 registers are updated during each sampling period (fs = 4.34 kHz). These registers can be read at any time. The following procedure is recommended for waveform sampling:

<1> Set up the SAMPMODE register to select the waveform source for the SAMP1 and SAMP2 registers.

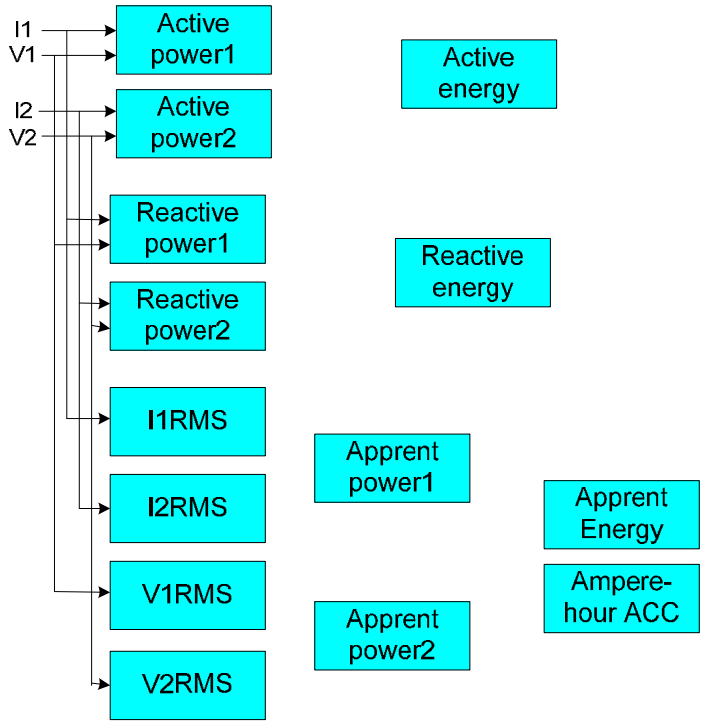
<2> Set the SAMPEN bit to enable waveform sampling. Clear the WFSMMK bit of the extended SFR interrupt mask flag register 22 (MK22) to enable interrupts to occur after updating the SAMP1 and SAMP2 registers.

<3> If an INTWFSM interrupt occurs, read the SAMP1 and SAMP2 registers to obtain new waveform sampling data, and then clear WFSMIF (the interrupt flag for waveform sampling).

22.4.10 Power-saving mode

A power-saving mode is available to reduce power consumption. This mode can stop unnecessary power calculations.

Figure 22-84. Power Configuration



There are 6 bits those used to control power saving function.

- PWREN (Bit 7 of PWCTL1 register)
  0: All Power calculation functions are disable
  1: All Power calculation functions are enable

- CHMD (bit 5 of ADM2 register)
  0: For two wire application
  1: For three wire application

- ACTDIS (bit 7 of PWCTL2)
  0: Active power calculation enable
  1: Active power calculation disable

- READIS (bit 6 of PWCTL1)
  0: Reactive power calculation enable
  1: Reactive power calculation disable

- APPDIS (bit 5 of PWCTL1)
  0: Apparent power calculation and ampere-hour ACC enable
  1: Apparent power calculation and ampere-hour ACC disable

- APPRMSCFCON (bit 2 of PWCTL1)
  0: Apparent power is accumulated
  1: Ampere-hour is accumulated

Table 22-11 List of Control Active Power and Energy

PWREN	CHMD	ACTDIS	Active power 1	Active power 2	Active energy
0	0/1	0/1	x	x	x
1	0/1	1	x	x	x
1	0	0	√	x	√
1	1	0	√	√	√

Table 22-12 List of Control Reactive Power and Energy

PWREN	CHMD	READIS	Reactive power 1	Reactive power 2	Reactive energy
0	0/1	0/1	x	x	x
1	0/1	1	x	x	x
1	0	0	√	x	√
1	1	0	√	√	√

Table 22-13 List of Control Apparent Power, Energy, RMS, and Ampere-hour ACC

PWREN	CHMD	APPDIS	APPRMS CFCON	Apparent power 1	Apparent power 2	Apparent energy	I1RMS	I2RMS	V1RMS	V2RMS	ampere-hour ACC
0	0/1	0/1	0/1	x	x	x	x	x	x	x	x
1	0	1	0/1	x	x	x	√	√	x	x	x
1	0	0	0	√	x	√	√	√	√	x	x
1	0	0	1	x	x	x	√	√	√	x	√
1	1	1	0/1	x	x	x	√	√	x	x	x
1	1	0	0	√	√	√	√	√	√	√	x
1	1	0	1	x	x	x	√	√	√	√	√

22.4.11 Notes on power calculation circuit

- The performance of the power calculation circuit is only guaranteed when the main clock is running at 10 MHz and the data rate is 10 MHz/(128^{18}).
- Many registers in the power calculation circuit contain 2 bytes or more. When reading from a register that contains 2 bytes or more, read the lower bytes first and then the higher bytes. Similarly, when writing to a register that contains 2 bytes or more, write the lower bytes first and then the higher bytes. Other access methods might not work correctly.
- When using the power-saving mode, do not perform waveform sampling on the corresponding channel.
  After specifying the power-saving mode, the corresponding energy accumulator does not change. Therefore, after specifying this mode, do not read the energy register for the corresponding channel.
  Before specifying the power-saving mode, the source for the digital frequency conversion circuit must be checked or changed to ensure that the source of the digital frequency conversion circuit is not delivered by the corresponding channel. For example, before ACTDIS is set, “00” is prohibited for [CFSEL1, CFSEL0] (When “00” is specified, active power is selected for the source of the digital frequency conversion circuit).

CHAPTER 23 POWER QUALITY MEASUREMENT CIRCUIT

The power quality measurement circuit is used to measure the quality of input signals.

23.1 Power Quality Measurement Circuit Functions

The power quality measurement circuit has the following functions:

- Zero-crossing detection
- Zero-crossing timeout detection
- SAG detection
- Peak measurement
- Period and frequency measurement
- Fault detection
- Current channel gain adjustment

23.1.1 Generated interrupt signals

The power quality measurement circuit generates the following interrupt signals.

Table 23-1. Interrupt Signal of Power Measurement Quality Circuit

Interrupt request signal	Interrupt request flag	Interrupt mask flag	Interrupt Source
INTZX1	ZX1IF	ZX1MK	Zero-crossing detection interrupt for voltage channel 1
INTZX2	ZX2IF	ZX2MK	Zero-crossing detection interrupt for voltage channel 2
INTZXTO1	ZXTO1IF	ZXTO1MK	Zero-crossing timeout interrupt for voltage channel 1
INTZXTO2	ZXTO2IF	ZXTO2MK	Zero-crossing timeout interrupt for voltage channel 2
INTSAG1	SAG1IF	SAG1MK	SAG detection interrupt for voltage channel 1
INTSAG2	SAG2IF	SAG2MK	SAG detection interrupt for voltage channel 2
INTPKI1	PKI1IF	PKI1MK	Peak detection interrupt for current channel
INTPKV1	PKV1IF	PKV1MK	Peak detection interrupt for voltage channel
INTFAULTSIGN	FAULTSIGNIF	FAULTSIGNMK	Fault detection interrupt

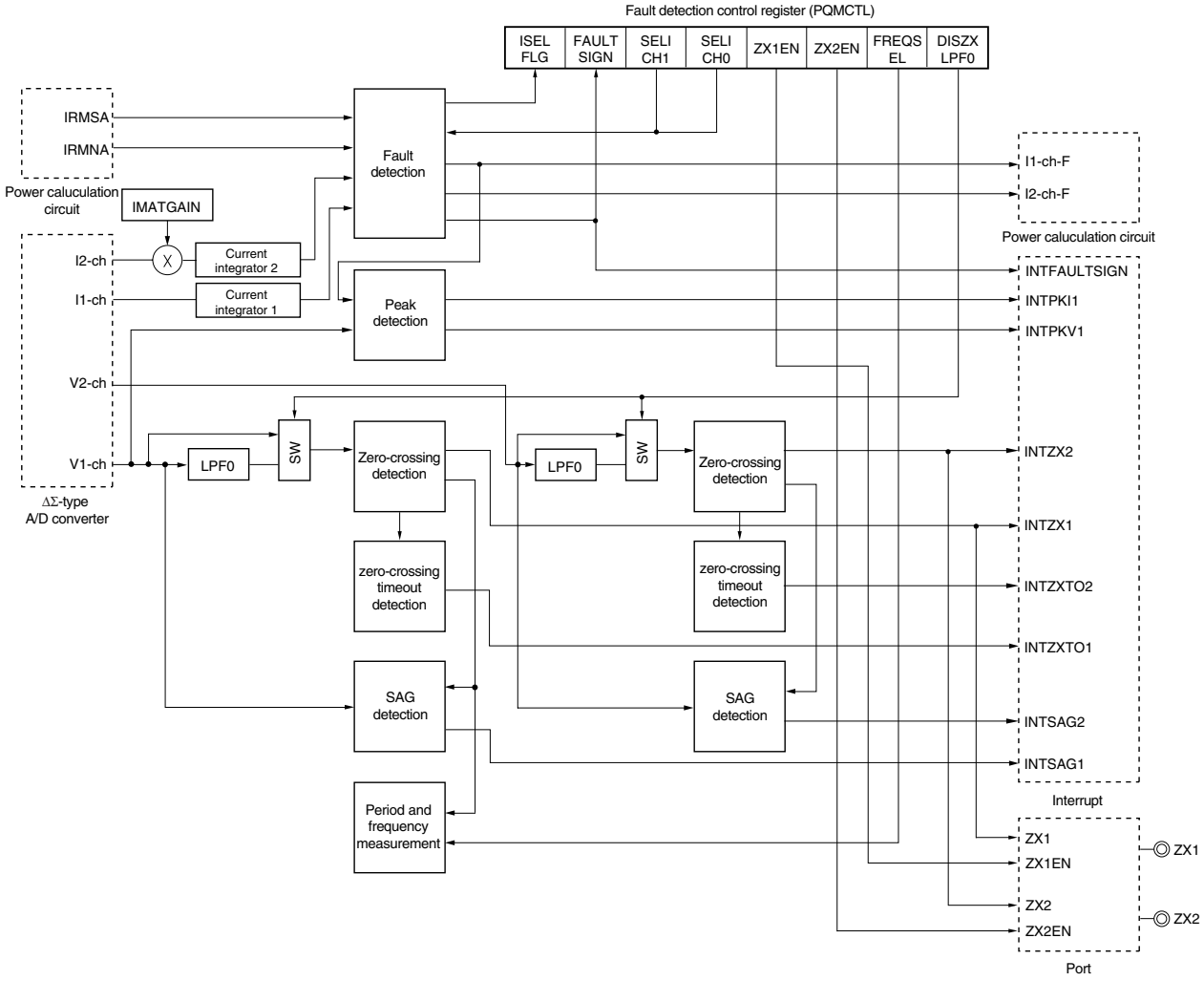
23.2 Configuration of Power Quality Measurement Circuit

The power quality measurement circuit includes the following hardware.

Table 23-2. Configuration of Power Quality Measurement Circuit

Item	Configuration
Controller	Zero-crossing detection circuit
	Zero-crossing timeout detection circuit
	SAG detection circuit
	Peak measurement circuit
	Period and frequency measurement circuit
	Fault detection circuit
	Current channel gain adjustment circuit
Registers	Period and frequency measurement result register (PFVAL)
	Peak current value register (IMAX)
	Peak current value clearing register (RSTIMAX)
	Peak voltage value register (VMAX)
	Peak voltage value clearing register (RSTVMAX)
Control registers	Zero-crossing timeout specification registers for voltage channels 1 and 2 (ZXTOUT1, ZXTOUT2)
	SAG line cycle number specification registers for voltage channels 1 and 2 (SAGNUM1, SAGNUM2)
	SAG level specification registers for voltage channels 1 and 2 (SAGVAL1, SAGVAL2)
	Peak current level specification register (IPKLMT)
	Peak voltage level specification register (VPKLMT)
	Gain specification register (IMATGAIN)
	Fault detection control register (PQMCTL)
	Fault detection threshold value specification register (IST)
	Fault control register (ICHK)

Figure 23-1. Block Diagram of Power Quality Measurement Circuit



(1) Zero-crossing detection circuit, zero-crossing timeout circuit

These circuits are used to monitor the status of the voltage signal input to the V1 and V2 channels.
Zero-crossing signal output is enabled by setting the ZX1EN and ZX2EN bits of the PQMCTL register to 1.

(a) Zero-crossing detection

For the V1 and V2 channel values input from the ΔΣ-type A/D converter, the inversion of the sign (a zero crossing) is detected. It is possible to specify that a zero-crossing interrupt (INTZXn) occur when the sign is inverted.

(b) Zero-crossing timeout

If no zero-crossing is detected within the specified timeout period, a zero-crossing timeout interrupt (INTZXTOn) occurs.
The timeout time is specified for the ZXTOUTn register as a number of sampling clock (fs = 4.34 kHz) counts.

(2) SAG detection circuit

This circuit is used to monitor for changes in the input voltage (on the V1 and V2 channels).
If the SAG detection voltage level specified for the SAGVALn register or a lower level is continuously applied during the period of the number of line cycles specified for the SAGNUMn register, a SAG interrupt (INTSAGn) occurs.

(3) Peak measurement circuit

This circuit is used to monitor for peaks in the input voltage (on the V1 channel) and the input current (on the I1 channel).
If the absolute value of the input voltage (on the V1 channel) or the input current (on the I1 channel) exceeds the peak detection voltage or current level specified for the VPKLMT or IPKLMT register, an interrupt (INTPKV1 or INTPKI1) occurs, and the detected peak value (an absolute value) is stored in the VMAX or IMAX register.

The following two modes are available for reading peak values, and registers are prepared for each reading mode:

- Normal reading (register names: VMAX and IMAX)
  Detected peak values are read.
- Reading with a reset (register names: RSTVMAX and RSTIMAX)
  Detected peak values are read. After reading, the register values are cleared.

Remark n= 1, 2

(4) Period and frequency measurement circuit

This circuit is used to measure the period and frequency of the voltage channel (only the V1 channel). The period and frequency can be switched using the PQMCTL register.

(a) Period measurement

The sampling clock (fs = 4.34 kHz) of the ΔΣ-type A/D converter is used to count a 20-line interval. This count result is stored in the PFVAL register.

(b) Frequency measurement

The sampling clock (fs = 4.34 kHz) of the ΔΣ-type A/D converter is used to count a 20-line interval. This count value is used to calculate the frequency. The calculation result is stored in the PFVAL register as 0.0625 Hz/LSB.

(5) Fault detection circuit

This circuit is only used in the single-phase two-wire mode. I1 is connected to the line side and I2 is connected to the neutral side to perform current detection by using two lines.

(a) Fault detection

If the following conditions are met, a fault is detected, the active channel is switched, and an interrupt can be generated.

- The difference between the average current values (RMS values) for the I1 and I2 channels exceeds the multiple[Note] (1/8, 1/16, 1/32, or 1/64) specified for the average active channel current value.
- The larger of the average current values (RMS values) for the I1 and I2 channels exceeds the value specified for the IST register.

Note This multiple is specified for the ICHK register.

(b) Active channel switching

If the automatic mode is specified for the PQMCTL register and a fault condition is detected, the active channel is automatically switched. Switching the channel can also be specified.

The PQMCTL register can be used to check the current active channel.

(c) Fault interrupt occurrence

An interrupt (INTFAULTSIGN) occurs when a fault is detected or when the system returns from the fault status.

(6) Current channel gain correction

To detect faults, a comparison is made using the difference between current I1 and current I2. Therefore, current I1 and current I2 must be adjusted to the same amount of current in advance. The current gain correction circuit performs correction by adding gain to input current value I2.

23.3 Power Quality Measurement Circuit

The power quality measurement circuit uses the following registers.
These registers are all allocated to the extended SFR space.
For details about how to access the extended SFR space, see **CHAPTER 17 EXTENDED SFR INTERFACE**.

- Period and frequency measurement result register (PFVAL)
- Zero-crossing timeout specification registers for voltage channels 1 and 2 (ZXTOUT1, ZXTOUT2)
- SAG line cycle number specification registers for voltage channels 1 and 2 (SAGNUM1, SAGNUM2)
- SAG level specification registers for voltage channels 1 and 2 (SAGVAL1, SAGVAL2)
- Peak current level specification register (IPKLMT)
- Peak voltage level specification register (VPKLMT)
- Peak current value register (IMAX)
- Peak current value clearing register (RSTIMAX)
- Peak voltage value register (VMAX)
- Peak voltage value clearing register (RSTVMAX)
- Gain specification register (IMATGAIN)
- Fault detection control register (PQMCTL)
- Fault detection threshold value specification register (IST)
- Fault control register (ICHK)

(1) Period and frequency measurement result register (PFVAL)

Period and frequency measurement result of voltage channel 1 is stored in this register.
PFVAL is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 0000H.

Figure 23-2. Format of Period and Frequency Measurement Result Register (PFVAL)

Address: 100H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
PFVALL	PFVAL7	PFVAL6	PFVAL5	PFVAL4	PFVAL3	PFVAL2	PFVAL1	PFVAL0

Address: 101H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
PFVALH	PFVAL15	PFVAL14	PFVAL13	PFVAL12	PFVAL11	PFVAL10	PFVAL9	PFVAL8

PFVAL15 to 0	Used to store the Period and frequency measurement result of voltage channel 1
0000H to FFFFH	Period and frequency measurement result

Remark The FREQSEL bit of the PQMCTL register can be used to specify whether to store the result of measuring the period or frequency in the register.

- If FREQSEL = 0, the result of measuring the period is stored in the register.
- If FREQSEL = 1, the result of measuring the frequency is stored in the register.

(2) Zero-crossing timeout specification registers for voltage channels 1 and 2 (ZXTOUT1, ZXTOUT2)

The ZXTOUT1 and ZXTOUT2 registers are used to set the zero-crossing timeout specification of voltage channels 1 and 2.

ZXTOUT1 and ZXTOUT2 are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 03FFH.

Figure 23-3. Format of Zero-crossing Timeout Specification Registers for Voltage Channels 1 and 2 (ZXTOUT1, ZXTOUT2)

(a) ZXTOUT1

Address: 102H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
ZXTOUT1L	ZXTOUT17	ZXTOUT16	ZXTOUT15	ZXTOUT14	ZXTOUT13	ZXTOUT12	ZXTOUT11	ZXTOUT10

Address: 103H After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
ZXTOUT1H	0	0	0	0	0	0	ZXTOUT19	ZXTOUT18

(b) ZXTOUT2

Address: 104H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
ZXTOUT2L	ZXTOUT27	ZXTOUT26	ZXTOUT25	ZXTOUT24	ZXTOUT23	ZXTOUT22	ZXTOUT21	ZXTOUT20

Address: 105H After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
ZXTOUT2H	0	0	0	0	0	0	ZXTOUT29	ZXTOUT28

ZXTOUTn9 to n0	Specify the zero-crossing timeout specification of voltage channels 1 and 2 (n = 1, 2)
0000H to 03FFH	zero-crossing timeout specification

Cautions 1. Be sure to clear bits 2 to 7 of the ZXTOUT1H and ZXTOUT2H to 0.

2. When CHMD (bit 5 of ADM2) = 0, ZXTOUT2 cannot be written. The read value is the reset value.

(3) SAG line cycle number specification registers for voltage channels 1 and 2 (SAGNUM1, SAGNUM2)

SAGNUM1 and SAGNUM2 registers are used to set the line cycle number of the SAG detection for voltage channels 1 and 2.

These registers can be set by a half line unit.

SAGNUM1 and SAGNUM2 are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to FFH.

Figure 23-4. Format of SAG Line Cycle Number Specification Registers for Voltage Channels 1 and 2 (SAGNUM1, SAGNUM2)

(a) SAGNUM1

Address: 106H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
SAGNUM1	SAGNUM17	SAGNUM16	SAGNUM15	SAGNUM14	SAGNUM13	SAGNUM12	SAGNUM11	SAGNUM10

(b) SAGNUM2

Address: 10AH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
SAGNUM2	SAGNUM27	SAGNUM26	SAGNUM25	SAGNUM24	SAGNUM23	SAGNUM22	SAGNUM21	SAGNUM20

SAGNUMn7 to n0	Specify line cycle number of SAG detection for voltage channel n (n = 1, 2)
00H to FFH	Line cycle number of SAG detection

Caution When CHMD (bit 5 of ADM2) = 0, SAGNUM2 cannot be written. The read value is the reset value.

(4) SAG level specification registers for voltage channels 1 and 2 (SAGVAL1, SAGVAL2)

SAGVAL1 and SAGVAL2 registers are used to set the voltage level of the SAG detection for voltage channels 1 and 2.

SAGVAL1 and SAGVAL2 are allocated to the extended SFR space.

Use the extended SFR interface to set up these registers.

Reset signal generation clears these registers to 000000H.

Figure 23-5. Format of SAG Level Specification Registers for Voltage Channels 1 and 2 (SAGVAL1, SAGVAL2)

(a) SAGVAL1

Address: 107H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL1L	SAGVAL17	SAGVAL16	SAGVAL15	SAGVAL14	SAGVAL13	SAGVAL12	SAGVAL11	SAGVAL10

Address: 108H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL1M	SAGVAL115	SAGVAL114	SAGVAL113	SAGVAL112	SAGVAL111	SAGVAL110	SAGVAL19	SAGVAL18

Address: 109H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL1H	0	0	SAGVAL121	SAGVAL120	SAGVAL119	SAGVAL118	SAGVAL117	SAGVAL116

(b) SAGVAL2

Address: 10BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL2L	SAGVAL27	SAGVAL26	SAGVAL25	SAGVAL24	SAGVAL23	SAGVAL22	SAGVAL21	SAGVAL20

Address: 10CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL2M	SAGVAL215	SAGVAL214	SAGVAL213	SAGVAL212	SAGVAL211	SAGVAL210	SAGVAL29	SAGVAL28

Address: 10DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SAGVAL2H	0	0	SAGVAL221	SAGVAL220	SAGVAL219	SAGVAL218	SAGVAL217	SAGVAL216

SAGVALn21 to n0	Specify voltage level of SAG detection for voltage channel n (n = 1, 2)
000000H to 3FFFFFH	Voltage level of SAG detection

Cautions 1. Be sure to clear bits 6 and 7 of the SAGVAL1H and SAGVAL2H to 0.

2. When CHMD (bit 5 of ADM2) = 0, SAGVAL2 cannot be written. The read value is the reset value.

(5) Peak current level specification register (IPKLMT)

IPKLMT register is used to set the current level of the peak detection for current channel 1.

IPKLMT is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to FFFFH.

Figure 23-6. Format of Peak Current Level Specification Register (IPKLMT)

Address: 10EH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IPKLMTL	IPKLMT7	IPKLMT6	IPKLMT5	IPKLMT4	IPKLMT3	IPKLMT2	IPKLMT1	IPKLMT0

Address: 10FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IPKLMTH	IPKLMT15	IPKLMT14	IPKLMT13	IPKLMT12	IPKLMT11	IPKLMT10	IPKLMT9	IPKLMT8

IPKLMT15 to 0	Specify peak detection current level for current channel 1
0000H to FFFFH	Current level of peak detection

(6) Peak voltage level specification register (VPKLMT)

VPKLMT register is used to set the voltage level of the peak detection for voltage channel 1.

VPKLMT is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to FFFFH.

Figure 23-7. Format of Peak Voltage Level Specification Register (VPKLMT)

Address: 110H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
VPKLMTL	VPKLMT7	VPKLMT6	VPKLMT5	VPKLMT4	VPKLMT3	VPKLMT2	VPKLMT1	VPKLMT0

Address: 111H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
VPKLMTH	VPKLMT15	VPKLMT14	VPKLMT13	VPKLMT12	VPKLMT11	VPKLMT10	VPKLMT9	VPKLMT8

VPKLMT15 to 0	Specify peak detection voltage level for voltage channel 1
0000H to FFFFH	Voltage level of peak detection

(7) Peak current value register (IMAX)

When the absolute value of current channel 1 exceeds the current peak detection level, the detected peak value (an absolute value) is stored in this register. This register value is not cleared after being read.

IMAX is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 23-8. Format of Peak Current Value Register (IMAX)

Address: 112H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
IMAXL	IMAX7	IMAX6	IMAX5	IMAX4	IMAX3	IMAX2	IMAX1	IMAX0

Address: 113H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
IMAXM	IMAX15	IMAX14	IMAX13	IMAX12	IMAX11	IMAX10	IMAX9	IMAX8

Address: 114H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
IMAXH	0	0	IMAX21	IMAX20	IMAX19	IMAX18	IMAX17	IMAX16

IMAX21 to 0	Store the detected peak current value (an absolute value)
000000H to 3FFFFFH	Peak current value (not cleared after reading)

(8) Peak current value clearing register (RSTIMAX)

When the absolute value of current channel 1 exceeds the current peak detection level, the detected peak value (an absolute value) is stored in this register. This register value is cleared after being read.

RSTIMAX is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 23-9. Format of Peak Current Value Clearing Register (RSTIMAX)

Address: 116H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTIMAXL	RSTIMAX7	RSTIMAX6	RSTIMAX5	RSTIMAX4	RSTIMAX3	RSTIMAX2	RSTIMAX1	RSTIMAX0

Address: 117H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTIMAXM	RSTIMAX15	RSTIMAX14	RSTIMAX13	RSTIMAX12	RSTIMAX11	RSTIMAX10	RSTIMAX9	RSTIMAX8

Address: 118H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTIMAXH	0	0	RSTIMAX21	RSTIMAX20	RSTIMAX19	RSTIMAX18	RSTIMAX17	RSTIMAX16

RSTIMAX21 to 0	Store the detected peak current value (an absolute value)
000000H to 3FFFFFH	Peak current value (cleared after reading)

(9) Peak voltage value register (VMAX)

When the absolute value of voltage channel 1 exceeds the current peak detection level, the detected peak value (an absolute value) is stored in this register. This register value is not cleared after being read.

VMAX is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 23-10. Format of Peak Voltage Value Register (VMAX)

Address: 119H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VMAXL	VMAX7	VMAX6	VMAX5	VMAX4	VMAX3	VMAX2	VMAX1	VMAX0

Address: 11AH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VMAXM	VMAX15	VMAX14	VMAX13	VMAX12	VMAX11	VMAX10	VMAX9	VMAX8

Address: 11BH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VMAXH	0	0	VMAX21	VMAX20	VMAX19	VMAX18	VMAX17	VMAX16

VMAX21 to 0	Store the detected peak voltage value (an absolute value)
000000H to 3FFFFFH	Peak voltage value (not cleared after reading)

(10) Peak voltage value clearing register (RSTVMAX)

When the absolute value of voltage channel 1 exceeds the current peak detection level, the detected peak value (an absolute value) is stored in this register. This register value is cleared after being read.

RSTVMAX is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 000000H.

Figure 23-11. Format of Peak Voltage Value Clearing Register (RSTVMAX)

Address: 11DH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTVMAXL	RSTVMAX7	RSTVMAX6	RSTVMAX5	RSTVMAX4	RSTVMAX3	RSTVMAX2	RSTVMAX1	RSTVMAX0

Address: 11EH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTVMAXM	RSTVMAX15	RSTVMAX14	RSTVMAX13	RSTVMAX12	RSTVMAX11	RSTVMAX10	RSTVMAX9	RSTVMAX8

Address: 11FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
RSTVMAXH	0	0	RSTVMAX21	RSTVMAX20	RSTVMAX19	RSTVMAX18	RSTVMAX17	RSTVMAX16

RSTVMAX21 to 0	Store the detected peak voltage value (an absolute value)
000000H to 3FFFFFH	Peak voltage value (cleared after reading)

(11) Gain specification register (IMATGAIN)

The IMATGAIN register is used to set the gain value of current channel 2.

IMATGAIN is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 0000H.

Figure 23-12. Format of Gain Specification Register (IMATGAIN)

Address: 120H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IMATGAINL	IMATGAIN7	IMATGAIN6	IMATGAIN5	IMATGAIN4	IMATGAIN3	IMATGAIN2	IMATGAIN1	IMATGAIN0

Address: 121H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
IMATGAINH	0	0	0	0	IMATGAIN11	IMATGAIN10	IMATGAIN9	IMATGAIN8

IMATGAIN11 to 0	Specify the gain value of current channel 2
0000H to 0FFFH	Gain value

Cautions 1. Be sure to clear bit 4 to 7 of the IMATGAINH to 0.

2. When CHMD (bit 5 of ADM2) = 1, IMATGAIN cannot be written. The read value is the reset value.

(12) Fault detection control register (PQMCTL)

This register controls current channel selection, fault interrupt settings, switching between period and frequency measurement, and zero-crossing detection.

PQMCTL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 23-13. Format of Fault Detection Control Register (PQMCTL)

Address: 122H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PQMCTL	ISELFLG	FAULTSIGN	SELICH1	SELICH0	ZX1EN	ZX2EN	FREQSEL	DISZXLPF0

ISELFLG	Active current channel during power measurement
0	Current channel 1
1	Current channel 2

FAULTSIGN	Specify the trigger for the fault detection interrupt (INTFAULTSIGN)
0	Triggers an interrupt when switching from the normal mode to the fault mode.
1	Triggers an interrupt when switching from the fault mode to the normal mode.

SELICH1	SELICH0	Specify the current channel used for power measurement
0	0	Automatically selects the current channel according to the fault status.
0	1	Selects current channel 1[Note] .
1	0	Selects current channel 2[Note] .
1	1	Automatically selects the current channel according to the fault status.

Note This setting is prohibited in the three-wire mode (CHMD = 1).

ZX1EN	Control zero-crossing output 1
0	Disables output of the zero-crossing 1 signal.
1	Enables output of the zero-crossing 1 signal.

ZX2EN	Control zero-crossing output 2
0	Disables output of the zero-crossing 2 signal.
1	Enables output of the zero-crossing 2 signal.

FREQSEL	Select period or frequency measurement
0	Stores the result of measuring the period in the PFVAL register.
1	Stores the result of measuring the frequency in the PFVAL register.

DISZXLPF0	Set up the low-pass filter used during zero-crossing detection
0	Enables the low-pass filter and outputs the zero-crossing signal ZX from LPF0.
1	Disables the low-pass filter and outputs the zero-crossing signal ZX from the ΔΣ-type A/D converter.

(13) Fault detection threshold value specification register (IST)

The IST register is used to set the threshold value of fault detection.

IST is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 8BH.

Figure 23-14. Format of Fault Detection Threshold Value Specification Register (IST)

Address: 123H After reset: 8BH R/W

Symbol	7	6	5	4	3	2	1	0
IST	IST7	IST6	IST5	IST4	IST3	IST2	IST1	IST0

IST7 to 0 (00H to FFH)	Specify the fault detection threshold value (% fs)
01H	0.00 %
8BH	0.30 % (default)
FFH	0.55 %

The IST adjustment range is 0.00216% fs/LSB.

For example, if 0.3% of the full-scale value is specified for the threshold value, IST is calculated as follows:

- IST = 0.3/0.00216 = 8BH

If the ICHKEN bit of the ICHK register is set to 1 and the current signal is larger than the IST value, a fault can be detected. If the current signal does not reach the threshold value specified for IST, fault detection is automatically disabled.

(14) Fault control register (ICHK)

This register is used to control fault detection and specify detection conditions.

ICHK is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 84H.

Figure 23-15. Format of Fault Control Register (ICHK)

Address: 124H After reset: 84H R/W

Symbol	7	6	5	4	3	2	1	0
ICHK	ICHKEN	0	0	0	ICHK3	ICHK2	ICHK1	ICHK0

ICHKEN[Note]	Control current fault detection
0	Disables current fault check
1	Enables current fault check

ICHK3	ICHK2	ICHK1	ICHK0	Current difference threshold value
1	x	x	x	Current difference threshold value = 1/8
0	1	x	x	Current difference threshold value = 1/16 (default)
0	0	1	x	Current difference threshold value = 1/32
0	0	0	1	Current difference threshold value = 1/64
0	0	0	0	Current difference threshold value = 1/16

Caution Be sure to clear bits 4 to 6 to 0.

Note The fault detection operation depends on the settings for the ICHK and IST registers as follows.

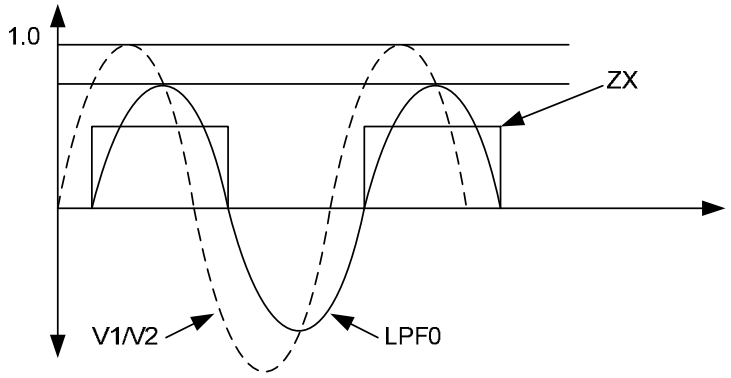
ICHIKEN	IST	ICHK3 to 0	Larger of Two Current Channel Values	Difference in Current Between Two Current Channels	Fault Detection Operation
0	x	xxxx	x	x	Fault detection unavailable
1	IST	xxxx	≤ IST	x	Fault detection unavailable
		1xxx	> IST	≤ 1/8	Normal status
				> 1/8	Fault status detected
		01xx		≤ 1/16	Normal status
				> 1/16	Fault status detected
		001x		≤ 1/32	Normal status
				> 1/32	Fault status detected
		0001		≤ 1/64	Normal status
				> 1/64	Fault status detected
		0000		≤ 1/16	Normal status
				> 1/16	Fault status detected

23.4 Power Quality Measurement Circuit Function Details

(1) Zero-crossing detection

Zero crossings are detected on the voltage channel. The input voltage is filtered using a low-pass filter (LPF0), and then zero-crossings are detected.

Figure 23-16. Zero-Crossing Detection Timing



The zero-crossing signal ZXn is output from LPF0 regardless of whether it is bypassed. LPF0 is a single-pole 68 Hz filter. Therefore, there is a phase delay of approximately 1.9 ms (at 50 Hz) between the LPF0 input and output. Similarly, there is a phase delay of approximately 1.1 ms (at 50 Hz) between the analog input and A/D converter output for the software block (the digital filter) of the ΔΣ-type A/D converter. Due to the phase delay of LPF0 and the A/D converter, there is a delay of approximately 1.1 ms (when bypassing LPF0) or 3.02 ms (when using LPF0) between the analog input and output of the zero-crossing signal ZXn on the voltage channel.

Table 23-3. Zero-Crossing Detection Delay Time

	Condition (at 50 Hz)	
	When Bypassing LPF0	When Using LPF0
Delay between the analog input and output of the zero-crossing signal ZXn on the voltage channel	1.1 ms	3.02 ms

Remark n = 1, 2

(2) Zero-crossing timeout

The zero-crossing timeout function generates an interrupt if no zero-crossing is detected for a fixed period of time. The zero-crossing timeout function can be used separately for the V1 and V2 channels.

When a zero crossing is detected by the zero-crossing detection circuit, the value of the ZXOUTn register is read to an internal counter. The counter value is decremented for each sampling clock (fs). If the counter value reaches 0 before the next zero crossing is detected, a zero-crossing timeout interrupt (INTZXTOn) occurs. Note that the default value of the ZXOUTn register is 3FFH, and up to 0.23 s can be counted.

Figure 23-17. Timing of Zero-crossing Timeout Interrupt (INTZXTOn)

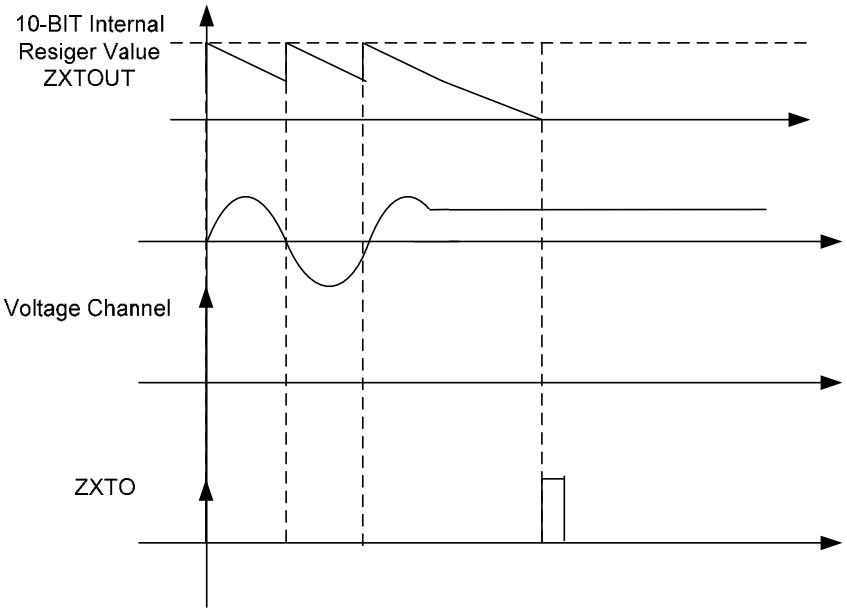
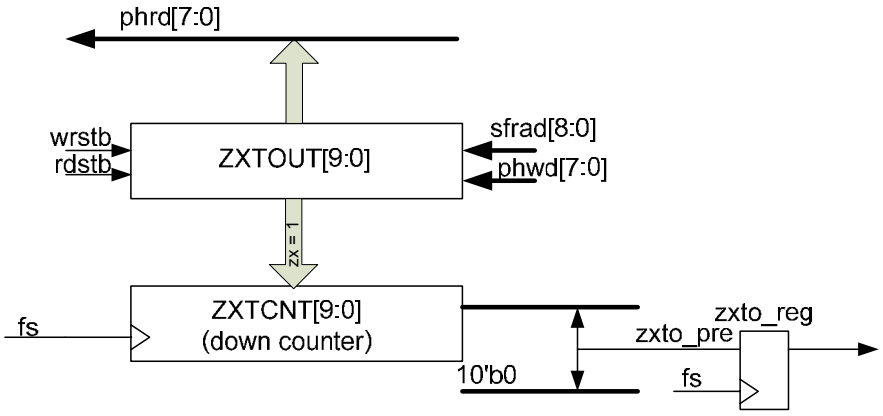


Figure 23-18. Internal Counter of ZXOUTn Register



Remark n = 1, 2

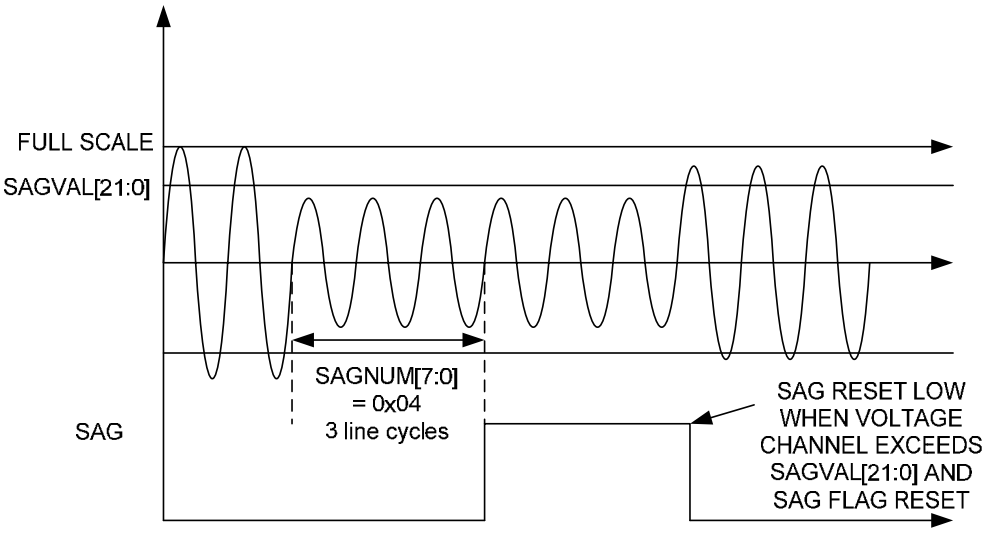
(3) SAG detection function

This function detects input voltage SAG. SAG can be detected separately for the V1 and V2 input voltages.

If the absolute value of the input voltage (23 bits) is less than or equal to the voltage value specified by the SAGVALn register for the duration specified by the SAGNUMn register, a SAG interrupt signal (INTSAGn) is generated.

The SAGNUMn register has an 8-bit format, and up to 255 line cycles can be specified for it. Note that the SAGVALn register has a 22-bit format.

Figure 23-19. Timing of SAG detection



Remark n = 1, 2

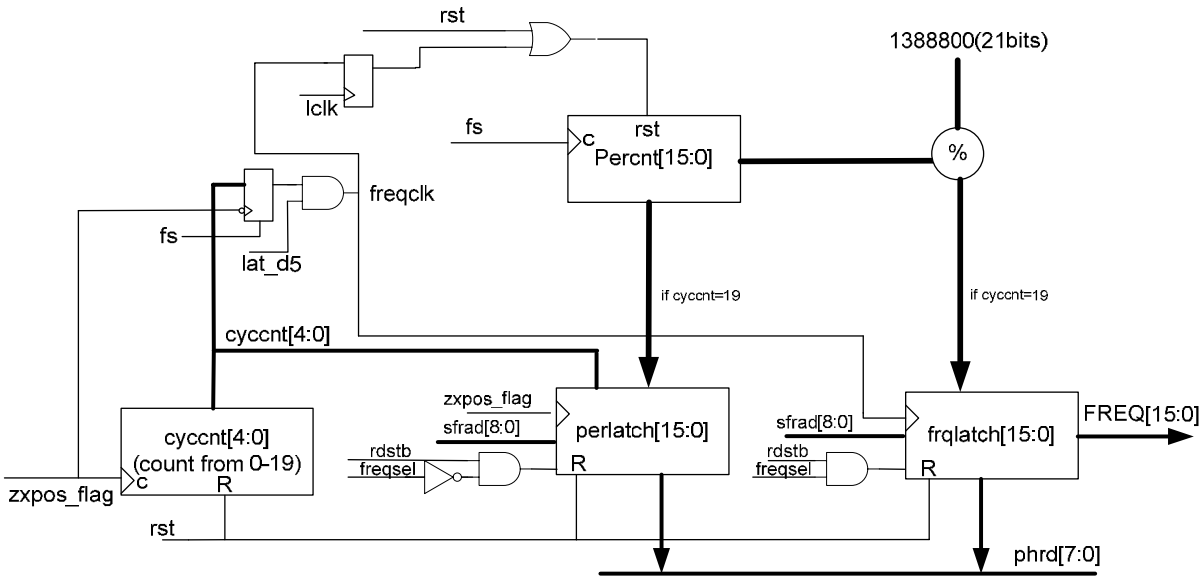
(4) Period and frequency measurement

The line cycle and frequency of the voltage channel (V1) can be measured. The PQMCTL register is used to specify whether to measure the line cycle or frequency. This measurement is performed for 20 line cycles at a time.

During cycle measurement, the fs (4.34 kHz) clock is used to count for 20 line cycles. Therefore, 11.5 μs/LSB (0.07% precision) is used. If the line frequency is 60 Hz, the counter value is 1,447.

During frequency measurement, the counter value is used to perform a calculation for 20 line cycles. If the line frequency is 60 Hz, the precision is 0.0625 Hz/LSB, and the calculation result is 960.

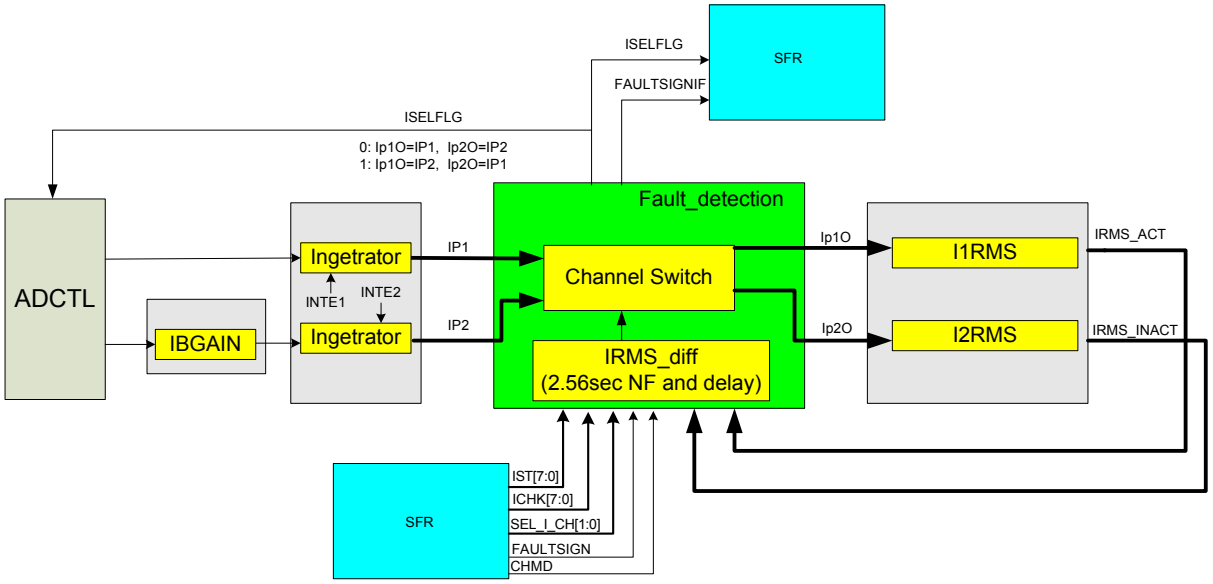
Figure 23-20. Period and Frequency Measurement circuit



(5) Fault detection

Fault detection can be performed only in the single-phase two-wire mode. By connecting I1 to the line side and I2 to the neutral side, two lines are used to detect the current. The fault detection circuit is positioned before the power calculation circuit.

Figure 23-21. Fault detector

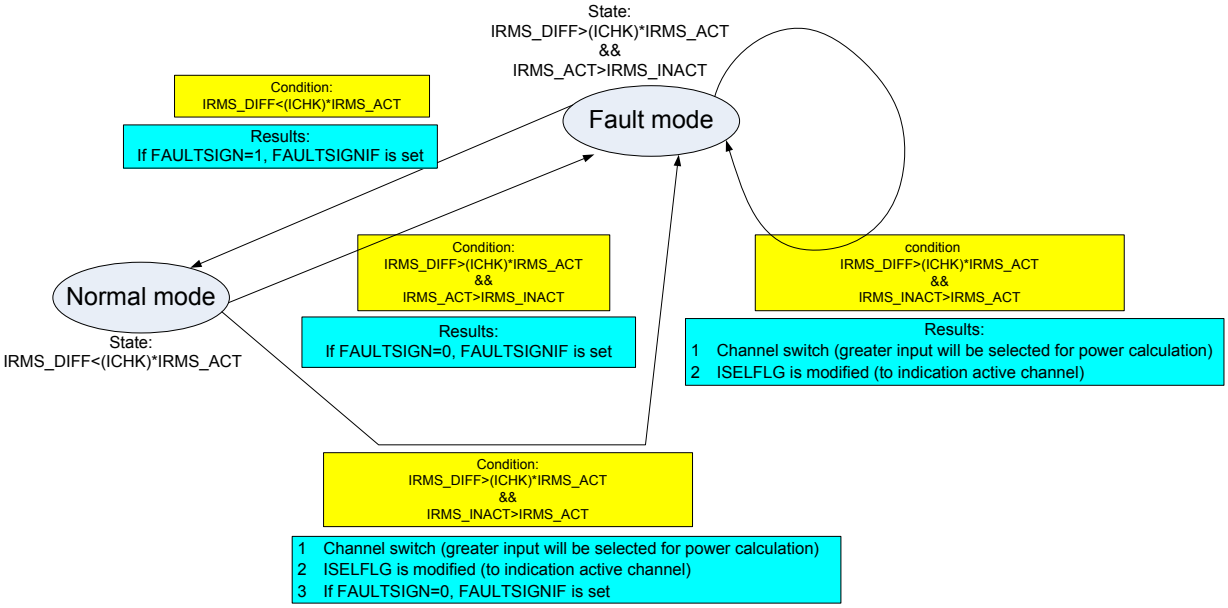


If the difference in current between Ip1 and Ip2 is greater than the multiple (1/8, 1/16, 1/32, or 1/64) specified for the active channel, a fault is detected. If a fault condition is detected and the current value for the inactive channel is larger than that for the active channel, the channels are switched, and the channel that has the larger current value automatically becomes the active channel. The active channel can be checked using the ISELFLG bit of the PQMCTL register. If this bit is 0, Ip1 channel is selected as the active channel, and, if the bit is 1, Ip2 channel is selected. This bit is automatically updated when the channel is switched.

The active channel can also be specified by using the SELICH1 and SELICH0 bits (a two-bit format) of the PQMCTL register. If both bits are set to either 0 or 1, the active channel is switched according to fault detection.

The following figure shows the transitions between the normal mode and fault mode.

Figure 23-22. Transitions Between the Normal Mode and Fault Mode



Remark IRMS_ACT: RMS value of the current channel used for power measurement
IRMS_INACT: RMS value of the current channel not used for power measurement
IRMS_DIFF: ABS (IRMS_ACT-IRMS_INACT)
IST: Fault detection threshold value
ICHK: Current difference threshold value
FAULTSIGN: Bit for specifying the fault interrupt trigger
FAULTSIGNIF: Fault mode change interrupt flag

Note that fault detection is automatically disabled for values less than the value specified by the IST register. This is to avoid misdetection for small amounts of current.

Because the difference between the Ip1 and Ip2 current signals is detected, the current value for the two channels must be corrected in advance. To perform this correction, the correction value must be specified for the IMATGAIN register. For details, see **(7) Current channel gain correction**.

To avoid incorrect power measurement when a fault event occurs, the input current is always monitored.
After a reset, the active channel is set to Ip1 by default, and this channel is used to calculate the active power, reactive power, and apparent power.

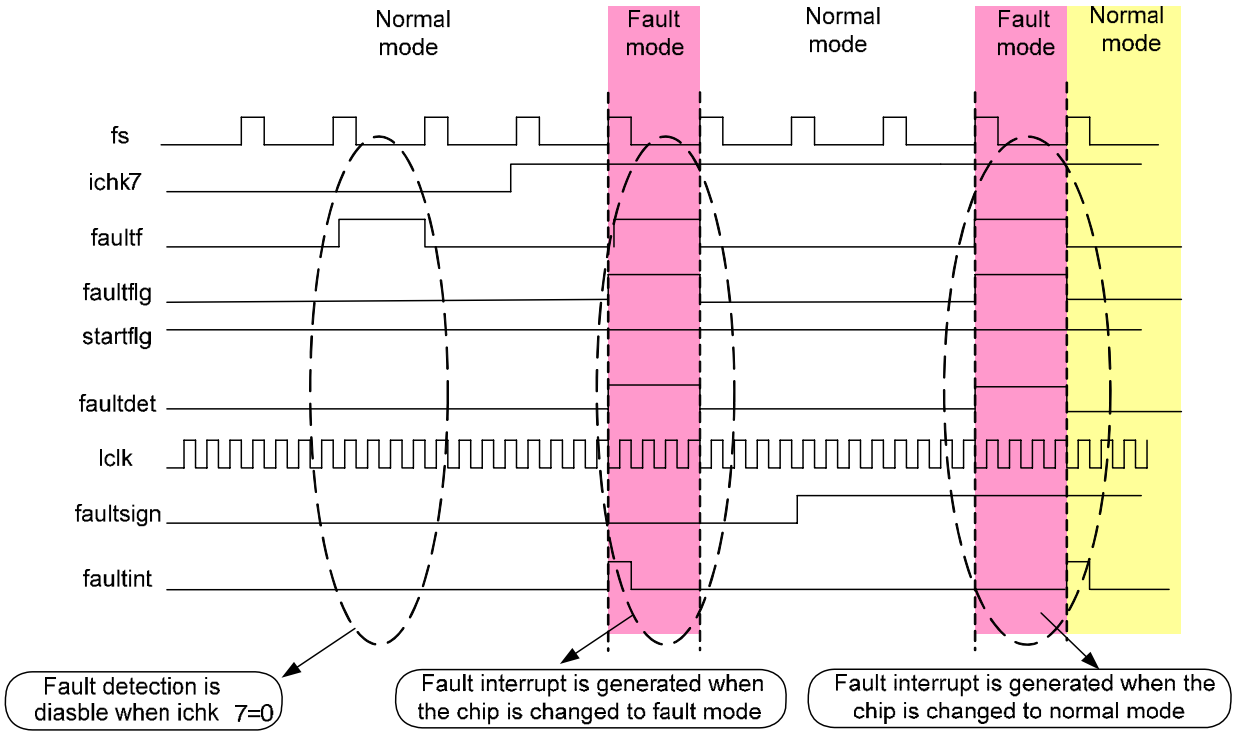
Remarks 1. To guarantee fault detection accuracy, it is recommended to set ZXRMS (bit 6 of the NLCTL register) to 1 if the fault detection current difference restriction is set to 1/64 or 1/32 (by using bits 3 to 0 of the ICHK register).

2. Fault detection is disabled in the single-phase three-wire mode (CHMD = 1).

If the FAULTSIGN bit of the PQMCTL register is cleared to 0, an interrupt occurs when a fault condition is detected (when the system transitions from the normal status to the fault status). If 1 is specified, an interrupt occurs when the system returns from the fault status (when the system transitions from the fault status to the normal status).

The fault interrupt and channel switching signals are passed through a filter to avoid misdetection. Therefore, there is a delay of approximately three seconds when a fault event occurs.

Figure 23-23. Fault Interrupt Timing



(6) Peak detection

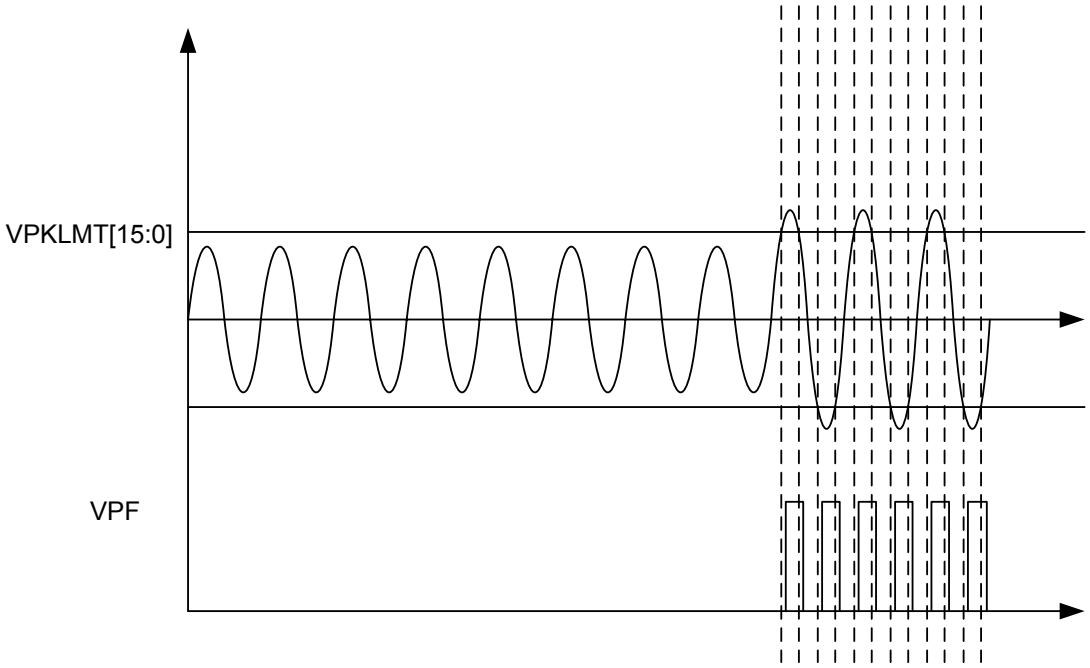
If the absolute value of the higher 16 bits of the voltage channel exceeds the peak voltage value (the VPKLMT register value), an INTPKV1 interrupt occurs.

If the absolute value of the higher 16 bits of the current channel exceeds the peak current value (the IPKLMT register value), an INTPKI1 interrupt occurs.

The maximum absolute value of the voltage channel is saved in the internal VMAX register, and the value can be read from the VMAX register in the extended SFR space. If the RSTVMAX register is used to read this value, the register value is cleared to 0 after being read.

The maximum absolute value of the current channel is saved in the internal IMAX register, and the value can be read from the IMAX register in the extended SFR space. If the RSTIMAX register is used to read this value, the register value is cleared to 0 after being read.

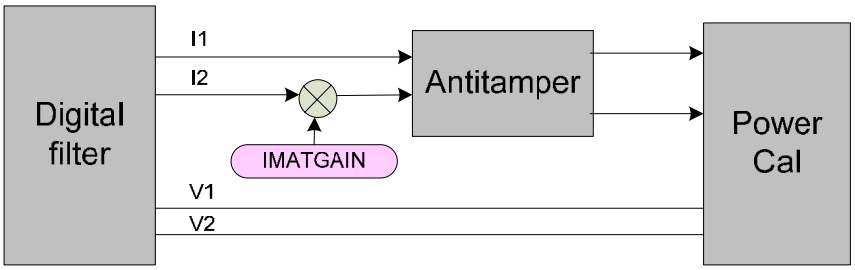
Figure 23-24. Peak Detection Timing



(7) Current channel gain correction

To detect faults, a comparison is made using the difference between current I1 and current I2. Therefore, current I1 and current I2 must be adjusted to the same amount of current in advance. The current gain correction circuit performs correction by adding gain to input current value I2.

Figure 23-25. Current Gain Correction Circuit



$$output\_IMATGAIN = input\_IMATGAIN \times (1 + \frac{IMATGAIN}{2^{12}})$$

IMATGAIN is a 12-bit signed integer register. The gain resolution for this register is 0.0244% LSB (2^{-12} = 0.0244%).

23.5 Notes on Power Quality Measurement Circuit

The registers for the power quality measurement circuit are allocated to the extended SFR space, and some of them contain 2 bytes or more. When reading from a register that contains 2 bytes or more, be sure to read the entire register and read the lower bytes first. Similarly, when writing to a register that contains 2 bytes or more, be sure to write to the entire register and write the lower bytes first. Reading and writing are not possible using other methods.

The target 2-byte registers are as follows.

Table 23-4. 2-byte Register List

Name	R/W	Read Buffer	Write Buffer
Period and frequency measurement result register (PFVAL)	R	Y	–
Zero-crossing timeout specification registers for voltage channel 1 (ZXTOUT1)	R/W	–	Y
Zero-crossing timeout specification registers for voltage channel 2 (ZXTOUT2)	R/W	–	Y
SAG level specification registers for voltage channel 1 (SAGVAL1)	R/W	–	Y
SAG level specification registers for voltage channel 2 (SAGVAL2)	R/W	–	Y
Peak current level specification register (IPKLMT)	R/W	–	Y
Peak voltage level specification register (VPKLMT)	R/W	–	Y
Peak current value register (IMAX)	R	Y	–
Peak current value clearing register (RSTIMAX)	R	Y	–
Peak voltage value register (VMAX)	R	Y	–
Peak voltage value clearing register (RSTVMAX)	R	Y	–
Gain specification register (IMATGAIN)	R/W	–	Y

CHAPTER 24 DIGITAL FREQUENCY CONVERSION CIRCUIT

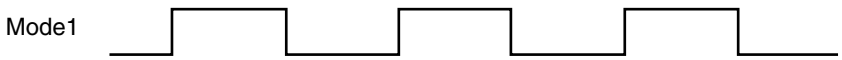
24.1 Digital Frequency Conversion Circuit Functions

The digital frequency conversion circuit integrates the measured active power, reactive power, and apparent power/average current (an RMS value), and then outputs the result as a pulse. There are two types of output pulse waveforms, and the frequency can be programmed by manipulating the CFMUL register.

(1) Mode 1

<R> Output in the range from 0 to 135 Hz is possible.
A waveform that has a pulse duty ratio of 50:50 is output.
However, if the cycle exceeds 180 ms, the high-level width is fixed to 90 ms.

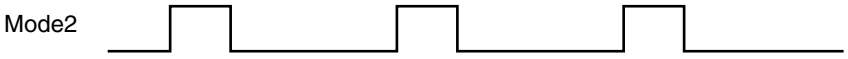
Figure 24-1. Output Pulse Waveform (Mode 1)



(2) Mode 2

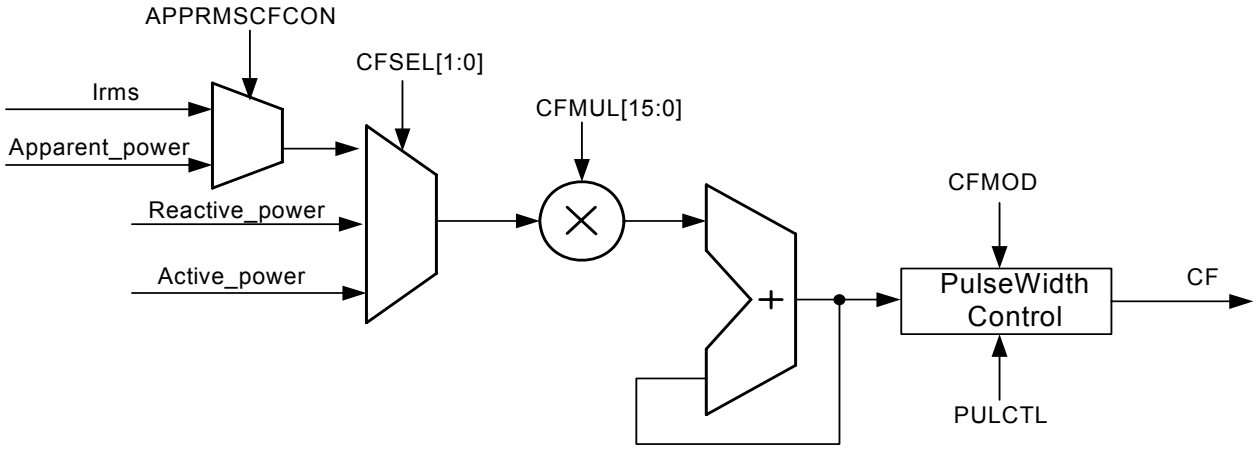
<R> Output in the range from 0 to 1,085 Hz is possible.
A pulse waveform that has a fixed high-level width is output. The high-level width can be specified for the PULCTL register as 30, 60, 90, or 180 μs.
This mode is mainly used in Japan.

Figure 24-2. Output Pulse Waveform (Mode 2)



24.2 Configuration of Digital Frequency Conversion Circuit

Figure 24-3. Block Diagram of Digital Frequency Conversion Circuit



24.3 Registers Controlling Digital Frequency Conversion Circuit

The power quality measurement circuit is controlled by the following three types of registers.
These registers are all allocated to the extended SFR space.
For details about how to access the extended SFR space, see **CHAPTER 17 EXTENDED SFR INTERFACE**.

- Frequency conversion control register (CFCTL)
- Frequency scaling specification register (CFMULL, CFMULH)
- Pulse width specification register (PULCTL)

(1) Frequency conversion control register (CFCTL)

This register is used to control CF pulse output and select the output mode.
CFCTL is allocated to the extended SFR space.
Use the extended SFR interface to set up this register.
Reset signal generation clears this register to 02H.

Figure 24-4. Format of Frequency Conversion Control Register (CFCTL)

Address: 150H After reset: 02H R/W

Symbol	7	6	5	4	3	2	1	0
CFCTL	0	0	0	0	CFSEL1	CFSEL0	DISCF	CFMOD

CFSEL1	CFSEL0	Select the CF pulse output (by selecting active power, reactive power, or apparent power/average current)
0	0	Outputs the active power as a CF pulse.
0	1	Outputs the reactive power as a CF pulse.
1	x	Outputs the apparent power/average current as a CF pulse.

DISCF	Enable or disable CF output
0	Enables CF output (A pulse is output from the CF pin).
1	Disables CF output (No pulse is output from the CF pin).

CFMOD	Select the CF output mode
0	Outputs the mode 1 waveform (which has a duty ratio of 50%)[Note].
1	Outputs the mode 2 waveform (which has a fixed high-level width).

Note If the output cycle exceeds 180 ms, the high-level width is fixed to 90 ms.

Caution Before specifying the power-saving mode, the source for the digital frequency conversion circuit must be checked or changed to ensure that the source of the digital frequency conversion circuit is not delivered by the corresponding channel. For example, before ACTDIS is set, "00" is prohibited for [CFSEL1, CFSEL0] (When "00" is specified, active power is selected for the source of the digital frequency conversion circuit).

(2) Frequency scaling specification register (CFMUL)

This register is used to specify the frequency scaling value.

CFMUL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to FFH.

Figure 24-5. Format of Frequency Scaling Specification Register (CFMUL)

Address: 151H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
CFMULL	CFMUL7	CFMUL6	CFMUL5	CFMUL4	CFMUL3	CFMUL2	CFMUL1	CFMUL0

Address: 152H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
CFMULH	CFMUL15	CFMUL14	CFMUL13	CFMUL12	CFMUL11	CFMUL10	CFMUL9	CFMUL8

CFMUL15 to 0	Specify the CF output pulse width
0000H to FFFFH	Specifies the scaling value for the CF output pulse.

Cautions 1. Only change the value specified for the CFMUL register while DISCF = 1.

2. Specifying 0000H for the CFMUL register is prohibited. If 0000H is specified, it is handled as FFFFH.

(3) Pulse width specification register (PULCTL)

This register is used to specify the high-level width of the pulse used during mode 2 operation.

PULCTL is allocated to the extended SFR space.

Use the extended SFR interface to set up this register.

Reset signal generation clears this register to 00H.

Figure 24-6. Format of Pulse Width Specification Register (PULCTL)

Address: 153H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PULCTL	0	0	0	0	0	0	PULCTL1	PULCTL0

PULCTL1	PULCTL0	Specify the high-level width of the pulse (at mode 2 operation)
0	0	30 μs
0	1	90 μs
1	0	60 μs
1	1	180 μs

Caution Only change the value specified for the PULCTL register while DISCF = 1.

24.4 Digital Frequency Conversion Circuit Functions

The digital frequency conversion circuit converts the measured power value to a pulse waveform. The circuit adds and accumulates power values calculated by the power calculation unit and outputs a pulse when the threshold value is exceeded.

Figure 24-7. Pulse Output (Mode 1)

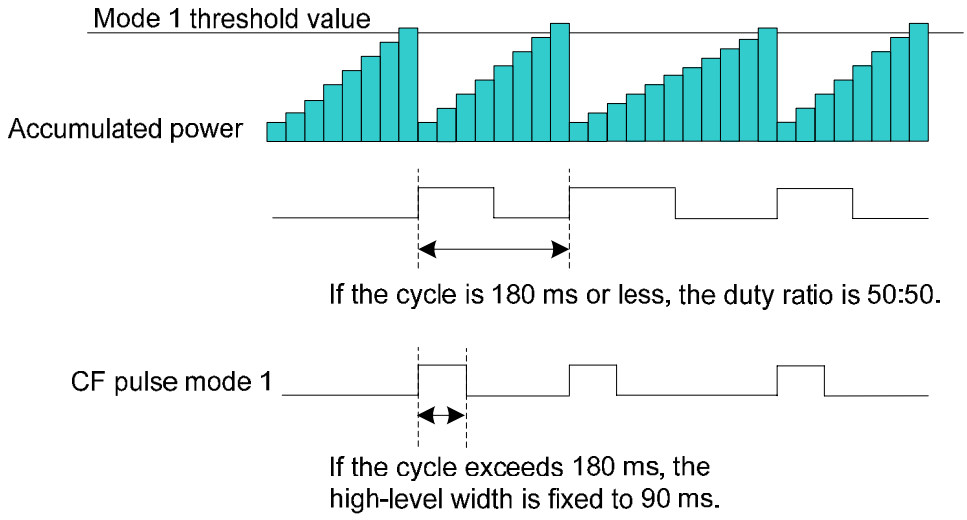
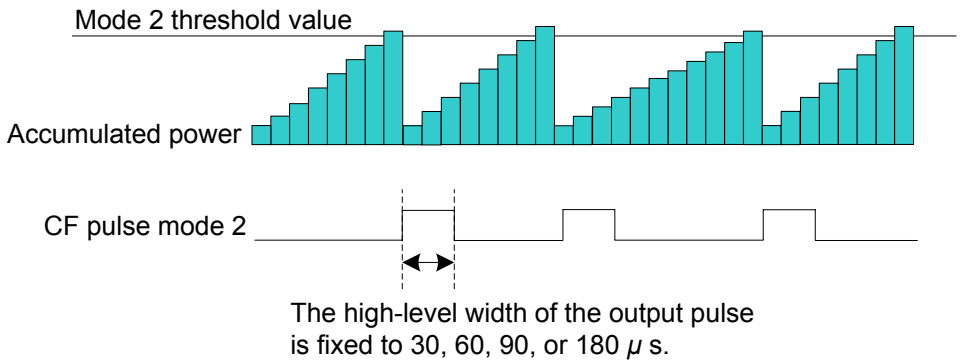


Figure 24-8. Pulse Output (Mode 2)



Cautions 1. In mode 1, if the cycle exceeds 180 ms, the high-level width is fixed to 90 ms.

2. For the same input voltage, the CF pulse frequency of mode 2 is eight times that of mode 1.

The power value for each sample is scaled and input to an accumulator. If the value in the accumulator exceeds the fixed threshold value, an overflow flag is set, and one pulse is output to the CF pin each time an overflow occurs. The threshold value for the accumulator is fixed, and the timing at which overflows occur can be adjusted by scaling the input power value to the value specified by the CFMUL register. A scaling value in the range from 1/(2^16) to (2^16-1)/(2^16) can be specified, in 1/(2^16) steps.

If the CFMUL register is set to 1, the input power value is scaled to 1/(2^16). If the CFMUL register is set to FFFFH, the input power value is scaled to (2^16-1)/(2^16).

(1) Input data selection method

The active power, reactive power, or apparent power/average current of the power calculation circuit can be selected as input to the digital frequency conversion circuit.

The CFSEL0 and CFSEL1 bits of the CFCTL register can be used to select which measurement result to output as a pulse. Only change these bits while the digital frequency conversion circuit is stopped (DISCF = 1).

(2) Value specified for the CFMUL register

The maximum value of CF output for full-scale input is 135.623 Hz (in mode 1) or 1084.984 Hz (in mode 2).

To obtain the rated CF frequency N Hz, the values specified for the CF frequency and CFMUL register have the following relationship.

(a) mode 1

CFMUL = 2^{16} x N / (135.623 x PowerRate)

(b) mode 2

CFMUL = 2^{16} x N / (1084.984 x PowerRate)

N : CF output frequency for rated input

PowerRate : Ratio of the rated power to the full-scale power

$$PowerRate = \frac{PowerGivenLoad}{PowerFullScale}$$

Remark When calculating PowerRate, use the same offset, gain, and scaling settings for the full-scale and rated input.

These settings can be specified using the following registers.

- Offset specification register : ACTnOS, REAnOS, InRMSOS, and VnRMSOS (n = 1, 2)
- Gain specification register : ACTnGAIN, REAnGAIN, APPnGAIN, and IRMSnGAIN (n = 1, 2)
- Scaling specification register : ACTDIV, READIV, and APPDIV

(3) CF output pulse

Two types of pulses can be output from CF pin. The pulse selection is set by using CFCTL register.

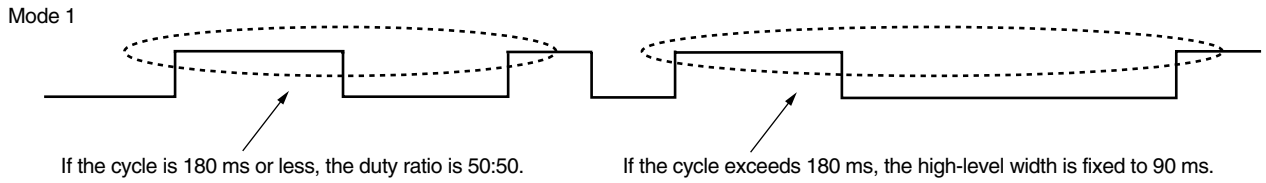
(a) Mode 1

<R> Output in the range from 0 to 135 Hz is possible.

A waveform that has a pulse duty ratio of 50:50 is output.

However, if the cycle exceeds 180 ms, the high-level width is fixed to 90 ms.

Figure 24-9. Waveform Output



(b) mode 2

<R> Output in the range from 0 to 1,085 Hz is possible.

A pulse waveform that has a fixed high-level width is output. The high-level width can be specified for the PULCTL register as 30, 60, 90, or 180 μs.

This mode is mainly used in Japan.

CHAPTER 25 STANDBY FUNCTION

25.1 Standby Function and Configuration

25.1.1 Standby function

The standby function is mounted onto all 78K0/Lx3-M microcontroller products.

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The subsystem clock oscillation cannot be stopped. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the 10-bit successive approximation type A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

The following sequence is recommended for operating current reduction of the 24-bit ΔΣ-type A/D converter when the standby function is used: First clear bit 7 (ADPON) and bit 6 (ADCE2) of the 24-bit ΔΣ-type A/D converter mode register (ADM2) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

25.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATOR**.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock or subsystem clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

Figure 25-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFA3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16

MOST11	MOST13	MOST14	MOST15	MOST16	Oscillation stabilization time status	
						fx = 10 MHz
1	0	0	0	0	2^{11}/fx min.	204.8 μs min.
1	1	0	0	0	2^{13}/fx min.	819.2 μs min.
1	1	1	0	0	2^{14}/fx min.	1.64 ms min.
1	1	1	1	0	2^{15}/fx min.	3.27 ms min.
1	1	1	1	1	2^{16}/fx min.	6.55 ms min.

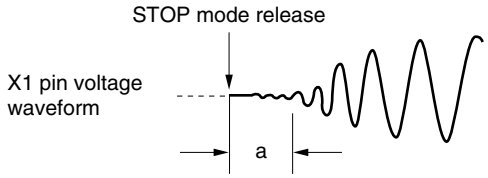
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

(2) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 25-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				fx = 10 MHz
0	0	1	2^{11}/fx	204.8 μs
0	1	0	2^{13}/fx	819.2 μs
0	1	1	2^{14}/fx	1.64 ms
1	0	0	2^{15}/fx	3.27 ms
1	0	1	2^{16}/fx	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

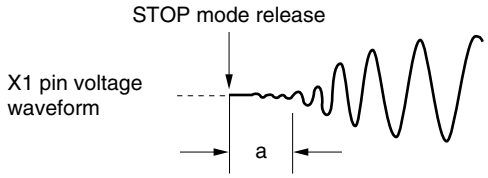
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

25.2 Standby Function Operation

25.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, internal high-speed oscillation clock, or subsystem clock. The operating statuses in the HALT mode are shown below.

Table 25-1. Operating Statuses in HALT Mode (1/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{RH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{RH}	Operation continues (cannot be stopped)	Status before HALT mode was set is retained	
		f_X	Status before HALT mode was set is retained	Operation continues (cannot be stopped)	Status before HALT mode was set is retained
		f_{EXCLK}	Operates or stops by external clock input		Operation continues (cannot be stopped)
	Subsystem clock	f_{XT}	Status before HALT mode was set is retained		
		f_{EXCLKS}			
	f_{RL}		Status before HALT mode was set is retained		
CPU			Operation stopped		
Flash memory			Operation stopped		
RAM			Status before HALT mode was set is retained		
Port (latch)			Status before HALT mode was set is retained		
16-bit timer/event counter 00			Operable		
8-bit timer/event counter		50			
		51			
		52			
8-bit timer		H0			
		H1			
		H2			
Real-time counter					
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
Buzzer output			Operable		
10-bit successive approximation type A/D converter					
24-bit ΔΣ-type A/D converter					
Serial interface		UART0			
		UART6			
		CSI10			
Extended SFR interface					
LCD controller/driver					
Remote controller transmitter					
Power calculation circuit					
Power quality measurement circuit					
Digital frequency conversion circuit					
Power-on-clear function					
Low-voltage detection function					
External interrupt					

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

Table 25-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXCLKS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{RH}	Status before HALT mode was set is retained	
		f_X		
		f_{EXCLK}	Operates or stops by external clock input	
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Status before HALT mode was set is retained
		f_{EXCLKS}	Operates or stops by external clock input	Operation continues (cannot be stopped)
	f_{RL}		Status before HALT mode was set is retained	
CPU			Operation stopped	
Flash memory			Operation stopped	
RAM			Status before HALT mode was set is retained	
Port (latch)			Status before HALT mode was set is retained	
16-bit timer/event counter 00Note			Operable	
8-bit timer/event counter		50Note		
		51Note		
		52		
8-bit timer		H0		
		H1		
		H2		
Real-time counter				
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.	
Buzzer output			Operable	
10-bit successive approximation type A/D converter			Operable. However, operation disabled when peripheral hardware clock (f_{PRS}) is stopped.	
24-bit ΔΣ-type A/D converter				
Serial interface	UART0		Operable	
	UART6			
	CSI10Note			
Extended SFR interface				
LCD controller/driver				
Remote controller transmitter				
Power calculation circuit			Operable. However, operation disabled when peripheral hardware clock (f_{PRS}) is stopped.	
Power quality measurement circuit				
Digital frequency conversion circuit				
Power-on-clear function			Operable	
Low-voltage detection function				
External interrupt				

Note When the CPU is operating on the subsystem clock and the internal high-speed oscillation clock high-speed system clock have been stopped, do not start operation of these functions on the external clock input from peripheral hardware pins.

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

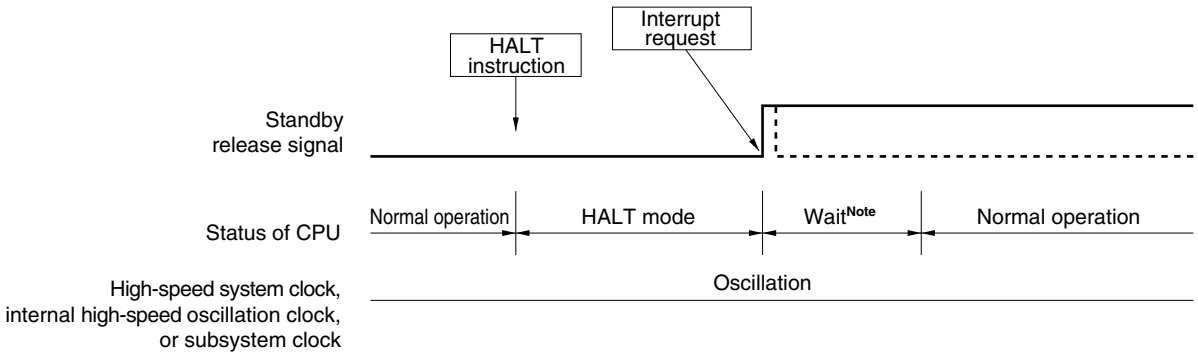
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 25-3. HALT Mode Release by Interrupt Request Generation



Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 10 or 11 clocks
- When vectored interrupt servicing is not carried out: 3 or 4 clocks

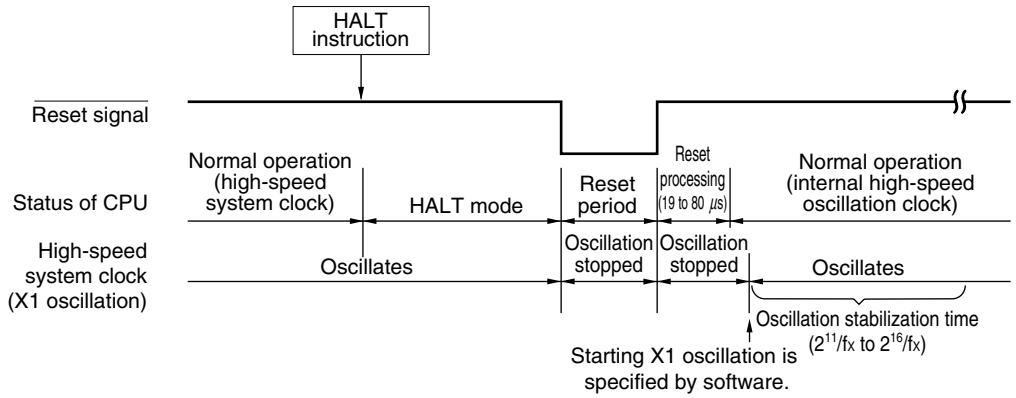
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

(b) Release by reset signal generation

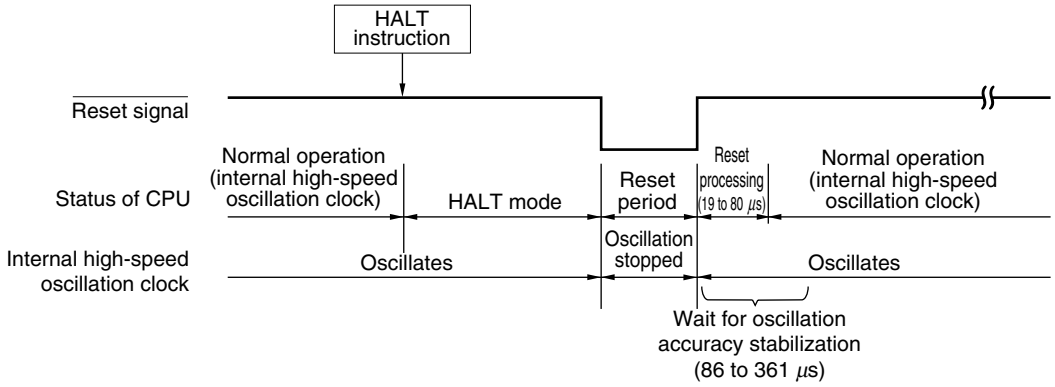
When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 25-4. HALT Mode Release by Reset

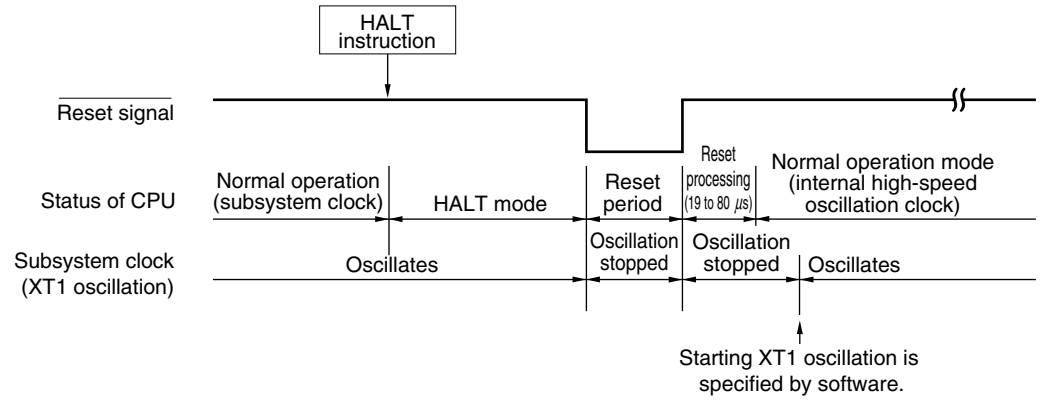
(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock is used as CPU clock



(3) When subsystem clock is used as CPU clock



Remark fx: X1 clock oscillation frequency

Table 25-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

25.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

Table 25-3. Operating Statuses in STOP Mode (1/2)

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{RH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{RH}	Stopped		
		f_X			
		f_{EXCLK}	Input invalid		
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXCLKS}			
	f_{RL}		Status before STOP mode was set is retained		
CPU			Operation stopped		
Flash memory			Operation stopped		
RAM			Status before STOP mode was set is retained		
Port (latch)			Status before STOP mode was set is retained		
16-bit timer/event counter 00			Operable only when subsystem clock is selected as the count clock		
8-bit timer/event counter		50Note	Operable only when TI50 is selected as the count clock		
		51Note	Operable only when TI51 is selected as the count clock		
		52	Operation stopped		
8-bit timer		H0	Operable only when TM50 output is selected as the count clock during 8-bit timer/event counter 50 operation		
		H1	Operable only when f_{RL}, $f_{RL}/2^7$, $f_{RL}/2^9$ is selected as the count clock		
		H2	Operation stopped		
Real-time counter			Operable		
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
Buzzer output			Operation stopped		
10-bit successive approximation type A/D converter					
24-bit ΔΣ-type A/D converter					
Serial interface	UART0		Operable only when TM50 output is selected as the serial clock during 8-bit timer/event counter 50 operation		
	UART6				
	CSI10Note		Operable only when external clock is selected as the serial clock		
Extended SFR interface			Operation stopped		
LCD controller/driver			Operable only when subsystem clock is selected as the count clock		
Remote controller transmitter			78K0/LE3-M: Operation stopped 78K0/LG3-M: In the following conditions, operable. In other conditions, operation stopped. • When operating 8-bit timer/event counter 50 • When TM50 output is selected as serial clock for UART0 • When TI50 is selected as count clock for TM50 • When f_{RL}, $f_{RL}/2^7$, and $f_{RL}/2^9$ is selected as the count clock for TMH1		

(**Note, Remarks,** and **Cautions** are listed on the next page.)

Table 25-3. Operating Statuses in STOP Mode (2/2)

STOP Mode Setting / Item	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
	When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{RH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
Power calculation circuit	Operation stopped		
Power quality measurement circuit			
Digital frequency conversion circuit			
Power-on-clear function	Operable		
Low-voltage detection function			
External interrupt			

Note Do not start operation of these functions on the external clock input from peripheral hardware pins in the stop mode.

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

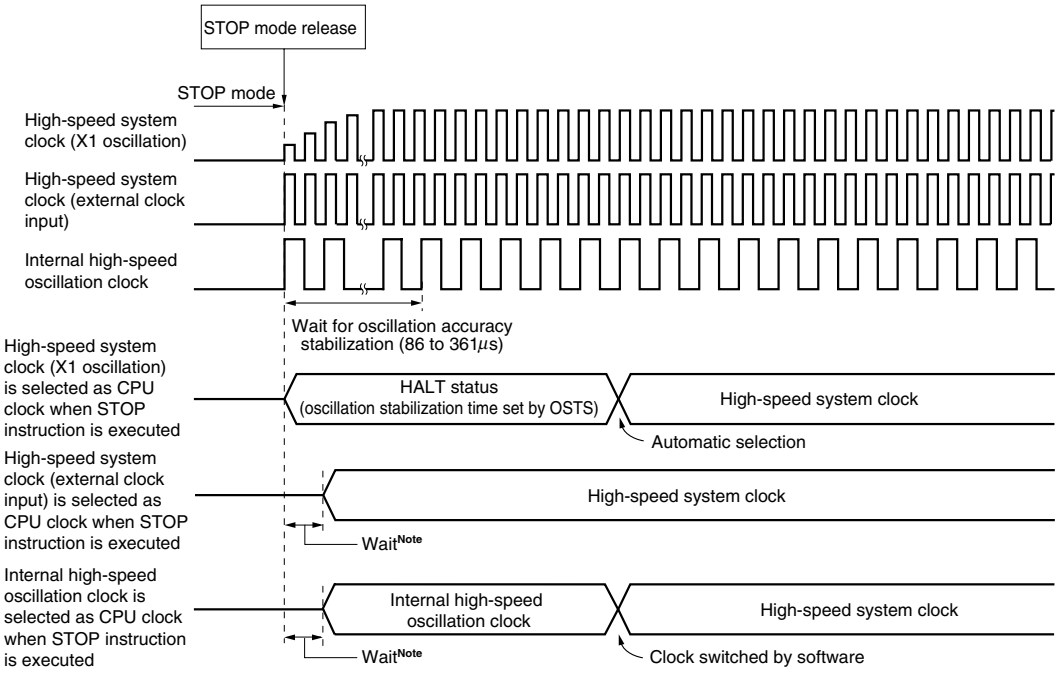
2. Even if "internal low-speed oscillator can be stopped by software" is selected by the option byte, the internal low-speed oscillation clock continues in the STOP mode in the status before the STOP mode is set. To stop the internal low-speed oscillator's oscillation in the STOP mode, stop it by software and then execute the STOP instruction.

3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction using the following procedure.
<1> Set RSTOP to 0 (starting oscillation of the internal high-speed oscillator) → <2> Set MCM0 to 0 (switching the CPU from X1 oscillation to internal high-speed oscillation) → <3> Check that MCS is 0 (checking the CPU clock) → <4> Check that RSTS is 1 (checking internal high-speed oscillation operation) → <5> Execute the STOP instruction
Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

4. Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

(2) STOP mode release

Figure 25-5. Operation Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated)



<R> **Note** The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

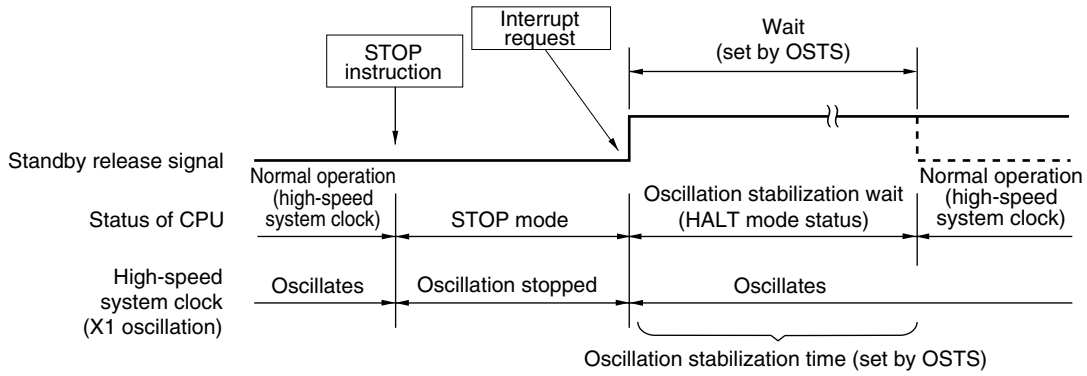
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

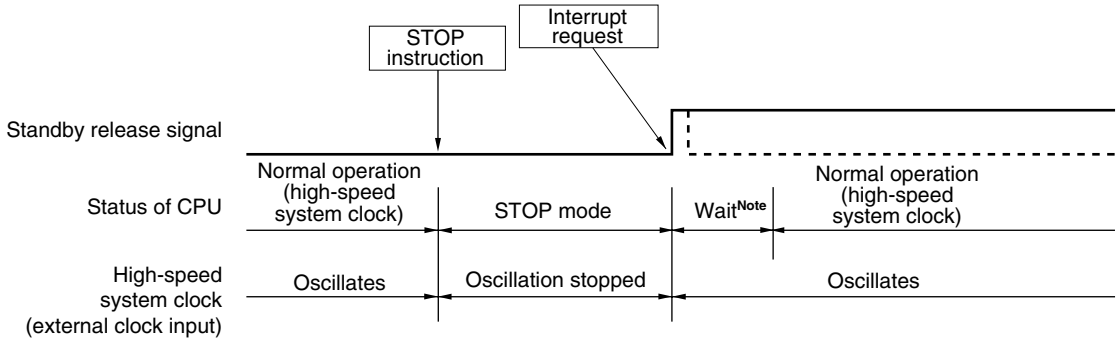
When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 25-6. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock



(2) When high-speed system clock (external clock input) is used as CPU clock



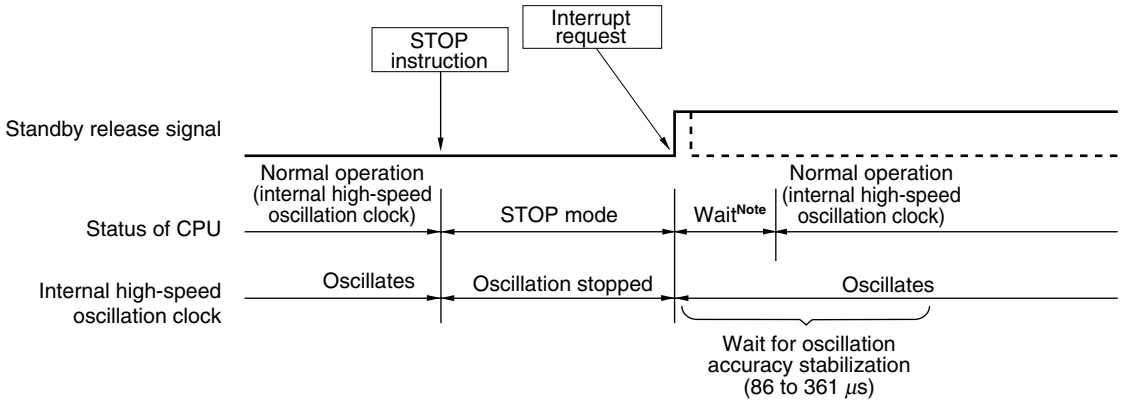
<R> **Note** The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 25-6. STOP Mode Release by Interrupt Request Generation (2/2)

(3) When internal high-speed oscillation clock is used as CPU clock



<R> **Note** The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

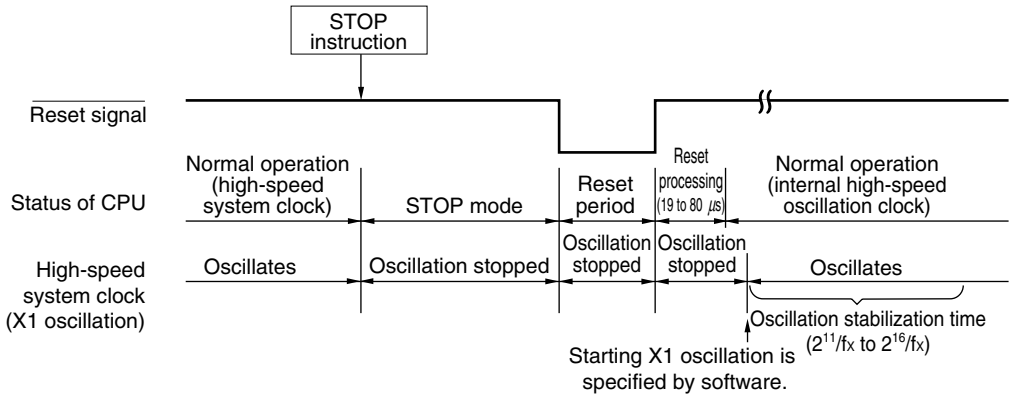
Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

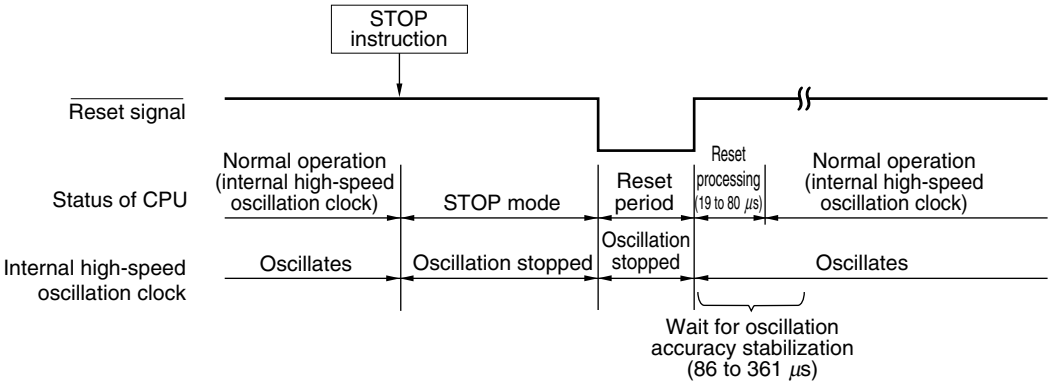
When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 25-7. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock is used as CPU clock



Remark fx: X1 clock oscillation frequency

Table 25-4. Operation in Response to Interrupt Request in STOP Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	STOP mode held
Reset	–	–	×	×	Reset processing

×: don't care

CHAPTER 26 RESET FUNCTION

The reset function is mounted onto all 78K0/Lx3-M microcontroller products.

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)

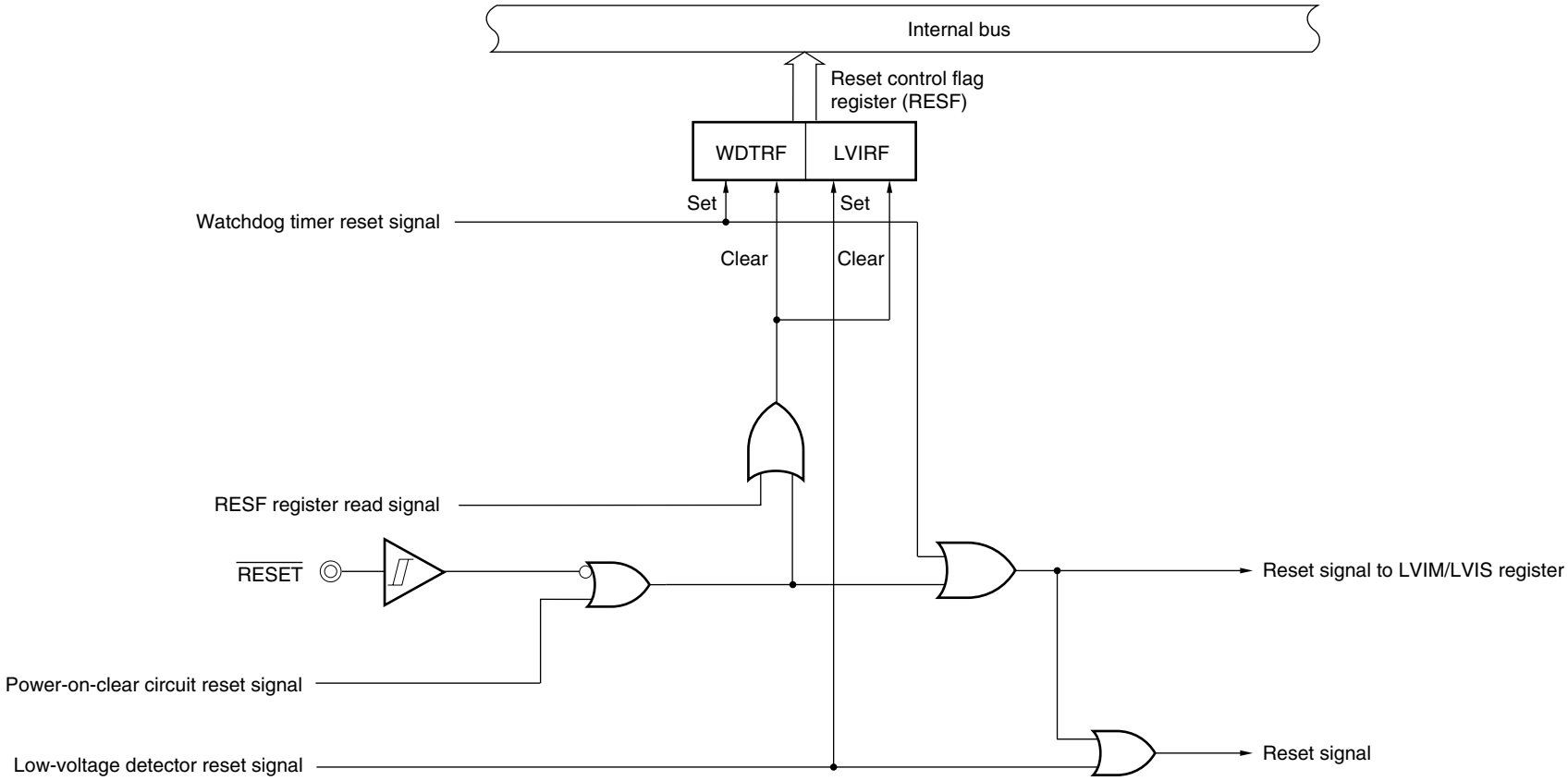
External and internal resets have no functional differences. In both cases, program execution starts at the address at 0000H and 0001H when the reset signal is generated.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Table 26-1 and Table 26-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (see Figures 26-2 to 26-4) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POC}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (see **CHAPTER 27 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 28 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
2. During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
3. When the STOP mode is released by a reset, the STOP mode contents are held during reset input. However, the port pins become high-impedance.
4. Extended SFRs are not reset by internal resets. To reset an extended SFR, set P17 to 1, clear it to 0, and then set it to 1 again.

Figure 26-1. Block Diagram of Reset Function



Caution An LVI circuit internal reset does not reset the LVI circuit.

Remarks 1. LVIM: Low-voltage detection register

2. LVIS: Low-voltage detection level selection register

Figure 26-2. Timing of Reset by $\overline{\text{RESET}}$ Input

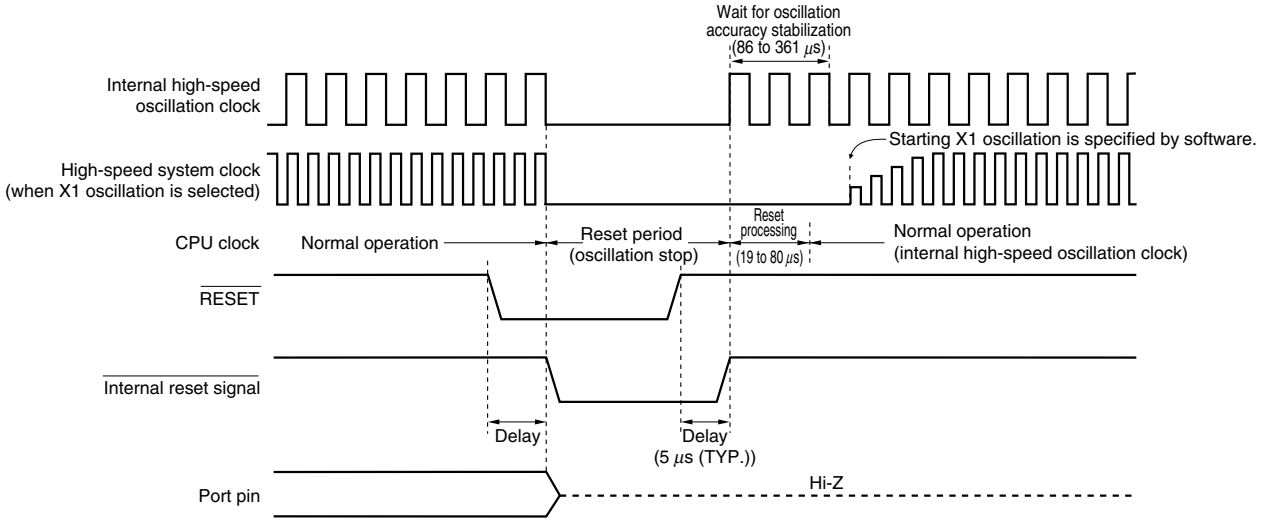
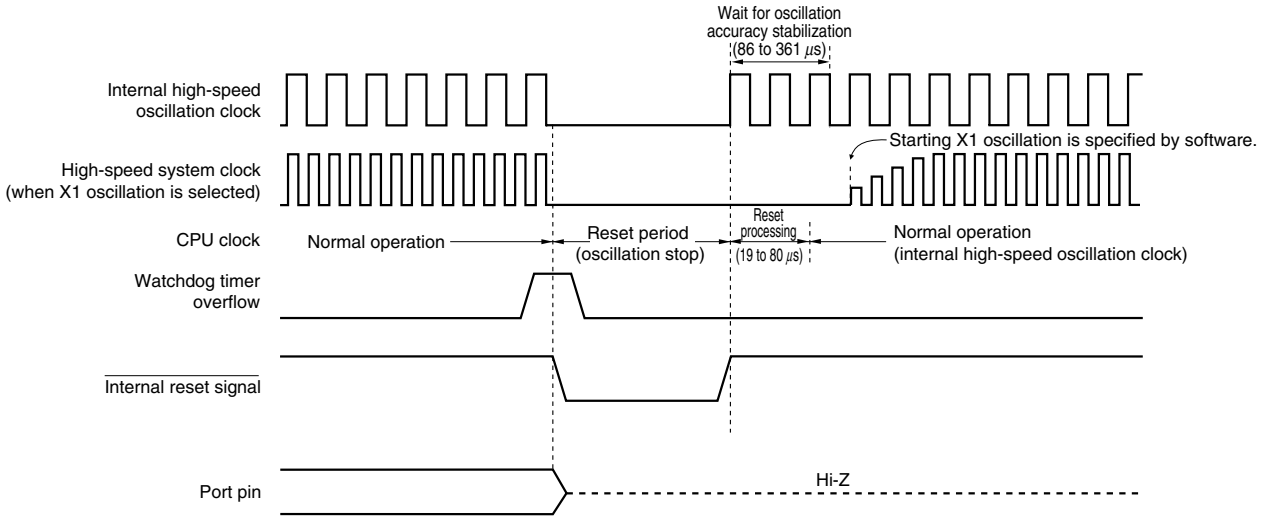
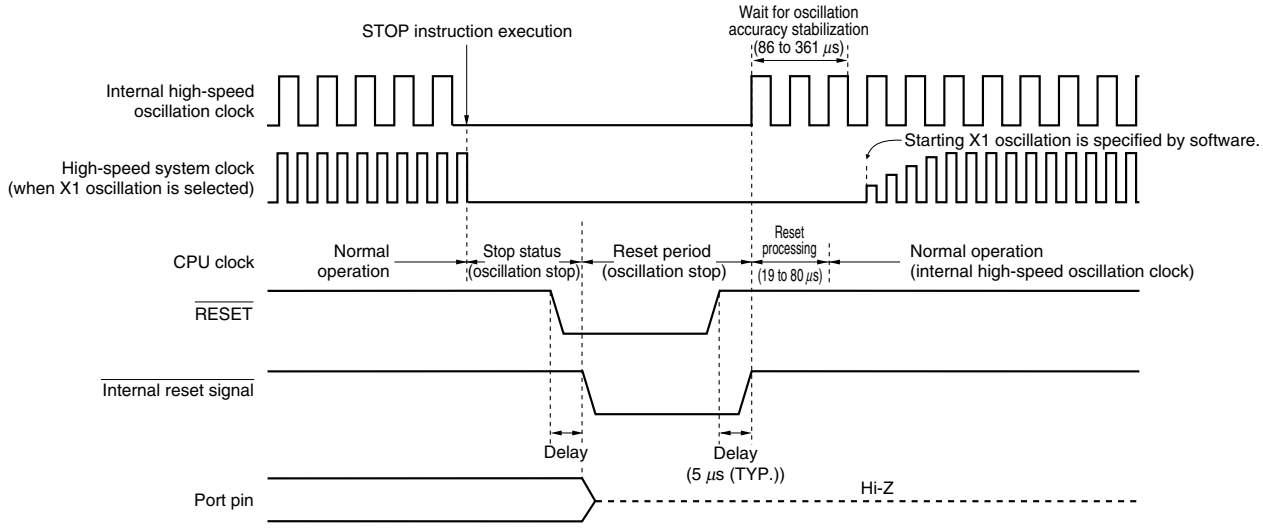


Figure 26-3. Timing of Reset Due to Watchdog Timer Overflow



Caution A watchdog timer internal reset resets the watchdog timer.

Figure 26-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input



Remark For the reset timing of the power-on-clear circuit and low-voltage detector, see **CHAPTER 27 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 28 LOW-VOLTAGE DETECTOR**.

Table 26-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{RH}	Operation stopped
		f_X	Operation stopped (pin is I/O port mode)
		f_{EXCLK}	Clock input invalid (pin is I/O port mode)
	Subsystem clock	f_{XT}	Operable
		f_{EXCLKS}	In the case of reset by the $\overline{\text{RESET}}$ pin: Clock input invalid In the case of reset by the other sources: Operable
	f_{RL}		Operation stopped
CPU			
Flash memory			
RAM			
Port (latch)			
16-bit timer/event counter		00	
8-bit timer/event counter		50	
		51	
		52	
8-bit timer		H0	
		H1	
		H2	
Real-time counter			In the case of reset by the $\overline{\text{RESET}}$ pin: Operation stopped In the case of reset by the other sources: Operable
Watchdog timer			Operation stopped
Buzzer output			
10-bit successive approximation type A/D converter			
24-bit ΔΣ-type A/D converter			
Serial interface	UART0		
	UART6		
	CSI10		
Extended SFR interface			
LCD controller/driver			
Remote controller transmitter			
Power calculation circuit			
Power quality measurement circuit			
Digital frequency conversion circuit			
Power-on-clear function			Operable
Low-voltage detection function			Operation stopped
External interrupt			

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

Table 26-2. Hardware Statuses After Reset Acknowledgment (1/5)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers (P1 to P4, P8 to P15, LP0, LP1) (output latches)		00H
Port mode registers (PM1 to PM4, PM8 to PM15, LPM0, LPM1)		FFH
Pull-up resistor option registers (PU1, PU3, PU4, PU8 to PU15, LPU0, LPU1)		00H
Port function register 1 (PF1)		00H
Port function register 2 (PF2)		00H
Port function register ALL (PFALL)		00H
Internal expansion RAM size switching register (IXS)		0CH[Note 3]
Internal memory size switching register (IMS)		CFH[Note 3]
Clock operation mode select register (OSCCTL)		00H
Processor clock control register (PCC)		01H
Internal oscillation mode register (RCM)		80H
Main OSC control register (MOC)		80H
Main clock mode register (MCM)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		05H
Internal high-speed oscillation trimming register (HIOTRM)		10H
16-bit timer/event counters 00	Timer counters 00 (TM00)	0000H
	Compare register 000 (CR000)	0000H
	Capture/compare registers 010 (CR010)	0000H
	Mode control registers 00 (TMC00)	00H
	Prescaler mode registers 00 (PRM00)	00H
	Capture/compare control registers 00 (CRC00)	00H
8-bit timer/event counters 50, 51, 52	Timer counters 50, 51, 52 (TM50, TM51, TM52)	00H
	Compare registers 50, 51, 52 (CR50, CR51, CR52)	00H
	Timer clock selection registers 50, 51, 52 (TCL50, TCL51, TCL52)	00H
	Mode control registers 50, 51, 52 (TMC50, TMC51, TMC52)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

3. The initial values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) after a reset release are constant (IMS = CFH, IXS = 0CH) in all the 78K0/Lx3-M microcontroller products, regardless of the internal memory capacity. Therefore, set the value corresponding to each product as indicated in **Table 3-1**.

Remark The special function registers (SFRs) mounted depend on the product. See **3.2.3 Special function registers (SFRs : Spetial Function Register)**, and **3.2.4 Extended Special function registers (2nd SFRs : 2nd Spetial Function Register).**

Table 26-2. Hardware Statuses After Reset Acknowledgment (2/5)

Hardware		Status After Reset Acknowledgment[Note 1]
8-bit timers H0, H1, H2	Compare registers 00, 10, 01, 11, 02, 12 (CMP00, CMP10, CMP01, CMP11, CMP02, CMP12)	00H
	Mode registers (TMHMD0, TMHMD1, TMHMD2)	00H
	Carrier control register 1 (TMCYC1)[Note 2]	00H
Real-time counter	Sub-count register (RSUBC)	0000H
	Second count register (SEC)	00H
	Minute count register (MIN)	00H
	Hour count register (HOUR)	12H
	Week count register (WEEK)	00H
	Day count register (DAY)	01H
	Month count register (MONTH)	01H
	Year count register (YEAR)	00H
	Watch error correction register (SUBCUD)	00H
	Alarm minute register (ALARMWM)	00H
	Alarm hour register (ALARMWH)	12H
	Alarm week register (ALARMWW)	00H
	Control register 0 (RTCC0)	00H
	Control register 1 (RTCC1)	00H
	Control register 2 (RTCC2)	00H
buzzer output controller	Clock output selection register (CKS)	00H
Watchdog timer	Enable register (WDTE)	1AH/9AH[Note 3]
10-bit successive approximation type A/D converter	10-bit A/D conversion result register (ADCR)	0000H
	8-bit A/D conversion result register (ADCRH)	00H
	A/D converter mode register (ADM)	00H
	Analog input channel specification register (ADS)	00H
	A/D port configuration register 0 (ADPC0)	08H
24-bit ΔΣ-type A/D converter	24-bit ΔΣ-type A/D converter mode register (ADM2)	00H
	High-pass filter control register 0 (HPFC0)	00H
	High-pass filter control register 1 (HPFC1)	00H
	24-bit ΔΣ-type A/D conversion result register n (ADCR0, ADCR1, ADCR2, ADCR3)	000000H
	Phase control registers 0 and 1 (PHC0, PHC1)	0000H
	A/D clock delay setting register (ADLY)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. 8-bit timer H1 only.

3. The reset value of WDTE is determined by the option byte setting.

Remark The special function registers (SFRs) mounted depend on the product. See **3.2.3 Special function registers (SFRs : Spetial Function Register)**, and **3.2.4 Extended Special function registers (2nd SFRs : 2nd Spetial Function Register).**

Table 26-2. Hardware Statuses After Reset Acknowledgment (3/5)

Hardware		Status After Reset Acknowledgment[Note]
Serial interface UART0	Receive buffer register 0 (RXB0)	FFH
	Transmit shift register 0 (TXS0)	FFH
	Asynchronous serial interface operation mode register 0 (ASIM0)	01H
	Asynchronous serial interface reception error status register 0 (ASIS0)	00H
	Baud rate generator control register 0 (BRGC0)	1FH
Serial interface UART6	Receive buffer register 6 (RXB6)	FFH
	Transmit buffer register 6 (TXB6)	FFH
	Asynchronous serial interface operation mode register 6 (ASIM6)	01H
	Asynchronous serial interface reception error status register 6 (ASIS6)	00H
	Asynchronous serial interface transmission status register 6 (ASIF6)	00H
	Clock selection register 6 (CKSR6)	00H
	Baud rate generator control register 6 (BRGC6)	FFH
	Asynchronous serial interface control register 6 (ASICL6)	16H
	Input switch control register (ISC)	00H
Serial interfaces CSI10	Transmit buffer registers 10 (SOTB10)	00H
	Serial I/O shift registers 10 (SIO10)	00H
	Serial operation mode registers 10 (CSIM10)	00H
	Serial clock selection registers 10 (CSIC10)	00H
Extended SFR interface	Serial operation mode specification register 0 (CSIMA0)	00H
	Serial status register 0 (CSIS0)	00H
	Divisor selection register 0 (BRGCA0)	03H
	Serial I/O shift register 0 (SIOA0)	00H
LCD controller/driver	LCD mode register (LCDMD)	00H
	LCD display mode register (LCDM)	00H
	LCD clock control register 0 (LCDC0)	00H
Key interrupt	Key return mode register (KRM)	00H

Note During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

Remark The special function registers (SFRs) mounted depend on the product. See **3.2.3 Special function registers (SFRs : Spetial Function Register)**, and **3.2.4 Extended Special function registers (2nd SFRs : 2nd Spetial Function Register).**

Table 26-2. Hardware Statuses After Reset Acknowledgment (4/5)

Hardware		Status After Reset Acknowledgment[Note]
Power calculation circuit	Power calculation mode control register 1 (PWCTL1)	00H
	Power calculation mode control register 2 (PWCTL2)	00H
	No-load level control register (NLCTL)	00H
	Active power scaling specification register (ACTDIV)	00H
	Reactive power scaling specification register (READIV)	00H
	Apparent power scaling specification register (APPDIV)	00H
	RMS registers for voltage channels 1 and 2 (V1RMS, V2RMS)	000000H
	RMS registers for current channels 1 and 2 (I1RMS, I2RMS)	000000H
	Active power accumulation reading register (ACTHR)	000000H
	Active power accumulation reading and resetting register (RACTHR)	000000H
	Active power accumulation synchronous reading register (LACTHR)	000000H
	Reactive power accumulation reading register (REAHR)	000000H
	Reactive power accumulation reading and resetting register (RREAHR)	000000H
	Reactive power accumulation synchronous reading register (LREAHR)	000000H
	Apparent power accumulation reading register (APPHR)	000000H
	Apparent power accumulation reading and resetting register (RAPPHR)	000000H
	Apparent power accumulation synchronous reading register (LAPPHR)	000000H
	Line cycle number specification register (LINNUM)	FFFFH
	Active power gain specification registers 1 and 2 (ACT1GAIN, ACT2GAIN)	0000H
	Reactive power gain specification registers 1 and 2 (REA1GAIN, REA2GAIN)	0000H
	Apparent power gain specification registers 1 and 2 APP1GAIN, APP2GAIN)	0000H
	RMS gain specification registers for current channels 1 and 2 (IRMS1GAIN, IRMS2GAIN)	0000H
	Active power offset specification registers 1 and 2 (ACT1OS, ACT2OS)	0000H
	Reactive power offset specification registers 1 and 2 (REA1OS, REA2OS)	0000H
	RMS offset specification registers for current channels 1 and 2 (I1RMSOS, I2RMSOS)	0000H
	RMS offset specification registers for voltage channels 1 and 2 (V1RMSOS, V2RMSOS)	0000H
	Sampling mode selection register (SAMPMODE)	00H
	Sampling result registers 1 and 2 (SAMP1, SAMP2)	000000H

Note During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

Remark The special function registers (SFRs) mounted depend on the product. See **3.2.3 Special function registers (SFRs : Spetial Function Register)**, and **3.2.4 Extended Special function registers (2nd SFRs : 2nd Spetial Function Register).**

Table 26-2. Hardware Statuses After Reset Acknowledgment (5/5)

Hardware		Status After Reset Acknowledgment[Note 1]
Power quality measurement circuit	Period and frequency measurement result register (PFVAL)	0000H
	Zero-crossing timeout specification registers for voltage channels 1 and 2 (ZXTOUT1, ZXTOUT2)	03FFH
	SAG line cycle number specification registers for voltage channels 1 and 2 (SAGNUM1, SAGNUM2)	FFH
	SAG level specification registers for voltage channels 1 and 2 (SAGVAL1, SAGVAL2)	000000H
	Peak current level specification register (IPKLMT)	FFFFH
	Peak voltage level specification register (VPKLMT)	FFFFH
	Peak current value register (IMAX)	000000H
	Peak current value clearing register (RSTIMAX)	000000H
	Peak voltage value register (VMAX)	000000H
	Peak voltage value clearing register (RSTVMAX)	000000H
	Gain specification register (IMATGAIN)	0000H
	Fault detection control register (PQMCTL)	00H
	Fault detection threshold value specification register (IST)	8BH
	Fault control register (ICHK)	84H
Digital frequency conversion circuit	Frequency conversion control register (CFCTL)	02H
	Frequency scaling specification register (CFMULL, CFMULH)	FFH
	Pulse width specification register (PULCTL)	00H
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 2]
	Low-voltage detection level selection register (LVIS)	00H[Note 2]
Interrupt	Request flag registers 0L, 0H, 1L, 1H (IF0L, IF0H, IF1L, IF1H)	00H
	Mask flag registers 0L, 0H, 1L, 1H (MK0L, MK0H, MK1L, MK1H)	FFH
	Extended SFR interrupt request flag registers 20, 21, 22, 23 (IF20, IF21, IF22, IF23)	00H
	Extended SFR Interrupt mask flag registers 20, 21, 22, 23 (MK20, MK21, MK22, MK23)	FFH
	Priority specification flag registers 0L, 0H, 1L, 1H (PR0L, PR0H, PR1L, PR1H)	FFH
	External interrupt rising edge enable register (EGP)	00H
	External interrupt falling edge enable register (EGN)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
RESF	WDTRF flag	Cleared (0)	Cleared (0)	Set (1)	Held
	LVIRF flag			Held	Set (1)
LVIM		Cleared (00H)	Cleared (00H)	Cleared (00H)	Held
LVIS					

Remark The special function registers (SFRs) mounted depend on the product. See **3.2.3 Special function registers (SFRs : Spetial Function Register)**, and **3.2.4 Extended Special function registers (2nd SFRs : 2nd Spetial Function Register).**

26.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the 78K0/Lx3-M microcontrollers. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-clear (POC) circuit, and reading RESF set RESF to 00H.

Figure 26-5. Format of Reset Control Flag Register (RESF)

Address: FFACH After reset: 00H[Note] R

Symbol	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LVIRF

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

Note The value after reset varies depending on the reset source.

Caution Do not read data by a 1-bit memory manipulation instruction.

The status of RESF when a reset request is generated is shown in Table 26-3.

Table 26-3. RESF Status When Reset Request Is Generated

Reset Source / Flag	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
WDTRF	Cleared (0)	Cleared (0)	Set (1)	Held
LVIRF			Held	Set (1)

26.2 Notes on supplying power supply voltage

Note the following when supplying power supply voltage to the 78K0/Lx3-M microcontrollers:

<1> Be sure to supply power in the following order: LV_{DD}, V_{DD}/AV_{DD}, and then AV_{REF}.

<2> After V_{DD} reaches the operating voltage, input a high-level signal to the $\overline{\text{RESET}}$ pin.

26.3 Notes on settings after reset release

After a reset release, be sure to specify the following settings:

<1> Enable output (PM10 = 0) for PM10 (bit 0 of the PM1 register), and then use the clock output selection register (CKS) to select the output clock.

<2> Enable output for PM47, PM46, PM17, PM16, and PM14 (PM47, PM46, PM17, PM16, PM14 = 0).

<3> Cancel the pull-down status (by setting the PUTCTL register to 01H).

Caution If an internal reset is triggered while using the extended SFR interface to transmit data, the data might not be correctly transmitted to an extended SFR.

CHAPTER 27 POWER-ON-CLEAR CIRCUIT

27.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit is mounted onto all 78K0/Lx3-M microcontroller products.
The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
  In the 1.59 V POC mode (option byte: POCMODE = 0), the reset signal is released when the supply voltage (V_{DD}) exceeds 1.59 V ±0.15 V.
  In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the reset signal is released when the supply voltage (V_{DD}) exceeds 2.7 V ±0.2 V.

- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V), generates internal reset signal when $V_{DD} < V_{POC}$.

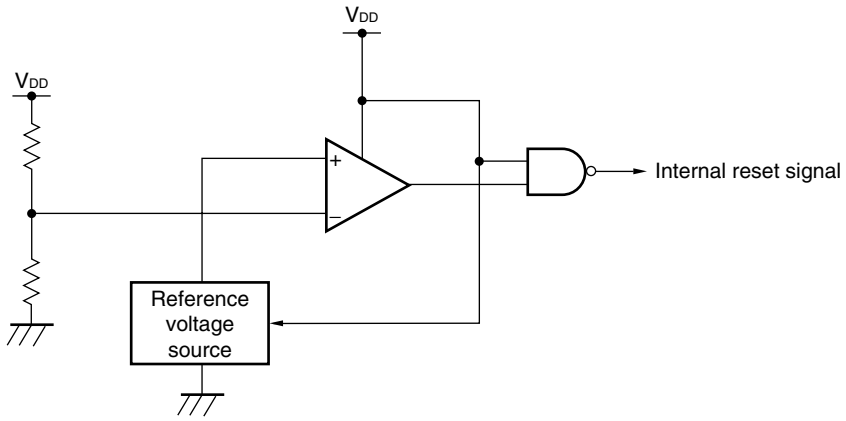
Caution If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

Remark 78K0/Lx3-M microcontrollers incorporate multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detector (LVI). RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

27.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 27-1.

Figure 27-1. Block Diagram of Power-on-Clear Circuit



27.3 Operation of Power-on-Clear Circuit

(1) In 1.59 V POC mode (option byte: POCMODE = 0)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59 V ±0.15 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{POC}$.

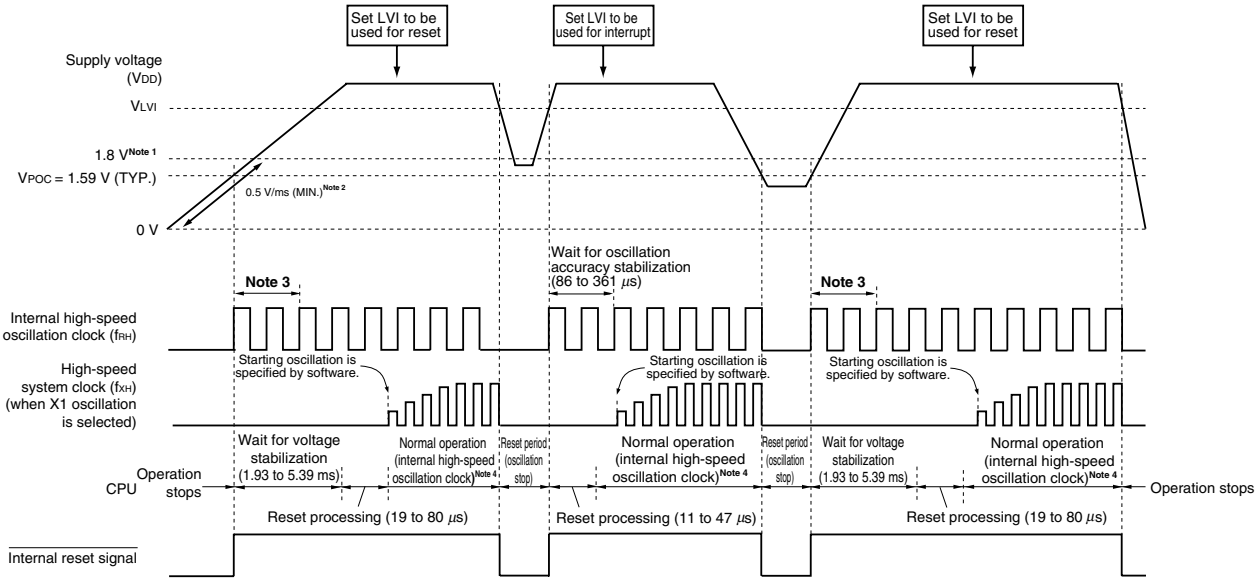
(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{DDPOC} = 2.7 V ±0.2 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{DDPOC}$.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

Figure 27-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 3.6 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. If the voltage rises to 1.8 V at a rate slower than 0.5 V/ms (MIN.) on power application, input a low level to the $\overline{\text{RESET}}$ pin after power application and before the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using an option byte (POCMODE = 1).

3. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

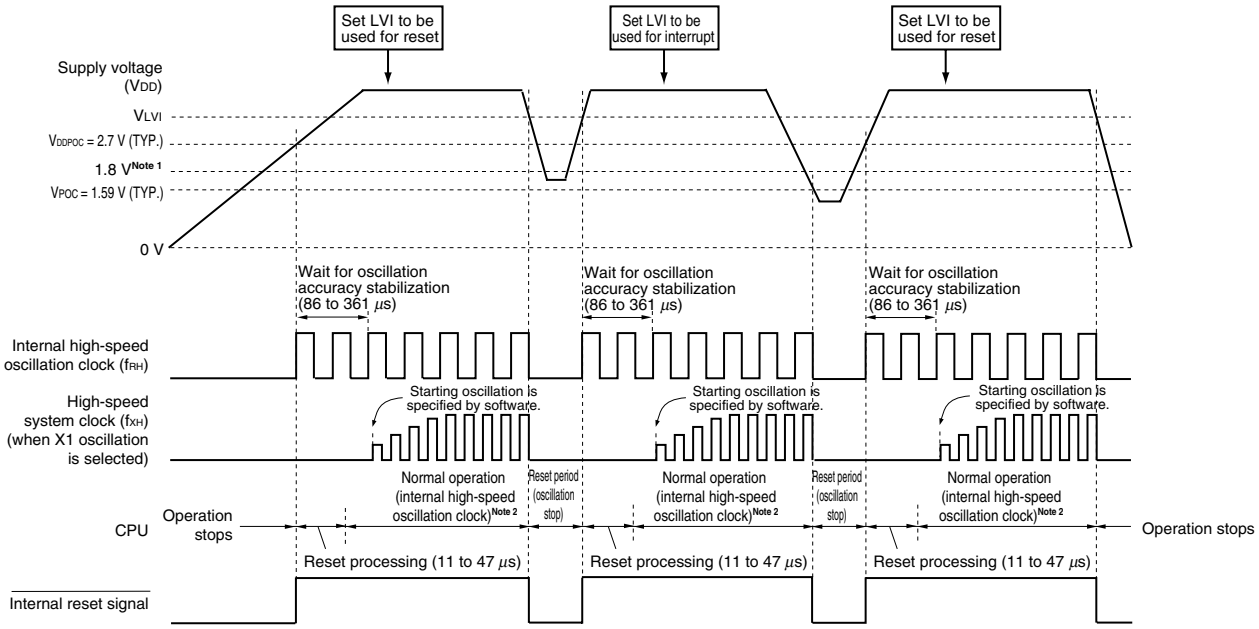
4. The internal high-speed oscillation clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Caution Set the low-voltage detector by software after the reset status is released (see CHAPTER 28 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POC}: POC detection voltage

Figure 27-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 3.6 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. The internal high-speed oscillation clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Cautions 1. Set the low-voltage detector by software after the reset status is released (see CHAPTER 28 LOW-VOLTAGE DETECTOR).

2. A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the time the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) is within 1.93 to 5.39 ms, a power supply stabilization wait time of 0 to 5.39 ms occurs automatically before reset processing and the reset processing time becomes 19 to 80 μs.

Remark V_{LVI}: LVI detection voltage
V_{POC}: POC detection voltage

27.4 Cautions for Power-on-Clear Circuit

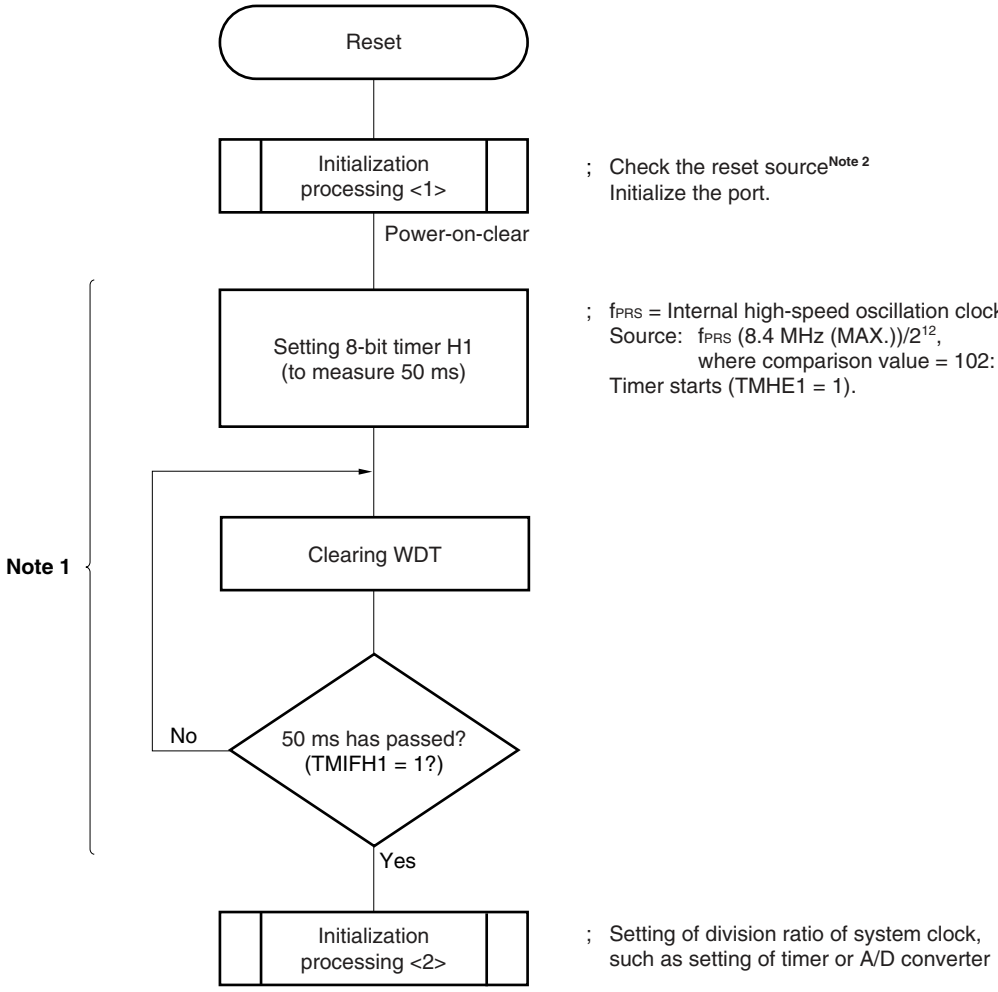
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 27-3. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage

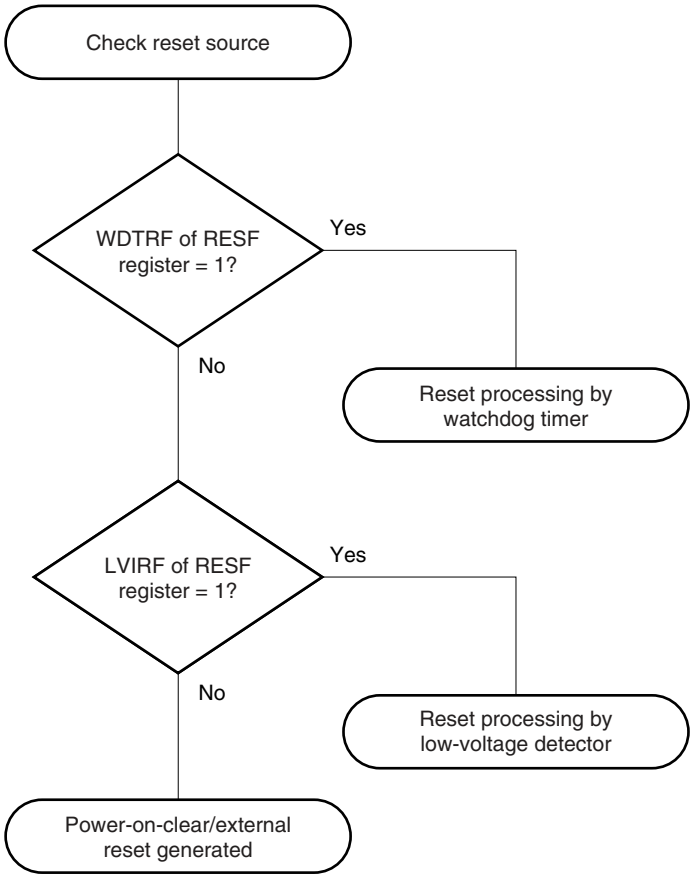


Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

Figure 27-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source



CHAPTER 28 LOW-VOLTAGE DETECTOR

28.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) is mounted onto all 78K0/Lx3-M microcontroller products.
The low-voltage detector (LVI) has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVI}) or the input voltage from an external input pin (EXLVI) with the detection voltage (V_{EXLVI} = 1.21 V (TYP.): fixed), and generates an internal reset or internal interrupt signal.
- The supply voltage (V_{DD}) or input voltage from an external input pin (EXLVI) can be selected by software.
- Reset or interrupt function can be selected by software.
- Detection levels (10 levels) of supply voltage can be changed by software.
- Operable in STOP mode.

The reset and interrupt signals are generated as follows depending on selection by software.

Selection of Level Detection of Supply Voltage (V_{DD}) (LVISEL = 0)		Selection Level Detection of Input Voltage from External Input Pin (EXLVI) (LVISEL = 1)	
Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).	Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).
Generates an internal reset signal when $V_{DD} < V_{LVI}$ and releases the reset signal when $V_{DD} \geq V_{LVI}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).	Generates an internal reset signal when EXLVI < V_{EXLVI} and releases the reset signal when EXLVI ≥ V_{EXLVI}.	Generates an internal interrupt signal when EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).

Remark LVISEL: Bit 2 of low-voltage detection register (LVIM)
LVIMD: Bit 1 of LVIM

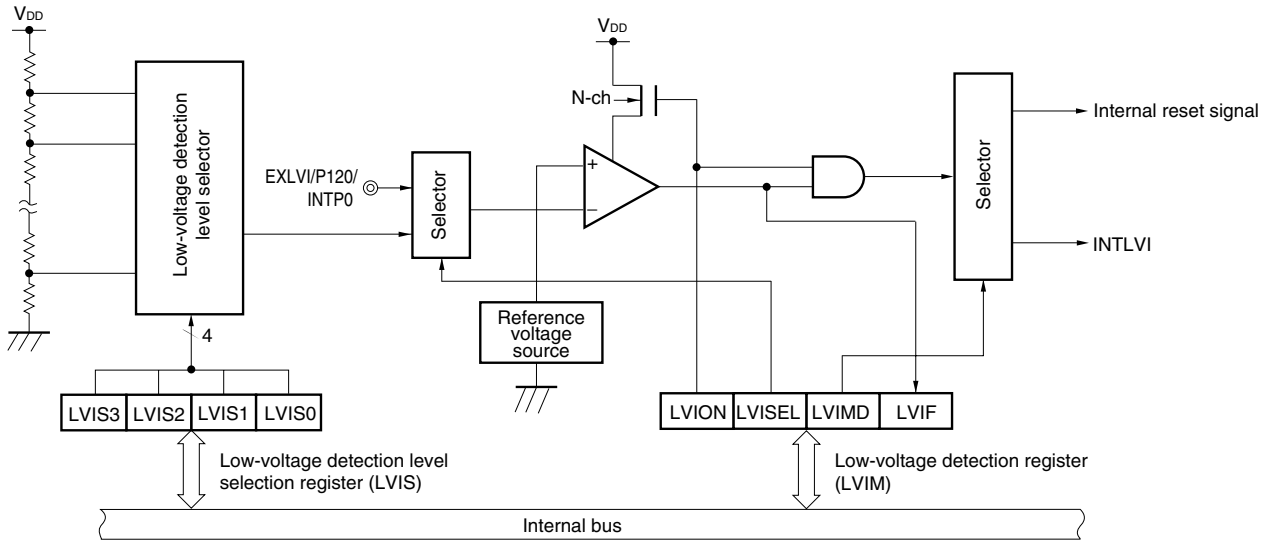
While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

28.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 28-1.

Figure 28-1. Block Diagram of Low-Voltage Detector



28.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Low-voltage detection level selection register (LVIS)
- Port mode register 12 (PM12)

(1) Low-voltage detection register (LVIM)

This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 28-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFBEH After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. This bit is cleared to 00H upon a reset other than an LVI reset.

2. Bit 0 is read-only.

3. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

4. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 μs (MIN.)) from when LVION is set to 1 until operation is stabilized. After operation has stabilized, the external input of 200 μs (MIN.) (Minimum pulse width: 200 μs (MIN.)) is required from when a state below LVI detection voltage has been entered, until LVIF is set (1).

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

3. When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 28-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	1	1	0	V_{LVI0} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI1} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI2} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI3} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI4} (2.70 V ±0.1 V)
1	0	1	1	V_{LVI5} (2.55 V ±0.1 V)
1	1	0	0	V_{LVI6} (2.39 V ±0.1 V)
1	1	0	1	V_{LVI7} (2.24 V ±0.1 V)
1	1	1	0	V_{LVI8} (2.08 V ±0.1 V)
1	1	1	1	V_{LVI9} (1.93 V ±0.1 V)
Other than above				Setting prohibited

Note The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

Cautions 1. Be sure to clear bits 4 to 7 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

(3) Port mode register 12 (PM12)

When using the P120/EXLVI/INTP0 pin for external low-voltage detection potential input, set PM120 to 1. At this time, the output latch of P120 may be 0 or 1.

PM12 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM12 to FFH.

Figure 28-4. Format of Port Mode Register 12 (PM12)

Address: FF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

PM120	P120 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

28.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

(1) Used as reset (LVIMD = 1)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)), generates an internal reset signal when EXLVI < V_{EXLVI}, and releases internal reset when EXLVI ≥ V_{EXLVI}.

(2) Used as interrupt (LVIMD = 0)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)). When EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}), generates an interrupt signal (INTLVI).

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

Remark LVIMD: Bit 1 of low-voltage detection register (LVIM)
LVISEL: Bit 2 of LVIM

28.4.1 When used as reset

(1) When detecting level of supply voltage (V_{DD})

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <5> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <6> Wait until it is checked that (supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})) by bit 0 (LVIF) of LVIM.
  - <7> Set bit 1 (LVIMD) of LVIM to 1 (generates reset when the level is detected).

  Figure 28-5 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

  Cautions 1. <1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <4>.
  2. If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

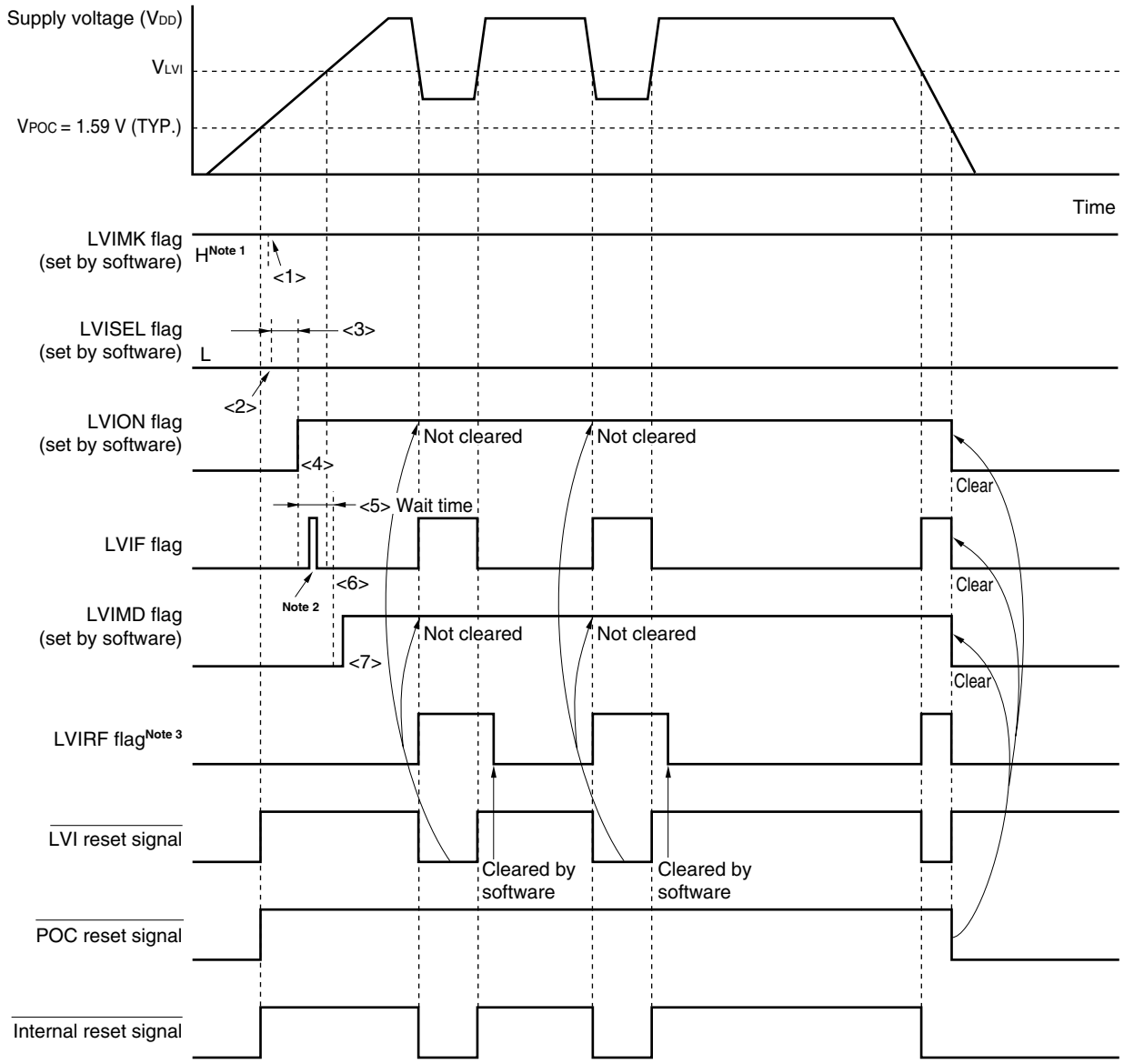
- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVIMD to 0 and then LVION to 0.

Figure 28-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Supply Voltage (V_{DD})) (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

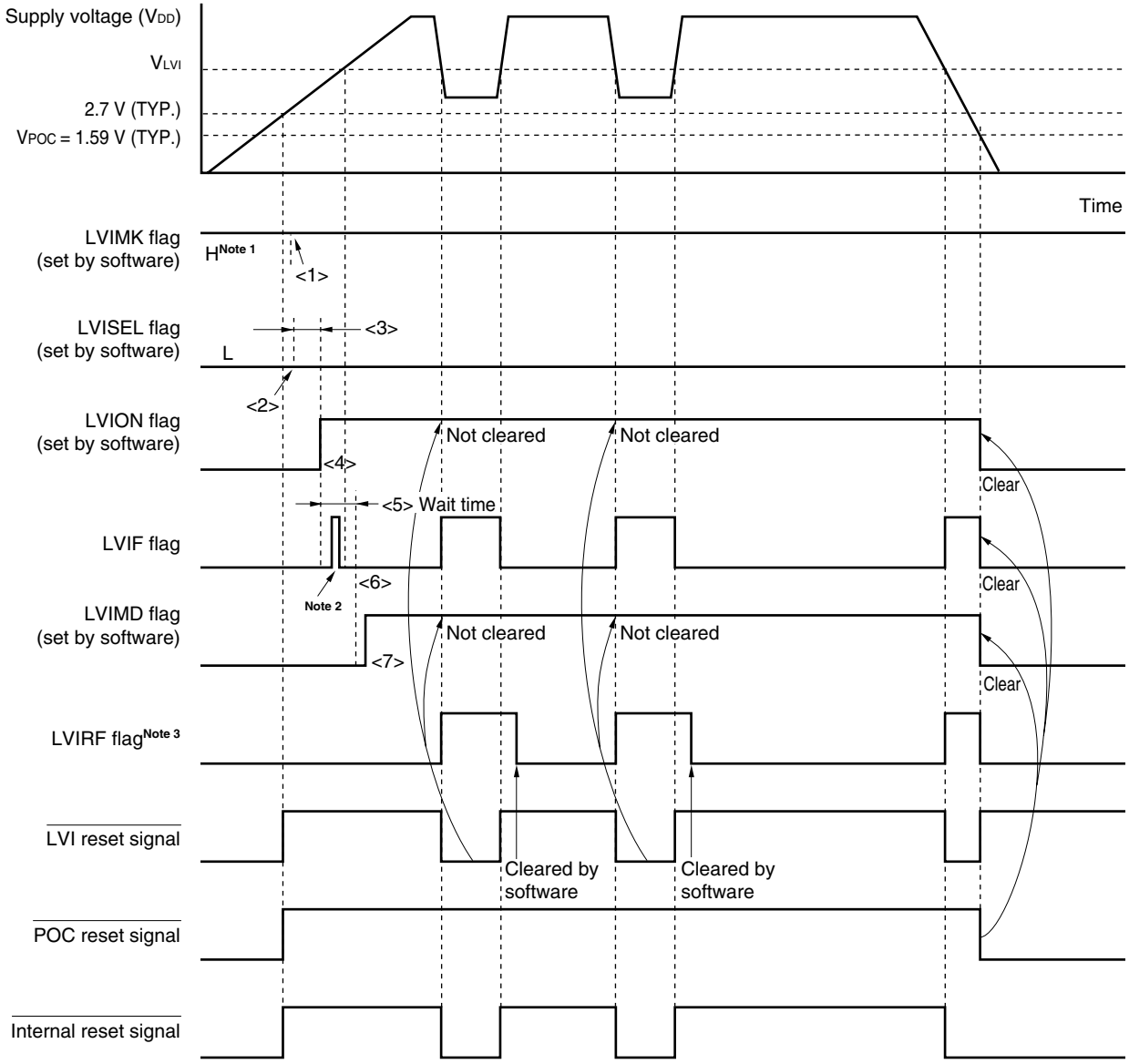
2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

Remark <1> to <7> in Figure 28-5 above correspond to <1> to <7> in the description of "When starting operation" in **28.4.1 (1) When detecting level of supply voltage (V_{DD})**.

Figure 28-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Supply Voltage (V_{DD})) (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

Remark <1> to <7> in Figure 28-5 above correspond to <1> to <7> in the description of "When starting operation" in **28.4.1 (1) When detecting level of supply voltage (V_{DD})**.

(2) When detecting level of input voltage from external input pin (EXLVI)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from external input pin (EXLVI)).
  - <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <4> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <5> Wait until it is checked that (input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.))) by bit 0 (LVIF) of LVIM.
  - <6> Set bit 1 (LVIMD) of LVIM to 1 (generates reset signal when the level is detected).

  Figure 28-6 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <6> above.

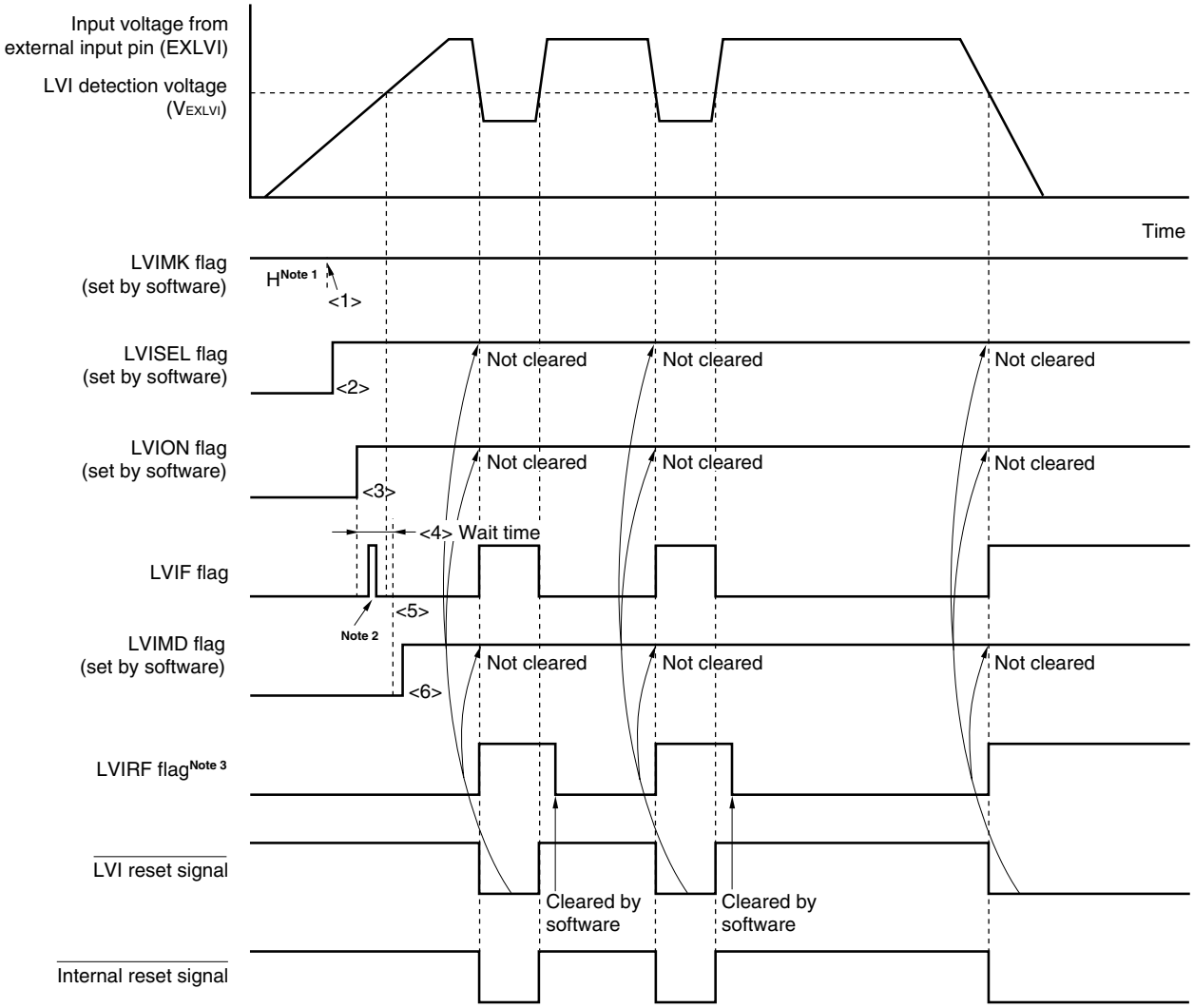
  Cautions 1. <1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.
  2. If input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.)) when LVIMD is set to 1, an internal reset signal is not generated.
  3. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVIMD to 0 and then LVION to 0.

Figure 28-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 26 RESET FUNCTION**.

Remark <1> to <6> in Figure 28-6 above correspond to <1> to <6> in the description of "When starting operation" in **28.4.1 (2) When detecting level of input voltage from external input pin (EXLVI)**.

28.4.2 When used as interrupt

(1) When detecting level of supply voltage (V_{DD})

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <5> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <6> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <7> Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of LVIM.
  - <8> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <9> Release the interrupt mask flag of LVI (LVIMK).
  - <10> Execute the EI instruction (when vector interrupts are used).

  Figure 28-7 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <9> above.

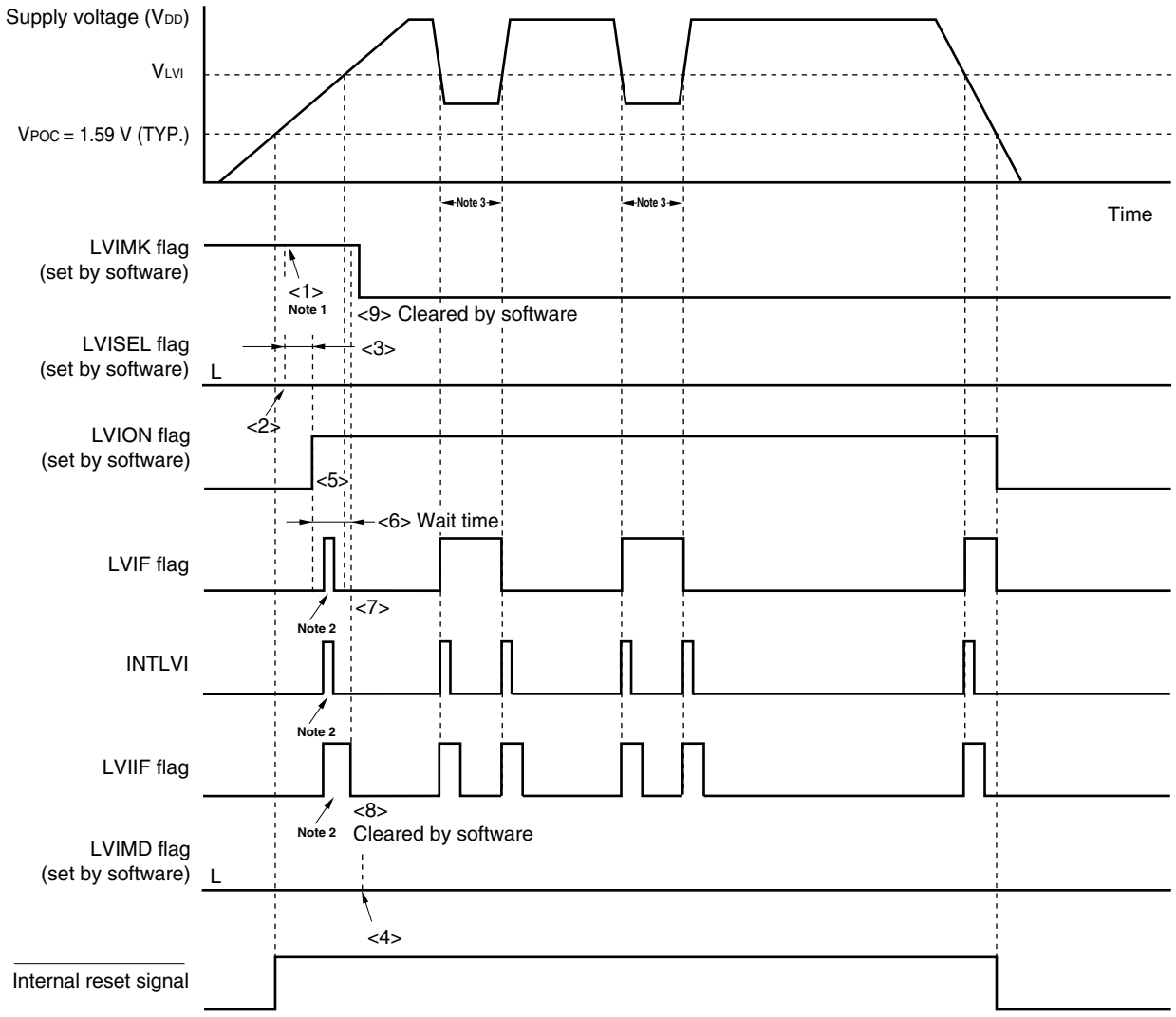
- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVION to 0.

Figure 28-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD})) (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

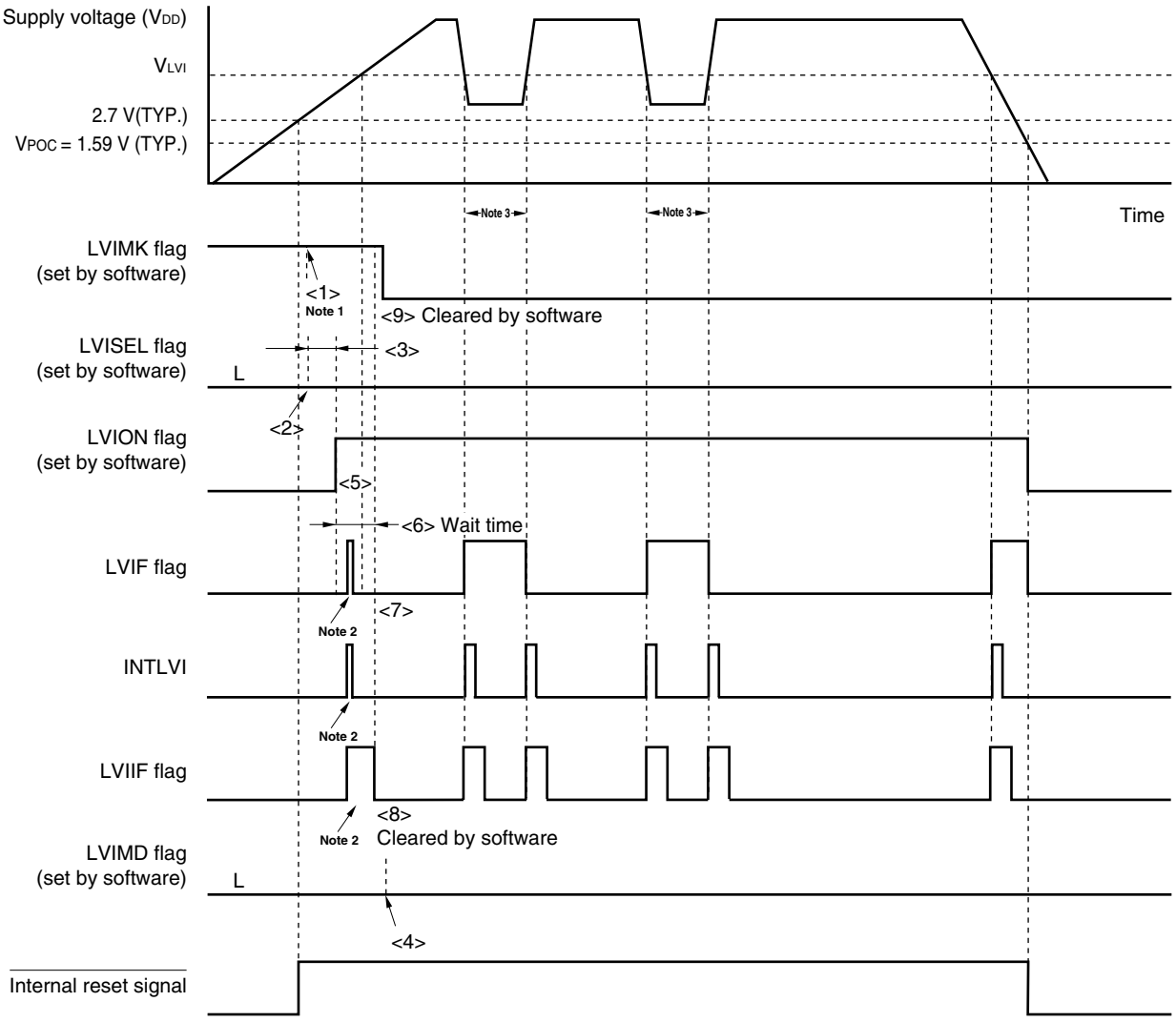
2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <9> in Figure 28-7 above correspond to <1> to <9> in the description of "When starting operation" in **28.4.2 (1) When detecting level of supply voltage (V_{DD})**.

Figure 28-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD})) (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <9> in Figure 28-7 above correspond to <1> to <9> in the description of "When starting operation" in **28.4.2 (1) When detecting level of supply voltage (V_{DD})**.

(2) When detecting level of input voltage from external input pin (EXLVI)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from external input pin (EXLVI)).
  - <3> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <4> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <5> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <6> Confirm that "input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.)" when detecting the falling edge of EXLVI, or "input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI} = 1.21 V (TYP.)" when detecting the rising edge of EXLVI, at bit 0 (LVIF) of LVIM.
  - <7> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <8> Release the interrupt mask flag of LVI (LVIMK).
  - <9> Execute the EI instruction (when vector interrupts are used).

  Figure 28-8 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <8> above.

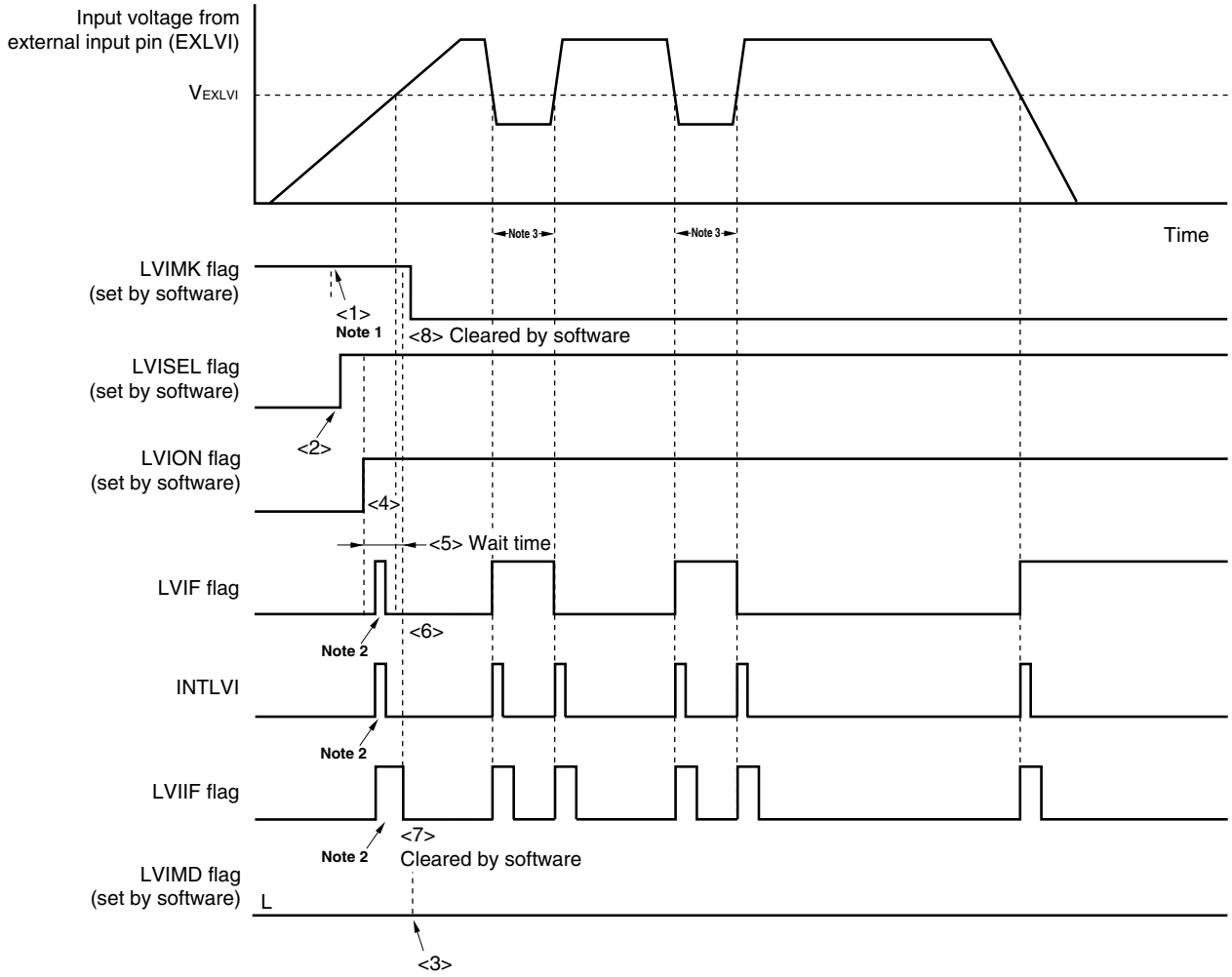
  Caution Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVION to 0.

Figure 28-8. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <8> in Figure 28-8 above correspond to <1> to <8> in the description of “When starting operation” in **28.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

28.5 Cautions for Low-Voltage Detector

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

(1) When used as reset

The system may be repeatedly reset and released from the reset status.

In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below.

(2) When used as interrupt

Interrupt requests may be frequently generated. Take (b) of action (2) below.

<Action>

(1) When used as reset

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 28-9**).

(2) When used as interrupt

(a) Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 0 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

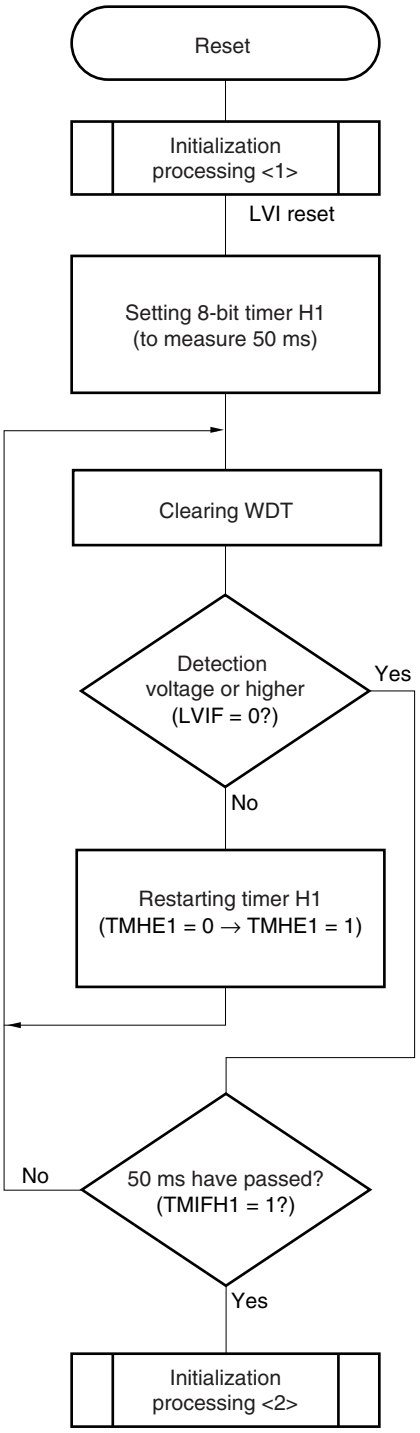
(b) In a system where the supply voltage fluctuation period is long in the vicinity of the LVI detection voltage, wait for the supply voltage fluctuation period, confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, using the LVIF flag, and clear the LVIIF flag to 0.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

Figure 28-9. Example of Software Processing After Reset Release (1/2)

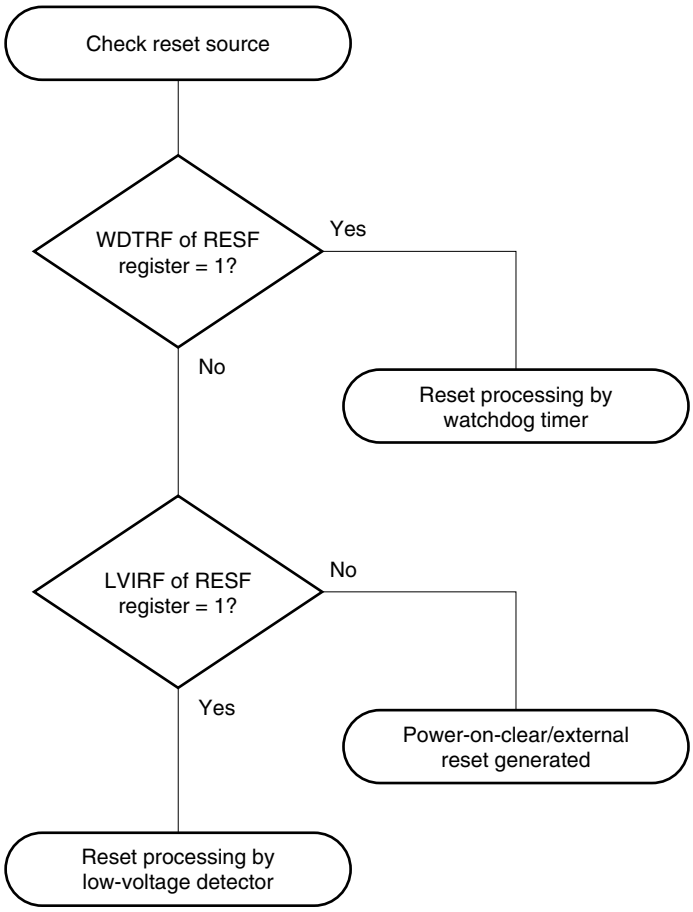
• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.

Figure 28-9. Example of Software Processing After Reset Release (2/2)

• Checking reset source



CHAPTER 29 OPTION BYTE

29.1 Functions of Option Bytes

The flash memory at 0080H to 0084H of the 78K0/Lx3-M microcontrollers is an option byte area. When power is turned on or when the device is restarted from the reset status, the device automatically references the option bytes and sets specified functions. When using the product, be sure to set the following functions by using the option bytes.

When the boot swap operation is used during self-programming, 0080H to 0084H are switched to 1080H to 1084H. Therefore, set values that are the same as those of 0080H to 0084H to 1080H to 1084H in advance.

Caution Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).

(1) 0080H/1080H

- Internal low-speed oscillator operation
  - Can be stopped by software
  - Cannot be stopped
- Watchdog timer overflow time setting
- Watchdog timer counter operation
  - Enabled counter operation
  - Disabled counter operation
- Watchdog timer window open period setting

Caution Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

(2) 0081H/1081H

- Selecting POC mode
  - During 2.7 V/1.59 V POC mode operation (POCMODE = 1)
    The device is in the reset state upon power application and until the supply voltage reaches 2.7 V (TYP.). It is released from the reset state when the voltage exceeds 2.7 V (TYP.). After that, POC is not detected at 2.7 V but is detected at 1.59 V (TYP.).
    If the supply voltage rises to 1.8 V after power application at a pace slower than 0.5 V/ms (MIN.), use of the 2.7 V/1.59 V POC mode is recommended.
  - During 1.59 V POC mode operation (POCMODE = 0)
    The device is in the reset state upon power application and until the supply voltage reaches 1.59 V (TYP.). It is released from the reset state when the voltage exceeds 1.59 V (TYP.). After that, POC is detected at 1.59 V (TYP.), in the same manner as on power application.

Caution POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

(3) 0084H/1084H

○ On-chip debug operation control

- Disabling on-chip debug operation
- Enabling on-chip debug operation and erasing data of the flash memory in case authentication of the on-chip debug security ID fails
- Enabling on-chip debug operation and not erasing data of the flash memory even in case authentication of the on-chip debug security ID fails

Caution To use the on-chip debug function, set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot operation.

29.2 Format of Option Byte

The format of the option byte is shown below.

Figure 29-1. Format of Option Byte (1/2)

Address: 0080H/1080H[Note]

7	6	5	4	3	2	1	0
0	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	LSROSC

WINDOW1	WINDOW0	Watchdog timer window open period
0	0	25%
0	1	50%
1	0	75%
1	1	100%

WDTON	Operation control of watchdog timer counter/illegal access detection
0	Counter operation disabled (counting stopped after reset release), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset release), illegal access detection operation enabled

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time
0	0	0	$2^{10}/f_{RL}$ (3.88 ms)
0	0	1	$2^{11}/f_{RL}$ (7.76 ms)
0	1	0	$2^{12}/f_{RL}$ (15.52 ms)
0	1	1	$2^{13}/f_{RL}$ (31.03 ms)
1	0	0	$2^{14}/f_{RL}$ (62.06 ms)
1	0	1	$2^{15}/f_{RL}$ (124.12 ms)
1	1	0	$2^{16}/f_{RL}$ (248.24 ms)
1	1	1	$2^{17}/f_{RL}$ (496.48 ms)

LSROSC	Internal low-speed oscillator operation
0	Can be stopped by software (stopped when 1 is written to bit 1 (LSRSTOP) of RCM register)
1	Cannot be stopped (not stopped even if 1 is written to LSRSTOP bit)

Note Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. Setting WINDOW1 = WINDOW0 = 0 is prohibited when using the watchdog timer at 1.8 V ≤ V_{DD} < 2.6 V.

3. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

4. If LSROSC = 0 (oscillation can be stopped by software), the count clock is not supplied to the watchdog timer in the HALT and STOP modes, regardless of the setting of bit 1 (LSRSTOP) of the internal oscillation mode register (RCM).
When 8-bit timer H1 operates with the internal low-speed oscillation clock, the count clock is supplied to 8-bit timer H1 even in the HALT/STOP mode.

5. Be sure to clear bit 7 to 0.

Remarks 1. f_{RL}: Internal low-speed oscillation clock frequency

2. ( ): f_{RL} = 264 kHz (MAX.)

Figure 29-1. Format of Option Byte (2/2)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POCMODE

POCMODE	POC mode selection
0	1.59 V POC mode (default)
1	2.7 V/1.59 V POC mode

Notes 1. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

2. To change the setting for the POC mode, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H, 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Note Be sure to set 00H to 0082H and 0083H, as these addresses are reserved areas. Also set 00H to 1082H and 1083H because 0082H and 0083H are switched with 1082H and 1083H when the boot swap operation is used.

Address: 0084H/1084H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Note To use the on-chip debug function, set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Remark For the on-chip debug security ID, see **CHAPTER 31 ON-CHIP DEBUG FUNCTION**.

Here is an example of description of the software for setting the option bytes.

```
OPT     CSEG   AT 0080H
OPTION: DB     30H      ; Enables watchdog timer operation (illegal access detection operation),
                        ; Window open period of watchdog timer: 50%,
                        ; Overflow time of watchdog timer: 2^10/fRL,
                        ; Internal low-speed oscillator can be stopped by software.
        DB     00H      ; 1.59 V POC mode
        DB     00H      ; Reserved area
        DB     00H      ; Reserved area
        DB     00H      ; On-chip debug operation disabled
```

Remark Referencing of the option byte is performed during reset processing. For the reset processing timing, see **CHAPTER 26 RESET FUNCTION**.

CHAPTER 30 FLASH MEMORY

The 78K0/Lx3-M microcontrollers incorporate the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

30.1 Internal Memory Size Switching Register

Select the internal memory capacity using the internal memory size switching register (IMS).
IMS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IMS to CFH.

Caution Be sure to set each product to the values shown in Table 30-1 after a reset release.

Figure 30-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	1	0	0	16 KB
1	0	0	0	32 KB
1	1	0	0	48 KB
1	1	1	1	60 KB
Other than above				Setting prohibited

Table 30-1. Internal Memory Size Switching Register (IMS) Settings

78K0/LE3-M	78K0/LG3-M	IMS Setting
μPD78F8052	–	04H
μPD78F8053	–	C8H
–	μPD78F8054	CCH
–	μPD78F8055	CFH

30.2 Internal Expansion RAM Size Switching Register

Select the internal expansion RAM capacity using the internal expansion RAM size switching register (IXS).
IXS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IXS to 0CH.

Cautions 1. Be sure to set each product to the values shown in Table 30-2 after a reset release.
2. A product that does not have an internal expansion RAM is not provided with IXS.

Figure 30-2. Format of Internal Expansion RAM Size Switching Register (IXS)

Address: FFF4H After reset: 0CH R/W

Symbol	7	6	5	4	3	2	1	0
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
1	1	0	0	0 byte
1	0	1	0	1024 bytes
Other than above				Setting prohibited

Table 30-2. Internal Expansion RAM Size Switching Register (IXS) settings

78K0/LE3-M	78K0/LG3-M	IXS Setting
μPD78F8052[Note]	–	0CH
μPD78F8053[Note]	–	
–	μPD78F8054	0AH
–	μPD78F8055	

Note A product that does not have an internal expansion RAM is not provided with IXS.

30.3 Writing with Flash memory programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0/Lx3-M microcontrollers have been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

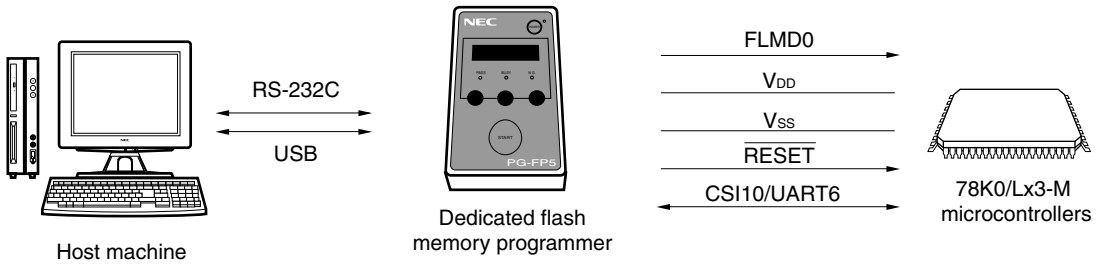
Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0/Lx3-M microcontrollers are mounted on the target system.

Remark The FA series is products of Naito Densei Machida Mfg. Co., Ltd.

30.4 Programming Environment

The environment required for writing a program to the flash memory of the 78K0/Lx3-M microcontrollers is illustrated below.

Figure 30-3. Environment for Writing Program to Flash Memory



A host machine that controls the dedicated flash memory programmer is necessary.

To interface between the dedicated flash memory programmer and the 78K0/Lx3-M microcontrollers, CSI10 or UART6 is used for manipulation such as writing and erasing. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

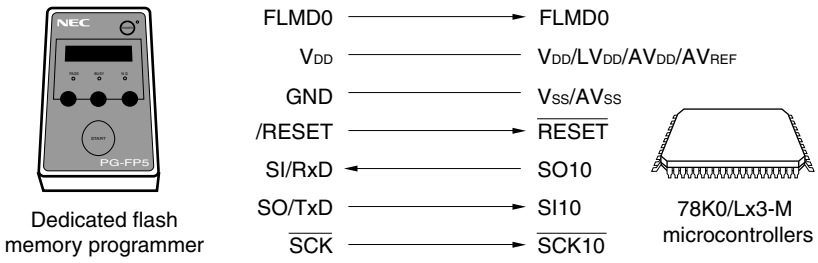
30.5 Communication Mode

Communication between the dedicated flash memory programmer and the 78K0/Lx3-M microcontrollers is established by serial communication via CSI10 or UART6 of the 78K0/Lx3-M microcontrollers,

(1) CSI10 (78K0/LG3-M only)

Transfer rate: 2.4 kHz to 2.5 MHz

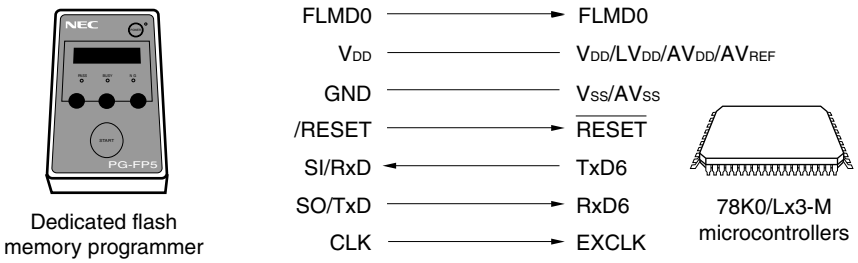
Figure 30-4. Communication with Dedicated Flash memory programmer (CSI10)



(2) UART6

Transfer rate: 115200 bps

Figure 30-5. Communication with Dedicated Flash memory programmer (UART6)



The dedicated flash memory programmer generates the following signals for the 78K0/Lx3-M microcontrollers. For details, refer to the user's manual for the PG-FP5 or FL-PR5.

Table 30-3. Pin Connection

Dedicated Flash memory programmer			78K0/Lx3-M microcontrollers	Connection	
Signal Name	I/O	Pin Function	Pin Name	CSI10	UART6
FLMD0	Output	Mode signal	FLMD0	◎	◎
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}, LV_{DD}, AV_{DD}, AV_{REF}	◎	◎
GND	–	Ground	V_{SS}, AV_{SS}	◎	◎
CLK	Output	Clock output to 78K0/Lx3-M microcontrollers	EXCLK/X2/P122	×Note 1	○Note 2
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎	◎
SI/RxD	Input	Receive signal	SO10 or TxD6	◎	◎
SO/TxD	Output	Transmit signal	SI10 or RxD6	◎	◎
SCK	Output	Transfer clock	$\overline{\text{SCK10}}$	◎	×

Notes 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. Only the X1 clock (f_X), external main system clock (f_{EXCLK}), or internal high-speed oscillation clock (f_{RH}) can be used when UART6 is used.

Remark ◎: Be sure to connect the pin.

○: The pin does not have to be connected if the signal is generated on the target board.

×: The pin does not have to be connected.

For the pins not to be used when the dedicated program adapter (FA series) is used, perform the processing described under the recommended connection of unused pins shown in **Table 2-2 Pin I/O Circuit Types**.

30.6 Connection of Pins on Board

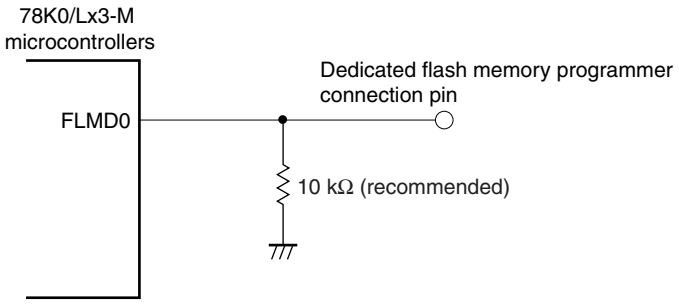
To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

30.6.1 FLMD0 pin

In the normal operation mode, 0 V is input to the FLMD0 pin. In the flash memory programming mode, the V_{DD} write voltage is supplied to the FLMD0 pin. An FLMD0 pin connection example is shown below.

Figure 30-6. FLMD0 Pin Connection Example



30.6.2 Serial interface pins

The pins used by each serial interface are listed below.

Table 30-4. Pins Used by Each Serial Interface

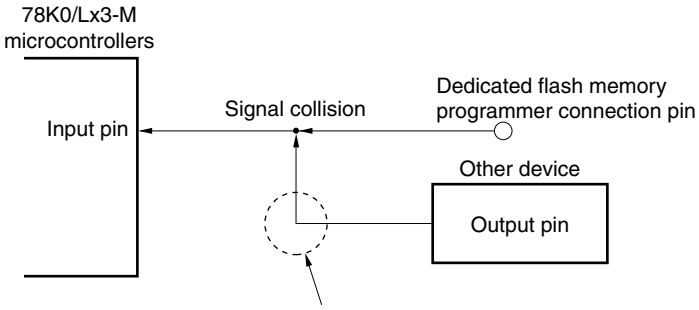
Serial Interface	Pins Used
CSI10	SO10, SI10, $\overline{SCK10}$
UART6	TxD6, RxD6

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(1) Signal collision

If the dedicated flash memory programmer (output) is connected to a pin (input) of a serial interface connected to another device (output), signal collision takes place. To avoid this collision, either isolate the connection with the other device, or make the other device go into an output high-impedance state.

Figure 30-7. Signal Collision (Input Pin of Serial Interface)

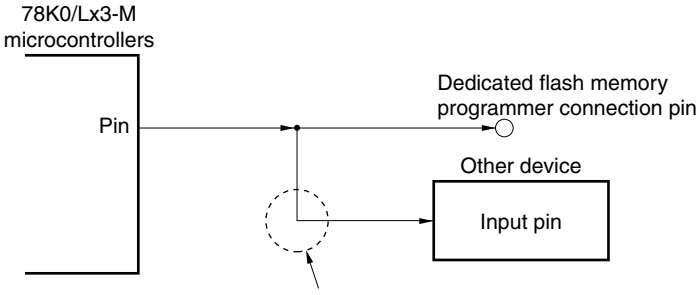


In the flash memory programming mode, the signal output by the device collides with the signal sent from the dedicated flash programmer. Therefore, isolate the signal of the other device.

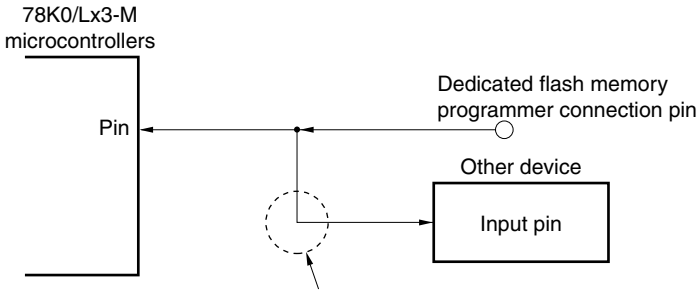
(2) Malfunction of other device

If the dedicated flash memory programmer (output or input) is connected to a pin (input or output) of a serial interface connected to another device (input), a signal may be output to the other device, causing the device to malfunction. To avoid this malfunction, isolate the connection with the other device.

Figure 30-8. Malfunction of Other Device



If the signal output by the 78K0/Lx3-M microcontrollers in the flash memory programming mode affects the other device, isolate the signal of the other device.



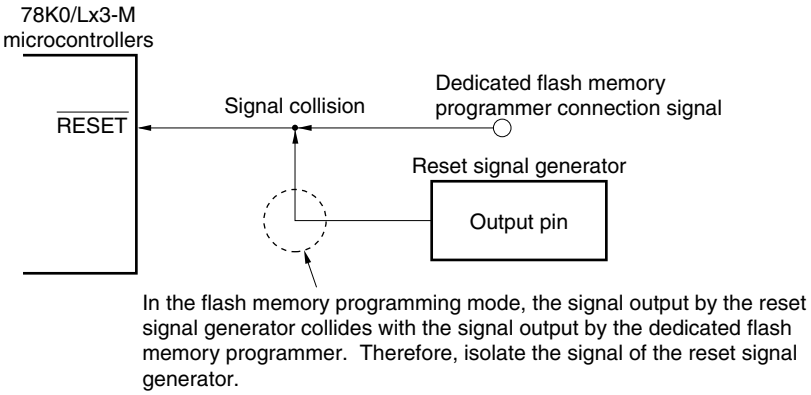
If the signal output by the dedicated flash memory programmer in the flash memory programming mode affects the other device, isolate the signal of the other device.

30.6.3 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 30-9. Signal Collision ($\overline{\text{RESET}}$ Pin)



30.6.4 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

30.6.5 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μF: recommended) in the same manner as during normal operation.

30.6.6 Other signal pins

Connect X1 and X2 in the same status as in the normal operation mode when using the on-board clock.

To input the operating clock from the dedicated flash memory programmer, however, connect CLK of the programmer to EXCLK/X2/P122.

Cautions 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. The X1 clock (f_X), external main system clock (f_{EXCLK}), or internal high-speed oscillation clock (f_{RH}) can be used when UART6 is used.

30.6.7 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer, even when using the on-board supply voltage.

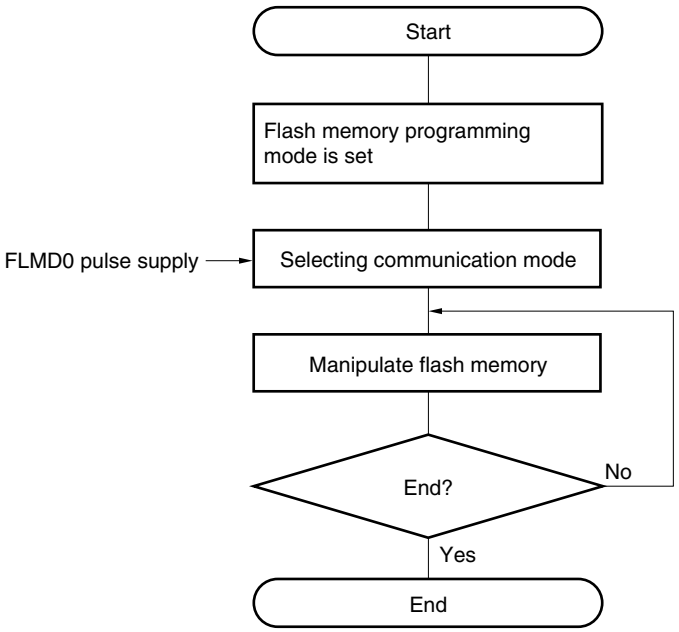
Supply the same other power supplies (AV_{DD}, LV_{DD}, AV_{REF}, and AV_{SS}) as those in the normal operation mode.

30.7 Programming Method

30.7.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 30-10. Flash Memory Manipulation Procedure



30.7.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/Lx3-M microcontrollers in the flash memory programming mode. To set the mode, set the FLMD0 pin to V_{DD} and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 30-11. Flash Memory Programming Mode

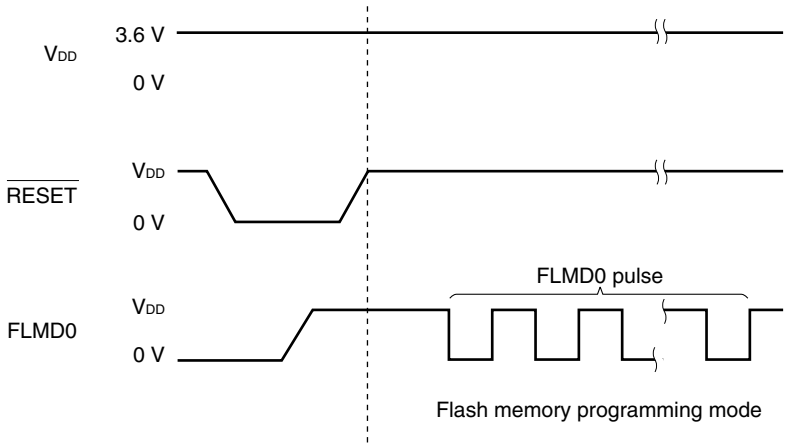


Table 30-5. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode

30.7.3 Selecting communication mode

In the 78K0/Lx3-M microcontrollers, a communication mode is selected by inputting pulses to the FLMD0 pin after the dedicated flash memory programming mode is entered. These FLMD0 pulses are generated by the flash memory programmer.

The following table shows the relationship between the number of pulses and communication modes.

Table 30-6. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used	Peripheral Clock	Number of FLMD0 Pulses
	Port	Speed	Frequency	Multiply Rate			
UART (UART6)	UART-Ext-OSC	115,200 bps[Note 3]	2 M to 10 MHz[Note 2]	1.0	TxD6, RxD6	f_X	0
	UART-Ext-FP5CLK					f_{EXCLK}	3
	UART-Internal-OSC		–			f_{RH}	5
3-wire serial I/O (CSI10)	CSI-Internal-OSC	2.4 kHz to 2.5 MHz	–		SO10, SI10, SCK10	f_{RH}	8

Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

2. The possible setting range differs depending on the voltage. For details, see **CHAPTER 33 ELECTRICAL SPECIFICATIONS**.

3. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

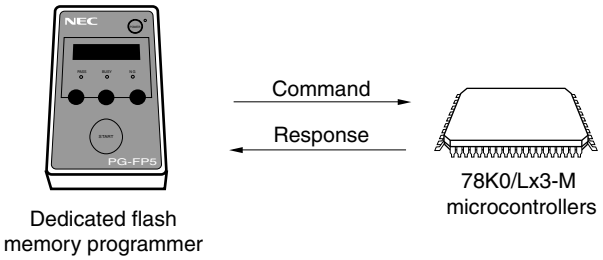
Caution When UART6 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash memory programmer after the FLMD0 pulse has been received.

Remark f_X: X1 clock
f_{EXCLK}: External main system clock
f_{RH}: Internal high-speed oscillation clock

30.7.4 Communication commands

The 78K0/Lx3-M microcontrollers communicates with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0/Lx3-M microcontrollers are called commands, and the signals sent from the 78K0/Lx3-M microcontrollers to the dedicated flash memory programmer are called response.

Figure 30-12. Communication Commands



The flash memory control commands of the 78K0/Lx3-M microcontrollers are listed in the table below. All these commands are issued from the programmer and the 78K0/Lx3-M microcontrollers perform processing corresponding to the respective commands.

Table 30-7. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Status	Gets the current operating status (status data).
	Silicon Signature	Gets 78K0/Lx3-M information (such as the part number and flash memory configuration).
	Version Get	Gets the 78K0/Lx3-M version and firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Oscillating Frequency Set	Specifies an oscillation frequency.

78K0/Lx3-M microcontrollers return a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0/Lx3-M microcontrollers are listed below.

Table 30-8. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

30.8 Security Settings

The 78K0/Lx3-M microcontrollers supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command. The security setting is valid when the programming mode is set next.

- Disabling batch erase (chip erase)
  Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited by this setting during on-board/off-board programming. Once execution of the batch erase (chip erase) command is prohibited, all of the prohibition settings (including prohibition of batch erase (chip erase)) can no longer be cancelled.

  Caution After the security setting for the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written, because the erase command is disabled.

- Disabling block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write
  Execution of the write and block erase commands for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

- Disabling rewriting boot cluster 0
  Execution of the block erase command, and write command on boot cluster 0 (0000H to 0FFFH) in the flash memory is prohibited by this setting. Execution of the batch erase (chip erase) command is prohibited.

  Caution If a security setting that rewrites boot cluster 0 has been applied, boot cluster 0 of that device and batch erase (chip erase) will not be rewritten.

The batch erase (chip erase), block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by on-board/off-board programming and self programming. Each security setting can be used in combination.

Prohibition of erasing blocks and writing is cleared by executing the batch erase (chip erase) command.

Table 30-9 shows the relationship between the erase and write commands when the 78K0/Lx3-M microcontrollers security function is enabled.

Table 30-9. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command		
	Batch Erase (Chip Erase)	Block Erase	Write
Prohibition of batch erase (chip erase)	Cannot be erased in batch	Blocks cannot be erased.	Can be performed[Note].
Prohibition of block erase	Can be erased in batch.		Can be performed.
Prohibition of writing			Cannot be performed.
Prohibition of rewriting boot cluster 0	Cannot be erased in batch	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after batch erase (chip erase) is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of batch erase (chip erase)	Blocks can be erased.	Can be performed.
Prohibition of block erase		
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Table 30-10 shows how to perform security settings in each programming mode.

Table 30-10. Setting Security in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set by using information library.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

30.9 Flash Memory Programming by Self-Programming

The 78K0/Lx3-M microcontrollers support a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the self-programming library, it can be used to upgrade the program in the field.

If an interrupt occurs during self-programming, self-programming can be temporarily stopped and interrupt servicing can be executed. To execute interrupt servicing, restore the normal operation mode after self-programming has been stopped, and execute the EI instruction. After the self-programming mode is later restored, self-programming can be resumed.

Cautions 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

2. Oscillation of the internal high-speed oscillator is started during self programming, regardless of the setting of the RSTOP flag (bit 0 of the internal oscillation mode register (RCM)). Oscillation of the internal high-speed oscillator cannot be stopped even if the STOP instruction is executed.

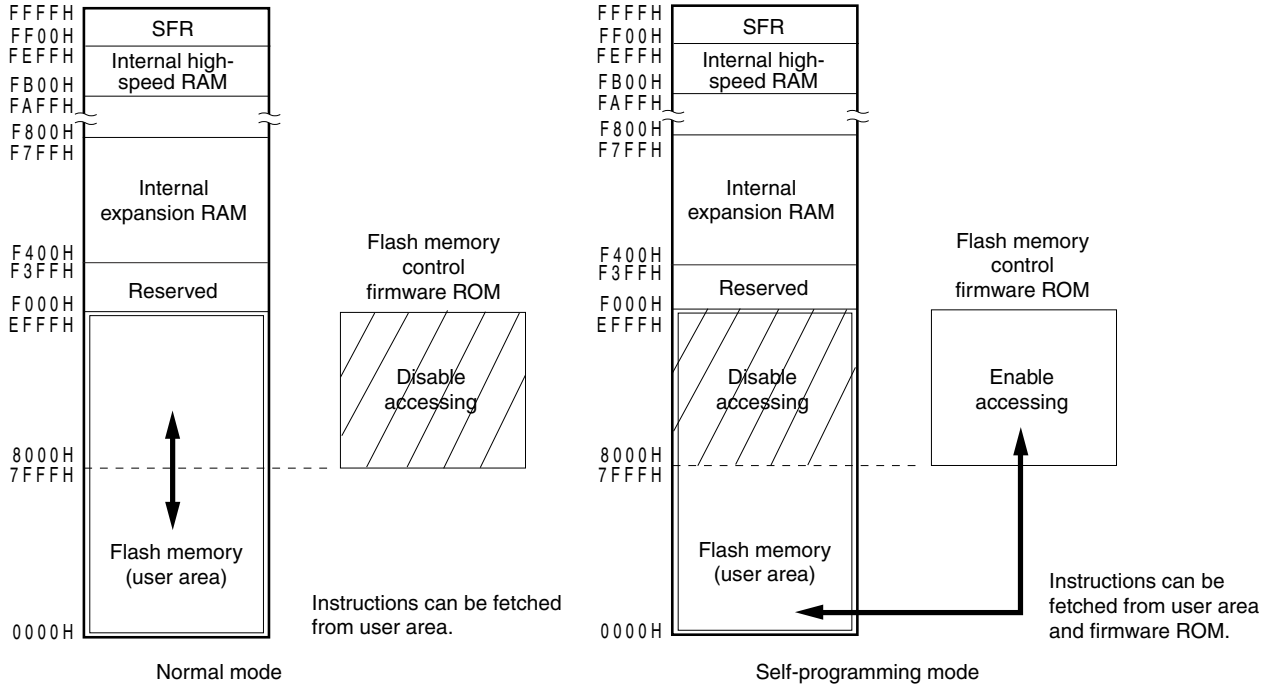
3. Input a high level to the FLMD0 pin during self-programming.

4. Be sure to execute the DI instruction before starting self-programming.
The self-programming function checks the interrupt request flags (IF0L, IF0H, IF1L, and IF1H). If an interrupt request is generated, self-programming is stopped.

5. Self-programming is also stopped by an interrupt request that is not masked even in the DI status. To prevent this, mask the interrupt by using the interrupt mask flag registers (MK0L, MK0H, MK1L, and MK1H).

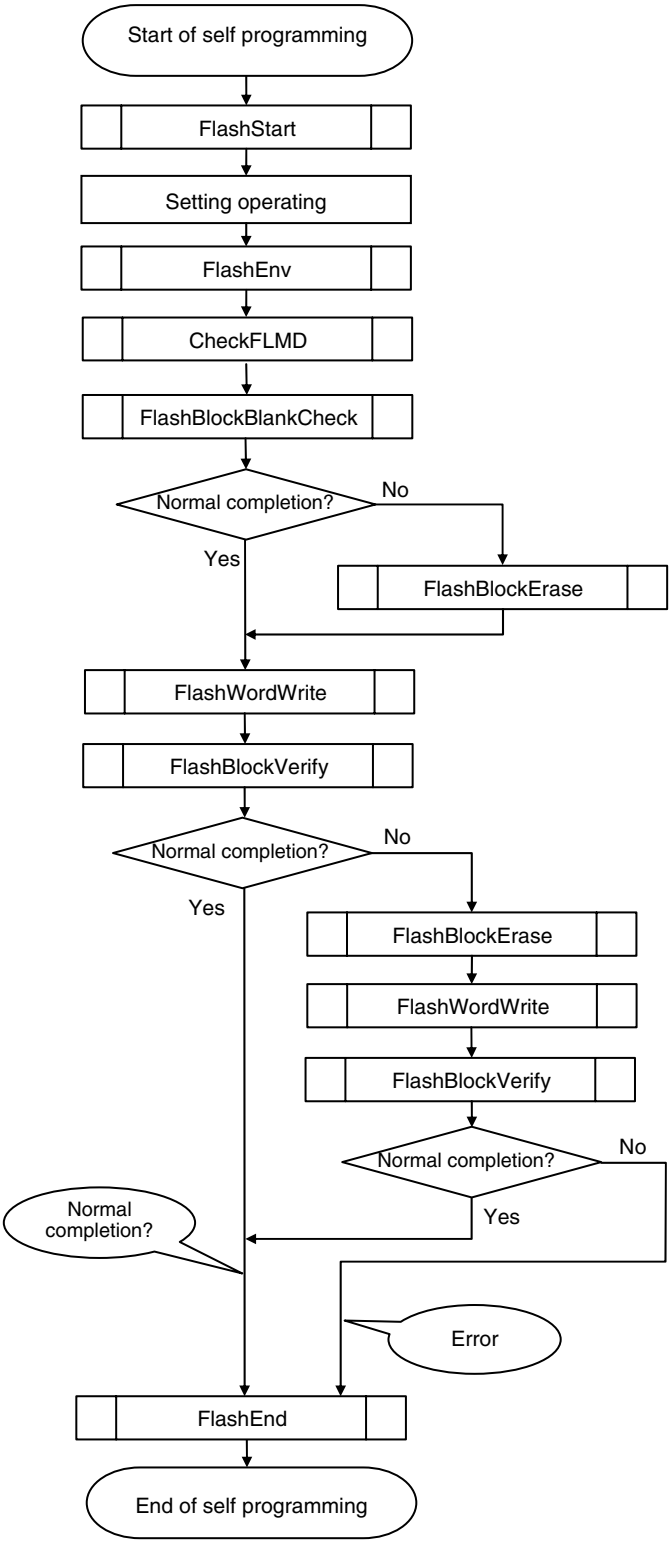
6. Allocate the entry program for self-programming in the 0000H to 7FFFH.

Figure 30-13. Operation Mode and Memory Map for Self-Programming (μPD78F8055)



The following figure illustrates a flow of rewriting the flash memory by using a self programming sample library.

Figure 30-14. Flow of Self Programming (Rewriting Flash Memory)



Remark For details of the self programming library, refer to **78K0 Microcontroller Self-Programming Library Type01 User's Manual (U18274E)**.

30.9.1 Boot swap function

If rewriting the boot area has failed during self-programming due to a power failure or some other cause, the data in the boot area may be lost and the program may not be restarted by resetting.

The boot swap function is used to avoid this problem.

Before erasing boot cluster 0[Note], which is a boot program area, by self-programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the 78K0/Lx3-M microcontrollers, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

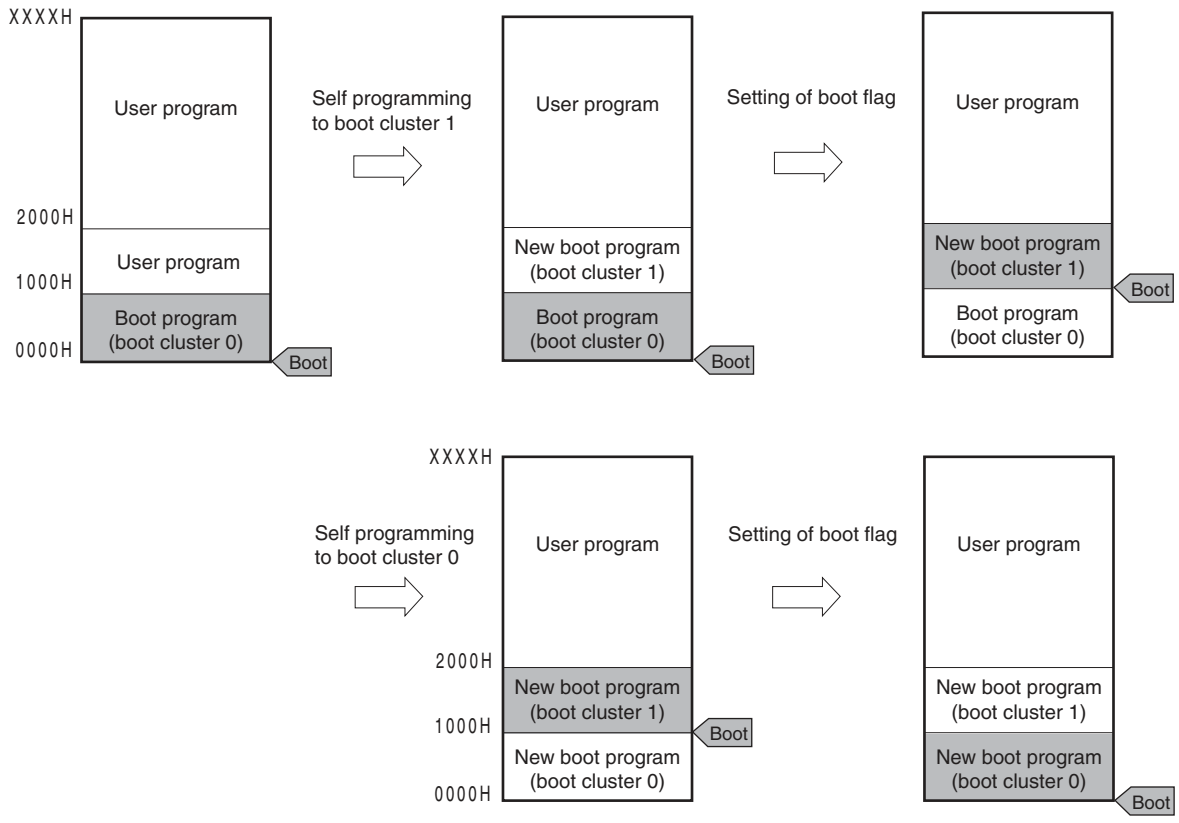
As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

If the program has been correctly written to boot cluster 0, restore the original boot area by using the set information function of the firmware of the 78K0/Lx3-M microcontrollers.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

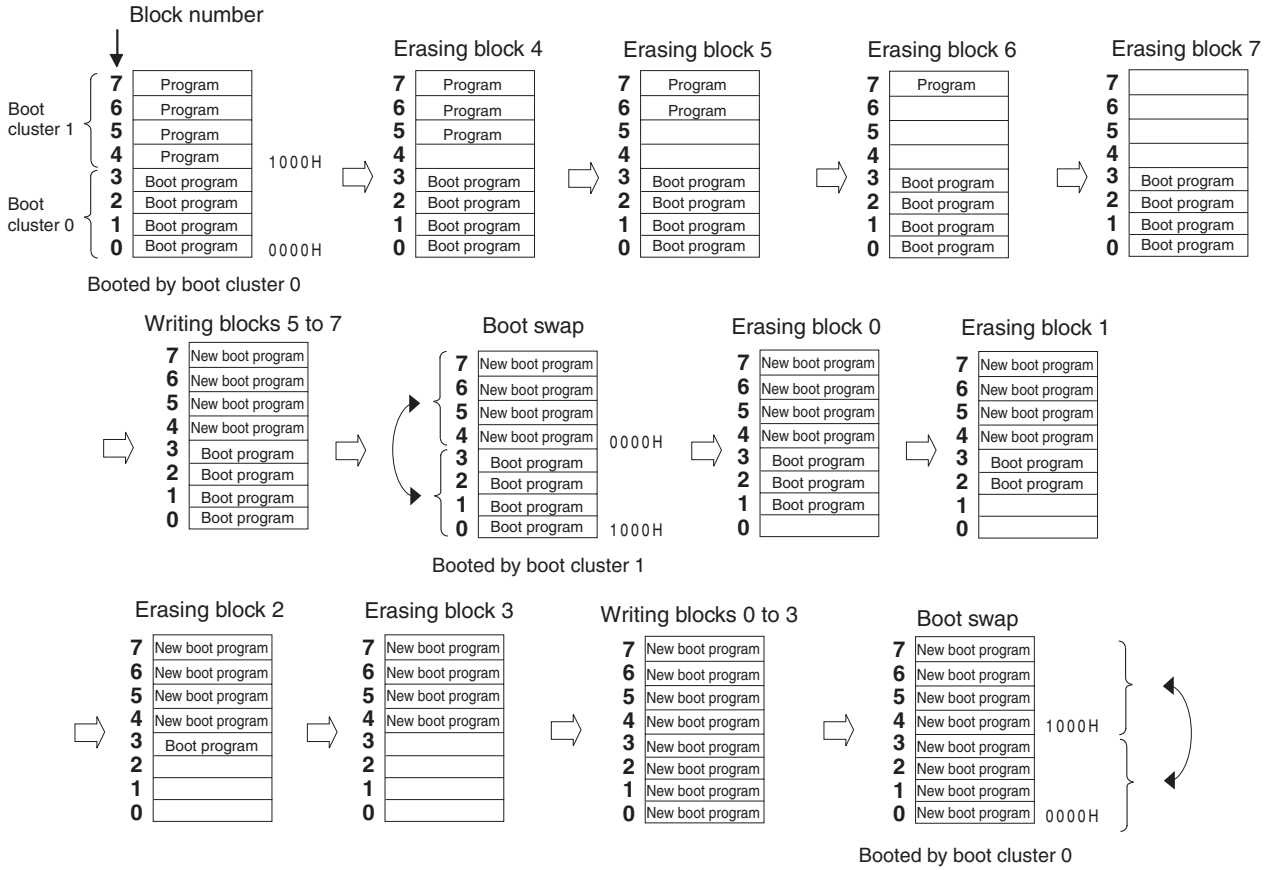
Boot cluster 0 (0000H to 0FFFH): Original boot program area
Boot cluster 1 (1000H to 1FFFH): Area subject to boot swap function

Figure 30-15. Boot Swap Function



Remark Boot cluster 1 becomes 0000H to 0FFFH when a reset is generated after the boot flag has been set.

Figure 30-16. Example of Executing Boot Swapping



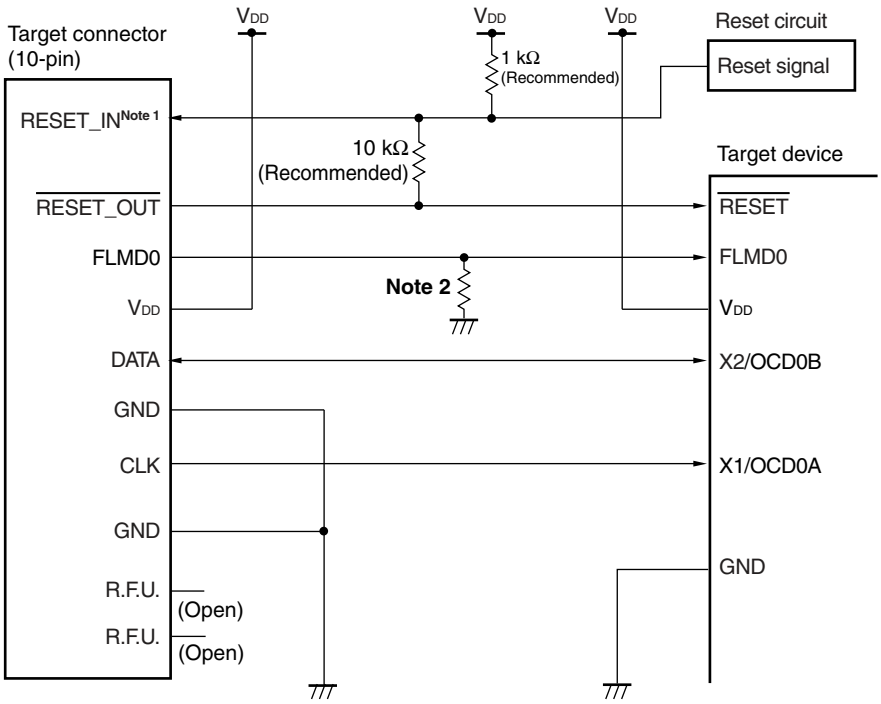
CHAPTER 31 ON-CHIP DEBUG FUNCTION

31.1 Connecting QB-MINI2 to 78K0/Lx3-M microcontrollers

The 78K0/Lx3-M microcontrollers uses the V_{DD}, FLMD0, $\overline{RESET}$, OCD0A/X1, OCD0B/X2, and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Caution The 78K0/Lx3-M microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 31-1. Connection Example of QB-MINI2 and 78K0/Lx3-M microcontrollers



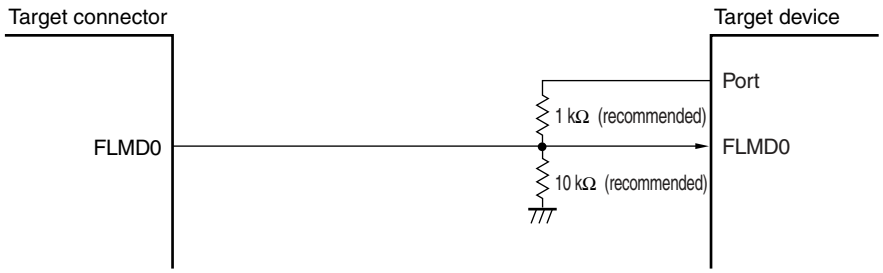
Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

Caution Input the clock from the OCD0A/X1 pin during on-chip debugging.

Connect the FLMD0 pin as follows when performing self programming by means of on-chip debugging.

Figure 31-2. Connection of FLMD0 Pin for Self Programming by Means of On-Chip Debugging



Caution When using the port that controls the FLMD0 pin, make sure that it satisfies the values of the high-level output current and FLMD0 supply voltage (minimum value: 0.8V_{DD}) stated in CHAPTER 33 ELECTRICAL SPECIFICATIONS.

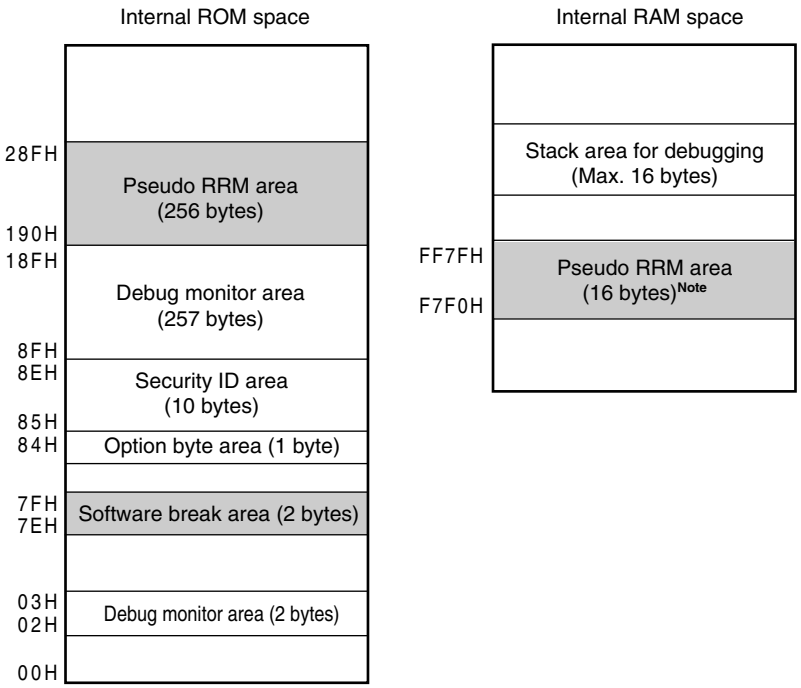
31.2 Reserved Area Used by QB-MINI2

QB-MINI2 uses the reserved areas shown in Figure 31-3 below to implement communication with the 78K0/Lx3-M microcontrollers, or each debug function. The shaded reserved areas are used for the respective debug functions to be used, and the other areas are always used for debugging. These reserved areas can be secured by using user programs and compiler options.

When using a boot swap operation during self programming, set the same value to boot cluster 1 beforehand.

For details on reserved area, refer to **QB-MINI2 User's Manual (U18371E)**.

Figure 31-3. Reserved Area Used by QB-MINI2



Note With products not incorporated the internal expansion RAM (78K0/LE3-M), it is not necessary to secure this area.

Remark Shaded reserved areas: Area used for the respective debug functions to be used
Other reserved areas: Areas always used for debugging

CHAPTER 32 INSTRUCTION SET

This chapter lists each instruction set of the 78K0/Lx3-M microcontrollers in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

32.1 Conventions Used in Operation List

32.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 32-1. Operand Identifiers and Specification Methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, see **Table 3-8 Special Function Register List**.

32.1.2 Description of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
RBS: Register bank select flag
IE: Interrupt request enable flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\ \ }$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

32.1.3 Description of flag operation column

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

32.2 Operation List

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	**MOV**	r, #byte	2	4	–	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	–	7	sfr ← byte	
		A, r Note 3	1	2	–	A ← r	
		r, A Note 3	1	2	–	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	–	5	A ← sfr	
		sfr, A	2	–	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	–	7	PSW ← byte	× × ×
		A, PSW	2	–	5	A ← PSW	
		PSW, A	2	–	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL + byte]	2	8	9	A ← (HL + byte)	
		[HL + byte], A	2	8	9	(HL + byte) ← A	
		A, [HL + B]	1	6	7	A ← (HL + B)	
		[HL + B], A	1	6	7	(HL + B) ← A	
		A, [HL + C]	1	6	7	A ← (HL + C)	
		[HL + C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	–	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	–	6	A ↔ (sfr)	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL + byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL + B]	2	8	10	A ↔ (HL + B)	
		A, [HL + C]	2	8	10	A ↔ (HL + C)	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	–	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	–	8	AX ← sfrp	
		sfrp, AX	2	–	8	sfrp ← AX	
		AX, rp Note 3	1	4	–	AX ← rp	
		rp, AX Note 3	1	4	–	rp ← AX	
		AX, !addr16	3	10	12	AX ← (addr16)	
		!addr16, AX	3	10	12	(addr16) ← AX	
	XCHW	AX, rp Note 3	1	4	–	AX ↔ rp	
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r	× × ×
		r, A	2	4	–	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r + CY	× × ×
		r, A	2	4	–	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + C	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE or HL

4. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r	× × ×
		r, A	2	4	–	r, CY ← r – A	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	× × ×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	× × ×
		r, A	2	4	–	r, CY ← r – A – CY	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	× × ×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×
		A, r Note 3	2	4	–	A ← A ∧ r	×
		r, A	2	4	–	r ← r ∧ A	×
		A, saddr	2	4	5	A ← A ∧ (saddr)	×
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×
		A, [HL]	1	4	5	A ← A ∧ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×
		A, r Note 3	2	4	–	A ← A ∨ r	×
		r, A	2	4	–	r ← r ∨ A	×
		A, saddr	2	4	5	A ← A ∨ (saddr)	×
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×
		A, [HL]	1	4	5	A ← A ∨ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×
	XOR	A, #byte	2	4	–	A ← A ⊻ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⊻ byte	×
		A, r Note 3	2	4	–	A ← A ⊻ r	×
		r, A	2	4	–	r ← r ⊻ A	×
		A, saddr	2	4	5	A ← A ⊻ (saddr)	×
		A, !addr16	3	8	9	A ← A ⊻ (addr16)	×
		A, [HL]	1	4	5	A ← A ⊻ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ⊻ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ⊻ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ⊻ (HL + C)	×
	CMP	A, #byte	2	4	–	A – byte	× × ×
		saddr, #byte	3	6	8	(saddr) – byte	× × ×
		A, r Note 3	2	4	–	A – r	× × ×
		r, A	2	4	–	r – A	× × ×
		A, saddr	2	4	5	A – (saddr)	× × ×
		A, !addr16	3	8	9	A – (addr16)	× × ×
		A, [HL]	1	4	5	A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A – (HL + C)	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit operation	**ADDW**	AX, #word	3	6	–	AX, CY ← AX + word	× × ×
	SUBW	AX, #word	3	6	–	AX, CY ← AX – word	× × ×
	CMPW	AX, #word	3	6	–	AX – word	× × ×
Multiply/ divide	**MULU**	X	2	16	–	AX ← A × X	
	DIVUW	C	2	25	–	AX (Quotient), C (Remainder) ← AX ÷ C	
Increment/ decrement	**INC**	r	1	2	–	r ← r + 1	× ×
		saddr	2	4	6	(saddr) ← (saddr) + 1	× ×
	DEC	r	1	2	–	r ← r – 1	× ×
		saddr	2	4	6	(saddr) ← (saddr) – 1	× ×
	INCW	rp	1	4	–	rp ← rp + 1	
	DECW	rp	1	4	–	rp ← rp – 1	
Rotate	**ROR**	A, 1	1	2	–	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1 time	×
	ROL	A, 1	1	2	–	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1 time	×
	RORC	A, 1	1	2	–	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1 time	×
	ROLC	A, 1	1	2	–	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1 time	×
	ROR4	[HL]	2	10	12	A_{3-0} ← $(HL)_{3-0}$, $(HL)_{7-4}$ ← A_{3-0}, $(HL)_{3-0}$ ← $(HL)_{7-4}$	
	ROL4	[HL]	2	10	12	A_{3-0} ← $(HL)_{7-4}$, $(HL)_{3-0}$ ← A_{3-0}, $(HL)_{7-4}$ ← $(HL)_{3-0}$	
BCD adjustment	**ADJBA**		2	4	–	Decimal Adjust Accumulator after Addition	× × ×
	ADJBS		2	4	–	Decimal Adjust Accumulator after Subtract	× × ×
Bit manipulate	**MOV1**	CY, saddr.bit	3	6	7	CY ← (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← sfr.bit	×
		CY, A.bit	2	4	–	CY ← A.bit	×
		CY, PSW.bit	3	–	7	CY ← PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← (HL).bit	×
		saddr.bit, CY	3	6	8	(saddr.bit) ← CY	
		sfr.bit, CY	3	–	8	sfr.bit ← CY	
		A.bit, CY	2	4	–	A.bit ← CY	
		PSW.bit, CY	3	–	8	PSW.bit ← CY	× ×
		[HL].bit, CY	2	6	8	(HL).bit ← CY	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Bit manipulate	**AND1**	CY, saddr.bit	3	6	7	CY ← CY ∧ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ∧ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ∧ A.bit	×
		CY, PSW.bit	3	–	7	CY ← CY ∧ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ∧ (HL).bit	×
	OR1	CY, saddr.bit	3	6	7	CY ← CY ∨ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ∨ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ∨ A.bit	×
		CY, PSW.bit	3	–	7	CY ← CY ∨ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ∨ (HL).bit	×
	XOR1	CY, saddr.bit	3	6	7	CY ← CY ⊻ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ⊻ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ⊻ A.bit	×
		CY, PSW. bit	3	–	7	CY ← CY ⊻ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ⊻ (HL).bit	×
	SET1	saddr.bit	2	4	6	(saddr.bit) ← 1	
		sfr.bit	3	–	8	sfr.bit ← 1	
		A.bit	2	4	–	A.bit ← 1	
		PSW.bit	2	–	6	PSW.bit ← 1	× × ×
		[HL].bit	2	6	8	(HL).bit ← 1	
	CLR1	saddr.bit	2	4	6	(saddr.bit) ← 0	
		sfr.bit	3	–	8	sfr.bit ← 0	
		A.bit	2	4	–	A.bit ← 0	
		PSW.bit	2	–	6	PSW.bit ← 0	× × ×
		[HL].bit	2	6	8	(HL).bit ← 0	
	SET1	CY	1	2	–	CY ← 1	1
	CLR1	CY	1	2	–	CY ← 0	0
	NOT1	CY	1	2	–	CY ← $\overline{CY}$	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Call/return	**CALL**	!addr16	3	7	–	(SP – 1) ← (PC + 3)H, (SP – 2) ← (PC + 3)L, PC ← addr16, SP ← SP – 2	
	CALLF	!addr11	2	5	–	(SP – 1) ← (PC + 2)H, (SP – 2) ← (PC + 2)L, PC15 – 11 ← 00001, PC10 – 0 ← addr11, SP ← SP – 2	
	CALLT	[addr5]	1	6	–	(SP – 1) ← (PC + 1)H, (SP – 2) ← (PC + 1)L, PCH ← (addr5 + 1), PCL ← (addr5), SP ← SP – 2	
	BRK		1	6	–	(SP – 1) ← PSW, (SP – 2) ← (PC + 1)H, (SP – 3) ← (PC + 1)L, PCH ← (003FH), PCL ← (003EH), SP ← SP – 3, IE ← 0	
	RET		1	6	–	PCH ← (SP + 1), PCL ← (SP), SP ← SP + 2	
	RETI		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
	RETB		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
Stack manipulate	**PUSH**	PSW	1	2	–	(SP – 1) ← PSW, SP ← SP – 1	
		rp	1	4	–	(SP – 1) ← rpH, (SP – 2) ← rpL, SP ← SP – 2	
	POP	PSW	1	2	–	PSW ← (SP), SP ← SP + 1	R R R
		rp	1	4	–	rpH ← (SP + 1), rpL ← (SP), SP ← SP + 2	
	MOVW	SP, #word	4	–	10	SP ← word	
		SP, AX	2	–	8	SP ← AX	
		AX, SP	2	–	8	AX ← SP	
Unconditional branch	**BR**	!addr16	3	6	–	PC ← addr16	
		$addr16	2	6	–	PC ← PC + 2 + jdisp8	
		AX	2	8	–	PCH ← A, PCL ← X	
Conditional branch	**BC**	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 1	
	BNC	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 0	
	BZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 1	
	BNZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 0	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Conditional branch	**BT**	saddr.bit, $addr16	3	8	9	PC ← PC + 3 + jdisp8 if (saddr.bit) = 1	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1	
		PSW.bit, $addr16	3	–	9	PC ← PC + 3 + jdisp8 if PSW.bit = 1	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 1	
	BF	saddr.bit, $addr16	4	10	11	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 0	
		PSW.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 0	
	BTCLR	saddr.bit, $addr16	4	10	12	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1 then reset (saddr.bit)	
		sfr.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit	
		PSW.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	× × ×
		[HL].bit, $addr16	3	10	12	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit	
	DBNZ	B, $addr16	2	6	–	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
		C, $addr16	2	6	–	C ← C –1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
		saddr, $addr16	3	8	10	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
CPU control	**SEL**	RBn	2	4	–	RBS1, 0 ← n	
	NOP		1	2	–	No Operation	
	EI		2	–	6	IE ← 1 (Enable Interrupt)	
	DI		2	–	6	IE ← 0 (Disable Interrupt)	
	HALT		2	6	–	Set HALT Mode	
	STOP		2	6	–	Set STOP Mode	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

32.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except “r = A”

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand / First Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

CHAPTER 33 ELECTRICAL SPECIFICATIONS

Caution The 78K0/Lx3-M microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +4.6	V
	LV_{DD}		−0.5 to +4.6	V
	AV_{DD}		−0.5 to LV_{DD} +0.5 Note 2	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} +0.3 Note 2	V
	AV_{REFIN} Note 1		−0.5 to AV_{DD} +0.5 Note 2	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD}	V
Input voltage	V_I	P11 to P13, P20 to P27, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120 to P123, P130 to P133, P140 to P143, P150 to P153, X1, X2, FLMD0	−0.3 to V_{DD} + 0.3 Note 2	V
	V_2	LP00 to LP05, LP10 to LP15, XT1, $\overline{\text{RESET}}$	−0.3 to LV_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P11 to P13, P20 to P27, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120, P130 to P133, P140 to P143, P150 to P153, COM0 to COM3, SEG0 to SEG3	−0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	−0.3 to LV_{DD} +0.3 Note 2	V
Analog input voltage	V_{AN1}	ANI0 to ANI7	−0.3 to AV_{REF} + 0.3 Note 2 and −0.3 to V_{DD} + 0.3 Note 2	V
	V_{AN2}	ANI00, ANI01, ANI10, ANI11, ANI20, ANI21, ANI30, ANI31	−0.5 to AV_{DD} + 0.5 Note 2	V

Notes 1. Voltage applied at AV_{REFIO} pin

2. Must be 4.6 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	−4	mA
			P11 to P13, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120, P130 to P133, P140 to P143, P150 to P153	−10	mA
<R>		Total of all pins −72 mA	P11 to P13, P30 to P33, P40 to P45, P120	−25	mA
<R>			P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	−12	mA
			LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	−35	mA
	I_{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	4	mA
			P11 to P13, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120, P130 to P133, P140 to P143, P150 to P153	30	mA
		Total of all pins 115 mA	P11 to P13, P30 to P33, P40 to P45, P120	40	mA
			P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	40	mA
			LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	35	mA
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

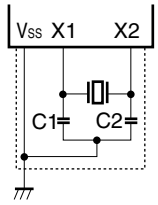
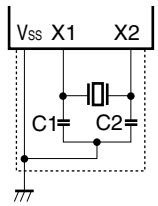
Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

X1 Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 3.6 V	2.0		10.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 3.6 V	2.0		10.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested oscillation themselves or apply to the resonator manufacturer for evaluation.

Internal Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

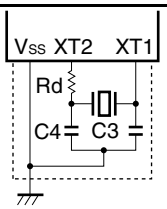
Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
8 MHz internal oscillator	Internal high-speed oscillation clock frequency (f_{RH})Note	RSTS = 1	2.5 V ≤ V_{DD} ≤ 3.6 V	7.6	8.0	8.4	MHz
			1.8 V ≤ V_{DD} < 2.5 V	6.75	8.0	8.4	MHz
		RSTS = 0		2.48	5.6	9.86	MHz
240 kHz internal oscillator	Internal low-speed oscillation clock frequency (f_{RL})	2.6 V ≤ V_{DD} ≤ 3.6 V		216	240	264	kHz
		1.8 V ≤ V_{DD} < 2.6 V		192	240	264	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Remark RSTS: Bit 7 of the internal oscillation mode register (RCM)

XT1 Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})Note		31	32.768	39	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (1/6)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V			–2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Per pin for P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	2.7 V ≤ V_{DD} ≤ 3.6 V			–0.1	mA
			1.8 V ≤ V_{DD} < 2.7 V			–0.1	mA
		Per pin for LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V			–2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Total[Note 2] of P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total[Note 2] of P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	2.7 V ≤ V_{DD} ≤ 3.6 V			–2.8	mA
			1.8 V ≤ V_{DD} < 2.7 V			–2.8	mA
		Total[Note 2] of LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total[Note 2] of all pins	2.7 V ≤ V_{DD} ≤ 3.6 V			–22.8	mA
			1.8 V ≤ V_{DD} < 2.7 V			–12.8	mA
	I_{OH2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			–0.1	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = –20.0 mA

Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/6)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Per pin for P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	2.7 V ≤ V_{DD} ≤ 3.6 V			0.4	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.4	mA
		Per pin for LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V			2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			1.0	mA
		Total[Note 2] of P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total[Note 2] of P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	2.7 V ≤ V_{DD} ≤ 3.6 V			11.2	mA
			1.8 V ≤ V_{DD} < 2.7 V			11.2	mA
		Total[Note 2] of LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total[Note 2] of all pins	2.7 V ≤ V_{DD} ≤ 3.6 V			41.2	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.2	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

2. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = –20.0 mA

Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/6)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P32, P80 to P83, P90 to P93, P100 to P103, P110 to P112, P130 to P133, P140 to P143, P150 to P153		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P11 to P13, P30, P31, P33, P40 to P45, P113, P120 to P123, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	LP00 to LP05, LP10 to LP15		0.7LV_{DD}		LV_{DD}	V
<R>	V_{IH5}	$\overline{RESET}$, EXCLKS		0.8LV_{DD}		LV_{DD}	V
Input voltage, low	V_{IL1}	P32, P80 to P83, P90 to P93, P100 to P103, P110 to P112, P130 to P133, P140 to P143, P150 to P153		0		0.3V_{DD}	V
	V_{IL2}	P11 to P13, P30, P31, P33, P40 to P45, P113, P120 to P123, EXCLK		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL4}	LP00 to LP05, LP10 to LP15		0		0.3LV_{DD}	V
<R>	V_{IL5}	$\overline{RESET}$, EXCLKS		0		0.2LV_{DD}	V
Output voltage, high	V_{OH1}	P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
		P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	I_{OH1} = –0.1 mA	V_{DD} – 0.5			V
<R>		LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH1} = –2.5 mA	LV_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	LV_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P11 to P13, P30 to P33, P40 to P45, P120	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL1} = 5.0 mA			0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA			0.4	V
		P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	I_{OL1} = 0.4 mA			0.4	V
		LP00 to LP05, LP10 to LP15, CF, TxD0, RTC1HZ	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL1} = 2.5 mA			0.4	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA			0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The high-level and low-level input voltages of P122/EXCLK vary between the input port mode and external clock mode.

DC Characteristics (4/6)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

	Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
	Input leakage current, high	I_{LIH1}	P11 to P13, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120, P123, P130 to P133, P140 to P143, P150 to P153, FLMD0	$V_I = V_{DD}$				1	μA
		I_{LIH2}	P20 to P27	$V_I = AV_{REF} = V_{DD}$				1	μA
		I_{LIH3}	P121, P122 (X1, X2)	$V_I = V_{DD}$	I/O port mode			1	μA
					OSC mode			20	μA
<R>		I_{LIH4}	XT1, XT2	$V_I = LV_{DD}$				5	μA
<R>		I_{LIH5}	LP00 to LP05, LP10 to LP15, $\overline{RESET}$	$V_I = LV_{DD}$				5	μA
	Input leakage current, low	I_{LIL1}	P11 to P13, P30 to P33, P40 to P45, P80 to P83, P90 to P93, P100 to P103, P110 to P113, P120, P123, P130 to P133, P140 to P143, P150 to P153, FLMD0	$V_I = V_{SS}$				–1	μA
		I_{LIL2}	P20 to P27	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				–1	μA
		I_{LIL3}	P121, P122 (X1, X2)	$V_I = V_{SS}$	I/O port mode			–1	μA
					OSC mode			–20	μA
<R>		I_{LIL4}	XT1, XT2	$V_I = V_{SS}$				–5	μA
<R>		I_{LIL5}	LP00 to LP05, LP10 to LP15, $\overline{RESET}$	$V_I = V_{SS}$				–5	μA
	Pull-up resistor	R_U	$V_I = V_{SS}$			10	20	100	kΩ
	FLMD0 supply voltage	V_{IL}	In normal operation mode			0		$0.2V_{DD}$	V
		V_{IH}	In self-programming mode			$0.8V_{DD}$		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

<R> **DC Characteristics (5/6)**

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = AV_{REF} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{XH} = 10 MHz Note 2, V_{DD} = 3.0 V	Square wave input			1.74	2.9	mA
				Resonator connection			1.9	3.3	
			f_{SUB} = 32.768 kHz Note 3, V_{DD} = LV_{DD} = 3.0 V	Square wave input	V_{DD} current		4.8	26	μA
					LV_{DD} current		2.5	47	
				Resonator connection	V_{DD} current		4.8	26	
					LV_{DD} current		2.5	47	
	I_{DD2} Note 1	HALT mode	f_{XH} = 10 MHz Note 2, V_{DD} = 3.0 V	Square wave input			0.38	1.4	mA
				Resonator connection			0.45	1.7	
			f_{SUB} = 32.768 kHz Note 3, V_{DD} = LV_{DD} = 3.0 V	Square wave input	V_{DD} current		2.39	22	μA
					LV_{DD} current		2.5	47	
				Resonator connection	V_{DD} current		2.39	22	
					LV_{DD} current		2.5	47	
	I_{DD3} Note 4	STOP mode	V_{DD} = LV_{DD} = 3.0 V	–40 to +85°C			1.2	57	μA
				–40 to +60°C				18	

Notes 1. Total current flowing into the internal power supply (V_{DD}), including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX. values include the peripheral operation current. However, the current flowing into the pull-up resistors and the output current of the port are not included.

2. Not including the operating current of the 8 MHz internal oscillator, 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer, LVI circuit, LCD controller/driver, real-time counter, and power calculation circuit.

3. Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer, LVI circuit, LCD controller/driver, real-time counter, and power calculation circuit.

4. Total current flowing into the internal power supply (V_{DD}), including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors and the output current of the port, the operating current of the 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer, LVI circuit, LCD controller/driver, real-time counter, and power calculation circuit are not included.

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

<R> **DC Characteristics (6/6)**

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = AV_{REF} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Watchdog timer operating current	I_{WDT} Note 1	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI} Note 2					9	18	μA
Successive approximation type A/D converter operating current	I_{ADC1} Note 3	AV_{REF} = 2.3 to 3.6 V, ADCE = 1				0.86	1.9	mA
LCD operating current	I_{LCD1} Note 5	f_{PRS} = 10 MHz, LCD source clock (f_{LCD}) = $f_{PRS}/2^6$, LCD clock (LCDCL) = $f_{LCD}/2^4$, When four-time-slice display mode	LCD non-display wave output	V_{DD} = 3.0 V		2.0	5.0	μA
	I_{LCD2} Note 5		LCD display wave output	V_{DD} = 3.0 V		2.0	5.0	μA
RTC operating current	I_{RTC} Note 6	LV_{DD} = 3.0 V, V_{DD} = 0 V		–40 to +85°C		2.5	41	μA
				–40 to +60°C			14	μA
		VDD = LVDD = 3.0 V, CPU operating in STOP mode		–40 to +85°C		4.0	61	μA
				–40 to +60°C			22	μA
ΔΣ-type A/D converter operating current	I_{ADC2} Note 4					8.1	13.5	mA
Power calculation circuit operating current	I_{CAL} Notes 7, 8	Power calculation, power quality measurement, and DFC operating current.				3.7	4.5	mA

Notes 1. This includes only the current that flows through the watchdog timer (including the operating current of the 240 kHz internal oscillator). When the watchdog timer is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{WDT} to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

2. This includes only the current that flows through the LVI circuit. When the LVI circuit is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{LVI} to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

3. This includes only the current that flows through the successive approximation type A/D converter (AV_{REF}-AV_{SS}). When the successive approximation type A/D converter is operating in operation mode or HALT mode, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{ADC1} to the supply current (I_{DD1} or I_{DD2}).

4. This includes only the current that flows through the ΔΣ-type A/D converter(AV_{DD}). When the ΔΣ-type A/D converter is operating in operation mode or HALT mode, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{ADC2} to the supply current (I_{DD1} or I_{DD2}).

5. This includes only the current that flows through the LCD controller/driver. Not including the current that flows through the LCD divider resistor. The current value of the 78K0/Lx3-M microcontrollers is obtained by adding the LCD operating current (I_{LCD1} or I_{LCD2}) to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

6. This includes only the current that flows through the real-time counter. When the real-time counter is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{RTC} to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

7. This includes only the current that flows through the power calculation circuit. When the power calculation circuit is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{CAL} to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

8. If the typical value of V_{DD}, AV_{DD}, and LV_{DD} is 3.3 V, this current flows to the AV_{DD} and LV_{DD} pins.

AC Characteristics

(1) Basic operation

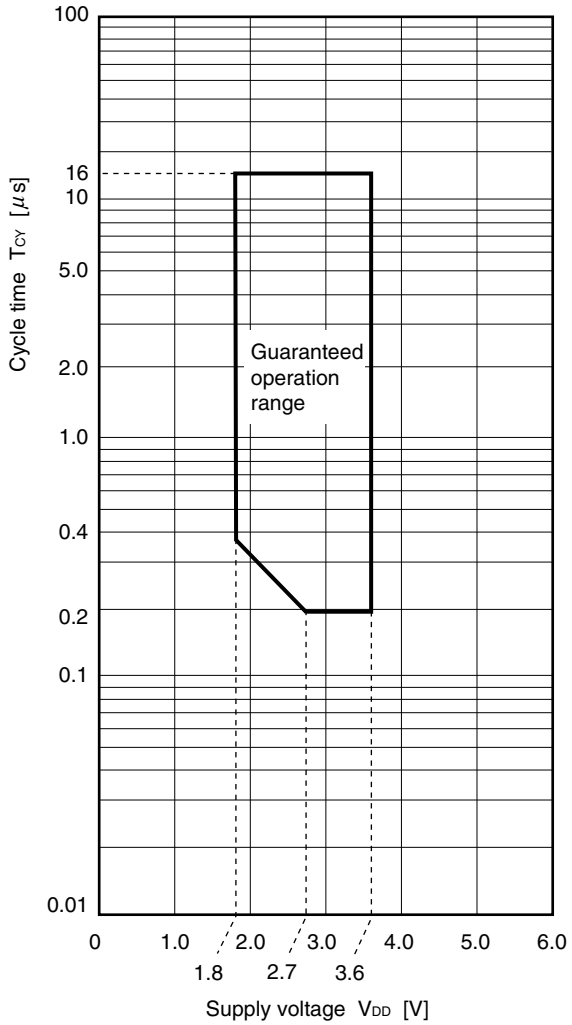
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	2.7 V ≤ V_{DD} ≤ 3.6 V	0.2		16	μs
			1.8 V ≤ V_{DD} < 2.7 V	0.4		16	μs
		Subsystem clock (f_{SUB}) operation		114	122	125	μs
Peripheral hardware clock frequency	f_{PRS}	XSEL = 1	2.7 V ≤ V_{DD} ≤ 3.6 V			10	MHz
			1.8 V ≤ V_{DD} < 2.7 V			5	MHz
		XSEL = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	7.6		8.4	MHz
<R>			1.8 V ≤ V_{DD} < 2.7 V[Note 1]	6.75		8.4	MHz
External main system clock frequency	f_{EXCLK}	2.7 V ≤ V_{DD} ≤ 3.6 V		2.0		10.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V		2.0		5.0	MHz
External main system clock input high-level width/low-level width	t_{EXCLKH}, t_{EXCLKL}	2.7 V ≤ V_{DD} ≤ 3.6 V		48			ns
		1.8 V ≤ V_{DD} < 2.7 V		96			ns
External subsystem clock frequency	f_{EXCLKS}	1.8 V ≤ V_{DD} ≤ 3.6 V		31	32.768	39	kHz
External subsystem clock input high-level width/low-level width	$t_{EXCLKSH}$, $t_{EXCLKSL}$	1.8 V ≤ V_{DD} ≤ 3.6 V		12			μs
TI000 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	2.7 V ≤ V_{DD} ≤ 3.6 V		$2/f_{sam}$ + 0.2[Note 2]			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$ + 0.5[Note 2]			μs
TI50, TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 3.6 V				10	MHz
		1.8 V ≤ V_{DD} < 2.7 V				5	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	2.7 V ≤ V_{DD} ≤ 3.6 V		50			ns
		1.8 V ≤ V_{DD} < 2.7 V		100			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
Key interrupt input low-level width	t_{KR}			250			ns
<R> $\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

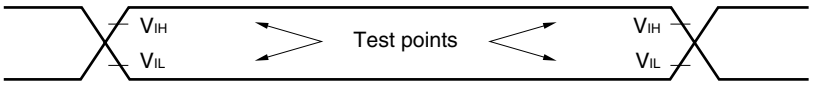
Notes 1. A characteristic of the main system clock frequency. Set the clock divider to be set using a peripheral function to $f_{RH}/2$ or less.

2. Selection of f_{sam} = f_{PRS}, $f_{PRS}/4$, $f_{PRS}/256$ is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode registers 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, f_{sam} = f_{PRS}.

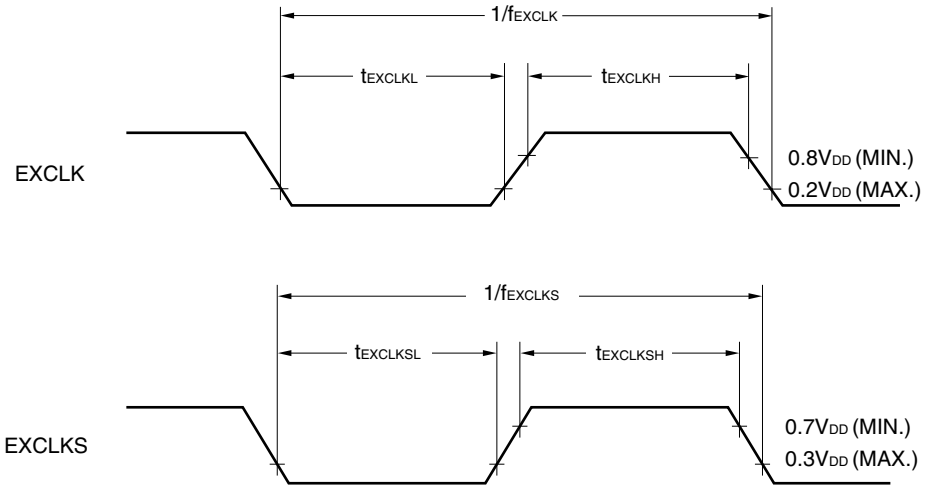
T_{CY} vs. V_{DD} (Main System Clock Operation)



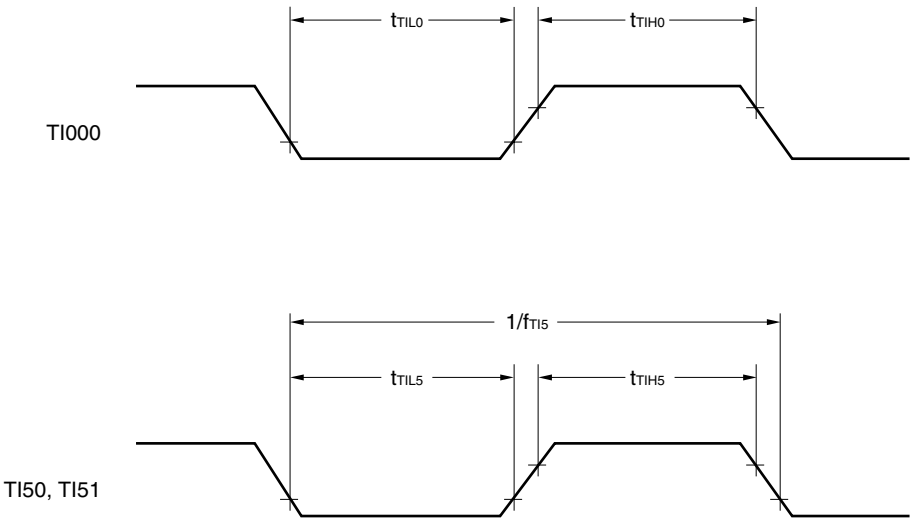
AC Timing Test Points (except external main system clock)



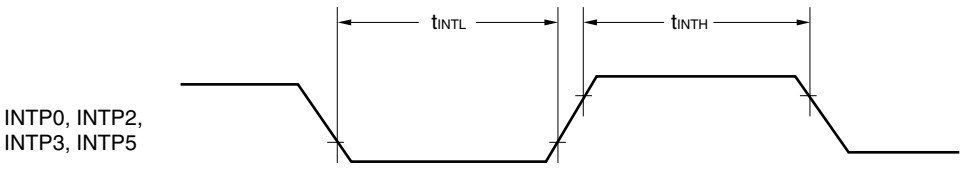
External Main System Clock Timing, External Subsystem Clock Timing



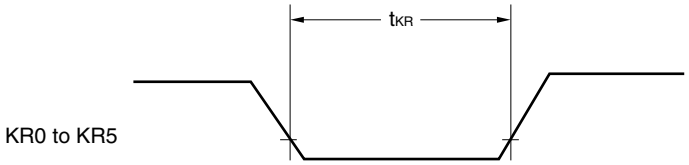
TI Timing



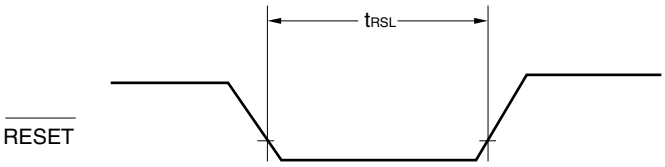
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) Serial interface

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = 0 V)

(a) UART6 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(c) CSI10 (Master mode, $\overline{SCK10}$... internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 3.6 V		250			ns
		1.8 V ≤ V_{DD} < 2.7 V		500			ns
$\overline{SCK10}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 25$ Note 1			ns
		1.8 V ≤ V_{DD} < 2.7 V		$t_{KCY1}/2 - 50$ Note 1			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		80			ns
		1.8 V ≤ V_{DD} < 2.7 V		170			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI1}			30			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO1}	C = 50pF Note 2	78K0/LE3-M			40	ns
<R>			78K0/LG3-M			60	ns

Notes 1. This value is when high-speed system clock (f_{XH}) is used.

2. C is the load capacitance of the $\overline{SCK10}$ and SO10 output lines.

(d) CSI10 (Slave mode, $\overline{SCK10}$... external clock input)

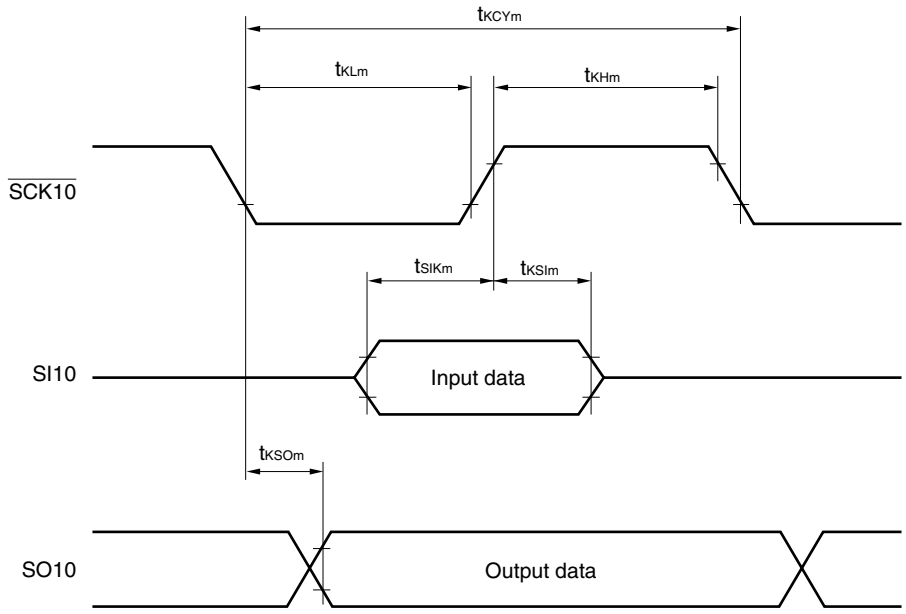
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}			400			ns
$\overline{SCK10}$ high-/low-level width	t_{KH2}, t_{KL2}			$t_{KCY2}/2$			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK2}			80			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI2}			50			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO2}	C = 50 pF Note	2.7 V ≤ V_{DD} ≤ 3.6 V			120	ns
			1.8 V ≤ V_{DD} < 2.7 V			165	ns

Note C is the load capacitance of the SO10 output line.

Caution The SO10 characteristics of 78K0/LE3-M is under evaluation.

Serial Transfer Timing

CSI10:



Remark m = 1, 2

10-bit successive approximation type A/D Converter Characteristics

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = AV_{REF} = LV_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES1}				10	bit
Overall error[Notes 1, 2]	A_{INL}	2.7 V ≤ AV_{REF} ≤ 3.6 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
<R> Conversion time	t_{CONV}	2.7 V ≤ AV_{REF} ≤ 3.6 V	12.2		84	μs
<R>		2.3 V ≤ AV_{REF} < 2.7 V	27		84	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	2.7 V ≤ AV_{REF} ≤ 3.6 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	2.7 V ≤ AV_{REF} ≤ 3.6 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE1}	2.7 V ≤ AV_{REF} ≤ 3.6 V			±4.5	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±6.5	LSB
Differential non-linearity error[Note 1]	D_{LE1}	2.7 V ≤ AV_{REF} ≤ 3.6 V			±2.0	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±2.0	LSB
Analog input voltage	V_{AIN1}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

24-bit ΔΣ-type A/D Converter Characteristics

(T_A = –40 to +85°C, 3.0 V ≤ AV_{REF} ≤ V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(a) Recommended operation condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
	LV_{DD}		3.0	3.3	3.6	V
Clock frequency	CLK_{ORG}	For decimation filter		10.0		MHz
Analog input voltage	$V_{ANI (V)}$	Voltage channel	–0.375		0.375	V
	$V_{ANI (I)}$	Current channel	–0.1875		0.1875	V
<R> Operating temperature	T_{OPR}		–40	25	85	°C

(b) Reference

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
External reference potential (input)	AV_{REFIO1}		1.20		1.25	V
Internal reference potential (output)	AV_{REFIO2}		1.165	1.226	1.287	V
Internal reference potential temperature coefficient	dREF/dT	**Note**		100		ppm/°C

Note Temperature coefficient of –40 to +25°C and +25 to +85°C

(c) Analog input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input signal DC level	ainDC	Voltage channel	–20	0	20	mV
		Current channel, gain 1 time	–20	0	20	mV
		Current channel, gain 2 times	–10	0	10	mV
		Current channel, gain 16 times	–1.25	0	1.25	mV
Input signal range	ainRANGE	Voltage channel	–0.375	0	0.375	V
		Current channel, gain 1 time	–0.375	0	0.375	V
		Current channel, gain 2 times	–0.1875	0	0.1875	V
		Current channel, gain 16 times	–23.4375	0	23.4375	mV
Input gain	ainGAIN	Voltage channel	0.93	1	1.07	Times
		Current channel, gain 1 time	0.93	1	1.07	Times
		Current channel, gain 2 times	1.86	2	2.14	Times
		Current channel, gain 16 times	14.88	16	17.12	Times
Input impedance	ainRIN	Voltage channel	100	131.25		kΩ
		Current channel, gain 1 time	60	78.75		kΩ
		Current channel, gain 2 times	60	78.75		kΩ
		Current channel, gain 16 times	60	78.75		kΩ

Caution All current channels must have the same gain setting (It is not possible to specify different gain settings for each channel).

(d) A/D converter part

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock	CLK_{ORG}				10		MHz
ΔΣ-type operating clock	CLK_{OSX3}	CLK_{OSX6}/2			1.667		MHz
Oversampling frequency	f_{OS}				555.6		kHz
Sampling frequency	f_S	f_{OS}/128			4.34		kHz
Output data rate	T_{DATA}	At 1/f_S DF output			230.4		μs
Data width	RES				24		bit
S/N	SNR	0 dB@60 Hz When inputting a single sine wave	Voltage channel	70	76		dB
			Current channel, gain 1 time	70	76		dB
			Current channel, gain 2 times	70	76		dB
			Current channel, gain 16 times	62	69		dB
THD	THD	0 dB@60 Hz When inputting a single sine wave	Voltage channel		–80	–72	dB
			Current channel, gain 1 time		–80	–72	dB
			Current channel, gain 2 times		–80	–72	dB
			Current channel, gain 16 times		–80	–72	dB
<R> Inter-channel isolation	XT		Voltage channel	80			dB
			Current channel, gain 1 time	80			dB
			Current channel, gain 2 times	80			dB
			Current channel, gain 16 times	72			dB
<R> Operating current	I_{AVDD}				3.9	7	mA

(e) Digital filter part

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Passband (low)	fchpf	–3 dB		0.73		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz@50 Hz 54 Hz to 66 Hz@60 Hz	–0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz@50 Hz 54 Hz to 330 Hz@60 Hz	–0.1		0.1	dB
In-band ripple 3	rp3	45 Hz to 1100 Hz@50 Hz 54 Hz to 1320 Hz@60 Hz	–0.1		0.1	dB
Stopband (high)	fatt	–80 dB		3020		Hz
Out-of-band attenuation	ATT		–80			dB

Caution All current channels must have the same gain setting (It is not possible to specify different gain settings for each channel).

Power Calculation Characteristics (T_A = –40 to +85°C, 3.0 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = 0 V, PF = 1, voltage channel gain = 1 time, current channel gain = 1 time or 2 times)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Phase error between channels PF = 0.8 capacitive		Phase lead: 37°		±0.05		°
Phase error between channels PF = 0.5 inductive		Phase lag: 60°		±0.05		°
Active energy measurement error		Dynamic range 1000 : 1 @ 25°C		0.1		%
Reactive energy measurement error		Dynamic range 1000 : 1 @ 25°C		0.5		%
Vrms measurement error		Dynamic range 100 : 1 @ 25°C		0.5		%
Irms measurement error		Dynamic range 500 : 1 @ 25°C		0.5		%

LCD Characteristics (T_A = –40 to +85°C)

(1) Resistance division method

(a) Static display mode (1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

(b) 1/2 bias method (1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

(c) 1/3 bias method (1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

Notes 1. Internal resistance division method only.

2. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2}, and V_{SS} pins, and either of the SEG and COM pins.

3. Set VAON based on the following conditions.

<When set to the static display mode>

- When 2.0V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method>

- When 2.7V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

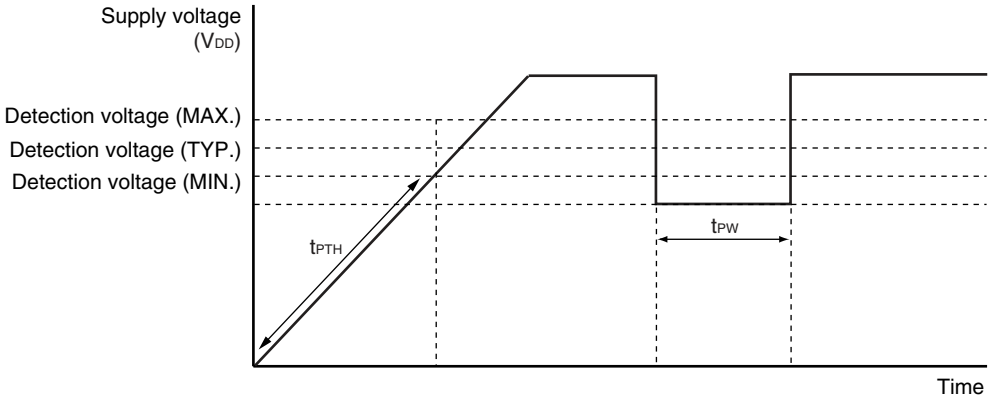
<When set to the 1/3 bias method>

- When 2.5V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

1.59 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.44	1.59	1.74	V
Power supply voltage rise inclination	t_{PTH}	V_{DD}: 0 V → change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	t_{PW}		200			μs

POC Circuit Timing

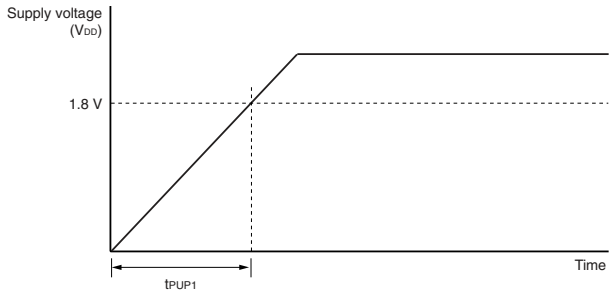


Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = 0 V)

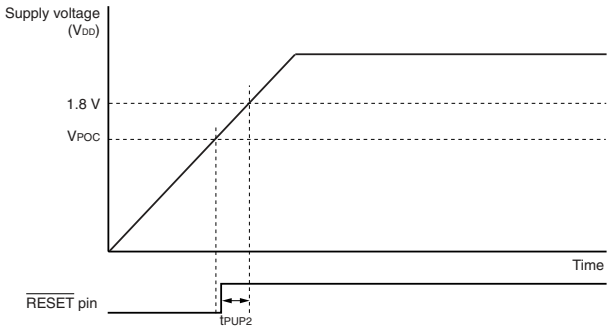
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	POCMODE (option byte) = 0, when $\overline{RESET}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (releasing $\overline{RESET}$ input → V_{DD}: 1.8 V)	t_{PUP2}	POCMODE (option byte) = 0, when $\overline{RESET}$ input is used			1.9	ms

Supply Voltage Rise Time Timing

- When $\overline{RESET}$ pin input is not used



- When $\overline{RESET}$ pin input is used



2.7 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.

LVI Circuit Characteristics (T_A = –40 to +85°C, $V_{POC} \le V_{DD} = LV_{DD} \le 3.6$ V, V_{SS} = 0 V)

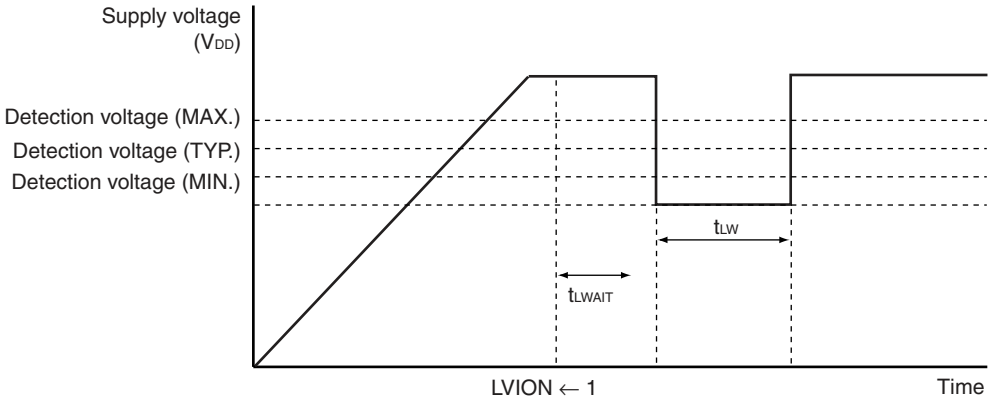
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		3.22	3.32	3.42	V
		V_{LVI1}		3.06	3.16	3.26	V
		V_{LVI2}		2.91	3.01	3.11	V
		V_{LVI3}		2.75	2.85	2.95	V
		V_{LVI4}		2.60	2.70	2.80	V
		V_{LVI5}		2.45	2.55	2.65	V
		V_{LVI6}		2.29	2.39	2.49	V
		V_{LVI7}		2.14	2.24	2.34	V
		V_{LVI8}		1.98	2.08	2.18	V
		V_{LVI9}		1.83	1.93	2.03	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 3.6 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The P120/INTP0/EXLVI pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization.

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 9

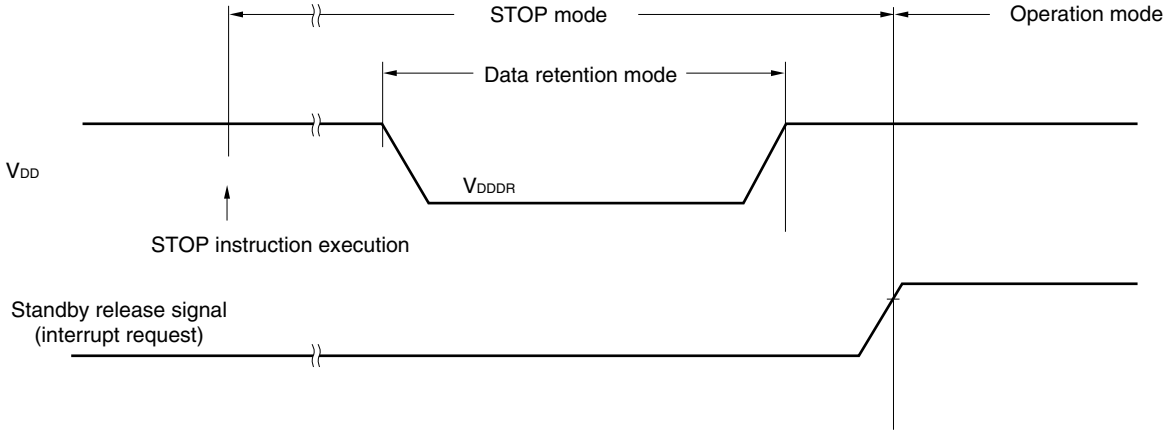
LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		3.6	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = LV_{DD} ≤ 3.6 V, V_{SS} = 0 V)

• Basic characteristics

Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}					4.5	11.0	mA
Erase time[Note 1, 2]	All block	T_{eraca}					20	200	ms
	Block unit	T_{erasa}					20	200	ms
Write time (in 8-bit units)[Note 1]		T_{wrwa}					10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note 3]	When a flash memory programmer is used, and the libraries provided by Renesas Electronics are used	Retention: 15 years	1000			Times
				When the EEPROM emulation libraries provided by Renesas Electronics are used, and the rewritable ROM size is 4 KB	Retention: 3 years[Note 4]	10000			Times

Notes 1. Characteristic of the flash memory.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

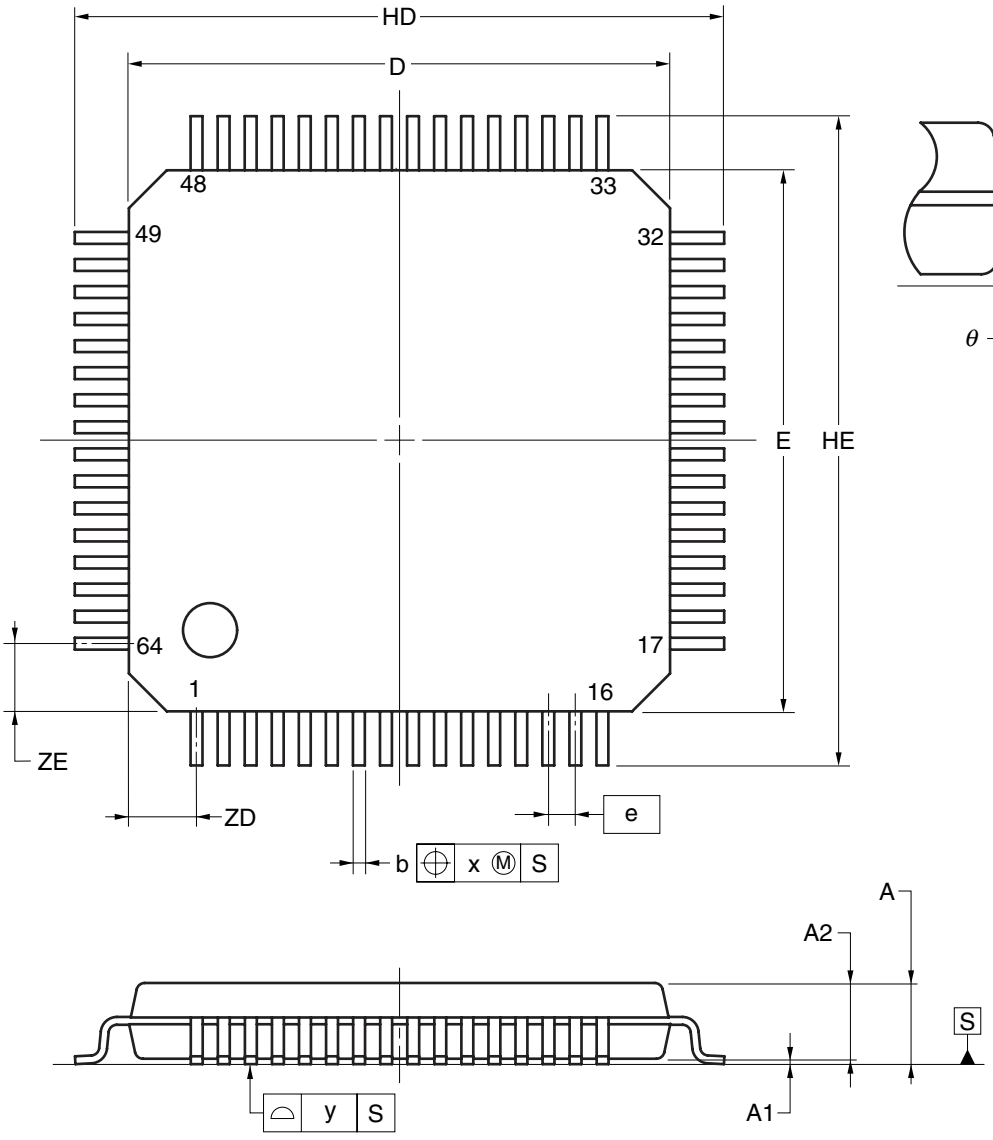
4. Data retention is guaranteed for three years after data has been written. If rewriting has been performed, data retention is guaranteed for another three years thereafter.

Remark f_{XP}: Main system clock oscillation frequency

CHAPTER 34 PACKAGE DRAWINGS

34.1 78K0/LE3-M

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



(UNIT:mm)

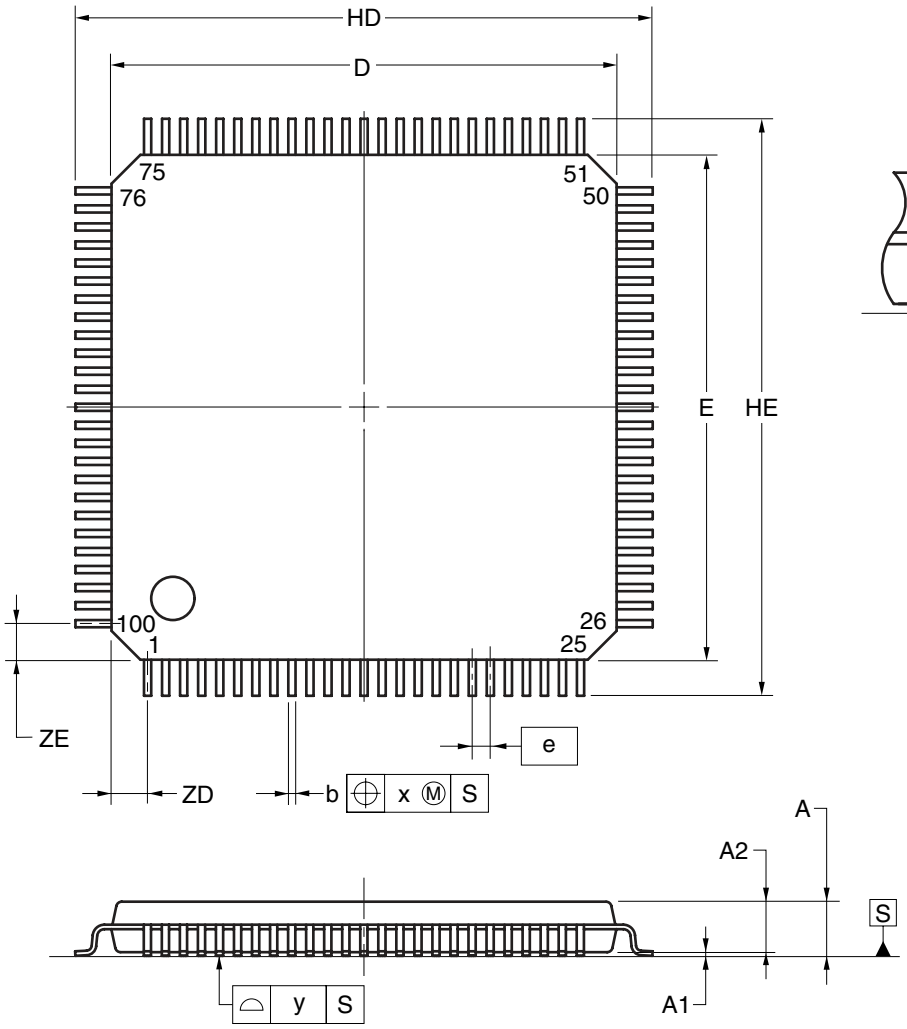
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-GAH

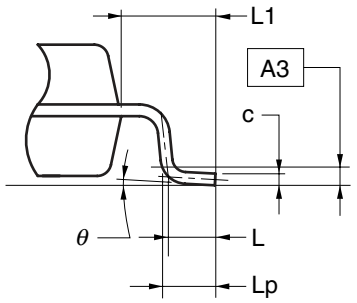
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

34.2 78K0/LG3-M

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

P100GC-50-UEU-1

CHAPTER 35 CAUTIONS FOR WAIT

35.1 Cautions for Wait

This product has two internal system buses.

One is a CPU bus and the other is a peripheral bus that interfaces with the low-speed peripheral hardware.

Because the clock of the CPU bus and the clock of the peripheral bus are asynchronous, unexpected illegal data may be passed if an access to the CPU conflicts with an access to the peripheral hardware.

When accessing the peripheral hardware that may cause a conflict, therefore, the CPU repeatedly executes processing, until the correct data is passed.

As a result, the CPU does not start the next instruction processing but waits. If this happens, the number of execution clocks of an instruction increases by the number of wait clocks (for the number of wait clocks, see **Table 35-1**). This must be noted when real-time processing is performed.

35.2 Peripheral Hardware That Generates Wait

Table 35-1 lists the registers that issue a wait request when accessed by the CPU, and the number of CPU wait clocks.

Table 35-1. Registers That Generate Wait and Number of CPU Wait Clocks

Peripheral Hardware	Register	Access	Number of Wait Clocks
Serial interface UART0	ASIS0	Read	1 clock (fixed)
Serial interface UART6	ASIS6	Read	1 clock (fixed)
10-bit successive approximation type A/D converter	ADM	Write	1 to 5 clocks (when $f_{AD} = f_{PRS}/2$ is selected) 1 to 7 clocks (when $f_{AD} = f_{PRS}/3$ is selected) 1 to 9 clocks (when $f_{AD} = f_{PRS}/4$ is selected) 2 to 13 clocks (when $f_{AD} = f_{PRS}/6$ is selected) 2 to 17 clocks (when $f_{AD} = f_{PRS}/8$ is selected) 2 to 25 clocks (when $f_{AD} = f_{PRS}/12$ is selected)
	ADS	Write	
	ADPC	Write	
	ADCR	Read	
	The above number of clocks is when the same source clock is selected for f_{CPU} and f_{PRS}. The number of wait clocks can be calculated by the following expression and under the following conditions. <Calculating number of wait clocks> • Number of wait clocks = $\frac{2 f_{CPU}}{f_{AD}} + 1$ * Fraction is truncated if the number of wait clocks ≤ 0.5 and rounded up if the number of wait clocks > 0.5. f_{AD}: A/D conversion clock frequency ($f_{PRS}/2$ to $f_{PRS}/12$) f_{CPU}: CPU clock frequency f_{PRS}: Peripheral hardware clock frequency f_{XP}: Main system clock frequency <Conditions for maximum/minimum number of wait clocks> • Maximum number of times: Maximum speed of CPU (f_{XP}), lowest speed of A/D conversion clock ($f_{PRS}/12$) • Minimum number of times: Minimum speed of CPU ($f_{SUB}/2$), highest speed of A/D conversion clock ($f_{PRS}/2$)		

Caution When the peripheral hardware clock (f_{PRS}) is stopped, do not access the registers listed above using an access method in which a wait request is issued.

Remark The clock is the CPU clock (f_{CPU}).

APPENDIX A REVISION HISTORY

A.1 Major Revisions in This Edition

(1/2)

Page	Description	Classification
CHAPTER 2 PIN FUNCTIONS		
p. 45	Change of **Table 2-2. Pin I/O Circuit Types (2/2)**	(c)
CHAPTER 4 PORT FUNCTIONS		
p. 135	Change of **Figure 4-26. Format of Port Mode Register (78K0/LE3-M)** and **Cautions**	(a)
CHAPTER 5 CLOCK GENERATOR		
p. 150	Change of description of **5.1 (2) Subsystem clock**	(c)
p. 158	Change of **Table 5-3. Whether Subsystem Clock Can Be Used**	(c)
p. 169	Change of description of **5.4.3 When subsystem clock is not used**	(c)
p. 180	Change of description of **5.6.3 (4) Example of setting procedure when stopping the subsystem clock**	(c)
CHAPTER 9 REAL-TIME COUNTER		
p. 283	Addition of **Caution** to **CHAPTER 9 REAL-TIME COUNTER**	(c)
p. 286	Change of description of CT2 to CT0 bits in **Figure 9-2. Format of Real-Time Counter Control Register 0 (RTCC0)**	(a)
p. 287	Change of description of WALE bit in **Figure 9-3. Format of Real-Time Counter Control Register 1 (RTCC1) (1/2)**	(a)
p. 297	Change of description of **9.3 (14) Watch error correction register (SUBCUD)**	(a)
p. 300	Change of **Figure 9-19. Procedure for Starting Operation of Real-Time Counter**	(a)
CHAPTER 12 10-BIT SUCCESSIVE APPROXIMATION TYPE A/D CONVERTER		
p. 331	Change of **(1) 2.7 V ≤ AV_{REF} ≤ 3.6 V (LV0 = 0) of Table 12-2**	(b)
CHAPTER 13 24-BIT ΔΣ-TYPE A/D CONVERTER		
p. 355	Addition of **Caution 2** to **Figure 13-5. Format of 24-Bit ΔΣ-Type A/D Conversion Result Registers n (ADCRn)**	(c)
CHAPTER 20 INTERRUPT FUNCTIONS		
p. 512	Change of **Table 20-4. Flags Corresponding to Extended SFR Interrupt Request Sources**	(a)
p. 516	Change of **20.3 (3) Extended SFR interrupt request flag registers (IF20, IF21, IF22, IF23)**	(a)
CHAPTER 22 POWER CALCULATION CIRCUIT		
p. 563	Change of description of **22.4.3 (5) Voltage channel RMS offset compensation**	(a)
CHAPTER 24 DIGITAL FREQUENCY CONVERSION CIRCUIT		
p. 636	Change of description of **24.1 Digital Frequency Conversion Circuit Functions**	(a)
p. 641	Change of description of **24.4 (3) CF output pulse**	(a)
CHAPTER 25 STANDBY FUNCTION		
p. 653	Change of **Note** of **Figure 25-5. Operation Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated)**	(b)
pp. 654, 655	Change of **Note** of **Figure 25-6. STOP Mode Release by Interrupt Request Generation**	(b)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

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