CY2544
CY2546

PRELIMINARY

Quad PLL Programmable Clock Generator with Spread Spectrum

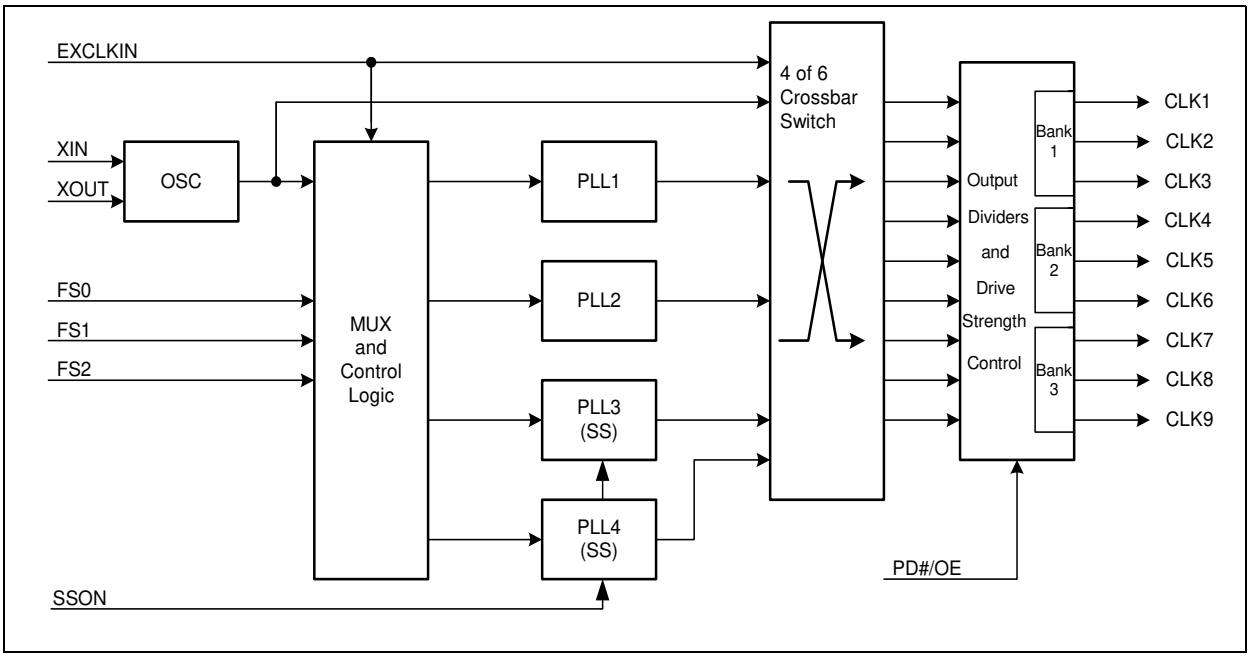
Features

- Four fully integrated phase-locked loops (PLLs)
- Input Frequency range:
  - — External crystal: 8 to 48 MHz
  - — External reference: 8 to 166 MHz clock
- Wide operating output frequency range
  - — 3 to 166 MHz
- Programmable Spread Spectrum with Center and Down Spread option and Lexmark modulation profile
- Two VDD core voltage options:
  - — 2.5V, 3.0V, and 3.3V for CY2544
  - — 1.8V for CY2546
- Selectable output voltages:
  - — 2.5V, 3.0V, and 3.3V for CY2544
  - — 1.8V for CY2546
- Frequency Select feature with option to select eight different frequencies
- Low jitter, high accuracy outputs
- Up to nine clock outputs
- Programmable output drive strength
- Glitch-free outputs while frequency switching
- 24-pin QFN package
- Commercial and Industrial temperature ranges

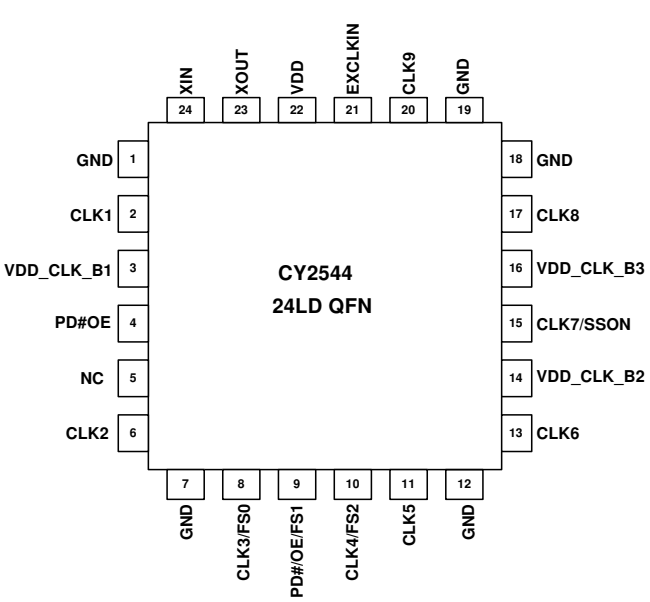
Benefits

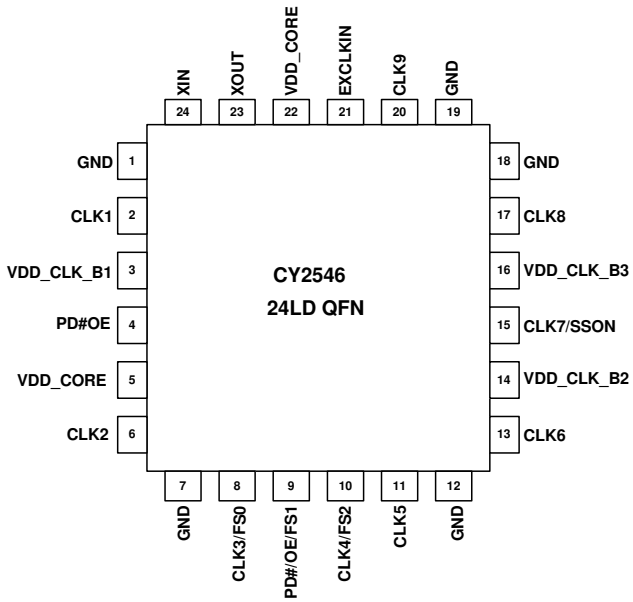
- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for customized PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Two Spread Spectrum capable PLLs with Linear or Lexmark profile for maximum EMI reduction
- Spread Spectrum PLLs can be disabled or enabled separately
- PLLs can be programmed for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitable for PC, consumer, and networking applications
- Ability to synthesize standard frequencies with ease
- Application compatibility in standard and low-power systems

Block Diagram



Pin Configuration





Pin Description - CY2544 (2.5V, 3.0V or 3.3V VDD)

Pin Number	Name	I/O	Description
1	GND	Power	Power Supply Ground for Core
2	CLK1	Output	Programmable Output Clock
3	VDD_CLK_B1	Power	2.5V/3.0V/3.3V Power Supply for Output Bank1 (CLK1, CLK2, CLK3) output
4	PD#/OE	Input	Power Down or Output Enable
5	NC	NC	No Connect
6	CLK2	Output	Programmable Output Clock
7	GND	Power	Power Supply Ground for Output Bank 1
8	CLK3/FS0	Output/Input	Multifunction Programmable pin,CLK3 Output Clock or Frequency Select pin FS0
9	PD#/OE/FS1	Input	Multifunction Programmable pin, Power Down, Output Enable or Frequency Select pin FS1
10	CLK4/FS2	Output/Input	Multifunction Programmable pin, CLK4 Output or Frequency Select input pin FS2
11	CLK5	Output	Programmable Output Clock
12	GND	Power	Power Supply Ground for Output Bank 2
13	CLK6	Output	Programmable Output Clock
14	VDD_CLK_B2	Power	2.5V/3.0V/3.3V Power Supply for Output Bank2 (CLK4, CLK5, CLK6) output
15	CLK7/SSON	Output/Input	Multifunction Programmable pin, CLK7 Output or SSON input
16	VDD_CLK_B3	Power	2.5V/3.0V/3.3V Power Supply for Output Bank3 (CLK7, CLK8, CLK9) output
17	CLK8	Output	Programmable Output Clock
18	GND	Power	Power Supply Ground for Output Bank 3

Pin Description - CY2544 (2.5V, 3.0V or 3.3V VDD) (continued)

Pin Number	Name	I/O	Description
19	GND	Power	Power Supply Ground for Core
20	CLK9	Output	Programmable Output Clock
21	EXCLKIN	Input	External Clock Input
22	VDD	Power	2.5V/3.0V/3.3V Power Supply
23	XOUT	Output	Crystal Output
24	XIN	Input	Crystal Input

Pin Description - CY2546 (1.8V VDD_CORE)

Pin Number	Name	I/O	Description
1	GND	Power	Power Supply Ground for Core
2	CLK1	Output	Programmable Output Clock
3	VDD_CLK_B1	Power	1.8V Power Supply for Output Bank1 (CLK1, CLK2, CLK3) output
4	PD#/OE	Input	Power Down or Output Enable
5	VDD_CORE	Power Supply	1.8V Power Supply for Core
6	CLK2	Output	Programmable Output Clock
7	GND	Power	Power Supply Ground For Output Bank 1
8	CLK3/FS0	Output/Input	Multifunction Programmable pin,CLK3 Output Clock or Frequency Select pin FS0
9	PD#/OE/FS1	Input	Multifunction Programmable pin, Power Down, Output Enable or Frequency Select pin FS1
10	CLK4/FS2	Output/Input	Multifunction Programmable pin, CLK4 Output or Frequency Select input pin FS2
11	CLK5	Output	Programmable Output Clock
12	GND	Power	Power Supply Ground for Output Bank 2
13	CLK6	Output	Programmable Output Clock
14	VDD_CLK_B2	Power	1.8V Power Supply for Output Bank2 (CLK4, CLK5, CLK6) output
15	CLK7/SSON	Output/Input	Multifunction Programmable pin, CLK4 Output or SSON input
16	VDD_CLK_B3	Power	1.8V Power Supply for Output Bank3 (CLK7, CLK8, CLK9) output
17	CLK8	Output	Programmable Output Clock
18	GND	Power	Power Supply Ground for Output Bank 3
19	GND	Power	Power Supply Ground for Core
20	CLK9	Output	Programmable Output Clock
21	EXCLKIN	Input	External Low Voltage Reference Clock Input
22	VDD_CORE	Power	1.8V Power Supply for Core
23	XOUT	Output	Crystal Output
24	XIN	Input	Crystal Input

General Description

The CY2544 and CY2546 are four-PLL programmable Spread Spectrum Clock Generators used to reduce EMI found in high-speed digital electronic systems. Two of the four PLLs have Spread Spectrum capability. The spread spectrum feature is turned on or off using the control pin SSON.

The advantage of having four PLLs is that a single device can generate up to four independent families of frequencies from a single crystal or reference input frequency. Generally, a design requires up to four oscillators to achieve the same result as a single CY2544 or CY2546.

The device uses Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. Frequency modulating the clock greatly reduces the measured EMI at the fundamental and harmonic frequencies. This reduction in radiated energy significantly reduces the cost of complying with regulatory agency (EMC) requirements and improves time-to-market without degrading the system performance.

The CY2544 and CY2546 use a factory/field-programmable configuration memory array to provide customization for output frequencies, frequency select options, spread characteristics like spread percentage and modulation frequency, output drive strength and crystal load capacitance. Customized devices are configured using CyberClocks™ software or by contacting the factory.

The spread percentage is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.125% to ±2.50%. The range for down spread is from –0.25% to –5.0%. Contact the factory for smaller or larger spread percentage amounts, if required.

The input to the CY2544 and CY2546 is either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz, and for clock signals is 8 MHz to 166 MHz. In addition, there is a separate input for a clock reference.

The CY2544 and CY2546 have nine clock outputs and each output has four possible input sources. There are three frequency select lines FS(2:0) that provide an option to select eight different sets of frequencies among each of the four PLLs. Each output has programmable output divider options. Output 1 has eight possible divider values and outputs 2–9 have four possible divider values for maximum flexibility. The 2-bit or 3-bit output dividers are programmable, providing a wide output frequency range.

The outputs are glitch-free when frequency is switched using output dividers. The outputs can have a predictable phase relationship, if the clock source is the same PLL and divider values are 2, 3, 4, or 6.

The output banking feature allows the three sets of frequencies to operate at three different voltages. Selectable output voltage options are 2.5V, 3.0V, or 3.3V for CY2544 and 1.8V for CY2546 part.

The CY2544 and CY2546 are available in 24-pin QFN packages with commercial and industrial operating temperature ranges.

Table 1. Supply Voltage Options

Device	V_{DD} Supply Voltage
CY2544	2.5V, 3.0V or 3.3V
CY2546	1.8V

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage for CY2544		–0.5	4.5	V
V_{DD_CORE}	Supply Voltage for CY2546		–0.5	2.6	V
$V_{DD\_CLK\_BX}$	Supply Voltage for CY2544		–0.5	4.5	V
	Supply Voltage for CY2546		–0.5	2.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	Volts
UL-94	Flammability Rating	@1/8 in.	V-0		
MSL	Moisture Sensitivity Level	QFN package	3		

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	VDD Operating at 3.3V for CY2544	3.00	–	3.60	V
V_{DD}	VDD Operating at 3.0V for CY2544	2.70	–	3.30	V
V_{DD}	VDD Operating at 2.5V for CY2544	2.25	–	2.75	V
V_{DD_CORE}	VDD_CORE Operating at 1.8V for CY2546	1.65	–	1.95	V
$V_{DD\_CLK\_BX}$	Output Driver Voltage for Bank 1, 2 and 3 Operating at 3.3V (CY2544)	3.00	–	3.60	V
$V_{DD\_CLK\_BX}$	Output Driver Voltage for Bank 1, 2 and 3 Operating at 3.0V (CY2544)	2.70	–	3.30	V
$V_{DD\_CLK\_BX}$	Output Driver Voltage for Bank 1, 2 and 3 Operating at 2.5V (CY2544)	2.25	–	2.75	V
$V_{DD\_CLK\_BX}$	Output Driver Voltage for Bank 1, 2 and 3 Operating at 1.8V (CY2546)	1.65	–	1.95	V
T_{AC}	Commercial Ambient Temperature	0	–	+70	°C
T_{AI}	Industrial Ambient Temperature	–40	–	+85	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD} pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage, All CLK pins	All V_{DD} levels, I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage, All CLK pins	All V_{DD} levels, I_{OH} = –8 mA	V_{DD} – 0.4	–	–	V
V_{IL}	All Inputs except XIN	All V_{DD} levels	–0.3	–	0.2 * V_{DD}	V
V_{IH}	All Inputs except XIN	All V_{DD} levels	0.8 * V_{DD}	–	V_{DD} + 0.3	V
V_{ILX}	Input Low Voltage, clock input to XIN pin	All V_{DD} levels	–0.3	–	0.36	V
V_{IHX}	Input High Voltage, clock input to XIN pin	All V_{DD} levels	1.44	–	2.0	V
I_{ILPDOE}	Input Low Current, PD#/OE and FS0,1,2 pins	V_{IN} = V_{SS} (No Internal pull up)	–	–	1	µA
I_{IHPDOE}	Input High Current, PD#/OE and FS0,1,2 pins	V_{IN} = V_{DD} (No Internal pull up)	–	–	1	µA
I_{ILSR}	Input Low Current, SSON pin	V_{IN} = V_{SS} (Internal pull down = 160k typical)	–	–	1	µA
I_{IHSR}	Input High Current, SSON pin	V_{IN} = V_{DD} (Internal pull down = 160k typical)	–	–	25	µA
I_{DD}[1]	Supply Current	All clocks running, No load	–	15	–	mA
I_{DDS}	Standby Current	All output power down	–	50	–	µA
C_{IN}	Input Capacitance - All inputs except XIN	SSON, OE, PD# or FS inputs	–	–	7	pF

AC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{IN} (crystal)	Crystal Frequency		8	–	48	MHz
F_{IN} (clock)	Input Clock Frequency (XIN or EXCLKIN)		8	–	166	MHz
F_{OUT}	Output Clock Frequency		3	–	166	MHz
DC	Output Duty Cycle All Clocks except Ref Out	Duty Cycle is defined in Figure 2, "Duty Cycle Definition," on page 8; t_1/t_2, 50% of V_{DD}	45	50	55	%
DC	Ref Out Duty Cycle	Ref In Min 45%, Max 55%	40		60	%
E_R	CLK1-9 Rising Edge Rate	V_{DD} = All, 20% to 80% V_{DD}	0.8	–	–	V/ns
E_F	CLK1-9 Falling Edge Rate	V_{DD} = All, 20% to 80% V_{DD}	0.8	–	–	V/ns
T_{CCJ1}	Cycle-to-cycle Jitter	Configuration dependent. See Table 2, “Configuration Example for Jitter,” on page 6	–	–	–	ps
T_{LTJ}	Long Term Jitter (1000 cycle period jitter)	Configuration dependent. See Table 2, “Configuration Example for Jitter,” on page 6	–	–	–	ns
T_{10}	PLL Lock Time		–	1	3	ms

Table 2. Configuration Example for Jitter

Reference	Description	Max Jitter (ps) on Output 1(48MHz)	Max Jitter (ps) on Output 2 (27 MHz)	Max Jitter (ps) on Output 3 (166 MHz)	Max Jitter (ps) on Output 4 (74.25 MHz)
Cycle-to-Cycle Jitter					
27MHz	T_{CCJ1}	155	255	170	195
48 MHz	T_{CCJ1}	135	225	100	125
Long Term Jitter					
27MHz	T_{LTJ}	770	580	630	1105
48 MHz	T_{LTJ}	535	575	520	795

Note
1. Configuration dependent.

Recommended Crystal Specification for SMD Package

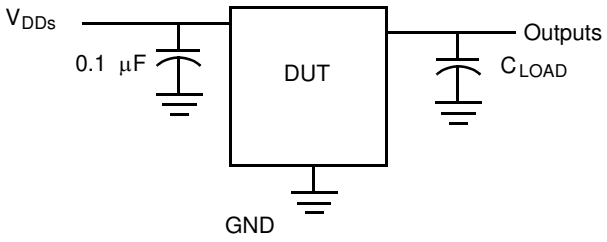
Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	28	MHz
Fmax	Maximum Frequency	14	28	48	MHz
R1(max)	Maximum Motional Resistance (ESR)	135	50	30	Ω
C0(max)	Maximum Shunt Capacitance	4	4	2	pF
CL(max)	Maximum Parallel Load Capacitance	18	14	12	pF
DL(max)	Maximum Crystal Drive Level	300	300	300	μW

Recommended Crystal Specification for Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	24	MHz
Fmax	Maximum Frequency	14	24	32	MHz
R1(max)	Maximum Motional Resistance (ESR)	90	50	30	Ω
C0(max)	Maximum Shunt Capacitance	7	7	7	pF
CL(max)	Maximum Parallel Load Capacitance	18	12	12	pF
DL(max)	Maximum Crystal Drive Level	1000	1000	1000	μW

Test and Measurement Setup

Figure 1. Test and Measurement Setup



Voltage and Timing Definitions

Figure 2. Duty Cycle Definition

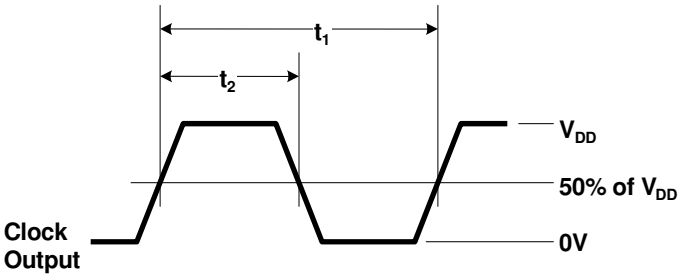
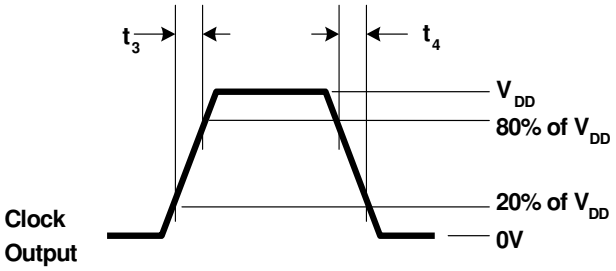


Figure 3. ER = (0.6 x V_{DD}) /t_3, EF = (0.6 x V_{DD}) /t_4



Ordering Information

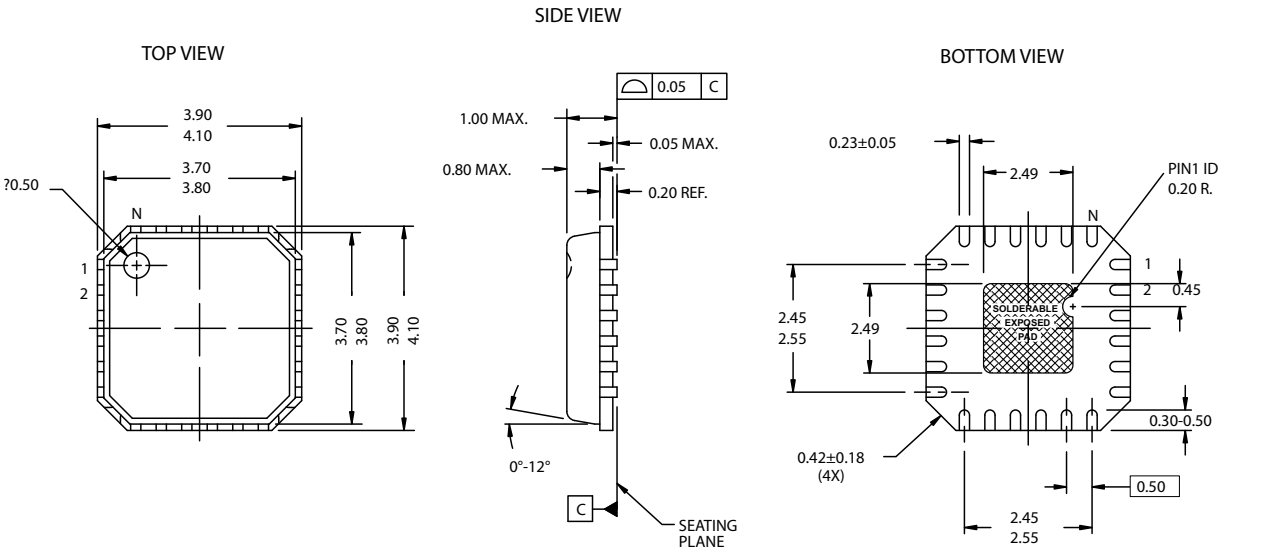
Part Number[2]	Type	VDD(V)	Temperature Range
Lead-free			
CY2544Cxxx	24-pin QFN	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY2544CxxxT	24-pin QFN -Tape & Reel	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY2544FC	24-pin QFN	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY2544FCT	24-pin QFN - Tape & Reel	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY2546Cxxx	24-pin QFN	1.8	Commercial, 0°C to 70°C
CY2546CxxxT	24-pin QFN -Tape & Reel	1.8	Commercial, 0°C to 70°C
CY2546FC	24-pin QFN	1.8	Commercial, 0°C to 70°C
CY2546FCT	24-pin QFN -Tape & Reel	1.8	Commercial, 0°C to 70°C
CY2544IxxxT	24-pin QFN -Tape & Reel	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY2544FI	24-pin QFN	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY2544FIT	24-pin QFN - Tape & Reel	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY2546Ixxx	24-pin QFN	1.8	Industrial, -40°C to +85°C
CY2546IxxxT	24-pin QFN -Tape & Reel	1.8	Industrial, -40°C to +85°C
CY2546FI	24-pin QFN	1.8	Industrial, -40°C to +85°C
CY2546FIT	24-pin QFN -Tape & Reel	1.8	Industrial, -40°C to +85°C

Note

2. xxx Indicates Factory Programmable are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative. F in the part number indicates field programmable using CyberClocks Online software.

Package Drawing and Dimensions

Figure 4. 24-Lead QFN 4x4 mm (Subcon Punch Type Pkg with 2.49x2.49 EPAD) LF24A



NOTES:

1. **HATCH IS SOLDERABLE EXPOSED METAL.**
2. **REFERENCE JEDEC#: MO-220**
3. **PACKAGE WEIGHT: 0.042g**
4. **ALL DIMENSIONS ARE IN MM [MIN/MAX]**
5. **PACKAGE CODE**

51-85203-*A

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

Document History Page

Document Title: CY2544/CY2546 Quad PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12563				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	690257	See ECN	RGL	New Data Sheet
*A	790516	See ECN	RGL	Separated the Pin Configuration drawing into two to show the difference between CY2544 and CY2546 pin outs. Changed the IDD from 22mA maximum to 25mA typical Changed I_{ILSR} Internal pull down from 100K to 160K Changed I_{IHSR} Internal pull down from 100k to 160K and changed the maximum value from 10µA to 25µA Changed I_{ILPDOE} to No Internal pull up and changed the maximum value from 10µA to 1µA Changed I_{IHPDOE} to no Internal pull up