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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E32RA-CW350-R

Overview:

- 3.2-inch TFT (55.0x77.2 I I)
- 240 ⇆320 iX⊄⇆⅓⇕
- Multiple Interfaces
- º ₲T ¤T Iix
- 6:00 Viewing Angle
- Transmissive
- Resistive Touch Panel
- 350 nits
- TFT IC: ST7789V
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit and a backlight unit. The resolution of the 3.2" TFT LCD contains 240(RGB)x320 pixels and can display up to 65k/262k colors.

TFT Features

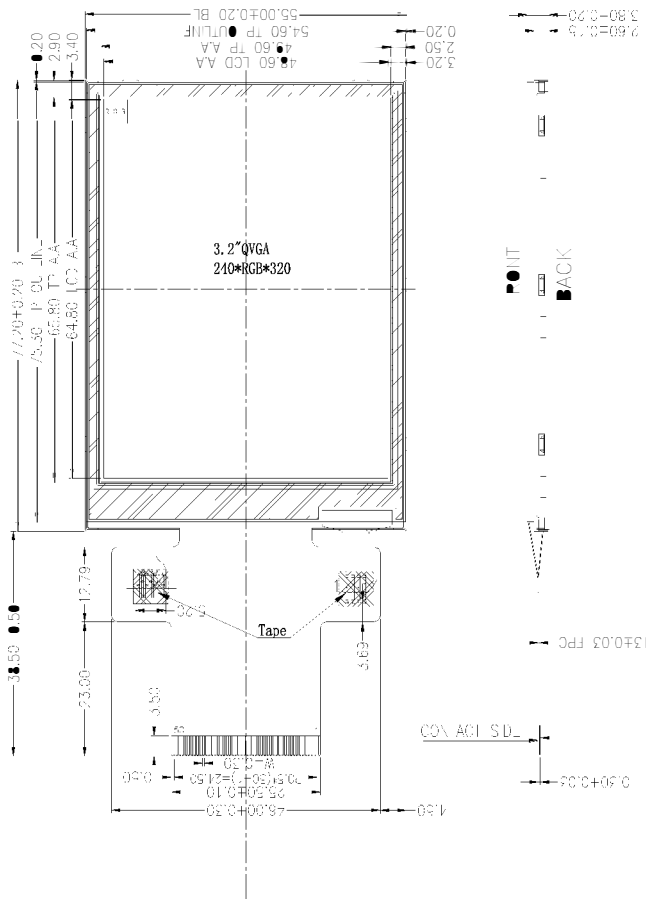
Low Input Voltage: 3.3V
Display Colors: 65k/262k
Interfaces: 8/9/16/18-bit MCU
3/4-line Serial
3/4SPI+16/18-bit RGB

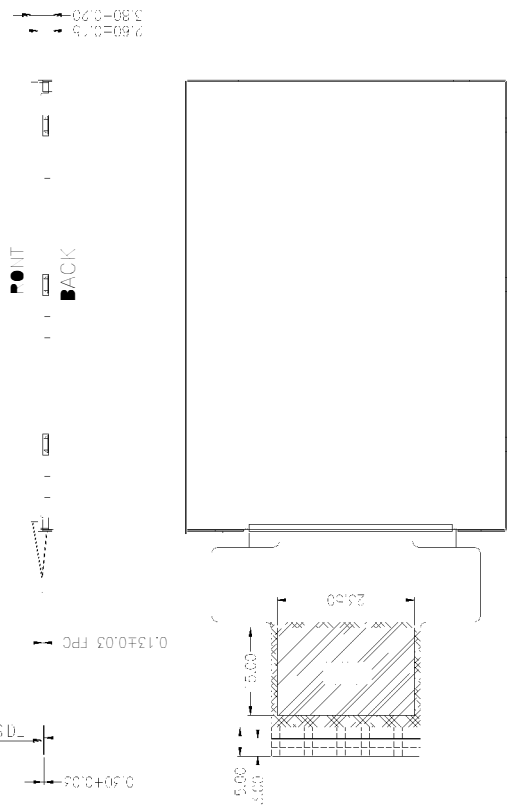
General Information Items	Specification Main Panel	Unit	Note
TFT Display area (AA)	48.60(H) x 64.80(V) (3.2 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	65k/262k	colors	-
Number of pixels	240(RGB)x320	pixels	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.2025(H)x0.2025(V)	mm	-
Viewing angle	6:00	o'clock	-
TFT Controller IC	ST7789V	-	-
TFT Interface	Parallel & Serial	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20-+70	℃	-
Storage temperature	-30-+80	℃	-

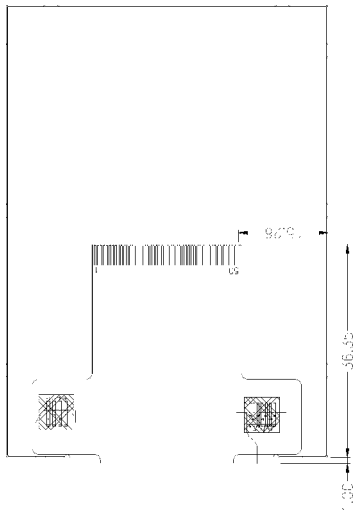
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		55.00		mm	-
	Vertical (V)		77.20		mm	-
	Depth (D)		2.60		mm	-
	Weight		--		g	

1. Outline Dimensions





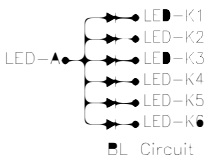


NO.	Pin Name
1	GND
2	XR
3	YD
4	XL
5	YU
6	IOVCC
7	IOVCC
8	VCI
9	VCI
10	IM2
11	IM1
12	IM0
13	RESET
14	CS
15	RS(SPI-SCL)
16	WR(SPI-HS)
17	RD
18	VSYNC
19	HSYNC
20	ENABLE
21	DOTCLK
22	SDA
23	DB0(B0)
24	DB01(B1)
25	DB02(B2)
26	DB03(B3)
27	DB04(B4)
28	DB05(B5)
29	DB06(G0)
30	DB07(G1)
31	DB08(G2)
32	DB09(G3)
33	DB10(G4)
34	DB11(G5)
35	DB12(R0)
36	DB13(R1)
37	DB14(R2)
38	DB15(R3)
39	DB16(R4)
40	DB17(R5)
41	SDO
42	GND
43	LEDA
44	LEDK1
45	LEDK2
46	LEDK3
47	LEDK4
48	LEDK5
49	LEDK6
50	GND

NOTE: MCU interface SET for IM PINS.

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 16-bit interface	DB17-DB10, DB8-DB1
0	0	1	DBI Tyb_ 8-bit interface	DB17-DB10
0	1	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	1	1	DBI Tyb_ 9-bit interface	DB17-DB9
1	0	1	3-Wire 9 BIT data serial interface.	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:
If not use PINS fix to the GND , IOVCC or NC.



NOTE: RGB interface

RGB Interface	DB Pin in use
16(565) Bit RGB interface	DB17-DB13, DB11-DB6, DB5-DB1
18(666) Bit RGB interface	DB17-DB0

NOTE: If used RGB mode must select serial interface!

1.) Display Type: 3.2" TFT, 65k/262k colors
2.) Display mode: Transmissive, Normally White
3.) 12:00 viewing direction
4.) TFT Driver IC: ST7789V (COG)
5.) VDD/VCI: 3.3V, IOVCC:1.8-3.3V
6.) Operating Tempe: -20-70 C, Storage Temp: -30-80 C
7.) Backlight: LED White, 6 LEDs, 120mA, 3.2+/-0.3V
8.) RoHS Compliant

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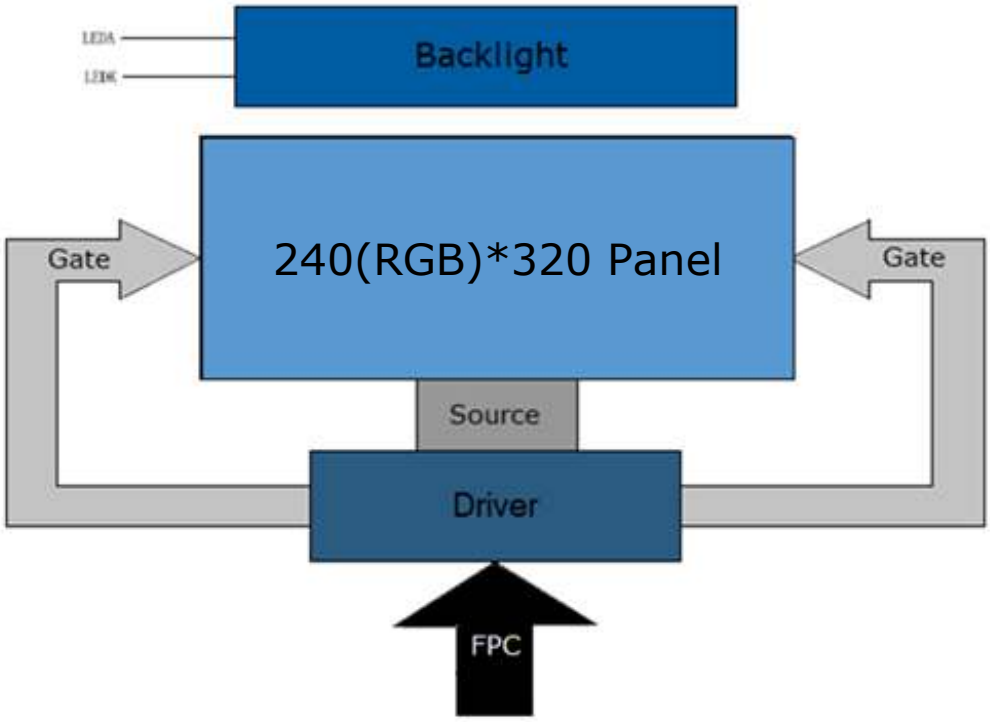
TOLERANCE	DRAWING NAME	
	PART NO.	E32RA-CW350-R
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn	Unit
	Checked	mm
Scale 1:1	Approve	Page 1/1

2. Block Diagram



3. Input Terminal Pin Assignment

Recommended TFT Connector: FH12S-50S-0.5SH(55) | Recommended RTP Connector: FH33-4S-1SH(10)

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	XR	Touch panel right glass terminal	A/D
3	YD	Touch panel bottom film terminal	A/D
4	XL	Touch panel left glass terminal	A/D
5	YU	Touch panel top film terminal	A/D
6	IOVCC	Supply voltage for I/O (1.8-3.3V)	P
7	IOVCC	Supply voltage for I/O (1.8-3.3V)	P
8	VCI	Supply voltage (3.3V)	P
9	VCI	Supply voltage (3.3V)	P
10	IM2	MPU Parallel interface bus and serial interface selection. If using the RGB interface you must select the serial interface.	P
11	IM1		I
12	IM0		I
13	RESET	Reset signal of the device.	I
14	CS	Chip select pin, low enable. Pin to VCI or GND when not used.	I
15	D/CX(SPI-SCL)	Data/command signal for the MCU parallel interface. D/CX=1: data, D/CX=0: command. The clock for the serial interface.	I
16	WR(SPI-RS)	Write signal for the parallel MCU interface. Serial register select signal for the 4-wire SPI interface. Pin to VCI or GND when not used.	I
17	RD	Read signal for the parallel MCU interface. Pin to VCI or GND when not used.	O
18	VSYNC	Frame synchronizing signal for the RGB interface. Pin to VCI or GND when not used.	I
19	HSYNC	Line synchronizing signal for the RGB interface. Pin to VCI or GND when not used.	I
20	ENABLE	Data enable signal for the RGB interface. Pin to VCI or GND when not used.	I
21	DOTCLK	Dotclock signal for the RGB interface. Pin to VCI or GND when not used.	I
22	SDA	Serial input signal for the serial interface. Pin to VCI or GND when not used.	I/O
23-40	DB[0:17]	18-bit bi-directional data bus for the parallel interfaces.	I/O
41	SDO	SPI Interface output pin. Leave pin open if not used.	O
42	GND	Ground	P
43	LEDA	Anode pin of the backlight	P
44	LEDK1	Cathode pin of the backlight	P
45	LEDK2	Cathode pin of the backlight	P
46	LEDK3	Cathode pin of the backlight	P
47	LEDK4	Cathode pin of the backlight	P
48	LEDK5	Cathode pin of the backlight	P
49	LEDK6	Cathode pin of the backlight	P
50	GND	Ground	P

I: Input, O: Output, P: Power

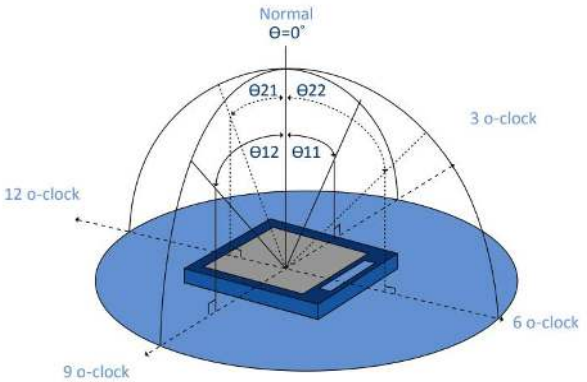
4. LCD Optical Characteristics

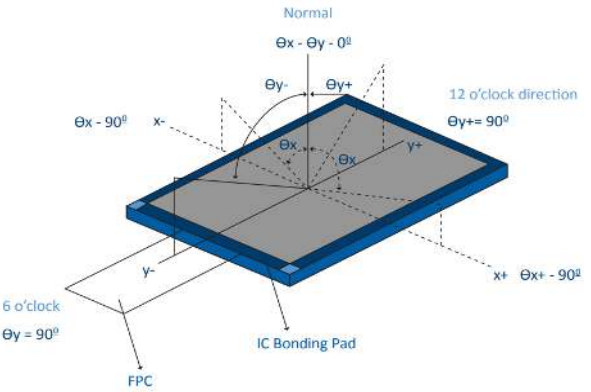
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%	θ=0 Normal viewing angle	--	60	--	%	(3)
Contrast Ratio		CR		400	500	--	%	(2)
Response Time	Rising	TR+TF		--	16	32	ms	(4)
	Falling							
Color Filter Chromaticity	White	W_X		0.283	0.303	0.323		(5)(6)
		W_Y		0.305	0.325	0.345		
	Red	R_X		0.606	0.626	0.646		
		R_Y		0.314	0.334	0.354		
	Green	G_X		0.257	0.277	0.297		
		G_Y		0.529	0.549	0.569		
	Blue	B_X		0.122	0.142	0.162		
		B_Y		0.102	0.122	0.142		
Viewing Angle	Hor.	ΘL	CR≥10	50	70	--	degrees	(1)(6)
		ΘR		50	70	--		
	Ver.	ΘT		60	75	--		
		ΘB		40	50	--		
Option View Direction		6:00						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



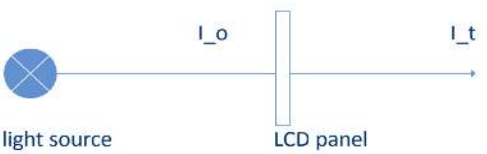


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

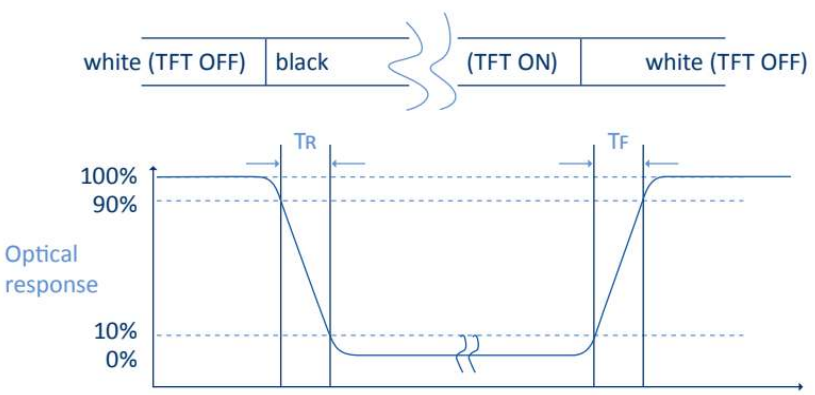
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

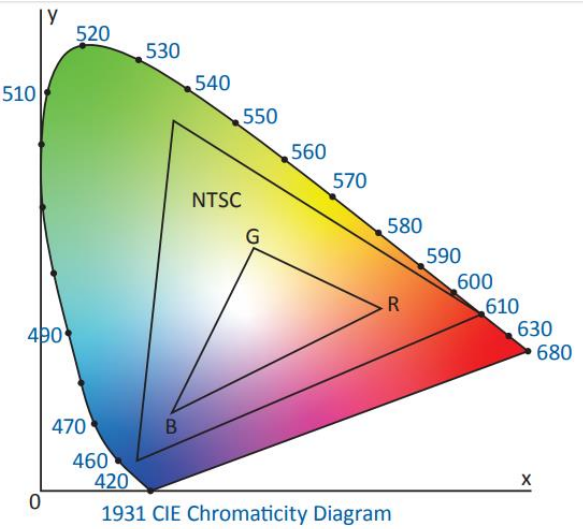
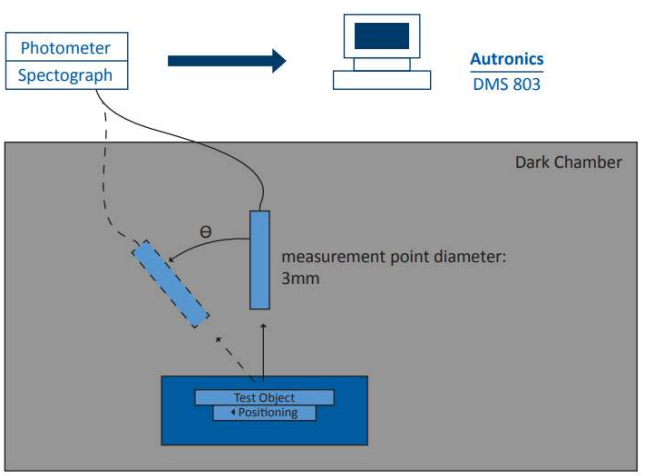


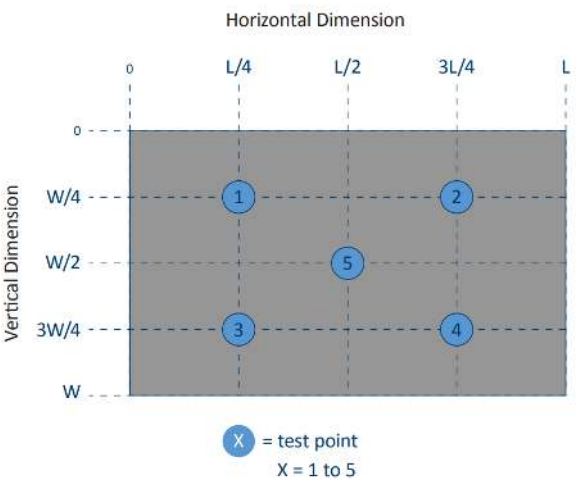
Fig. 1931 CIE chromacity diagram

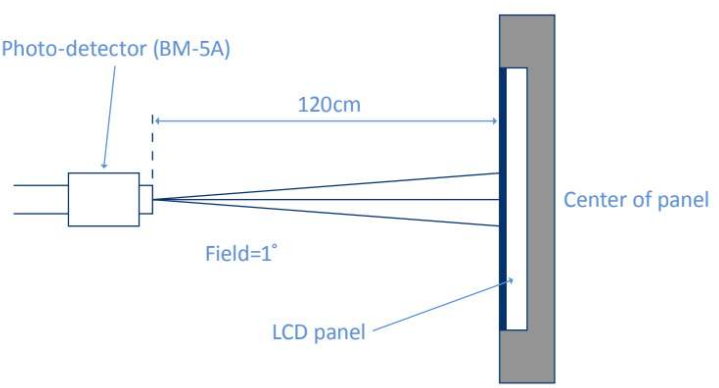
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.8	V
DC/DC Supply Voltage	IOVCC	-0.3	4.6	
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VCI	2.4	3.3	3.6	V	
Digital Supply Voltage	IOVCC	1.65	3.3	4.8	V	
Normal Mode Current	IDD	--	8	--	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC		
	VIL	GND	--	0.3IOVCC		
Level Output Voltage	VOH	0.8IOVCC	--	IOVCC		
	VOL	GND	--	0.2IOVCC		

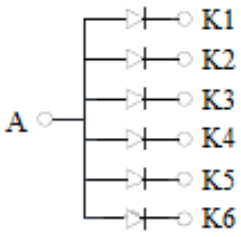
5.4 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	90	120	--	mA	
Forward Voltage	VF	--	3.2	--	V	
LCM Luminance	LV	350	--	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 6 white LEDs.

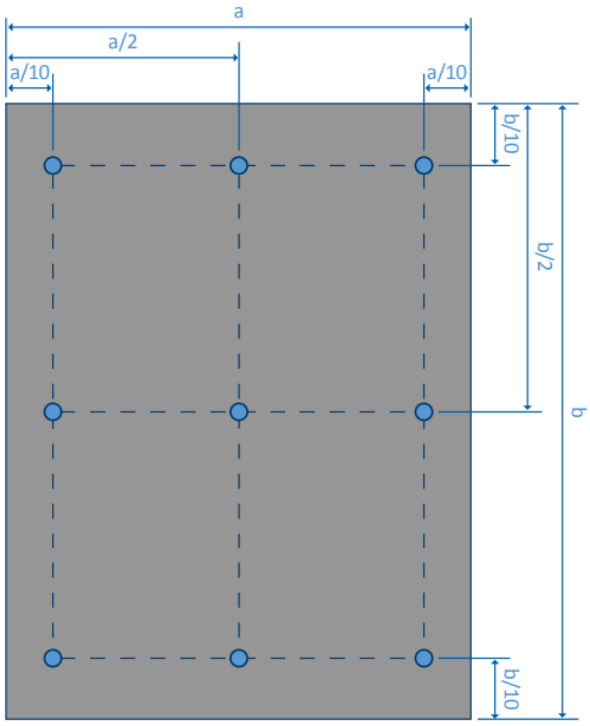
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=120mA. The LED lifetime could be decreased if operating IL is larger than 120mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristic

6.1 Parallel RGB Interface Characteristics

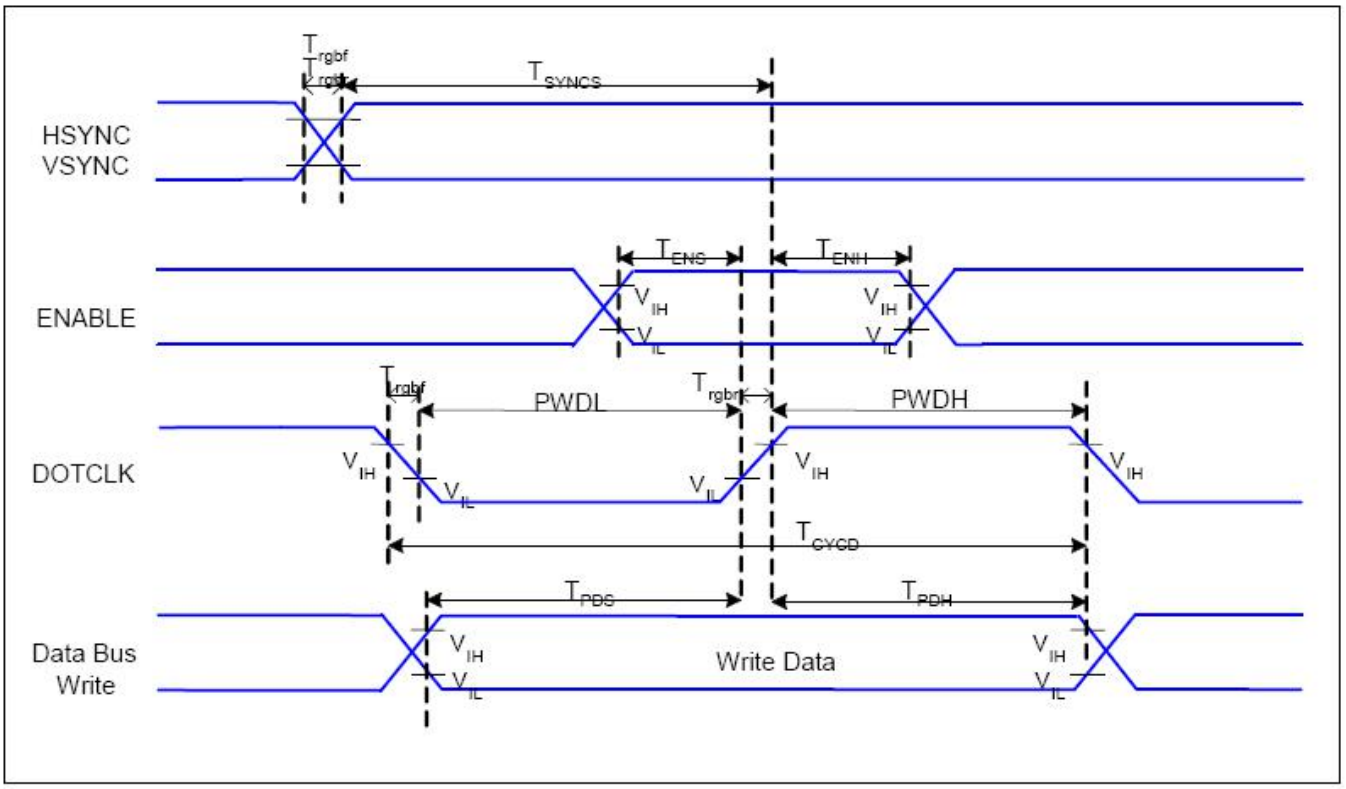


Figure 6.1: Parallel RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK Rise/Fall Time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 6.1: Parallel RGB Interface Timing Characteristics

6.2 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

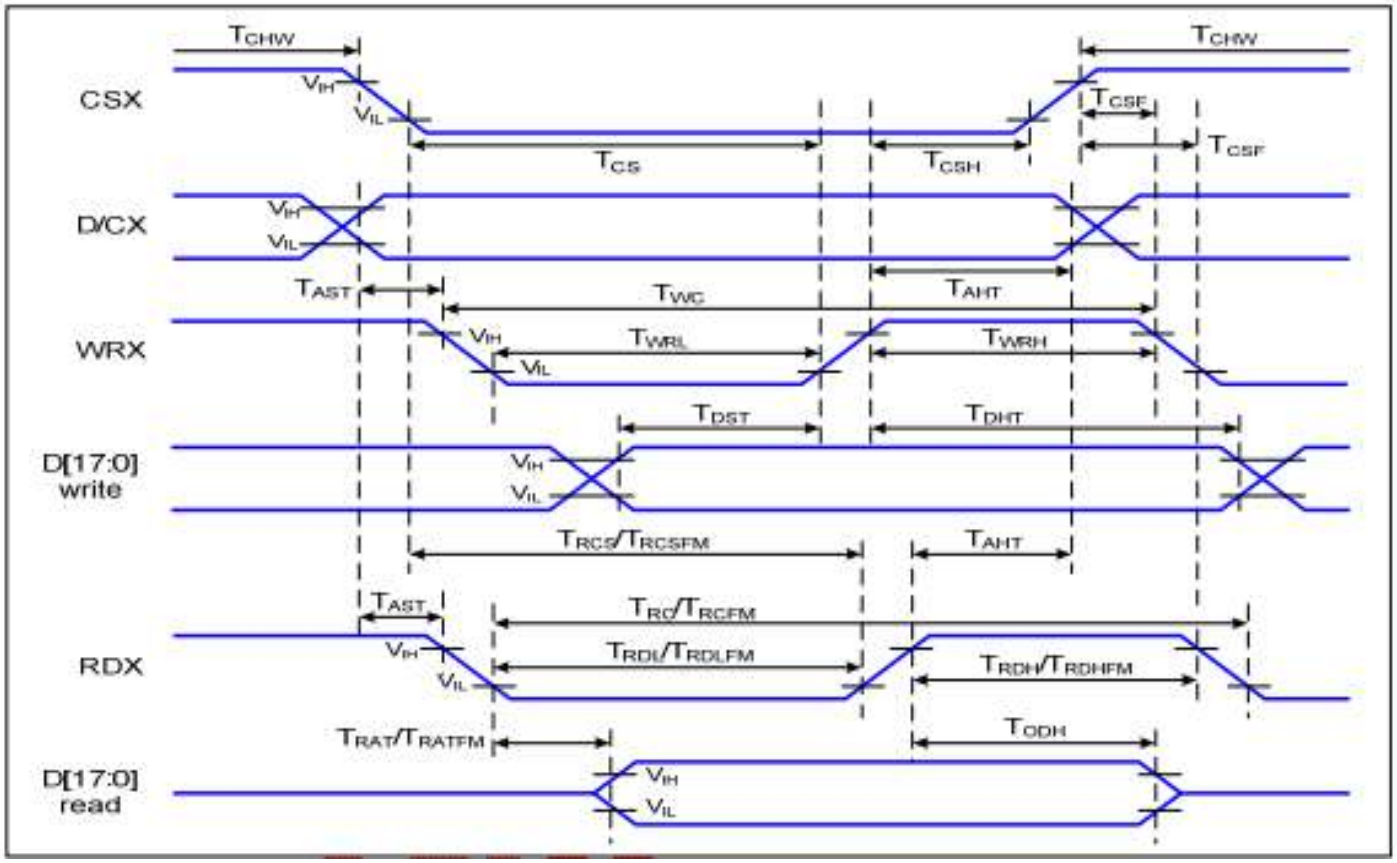


Figure 6.2: Parallel Interface Timing Characteristics (8080-Series MCU Interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0	-	ns	
	T_{AHT}	Address hold time (Write/Read)	10	-	ns	
CSX	T_{CHW}	Chip select "H" pulse width	0	-	ns	
	T_{CS}	Chip select setup time (Write)	15	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	45	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
WRX	T_{WC}	Write cycle	66	-	ns	
	T_{WRH}	Control pulse "H" duration	15	-	ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160	-	ns	
	T_{RDH}	Control pulse "H" duration (ID)	90	-	ns	
	T_{RDL}	Control pulse "L" duration	45	-	ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450	-	ns	
	T_{RDHFM}	Control pulse "H" duration (FM)	90	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355	-	ns	
D[17:0] D[15:0], D[8:0], D[7:0]	T_{DST}	Write data setup time	10	-	ns	
	T_{DHT}	Write data hold time	10	-	ns	For max CL=30pF
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	For min CL=8pF
	T_{ROD}	Output disable time	20	80	ns	

Table 6.2: 8080 Series MCU Parallel Timing Characteristics

6.3 Display Serial Interface Characteristics (3-line SPI system)

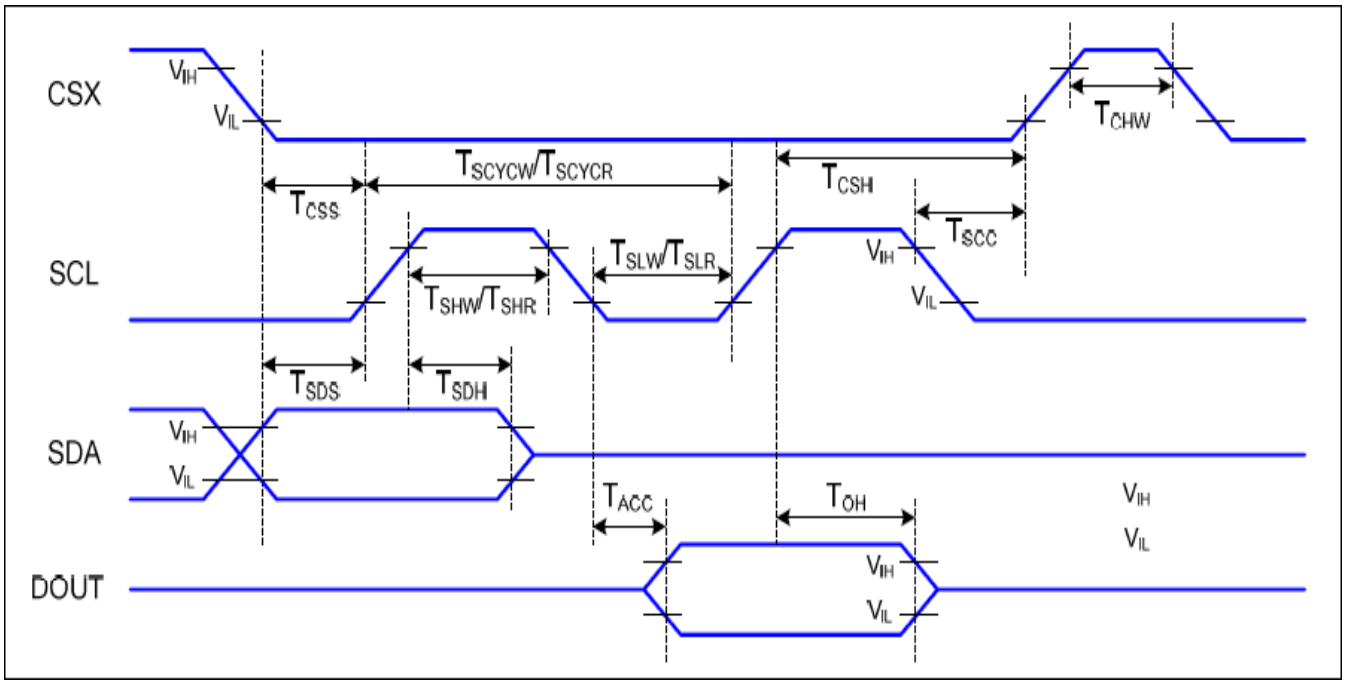


Figure 6.3: Serial Interface **3-SPI Timing Diagram**

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 Cº

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10			
DOUT	T_{ACC}	Access time	10	50	ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50		

Table 6.4: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.4 Display Serial Interface Characteristics (4-line SPI serial)

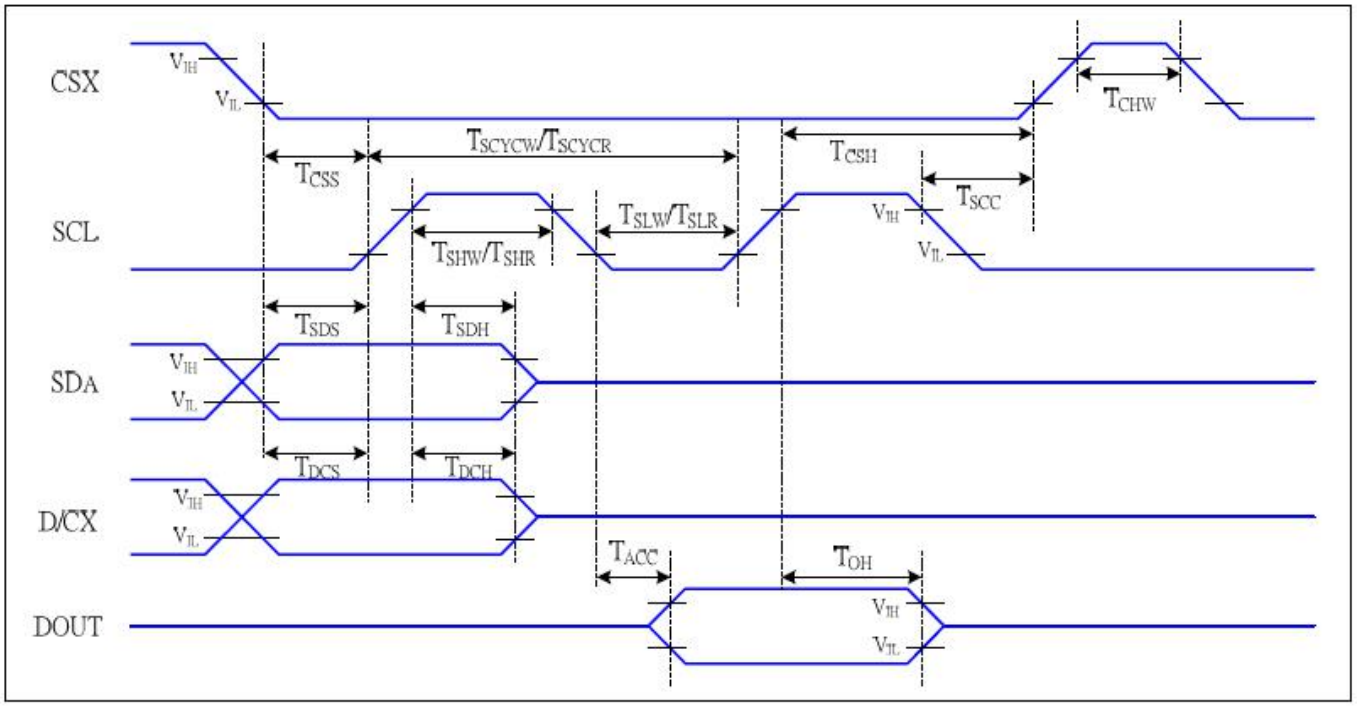


Figure 6.4: Serial Interface **4-SPI Timing Diagram**

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	write command & data ram
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	read command & data ram
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 6.5: 4-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.5 Reset Timing

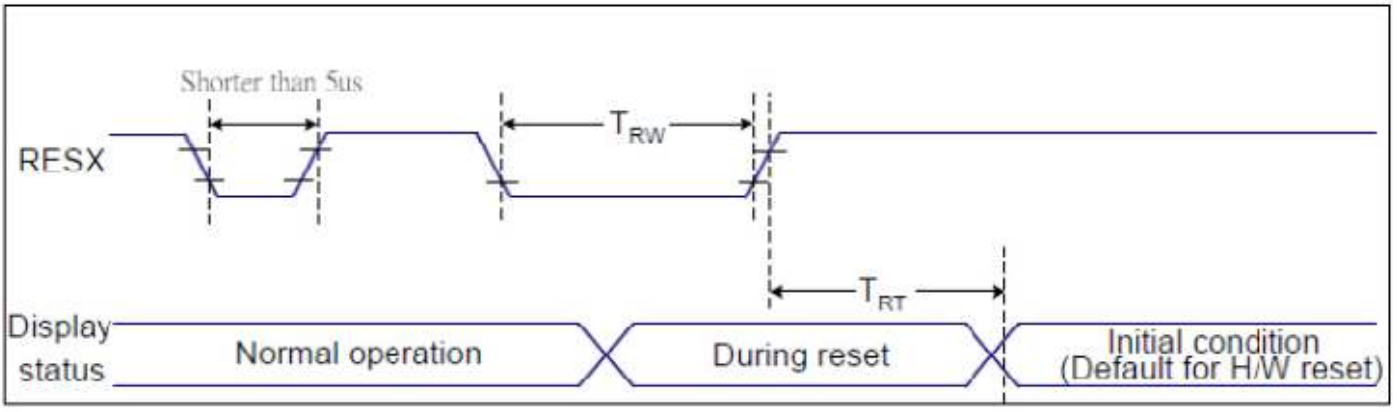


Figure 6.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

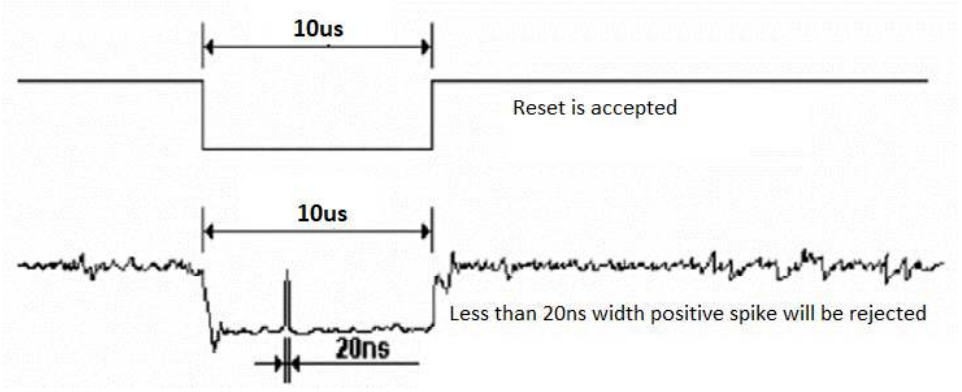
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.