

## Fast CMOS Octal Registered Transceivers

### Product Features:

- PI74FCT646T/648T/651T/652T/2646T/2652T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
  - 24-pin 300 mil wide plastic DIP (P)
  - 24-pin 150 mil wide plastic QSOP (Q)
  - 24-pin 150 mil wide plastic TQSOP (R)
  - 24-pin 300 mil wide plastic SOIC (S)
- Device models available upon request

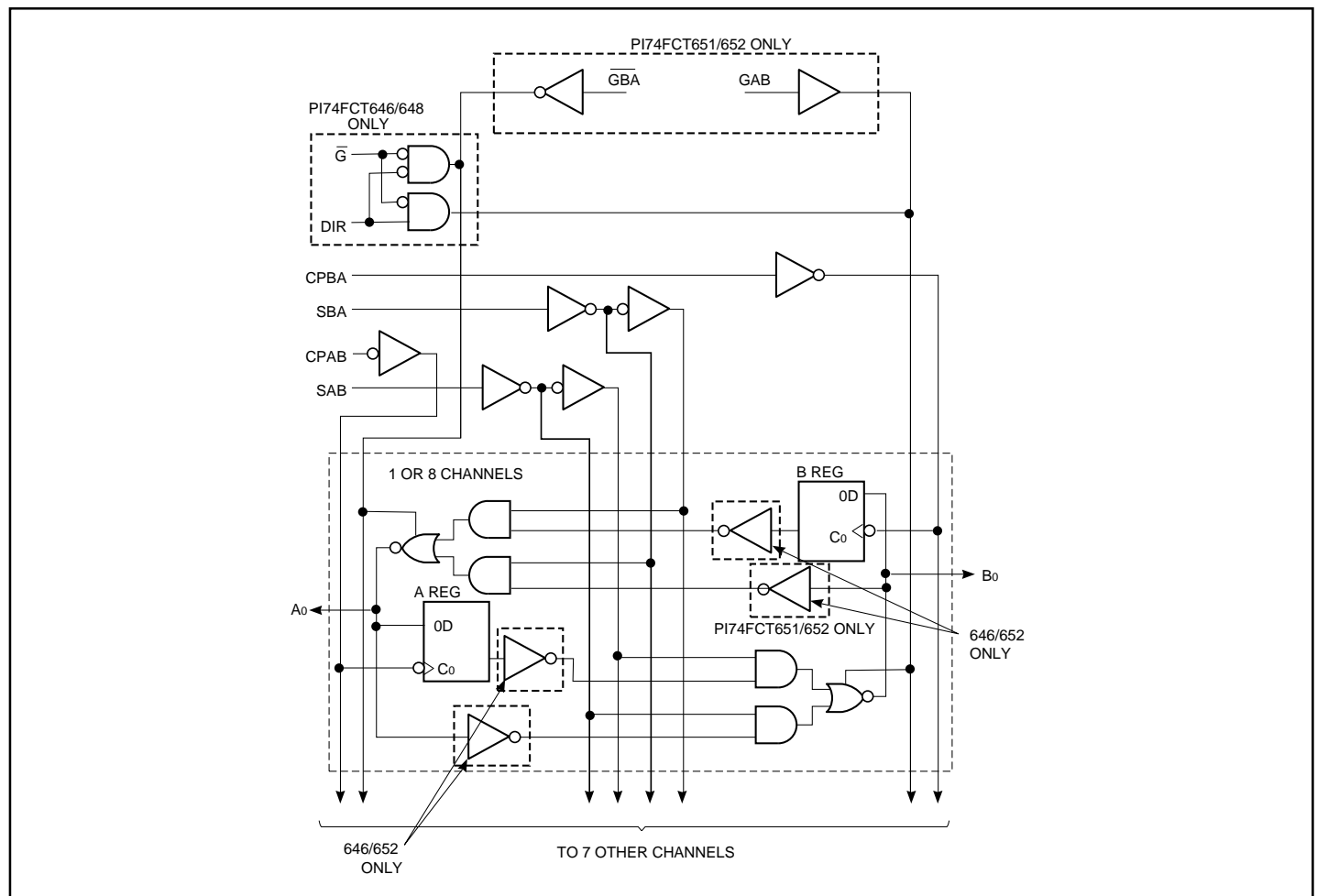
### Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6/0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

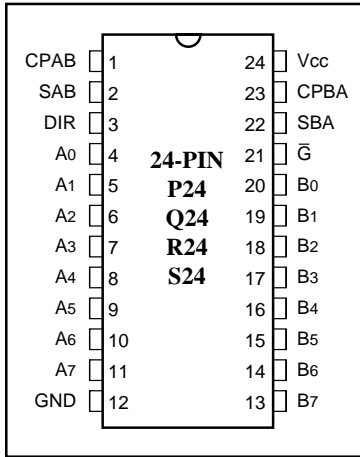
The PI74FCT646T/648T/651T/652T and PI74FCT2646T/2652T are designed with a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The PI74FCT651/652T/2652T utilize GAB and GBA signals to control the transceiver functions. The PI74FCT646/2646T/648T utilize the enable control (G) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT646T is a non-inverting option of the PI74FCT648T. The PI74FCT652T is a non-inverting option of the PI74FCT651T.

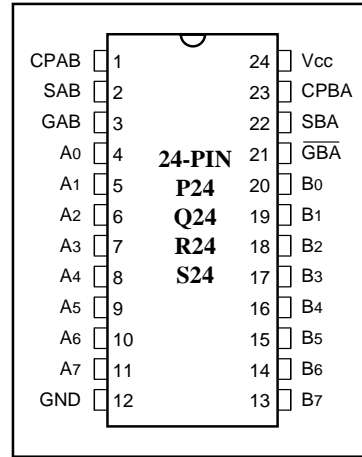
### Logic Block Diagram



**PI74FCT646/648T**  
**Product Pin Configuration**



**PI74FCT651/652T**  
**Product Pin Configuration**



**Product Pin Description**

Pin Name	Description
A0-A7	Data Register A Inputs Data Register B Outputs
B0-B7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\bar{G}$	Output Enable Inputs (646/648/2646)
GAB, $\bar{G}\bar{B}\bar{A}$	Output Enable Inputs (651/652/2652)
GND	Ground
Vcc	Power

**PI74FCT646/648/2646T Truth Table**

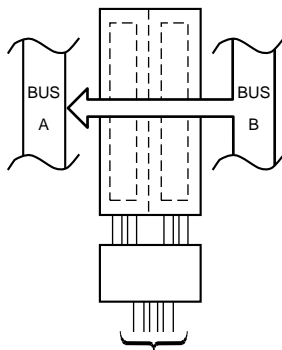
PI74FCT646/2646T Function/Operation	PI74FCT648T Function/Operation	Inputs						DATA I/O <sup>(2)</sup>	
		$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	Real Time $\bar{B}$ Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	Stored $\bar{B}$ Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	Real Time $\bar{A}$ Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus	L	H	H or L	X	H	X		

**PI74FCT651/652/2652T Truth Table**

PI74FCT651T Function/Operation	PI74FCT652/2652T Function/Operation	Inputs						DATA I/O <sup>(2)</sup>	
		GAB	$\bar{G}\bar{B}\bar{A}$	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified <sup>(1)</sup>
Store A in Both Registers <sup>(3)</sup>	Store A in Both Registers	H	H	↑	↑	X <sup>(2)</sup>	X	Input	Output
Hold A, Store B	Hold A, Store B	L	X	H or L	↑	X	X	Unspecified <sup>(1)</sup>	Input
Store B in Both Registers <sup>(4)</sup>	Store B in Both Registers	L	L	↑	↑	X	X <sup>(2)</sup>	Output	Input
Real Time $\bar{B}$ Data to A Bus	Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored $\bar{B}$ Data to A Bus	Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time $\bar{A}$ Data to B Bus	Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored $\bar{A}$ Data to B Bus	Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored $\bar{A}$ Data to B Bus and Stored $\bar{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

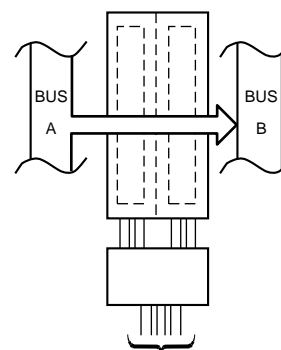
- The data output functions may be enabled or disabled by various signals at the GAB or  $\bar{G}\bar{B}\bar{A}$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.  
Select control = H: clocks must be staggered in order to load both registers.
- $\bar{A}$  in B Register
- $\bar{B}$  in A Register

**REAL-TIME TRANSFER  
BUS B TO A**



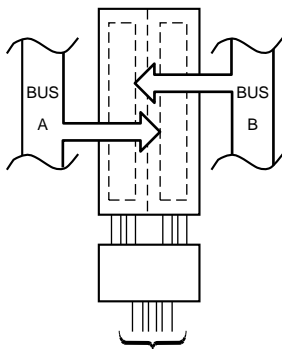
<b>646/648/ 2646</b>	<b>DIR</b>	$\bar{\mathbf{G}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	L	L	X	X	X	L
<b>651/652/ 2652</b>	<b>GAB</b>	$\bar{\mathbf{GBA}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	L	L	X	X	X	L

**REAL-TIME TRANSFER  
BUS A TO B**



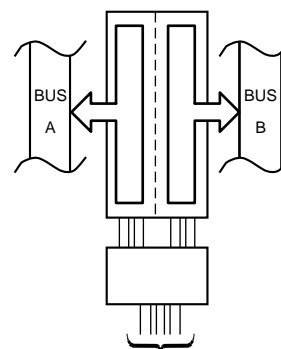
<b>646/648/ 2646</b>	<b>DIR</b>	$\bar{\mathbf{G}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	H	L	X	X	L	X
<b>651/652/ 2652</b>	<b>GAB</b>	$\bar{\mathbf{GBA}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	H	H	X	X	L	X

**STORAGE FROM  
A AND/OR B**



<b>646/648/ 2646</b>	<b>DIR</b>	$\bar{\mathbf{G}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
<b>651/652/ 2652</b>	<b>GAB</b>	$\bar{\mathbf{GBA}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

**TRANSFER STORES  
DATA TO A AND/OR B**



<b>646/648<sup>(1)</sup> 2646</b>	<b>DIR</b>	$\bar{\mathbf{G}}$	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
<b>651/652/ 2652</b>	<b>GAB</b>	<b>GBA</b>	<b>CPAB</b>	<b>CPBA</b>	<b>SAB</b>	<b>SBA</b>
	H	L	H or L	H or L	H	H

1. Note: The FCT646/2646 cannot transfer data to A bus and B bus simultaneously.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) .....	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current .....	120 mA
Power Dissipation .....	0.5W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 64 mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12 mA (25Ω Series)		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = MAX.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
Vik	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
Ios	Short Circuit Current	VCC = Max. <sup>(3)</sup> , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

### Capacitance (TA = 25°C, f = 1 MHz)

Parameters <sup>(4)</sup>	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

**Notes:**

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

### Power Supply Characteristics

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND or V <sub>CC</sub>		0.1	500	μA
ΔI <sub>CC</sub>	Supply Current per Input @ TTL HIGH	V <sub>CC</sub> = Max.,	V <sub>IN</sub> = 3.4V <sup>(3)</sup>		0.5	2.0	mA
I <sub>CCD</sub>	Supply Current per Input per MHz <sup>(4)</sup>	V <sub>CC</sub> = Max., Outputs Open $\overline{G} = \overline{DIR} = \text{GND}$ or $GAB = \overline{GBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10 MHz 50% Duty Cycle $\overline{G} = \overline{DIR} = \text{GND}$ or $GAB = \overline{GBA} = \text{GND}$ f <sub>I</sub> = 5 MHz One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		1.5	3.5 <sup>(5)</sup>	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND		2.0	5.5 <sup>(5)</sup>	
		V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10 MHz 50% Duty Cycle $\overline{G} = \overline{DIR} = \text{GND}$ or $GAB = \overline{GBA} = \text{GND}$ Eight Bits Toggling f <sub>I</sub> = 2.5 MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		3.8	7.3 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND		6.0	16.3 <sup>(5)</sup>	

**Notes:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

6. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

### PI74FCT646/2646T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	646T/2646T		646AT/2646AT		646CT		646DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
tpZH tpZL	Output Enable Time Ḡ, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> Ḡ, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width <sup>(3)</sup> HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

### PI74FCT648T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	648T		648AT		648CT		648DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
tpZH tpZL	Output Enable Time Ḡ, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> Ḡ, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width <sup>(3)</sup> HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

**Notes:**

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.

### PI74FCT651T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	651T		651AT		651CT		651DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
tpZH tpZL	Output Enable Time G <sub>BA</sub> , G <sub>AB</sub> to Bus		2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> G <sub>BA</sub> , G <sub>AB</sub> to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay S <sub>BA</sub> or S <sub>AB</sub> to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width <sup>(3)</sup> HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

### PI74FCT652/2652T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	652T/2652T		652AT/2652AT		652CT		652DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
tpZH tpZL	Output Enable Time G <sub>BA</sub> , G <sub>AB</sub> to Bus		2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> G <sub>BA</sub> , G <sub>AB</sub> to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay S <sub>BA</sub> or S <sub>AB</sub> to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width <sup>(3)</sup> HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

**Notes:**

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.