HARRIS
SEMICONDUCTOR

HM-65162

2K x 8 Asynchronous CMOS Static RAM

January 1992

Features

- **Fast Access Time** . . . . **70/90ns Max**
- **Low Standby Current** . . . . **50µA Max**
- **Low Operating Current** . . . . **70mA Max**
- **Data Retention at 2.0 Volts** . . . . **20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout (2716, 6116 Type)**
- **No Clocks or Strobes Required**
- **Equal Cycle and Access Time**
- **Single 5 Volt Supply**
- **Gated Inputs**
  - **No Pull-Up or Pull-Down Resistors Required**

Description

The HM-65162 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8 bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8 bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Ordering Information

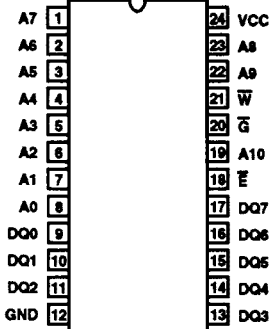| PACKAGE	TEMPERATURE RANGE	55ns/40µA*	70ns/20µA*	90ns/40µA*	90ns/300µA*
Ceramic DIP	-40°C to +85°C	HM1-65162S-9	HM1-65162B-9	HM1-65162-9	HM1-65162C-9
/883**	-55°C to +125°C	-	HM1-65162B/883	HM1-65162/883	HM1-65162C/883
JAN#		-	29110BJA	29104BJA	-
SMD#		-	8403606JA	8403602JA	8403603JA
LCC	-40°C to +85°C	-	HM4-65162B-9	HM4-65162-9	HM4-65162C-9
/883**	-55°C to +125°C	-	HM4-65162B/883	HM4-65162/883	HM4-65162C/883
JAN#		-	29110BXA	29104BXA	-
SMD#		-	8403606ZA	8403602ZA	8403603ZA

* Access Time/Data Retention Supply Current.

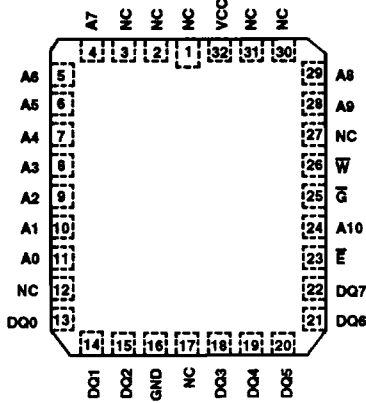** Respective /883 specifications are included at the end of this data sheet.

File Number **3000**

Pinouts

24 LEAD DIP
TOP VIEW

A7 1	24 VCC
A6 2	23 A8
A5 3	22 A9
A4 4	21 W̄
A3 5	20 Ḡ
A2 6	19 A10
A1 7	18 Ē
A0 8	17 DQ7
DQ0 9	16 DQ6
DQ1 10	15 DQ5
DQ2 11	14 DQ4
GND 12	13 DQ3

32 LEAD LCC
TOP VIEW

A7 NC NC NC VCC NC NC
4 3 2 1 32 31 30

A6 5		29 A8
A5 6		28 A9
A4 7		27 NC
A3 8		26 W̄
A2 9		25 Ḡ
A1 10		24 A10
A0 11		23 Ē
NC 12		22 DQ7
DQ0 13		21 DQ6

14 15 16 17 18 19 20
DQ1 DQ2 GND NC DQ3 DQ4 DQ5

PIN NAMES

PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
Ē	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
W̄	Write Enable
Ḡ	Output Enable

Functional Diagram
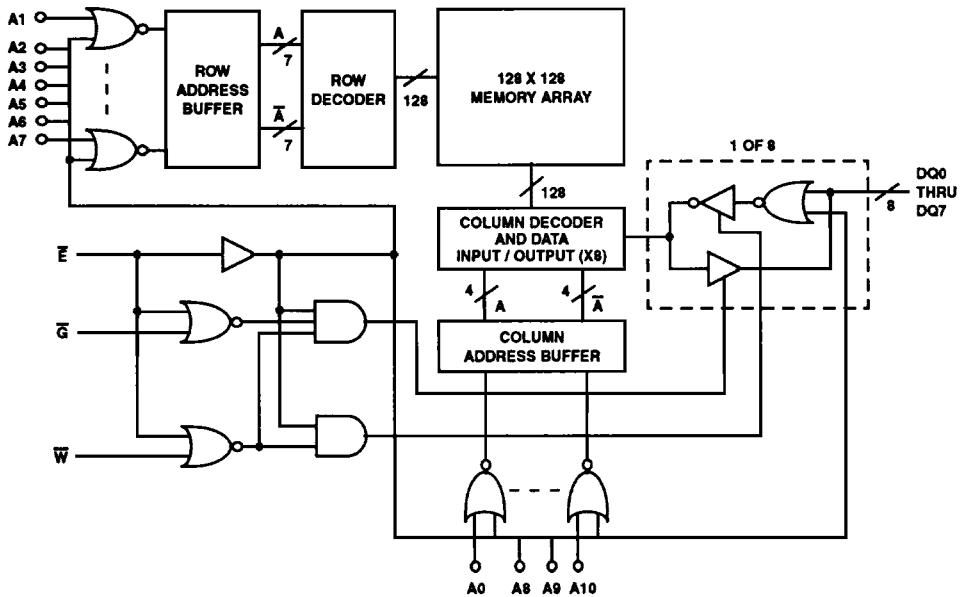
Absolute Maximum Ratings

Supply Voltage . . . . +7.0V
Input, Output or I/O Voltage . . . . GND-0.3V to VCC+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature. . . . . +175°C
Lead Temperature (Soldering 10s). +300°C
Typical Derating Factor . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1W
Ceramic LCC Package 0.58W
Gate Count . . . . 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +4.5V to +5.5V

Operating Temperature Range
HM-65162S-9, HM-65162B-9,
HM-65162-9, HM65162C-9 . . . . -40°C to +85°C

DC Electrical Specifications VCC = 5V ± 10%; T_A = -40°C to +85°C (HM-65162S-9, HM-65162B-9, HM-65162-9, HM-65162C-9)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
ICCSB1	Standby Supply Current	-	50	μA	HM-65162B-9, IO = 0mA, $\overline{E}$ = VCC - 0.3V, VCC = 5.5V
		-	100	μA	HM-65162S-9, HM65162-9, IO = 0mA, $\overline{E}$ = VCC - 0.3V, VCC = 5.5V
		-	900	μA	HM-65162C-9, IO = 0mA, $\overline{E}$ = VCC - 0.3V, VCC = 5.5V
ICCSB	Standby Supply Current	-	8	mA	$\overline{E}$ = 2.2V, IO = 0mA, VCC = 5.5V
ICCEN	Enabled Supply Current	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, VCC = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, f = 1MHz, VCC = 5.5V
ICCDR	Data Retention Supply Current	-	20	μA	HM-65162B-9, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V
		-	40	μA	HM-65162S-9, HM-65162-9, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V
		-	300	μA	HM-65162C-9, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND, VCC = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND, VCC = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 4.5V
VIH	Input High Voltage	2.2	VCC+0.3	V	VCC = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA, VCC = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA, VCC = 4.5V
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100μA, VCC = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	12	pF	

NOTES: 1. Typical derating 5mA/MHz increase in ICCOP.

2. Tested at initial design and after major design changes.

AC Electrical Specifications VCC = 5V ± 10%, T$_A$ = -40°C to +85°C (HM-65162S-9, HM-65162B-9, HM65162-9, HM-65162C-9)

|		LIMITS									
		HM-65162S-9		HM-65162B-9		HM-65162-9		HM-65162C-9			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
READ CYCLE											
(1) TAVAX	Read Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3, 4)
(3) TELQV	Chip Enable Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3)
(4) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(5) TGLQV	Output Enable Access Time	-	35	-	50	-	65	-	65	ns	(Notes 1, 3)
(6) TGLQX	Output Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(7) TEHQZ	Chip Enable Output Disable Time	-	35	-	35	-	50	-	50	ns	(Notes 2, 3)
(8) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(9) TAVQX	Output Hold From Address Change	5	-	5	-	5	-	5	-	ns	(Notes 1, 3)
WRITE CYCLE											
(10) TAVAX	Write Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(11) TELWH	Chip Selection to End of Write	45	-	45	-	55	-	55	-	ns	(Notes 1, 3)
(12) TAVWL	Address Setup Time	5	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(13) TWLWH	Write Enable Pulse Width	40	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(14) TWHAX	Write Enable Read Setup Time	10	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(15) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(16) TWLQZ	Write Enable Output Disable Time	-	30	-	40	-	50	-	50	ns	(Notes 2, 3)
(17) TDVWH	Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(18) TWHDX	Data Hold Time	10	-	10	-	15	-	15	-	ns	(Notes 1, 3)
(19) TWHQX	Write Enable Output Enable Time	0	-	0	-	0	-	0	-	ns	(Notes 1, 3)
(20) TWLEH	Write Enable Pulse Set-up Time	45	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(21) TDVEH	Chip Enable Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(22) TAVWH	Address Valid to End of Write	45	-	50	-	65	-	65	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.

2. Tested at initial design and after major design changes.

3. VCC = 4.5 and 5.5V.

4. TAVQV = TELQV + TAVEL.

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CMOS MEMORY

Timing Waveforms

READ CYCLE
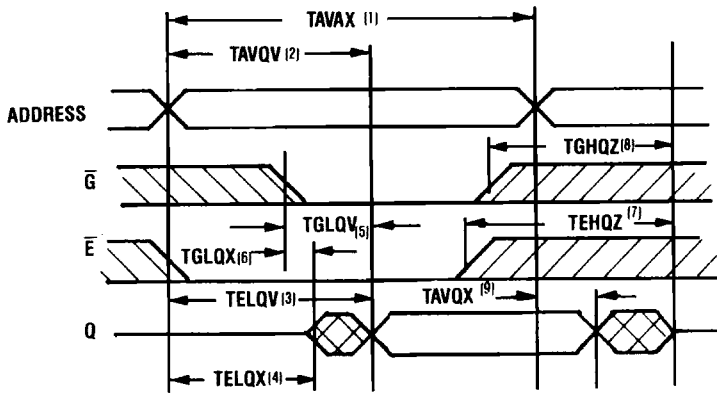
NOTE: $\overline{W}$ is High for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq$ VIL and $\overline{W} \geq$ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

WRITE CYCLE I
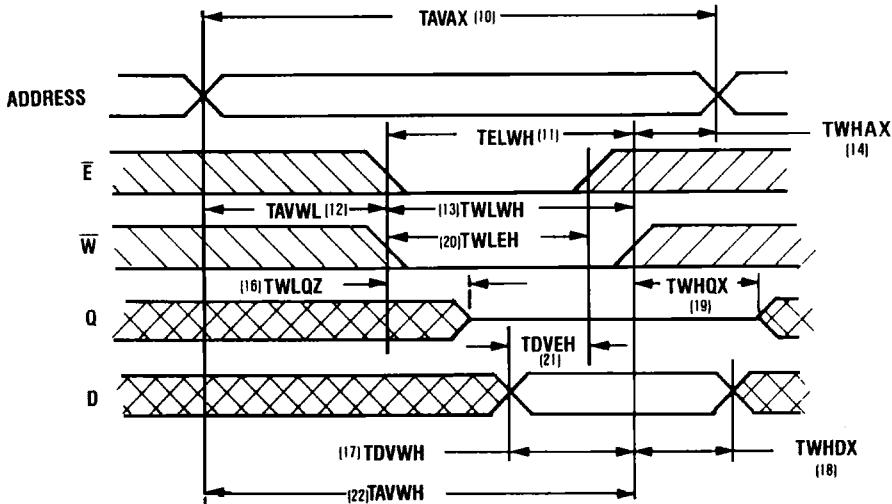
NOTE: $\overline{G}$ is Low throughout Write Cycle

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

WRITE CYCLE II
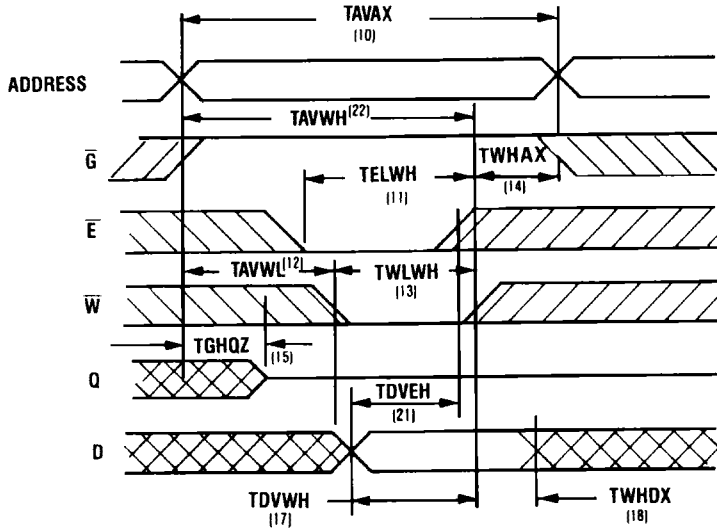
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC - 0.3V to VCC + 0.3V.

2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.

3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and down transitions.

4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING
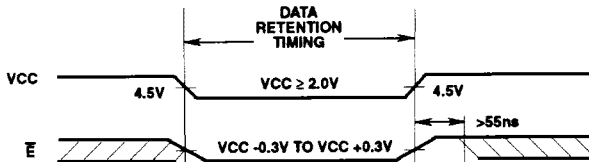
Performance Curve

TYPICAL ICCDR vs T$_A$