



# Central semiconductor Corp.

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# DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLTVS5-4 is a 4-line TVS/Diode array packaged in a TLM1031 surface mount case. With its ultra low capacitance, this device was designed to protect four high speed data or transmission lines from over-voltage transients and ESD damage.

# MARKING CODE: CTL5

# FEATURES:

- Low capacitance
- HDMI Interface Protection
- Tablets, Monitors, Displays, Smart Phones

USB 3.0 Power and Data Line Protection

Ethernet Ports

**APPLICATIONS:** 

- Low clamping voltage
- Protects four I/O lines

MAXIMUM RATINGS: (T <sub>A</sub> =25°C)	SYMBOL		UNITS
Peak Pulse Current (8x20µs)	IPP	2.5	А
Peak Power Dissipation (8x20µs)	PPK	32.5	W
Electrical Fast Transient (IEC 61000-4-4) (5x50ns)	EFT	40	А
ESD Voltage (IEC 61000-4-2, Air)	V <sub>ESD</sub>	15	kV
ESD Voltage (IEC 61000-4-2, Contact)	V <sub>ESD</sub>	8.0	kV
Operating and Storage Junction Temperature	т <sub>Ј</sub> , т <sub>stg</sub>	-55 to +150	°C

# ELECTRICAL CHARACTERISTICS PER DIODE: (T<sub>A</sub>=25°C)

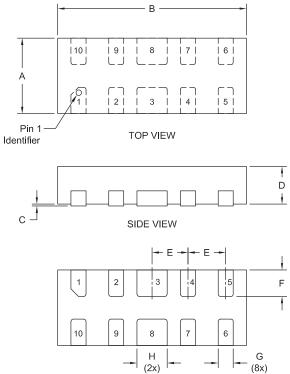
Maximum Reverse Stand-off	Reverse Breakdown Voltage		Maximum Reverse Leakage Current	Clamping	Maximum Clamping Voltage T I/O to GND		iical amping tage	Typical Dynamic Resistance	Junction C	Off State apacitance =1.0MHz)
Voltage	I/O to	GND	I/O to GND	(8x2	0µs)	(Not	te 1)	(Note 1)	I/O to GND	I/O to I/O
V <sub>RWM</sub>	V <sub>Z</sub> @	1.0mA	I <sub>R</sub> @ V <sub>RWM</sub>	V <sub>C</sub> @	D I <sub>PP</sub>	V <sub>CL</sub> @	@ I <sub>PP</sub>	R <sub>DYN</sub>	СJ	СJ
v	MIN V	MAX V	μΑ	v	А	v	А	Ω	pF	pF
5.0	6.0	9.0	1.0	12	1.0	12	4.0	0.5	0.8	0.4
5.0	6.0 9.0	1.0	13	2.5	14	8.0	0.5	0.0 0.4	0.4	

Note 1: Transmission Line Pulse (TLP) conditions: Z<sub>0</sub>=50Ω, tp=100ns

R4 (4-September 2015)







# 

R0

DIMENSIONS					
	INCHES		MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	
А	0.037	0.041	0.95	1.05	
В	0.096	0.100	2.45	2.55	
С	0.000	0.002	0.00	0.05	
D	0.018	0.022	0.45	0.55	
E	0.020		0.50		
F	0.012	0.016	0.30	0.40	
G	0.006	0.010	0.15	0.25	
Н	0.014	0.018	0.35	0.45	
TLM1021 (DE)/(DO)					

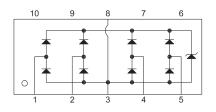
TLM1031 (REV:R0)

1) I/O	6) N/C
2) I/O	7) N/C
3) Ground	8) Ground
4) I/O	9) N/C
5) I/O	10) N/C

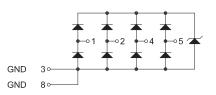
MARKING CODE: CTL5

PIN CONFIGURATION

BOTTOM VIEW



SCHEMATIC

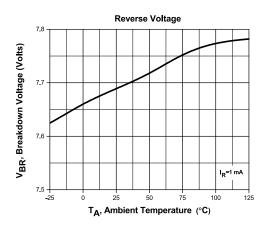


R4 (4-September 2015)

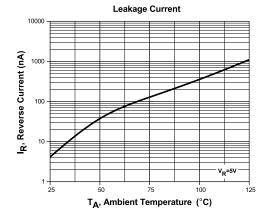
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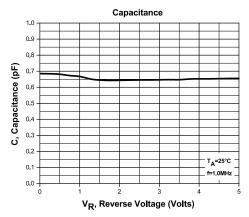




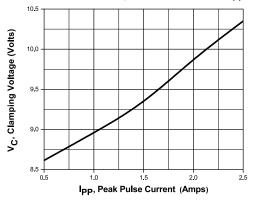


# TYPICAL ELECTRICAL CHARACTERISTICS







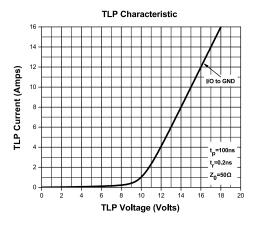


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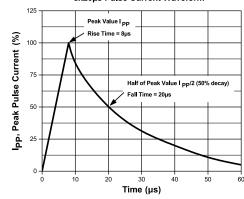
R4 (4-September 2015)



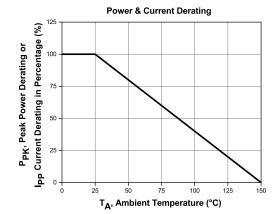








## 8x20µs Pulse Current Waveform





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# **OUTSTANDING SUPPORT AND SUPERIOR SERVICES**

#### **PRODUCT SUPPORT**

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- · Consolidated shipping options

#### **DESIGNER SUPPORT/SERVICES**

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities

Special wafer diffusions

· Custom product packing

- PbSn plating options
- Package details
- Application notes
- · Application and design sample kits

Custom bar coding for shipments

Custom product and package development

### **REQUESTING PRODUCT PLATING**

- 1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
- If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

#### CONTACT US

### **Corporate Headquarters & Customer Support Team**

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