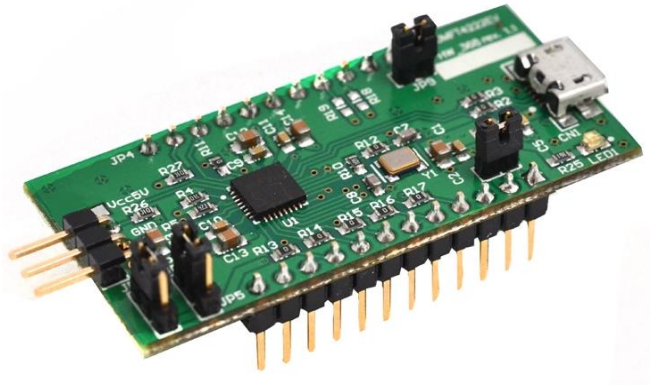
Future Technology Devices International Ltd

UMFT4222EV

USB2.0 to QuadSPI/I2C Bridge Development Module Datasheet



1 Introduction

The UMFT4222EV is a development module which uses FTDI's FT4222H, a Hi-Speed USB2.0 to QuadSPI/I^{2}C Bridge in compact 32-pin QFN package. FT4222H requires an external Crystal (12MHz) for the internal PLL to operate. It supports multi-voltage IO, 3.3V, 2.5V or 1.8V. It also provides 128 Bytes one-time-programmable (OTP) memory space for storing vendor specific information. The FT4222H contains SPI/ I^{2}C configurable interfaces. The SPI interface can be configured as master mode with single, dual, or quad bits data width transfer or slave mode with single bit data width transfer. The I^{2}C interface can be configured as master or slave mode.

The UMFT4222EV is supplied as a small PCB which is designed to plug into a standard 0.8" wide 24 pin DIP socket. All components are Pb-free (RoHS compliant).

1.1 USB Compliant

The UMFT4222EV is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 10007740.

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2 Features

The UMFT4222EV has the following features:

- Single Hi-Speed USB 2.0 chip (FT4222H) to flexible and configurable SPI/I^2C interfaces.
- SPI interface support for Single / Dual / Quad SPI Master Mode with configurable target operating speed.
- Up to 28Mbps data transfer rate in SPI mode with quad data mode.
- Support up to 4 slave selection control pins in SPI master mode.
- Support Single SPI Slave Mode with SCK operating frequency up to 20MHz.
- I^2C interface support 7-bits address and fully compatible to v2.1 and v3 specification for I^2C Master/Slave Mode with configurable target operating speed for 100kbit/S standard mode, 400kbit/S fast mode 1Mbit/S Fast mode plus and 3.4Mbit/S high speed mode.
- Configurable GPIOs controlled by application software via USB bus
- Fully support USB2.0 suspend/resume and remote wakeup
- Support Battery Charger Detection
- OTP memory inside for USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other vendor specific data.
- USB Power Configurations; bus-powered and self-powered.
- On board jumper for FT4222H configuration mode, USB power configuration and VCCIO source selection
- Integrated power-on-reset circuit.
- True 3.3V CMOS drive output and TTL input. (operates down to 1.8V with external 1.8V power input to VCCIO)
- USB2.0 Low operating and suspend current; 68mA (active-typ.) and 375uA (suspend-typ.).
- Configurable I/O pin output drive strength: 4 mA(min) and 16 mA(max)
- UHCI / OHCI / EHCI / XHCI host controller compatible
- FTDI's royalty-free Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases
- Supplied PCB designed to fit a standard 20.2mm (0.8") wide 24 pin DIP socket. Pins are on a 2.54mm (0.1") pitch.
- On board USB Micro-B receptacle allows module to be connected to a PC.

2.1 Typical Applications

- USB to single mode SPI master controller
- USB to dual mode SPI master controller
- USB to quad mode SPI master controller
- USB to single SPI slave controller
- USB to I^2C master interface controller
- USB to I^2C slave interface controller
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- USB Industrial Control
- USB Data Acquisition
- USB dongle implementations for Software/ Hardware Encryption and Wireless Modules
- Detect USB dedicated charging ports, to allow for high current battery charging in portable devices.

2.2 Driver Support

Royalty free D2XX Direct Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32, 64-bit
- Windows 8.1 32, 64-bit
- Windows 8 32, 64-bit
- Windows 7 32, 64-bit
- Server 2008 R2
- Server 2012 R2
- Linux
- MAC OSX
- Android

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com).

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

2.3 Ordering information

The following table gives details of the available UMFT4222EV.

Part Number	Description
UMFT4222EV-D	FT4222H evaluation module with D version chip.

Table 1 UMFT4222EV Descriptions & Part Numbers

3 FT4222H Features and Enhancement

Functional Integration: The FT4222H is a USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable SPI/I2C interfaces device. The FT4222H includes an integrated +1.8V and +3.3V Low Drop-Out (LDO) regulator and a 12MHz to 480MHz PLL. It also includes Power-On-Reset (POR), VBUS detection with 5V-tolerance and 128 bytes one-time-programmable (OTP) memory which simplifies external circuit design and reduces external component count.

USB2.0 Hi-Speed Device Controller: The FT4222H integrates a USB protocol engine which controls the physical Universal Transceiver Macro cell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. The device contains one control endpoint and 4 IN and OUT endpoint pairs. These endpoints can be configured to implement up to 4 independent interfaces/applications mapped to I2C+GPIO or SPI+GPIO.

Highly Integrated USB2.0 to Configurable SPI Bridge: The FT4222H provides the bridge function between a USB2.0 and SPI Master/Slave.

The support library, LibFT4222, based on FTDI's D2XX driver, enables easy configuration of the SPI as a master or slave. Operating clock frequency on the SPI bus, clock phase and polarity, transfer data bit width mode, and the number of slave selection controls are also configurable.

The max SPI interface operating clock can be set up to 30MHz in master mode and 20MHz in slave mode. With quad mode (4-bits) data bus width, the max data transfer throughput can be up to 28Mbps.

USB to Configurable I^2C Controller: The FT4222H also provides the bridge function between a USB2.0 and an I^2C Master/Slave.

The support library, LibFT4222, based on FTDI's D2XX driver, enables easy configuration of the I^2C as either a master or slave, including target operating speed and bus protocol on I^2C bus.

The device can run at common I2C bus speeds, 100kbit/s standard mode (SM), 400 Kbit/s fast mode (FM), 1 Mbit/s Fast mode plus (FM+), and 3.4 Mbit/s High Speed mode (HS). Clock stretching is also supported to conform to v2.1 and v3.0 of the I2C specification.

Configurable GPIOs: The GPIOs in the FT4222H can be fully controlled by an application utility over USB. There are 4 GPIO pins that can be configured for different purposes, such as a suspend indicator output, and remote wake up input.

The signal drive strength and slew rate can be configured via USB vendor commands for different design needs.

Embedded OTP memory: The internal OTP memory in the FT4222H is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. With this embedded OTP memory, the device can store vendor specific information and save BOM cost. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com).

Power management: Fully supports USB2.0 suspend/resume and remote wakeup. The PHY will be put to a power saving mode and the clock to most of the digital circuits will be stopped when the device is suspended.

Source Power and Power Consumption: The FT4222H is capable of operating at a voltage supply +3.3V or +5.0V with a nominal operational mode current of 68mA and a nominal USB suspend mode current of 375µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the FT4222H allows the interface logic to run at +1.8V, 2.5V or +3.3V. (Note: External pull-ups are recommended for IO <3V3).

4 UMFT4222EV Pin Out and Signal Descriptions

4.1 UMFT4222EV Pin Out

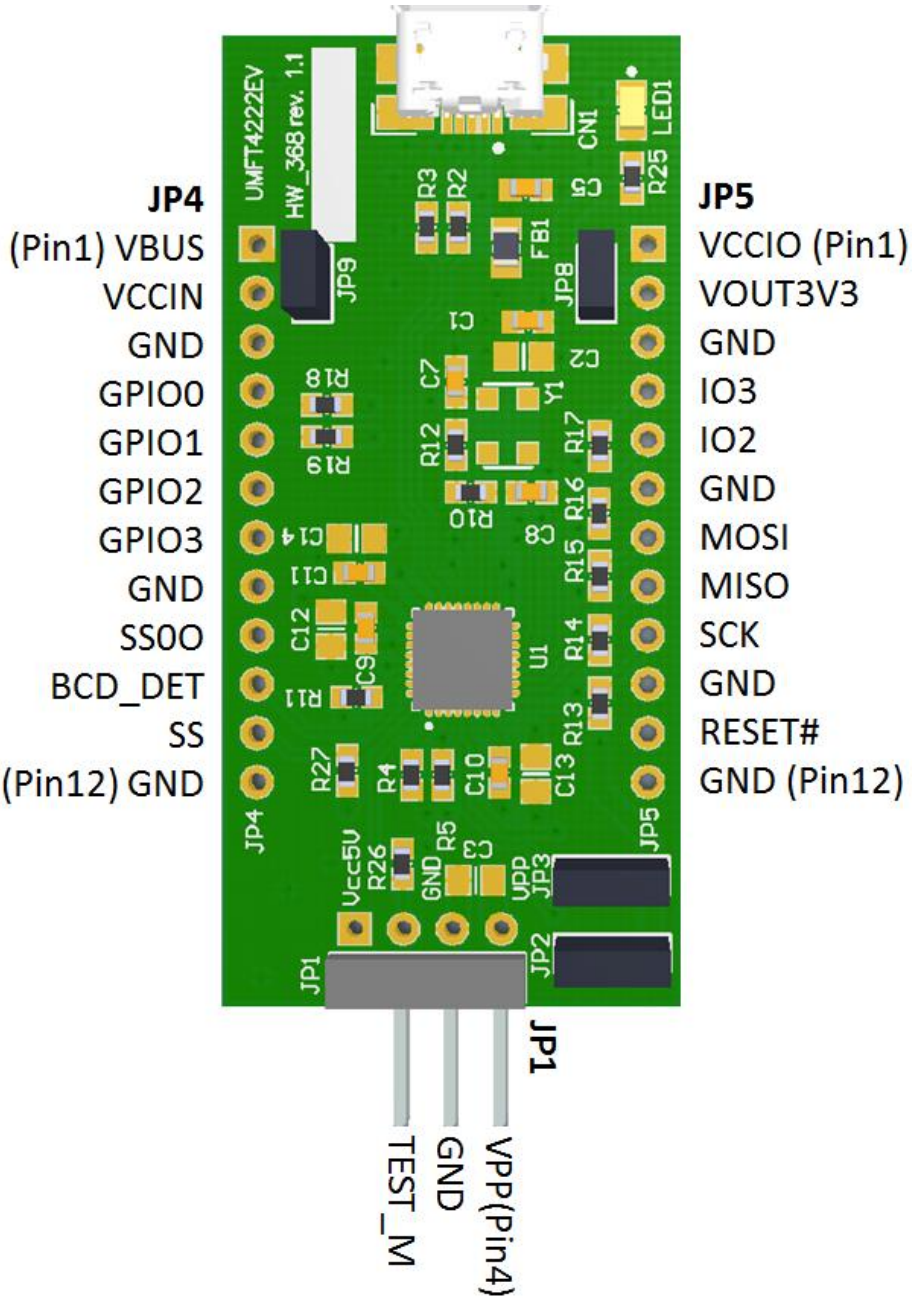

Figure 4-1 Module Pin Out and Jumper Locations

4.2 Signal Descriptions

Pin No.	Name	Type	Description
JP4. 1	VBUS	Output	5V Power output from USB Connector. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
JP4. 2	VCCIN	PWR	To power the module from the 5V supply on the USB bus, need to connect jumper JP9 pin 1 and pin 2 together (this is the module default configuration). In this case this pin would have the same description as JP4 pin 1. To use the UMFT4222EV module in a self-powered configuration ensure that jumper JP9 pins 1 and 2 are not connected together, and apply an external 3.3V or 4.0V to 5.25V supply to this pin (3.3V input for self-power low power configuration). This Pin is also connected to JP1 Pin 1.
JP4. 3	GND	PWR	Module Ground Supply Pins
JP4. 4	GPIO0	I/O	GPIO0(default) can be configured as slave selection 1, output pin for SPI master mode or serial clock for I^2C mode
JP4. 5	GPIO1	I/O	GPIO1(default) can be configured as slave selection 2, output pin for SPI master mode or serial data for I^2C mode
JP4. 6	GPIO2	I/O	GPIO2(default) can be configured as slave selection 3, output pin for SPI master mode or USB suspend output indicator
JP4. 7	GPIO3	I/O	GPIO3(default) can be configured as USB remote wakeup input pin or interrupt input
JP4. 8	GND	PWR	Module Ground Supply Pins
JP4. 9	SS0O	Output	Slave selection 0, output pin for SPI master mode.
JP4. 10	BCD_DET	Output	Battery charger detection asserted when the device is connected to a dedicated charging port. Polarity can be defined
JP4. 11	SS	Input	SPI slave selection indicator from SPI master. This pin is active in SPI slave mode. It must be tied to high when SPI master mode enabled.
JP4. 12	GND	PWR	Module Ground Supply Pins

Pin No.	Name	Type	Description
JP5. 1	VCCIO	PWR Input	+3.3V/2.5V/1.8V supply voltage for all the FT4222H I/O pins. For 3.3V application, this pin can use FT4222H VOUT3V3 power supply by connecting JP8 pins 1 and 2. This pin can also be supplied with an external 1.8V or 2.5V supply in order to drive out at lower levels.
JP5. 2	VOUT3V3	PWR Output or Input	3.3V output from integrated LDO regulator. This pin is decoupled from ground on the module. The prime purpose of this pin is to provide the internal 3.3V supply to USB transceiver cell. Up to 100mA can be drawn from this pin to power FT4222H and external logic if required. This pin can also be used to supply the FT4222H VCCIO pin by connecting JP8 pins 1 and 2. If VCCIN is supplied with 3.3V, this pin must also be driven with 3.3V power source.
JP5. 3	GND	PWR	Module Ground Supply Pins
JP5. 4	IO3	I/O	Quad SPI data bus bit 3
JP5. 5	IO2	I/O	Quad SPI data bus bit 2
JP5. 6	GND	PWR	Module Ground Supply Pins
JP5. 7	MOSI	I/O	In SPI master single mode, it is master serial data output. In SPI master dual/quad mode, it is SPI data bus bit 0. In SPI slave mode, it is slave serial data input.
JP5. 8	MISO	I/O	In SPI master single mode, it is master serial data input. In SPI master dual/quad mode, it is SPI data bus bit 1. In SPI slave mode, it is slave serial data output.
JP5. 9	SCK	I/O	SPI interface clock. In SPI master mode, it is Serial clock output. In SPI Slave mode, it is Serial clock input.
JP5. 10	GND	PWR	Module Ground Supply Pins
JP5. 11	Reset#	Input	Reset input for normal operation, active low.
JP5. 12	GND	PWR	Module Ground Supply Pins

Table 2 Module Pin out Description

Pin No.	Name	Type	Description
JP1. 1	-	-	Not connected.
JP1. 2	TEST_M	Input	Test Pin, leave floating.
JP1. 3	GND	PWR	Module Ground Supply Pins
JP1. 4	VPP	PWR Input	It is a power source for Programming FT4222H embedded OTP with 6.5V voltage. Leave floating or 0V when not in programming mode.

Table 3 Module JP1 Pin out Description

4.3 Jumper Configuration Options

Pin No.	Name	Type	Description
1	VCCIO	PWR	Set DCNF0 mode configuration bit High.
2	DCNF0	Input	USB endpoint configuration selection bit 0. Refer to FT4222H datasheet.
3	GND	PWR	Set DCNF0 mode configuration bit Low.

Table 4 Jumper JP2 Pin Description

Pin No.	Name	Type	Description
1	VCCIO	PWR	Set DCNF1 mode configuration bit High.
2	DCNF1	Input	USB endpoint configuration selection bit 1. Refer to FT4222H datasheet.
3	GND	PWR	Set DCNF1 mode configuration bit Low.

Table 5 Jumper JP3 Pin Description

Pin No.	Name	Type	Description
1	VCCIO	PWR Input	Connect to jumper JP8 pin 2 in order to supply the board from the USB FT4222H. Otherwise, VCCIO should have external power supply on JP5 pin 1.
2	VOUT3V3	PWR Output	FT4222H 3.3V regulator output. Connect to jumper JP8 pin 1 in order to supply the IO voltage with 3.3V tolerance.

Table 6 Jumper JP8 Pin Description

Pin No.	Name	Type	Description
1	VBUS	PWR	Connect to jumper JP9 pin 2 in order to supply power for FT4222H from the USB port.
2	VCCIN	PWR Input	FT4222H 5V power input, connect to jumper JP9 pin 1 to supply power from the USB port. Otherwise, VCCIN should have external 3.3V/5V power supply on JP4 pin 2.

Table 7 Jumper JP9 Pin Description

5 UMFT4222EV Mode Configuration

5.1 Mode Configuration

The FT4222H has 4 configuration modes selected by {DCNF1, DCNF0}. The chip configuration mode will determine the number of USB interfaces for data streams and for GPIOs control. The data stream interface is for data transfer between the USB2.0 host and the SPI/ I2C device. The purpose of the GPIO interface is for fully controlling the GPIOs.

With UMFT4222EV module, user can easily configure chip mode through jumpers (JP2 and JP3). Please refer to Table 4 and 5 for details. A chip reset or power cycling is required after configuration changing. The following table shows the pin functions corresponding to chip configuration mode.

Pin Functions	CNFMODE0 {DCNF1, DCNF0} = 00	CNFMODE1 {DCNF1, DCNF0} = 01	CNFMOD2 {DCNF1, DCNF0} = 10	CNFMODE3 {DCNF1, DCNF0} = 11
USB interface number	1 for data stream 1 for GPIOs	3 for data stream 1 for GPIOs	4 for data stream	1 for data stream
SPI Master(SPIM) related pins (SCK, MISO, SIMO, IO2,IO3, SS0O)	SPIM*	Active USB interface-0	Active USB interface-0	SPIM*
SPI Slave(SPIS) related pins (SCK, MISO, SIMO, SS)	SPIS*	Disable	Disable	SPIS*
GPIO0	GPIO/SCL*	SS1O USB interface-1	SS1O USB interface-1	SCL*
GPIO1	GPIO/SDA*	SS2O USB interface-2	SS2O USB interface-2	SDA*
GPIO2	GPIO/SUSP	GPIO/SUSP	SS3O USB interface-3	SUSP
GPIO3	GPIO/WAKE/INTR	GPIO/WAKE/INTR	WAKE	WAKE

Table 8 FT4222H Pin Functions on Chip Configuration Mode

*One of the SPIM, SPIS, I^2C function is selected, the other 2 functions will be disable

Note: GPIO pins can't be controlled by driver when GPIO pins play the role as SPIM SSxO, I^2C SCL/SDA, SUSP or WAKE.

Chip Configuration only determines the number of interface/function supported but do not decide which bus interface (SPI/ I^2C /GPIO) or which role (master/slave) that the FT4222H will take.

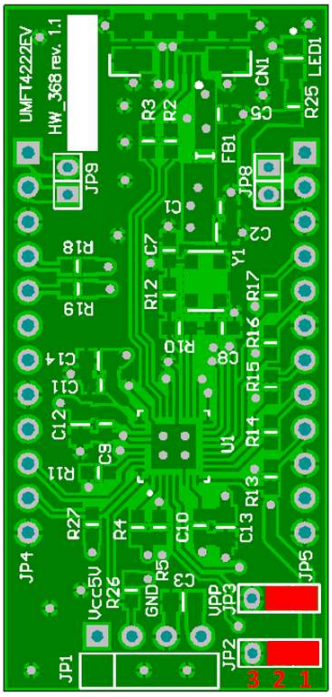

Figure 5-1 JP2/JP3 configuration example: Mode 3 (DCNF0 = 1, DCNF1 = 1)

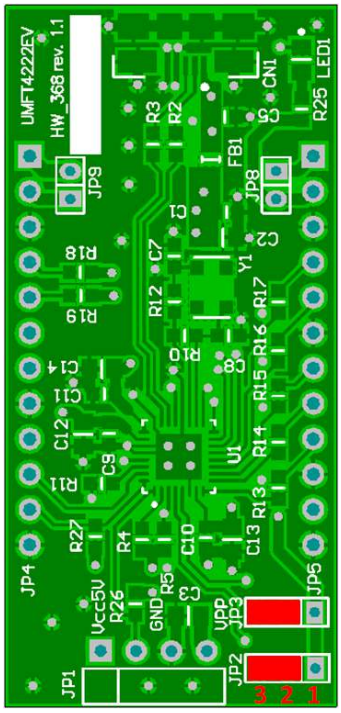

Figure 5-2 JP2/JP3 configuration example: Mode 0 (DCNF0 = 0, DCNF1 = 0)

5.2 SPI Pin Definition

The QuadSPI function in the FT4222H is a fully configurable SPI master/slave device. Users can utilize the API in LibFT4222, FT4222_SPIMaster_Init or FT4222_SPISlave_Init, to select in which mode (master or slave) the FT4222H will function. When the FT4222H is set as a USB-to-SPI bridge function, and chip configuration mode is chosen, the pins of the FT4222H will be mapped accordingly. The SPI related pins are -

- Clock – SCK JP5 pin 9. Clock output in SPI master mode.

  It will become clock input in SPI slave mode.
- Data – MISO JP5 pin 8. Data transfer from slave to master for single mode.

  It can also become data bus bit-1 for dual and quad mode.

  – MOSI JP5 pin 7. Data transfer from master to slave for single mode.

  It can also become data bus bit-0 for dual and quad mode.

  – IO2 JP5 pin 5. Data bus bit-2 for quad mode

  – IO3 JP5 pin 4. Data bus bit-3 for quad mode
- Slave Selection when QuadSPI acts as SPI master

  – SS0O JP4 pin 9. Slave selection to slave device-0.

  – SS1O JP4 pin 4. Slave selection to slave device-1.

  – SS2O JP4 pin 5. Slave selection to slave device-2.

  – SS3O JP4 pin 6. Slave selection to slave device-3.
- Slave Selection when QuadSPI acts as SPI slave

  – SS JP4 pin 11. Slave selection for SPI master control.

  This pin must tie to high when QuadSPI acts as SPI master.

5.3 I²C Pin Definition

The I²C function in the FT4222H is a fully configurable I2C master/slave device. When the chip configuration is set as CNFMODE0 or CNFMODE3 and USB-to- I²C bridge function is enabled, the I²C related pins of the FT4222H are:

- Clock – SCL JP4 pin 4. It is a clock output with open-drain design when the I²C is set as master. It is a clock input when the I²C is set as a slave.
- Data – SDA JP4 pin 5. It is command/address/data transfer between master and slave with open-drain design.

5.4 GPIO Pin Definition

The FT4222H contains 4 GPIO pins for various functions. The driving strength, slew rate control and pull high/low resistors can be controlled.

- GPIO0 JP4 pin 4. This pin can be configured as GPIO0 or I²C SCL in I²C mode or SPI master mode slave selection SS1O.
- GPIO1 JP4 pin 5. This pin can be configured as GPIO1 or I²C SDA in I²C mode or SPI master mode slave selection SS2O.
- GPIO2 JP4 pin 6. This pin can be configured as GPIO2 or USB suspend status output (SUSP) or SPI master mode slave selection SS3O.
- GPIO3 JP4 pin 7. This pin can be configured as GPIO3 or USB remote wake-up input (WAKE).

5.5 Other Pin Definitions

UMFT4222EV contains BCD_DET and RESET# signals for user use.

- BCD_DET JP4 pin 10. Battery charger detection asserted when the device is connected to a dedicated charging port. The polarity of this pin can be defined.
- RESET# JP5 pin 11. This pin used to reset the FT4222H, it is active low.

6 Module Dimensions

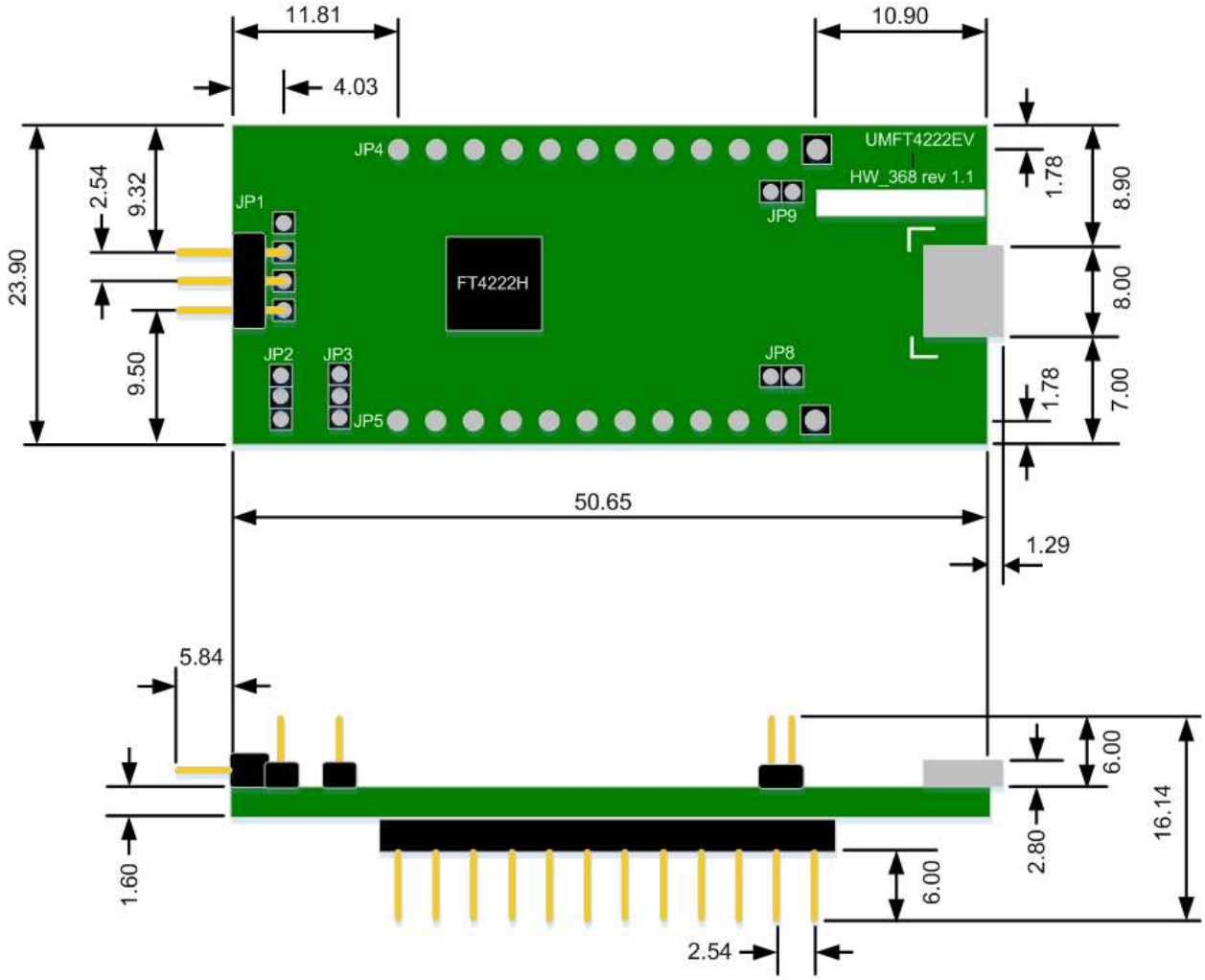

Figure 6-1 UMFT4222EV Module Dimensions

All dimensions are in millimetres. Tolerance is +/-0.2mm.

7 Power Configurations

7.1 BUS Powered Configuration

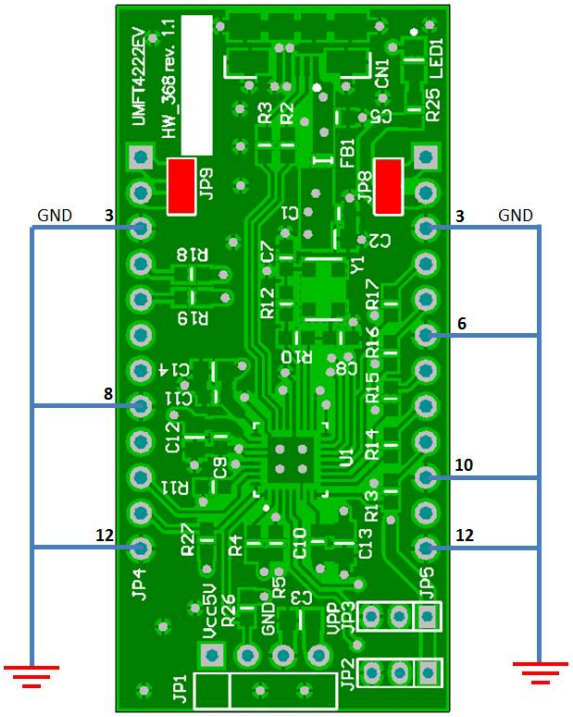

Figure 7-1 Bus Powered Configuration: Short JP9

Figure 6.1 illustrates the UMFT4222EV module in a typical USB bus powered design configuration. This is done by fitting the jumpers on JP8 and JP9, as shown above. The UMFT4222EV is supplied in this configuration by default.

A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus Power devices are as follows:

i) On plug-in to USB, the device must draw no more than 100mA.

ii) On USB suspend the device must draw no more than 2500µA.

iii) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.

iv) No device can draw more that 500mA from the USB Bus.

Interfacing the UMFT4222EV module to a SPI Flash, microcontroller (MCU), or other logic for a bus powered design would be done in exactly the same way as for a self-powered design, except that the MCU or external logic would take its power supply from the USB bus (either the 5V on the USB pin, or 3.3V on the VCCIO pin).

7.2 Self Powered Configuration

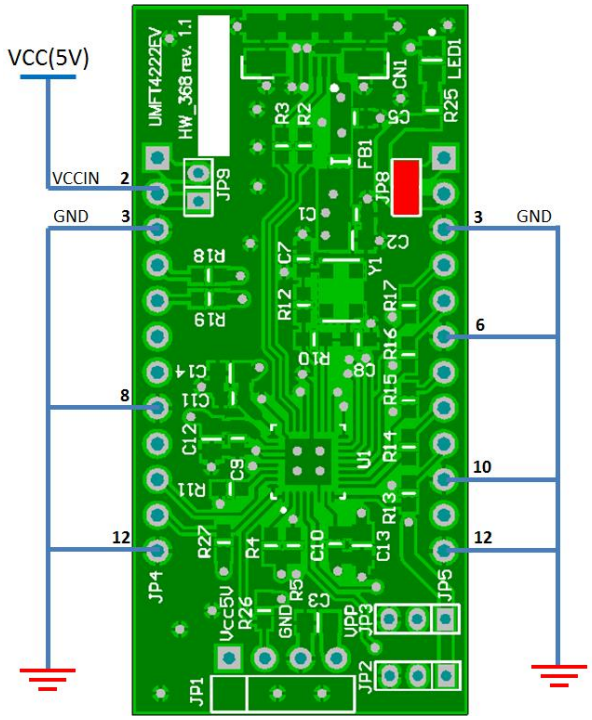

Figure 7-2 Self-Powered Configuration: Remove Jumper on JP9

Figure 6.2 illustrates the UMFT4222EV in a typical USB self-powered configuration. In this case the jumper on JP9 is removed, and an external supply is connected to the module JP4 pin 2 (VCCIN).

A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self powered devices are as follows:

i. A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller bus powered down.

ii. A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.

iii. A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hub. In this case the power descriptor in the internal EEPROM should be programmed to a value of zero (self-powered).

In order to meet above rule (i), the USB Bus Power is connected to the VBUS_DET Pin which is a 5V tolerance input pin even when FT4222H works at low power mode and VCCIN is supply with 3.3V. When USB Bus Power is down, VBUS_DET will be 0V and FT4222H will enter suspend mode.

7.3 Using internal regulator of FT4222H

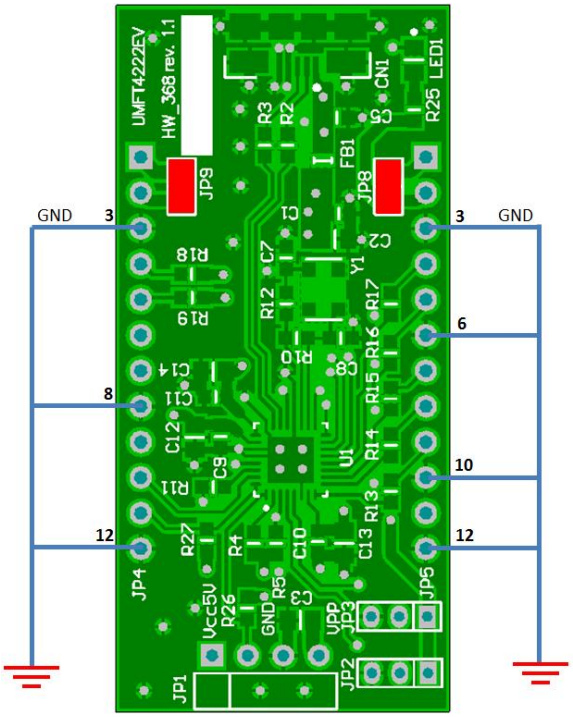

Figure 7-3 Use FT4222H internal regulator: Short JP8

Figure 6.3 shows a configuration for USB bus powered and using internal regulator of FT4222H

The Jumper JP8 allows the FT4222H to use the internal regulator in FT4222H.

The FT4222H VCCIO pin is supplied from FT4222H internal 3.3V regulator output pin(VOUT3V3) when it connects JP8 pins 1 and 2 with jumper.

FT4222H can provide VOUT3V3 up to 100mA which includes the power consumption of the FT4222H. It can also be used to supply external logic, but the total power consumption of FT4222H and external logic should not exceed 100mA.

7.4 Using external power source for FT4222H IO Supply Voltage

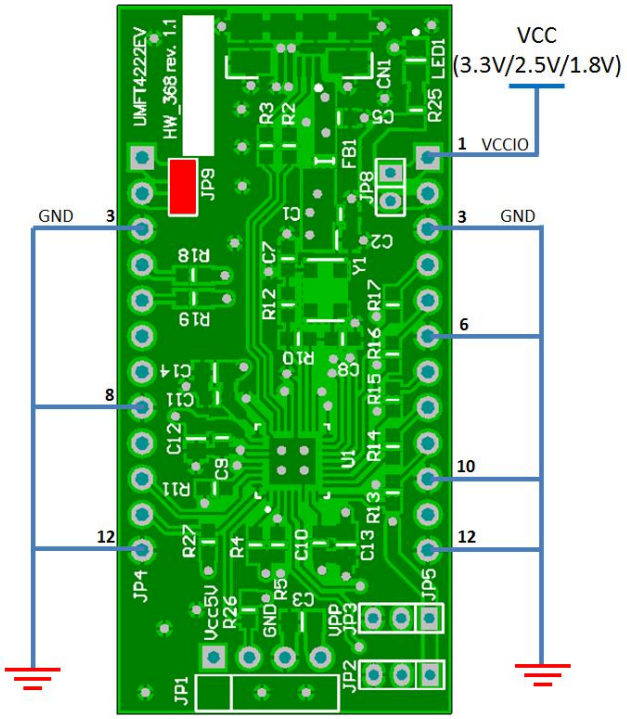

Figure 7-4 Use external power source for FT4222H IO Supply Voltage: Remove Jumper on JP8

Figure 6.4 shows a configuration for using an external power source for the FT4222H IO supply voltage.

When removing the jumper JP8 on UMFT4222EV module, the FT4222H can use an external power source to FT4222H VCCIO pin through JP5 pin 1.

FT4222H VCCIO pin can accept 3.3V/2.5V/1.8V supply voltage for all the FT4222H I/O pins include SPI interface. User can implement an external regulator to generate 3.3V from the USB Bus Power.

User can use a discrete low dropout regulator supplied by the USB Bus power to generate 3.3V or 1.8V output for UMFT4222EV JP5 Pin 1(VCCIO) and the external logic. UMFT4222EV also provide JP4 Pin 1(VBUS) to supply 5V source for external regulator. With the external regulator connected, UMFT4222EV I/O pins will drive out 3.3V or 1.8V logic levels.

The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 2500 µA during USB suspend.

8 UMFT4222EV Module Circuit Schematic

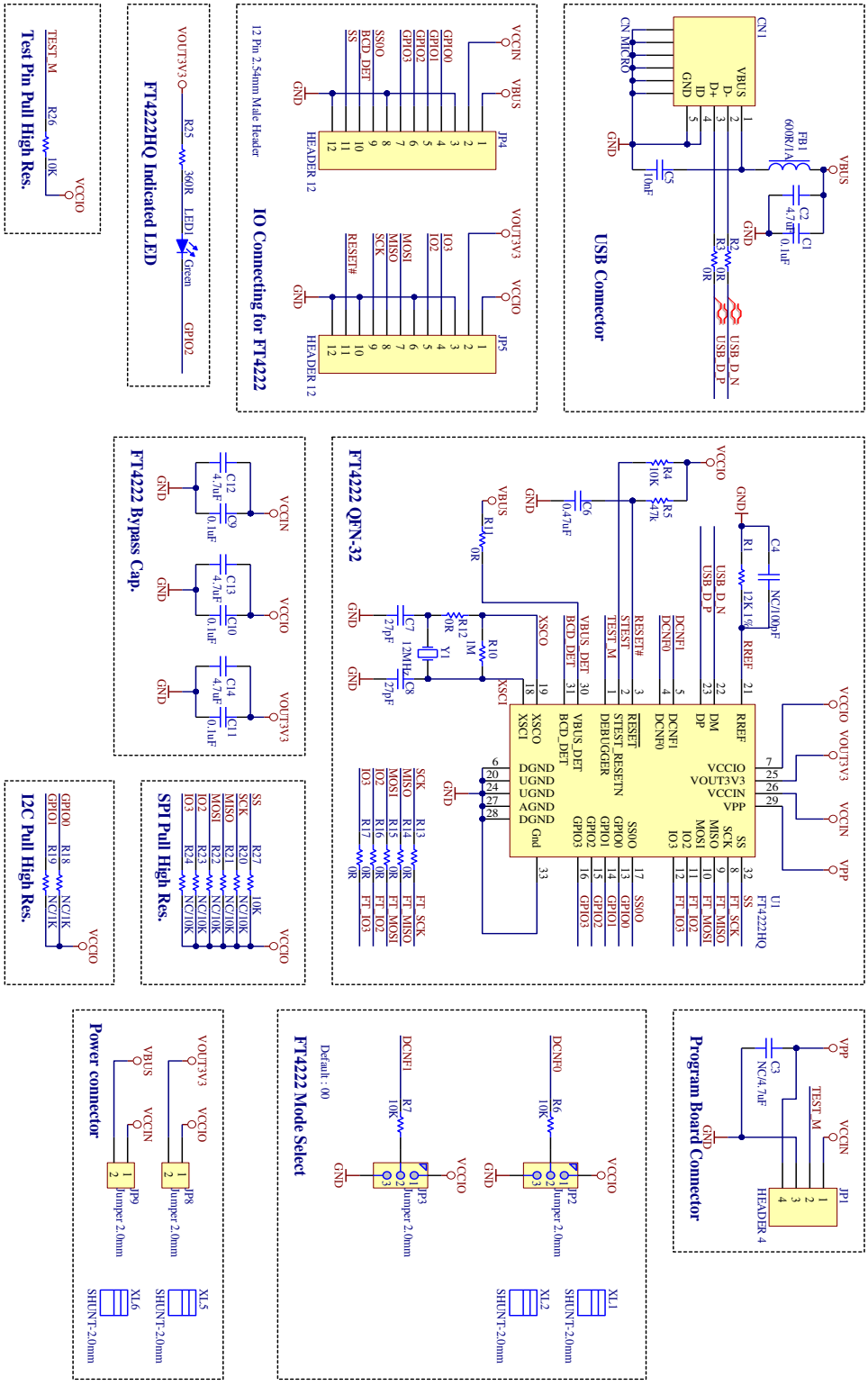

Figure 8-1 Module Circuit Schematic

9 Internal OTP Memory Configuration

The FT4222H includes an internal OTP memory which holds the USB configuration descriptors, other configuration data for the chip and also user data areas. Following a power-on reset or a USB reset the FT4222H will scan its internal OTP memory and read the USB configuration descriptors stored there.

In many cases, the default values in OTP memory are suitable and no necessary to do re-programming. The defaults can be found in the FT4222H datasheet.

The OTP memory in the FT4222H can be programmed over USB if the values need to be changed for a particular application. Further details of this are provided from Section 9.1 onwards.

Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. See TN_100 – USB Vendor ID/Product ID Guidelines for more details.

9.1 Method of Programming the OTP Memory

The OTP memory on a FT4222H device can be programmed over USB.

For the UMFT4222EV module, another module, named UMFT4222PROG, is required for programming the FT4222H. In order to program the OTP memory, the FT4222H requires an additional programming voltage (6.5V) on its VPP pin from JP1 pin 4. The UMFT4222PROG will generate the 6.5V.

Refer to the datasheet UMFT4222PROG module for details.

10 Contact Information

Head Office – Glasgow, UK

Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Taipei, Taiwan

2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Shanghai, China

Room 1103, No. 666 West Huaihai Road,
Changning District
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

FT4222H Datasheet

UMFT4222PROG Datasheet

Windows/Linux/Mac/Android library and examples:

http://www.ftdichip.com/Products/ICs/FT4222H.html

Acronyms and Abbreviations

Terms	Description
API	Application Programming Interface
DIP	Dual in-line Package
EHCI	Enhanced Host Controller Interface
EEPROM	Electrically Erasable Programmable Read-Only Memory
I2C	Inter-Integrated Circuit
LDO	Low Drop Out
MCU	Micro Controller Unit
OTP	One Time Programmable
OHCI	Open Host Controller Interface
PCB	Printed Circuit Board
PID	Product ID
PLL	Phase Locked Loop
POR	Power On Reset
QFN	Quad Flat No-Lead
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UHCI	Universal Host Controller Interface

VID	Vendor ID
XHCI	eXtensible Host Controller Interface

Appendix B – List of Tables and Figures

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Appendix C – Revision History

Document Title: UMFT4222EV - USB2.0 to QuadSPI/I2C Bridge Development Module Datasheet

Document Ref. No.: FT_001057

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Product Page: http://www.ftdichip.com/FTProducts.htm

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Revision	Changes	Date
Version 1.0	Initial Release	2014-09-26
Version 1.1	Updated Ordering Information & Contact Details	2016-06-06
Version 1.2	Updated Ordering Information	2016-10-17
Version 1.3	Updated Schematic in Section 8	2016-11-08
Version 1.4	Updated Ordering information for Rev D	2018-04-02