GAL®26V12 Device Datasheet

September 2010

All Devices Discontinued!

Product Change Notifications (PCNs) have been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
GAL26V12	GAL26V12C-10LP	Discontinued	PCN#06-07
	GAL26V12C-15LP		
	GAL26V12C-20LP		
	GAL26V12C-10LPI		
	GAL26V12C-15LPI		
	GAL26V12C-20LPI		
	GAL26V12C-7LJ		PCN#13-10
	GAL26V12C-10LJ		
	GAL26V12C-15LJ		
	GAL26V12C-20LJ		
	GAL26V12C-10LJI		
	GAL26V12C-15LJI		
	GAL26V12C-20LJI		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

GAL26V12

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **7.5 ns Maximum Propagation Delay**
  - **Fmax = 142.8 MHz**
  - **4.5 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 16 mA Outputs**
  - **UltraMOS® Advanced CMOS Technology**
- **LOW POWER CMOS**
  - **90 mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<100ms)**
  - **20 Year Data Retention**
- **TWELVE OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **DMA Control**
  - **State Machine Control**
  - **High Speed Graphics Processing**
  - **Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

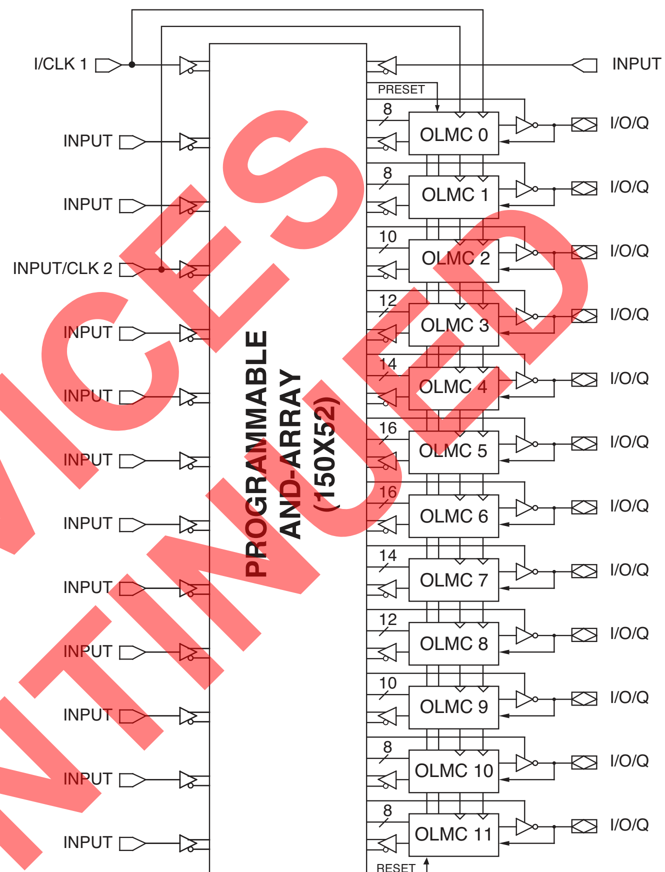
DESCRIPTION

The GAL26V12, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 26V12 device on the market. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26V12 is fully function/fuse map/parametric compatible with other 26V12 devices.

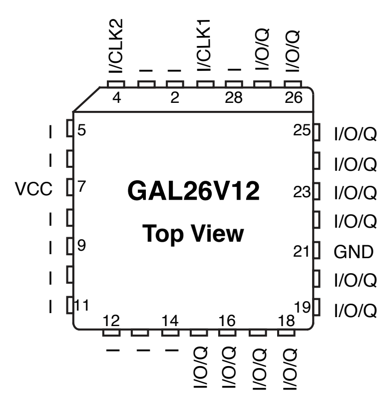
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles.

FUNCTIONAL BLOCK DIAGRAM

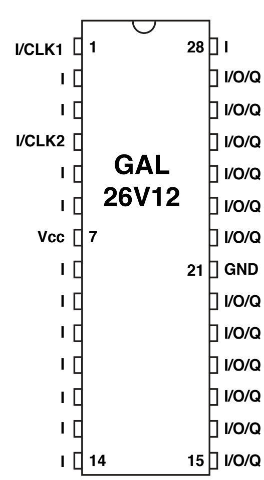


PACKAGE DIAGRAMS

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 268-8000 or 1-800-LATTICE; FAX (503) 268-8556

November 2000

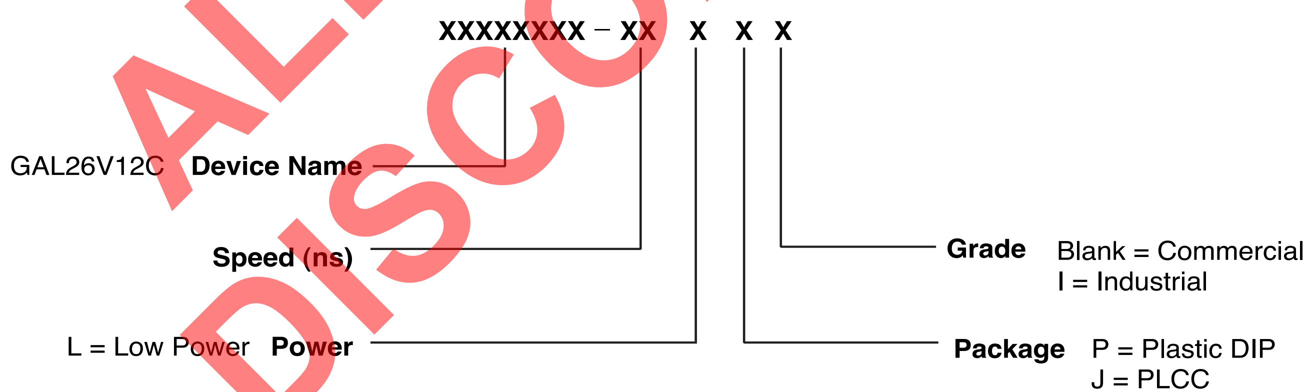
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6	4.5	130	GAL26V12C-7LJ	28-Lead PLCC
10	7	7	130	GAL26V12C-10LP[1]	28-Pin Plastic DIP
			130	GAL26V12C-10LJ	28-Lead PLCC
15	10	8	105	GAL26V12C-15LP[1]	28-Pin Plastic DIP
			105	GAL26V12C-15LJ	28-Lead PLCC
20	12	12	105	GAL26V12C-20LP[1]	28-Pin Plastic DIP
			105	GAL26V12C-20LJ	28-Lead PLCC

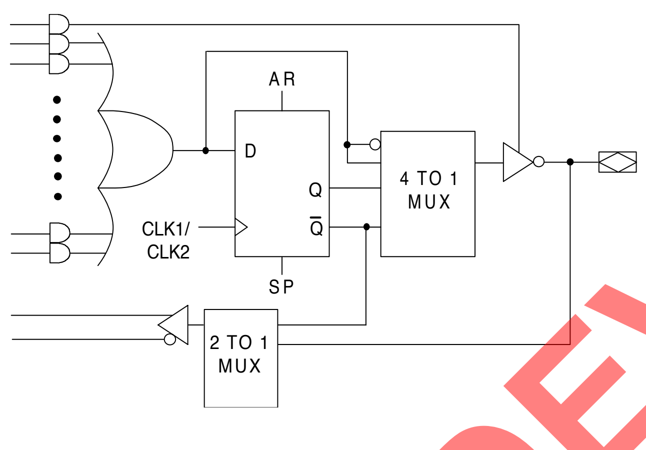
Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	150	GAL26V12C-10LPI[1]	28-Pin Plastic DIP
			150	GAL26V12C-10LJI	28-Lead PLCC
15	10	8	150	GAL26V12C-15LPI[1]	28-Pin Plastic DIP
			150	GAL26V12C-15LJI	28-Lead PLCC
20	12	12	150	GAL26V12C-20LPI[1]	28-Pin Plastic DIP
			150	GAL26V12C-20LJI	28-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.



The GAL26V12 has a variable number of product terms per OLMC. Of the ten available OLMCs, four OLMCs have access to eight product terms (pins 15, 16, 26 and 27), two have ten product terms (pins 17 and 25), two have twelve product terms (pins 18 and 24), two have fourteen product terms (pins 19 and 23), and two OLMCs have sixteen product terms (pins 20 and 22). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.



GAL26V12 OUTPUT LOGIC MACROCELL (OLMC)

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

In the registered mode configuration the clock source for the register can be selected. The two clock options, CLK1 and CLK2, originate from input pin1 and pin4 respectively.

The GAL26V12 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.

Each of the Macrocells of the GAL26V12 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by four architecture bits (S0, S1, S2 and S3), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED MODE

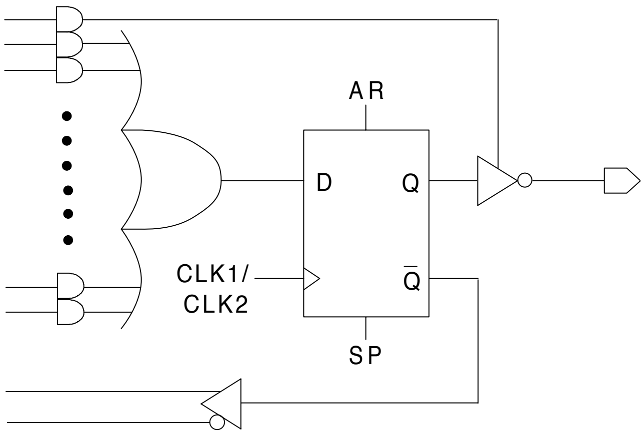
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation.

There are two options for the feedback of the registered mode - - internal /Q feedback and I/O pin feedback. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array. Similarly the I/O pin feedback with both true and complement input to the AND array. The resulting polarity depends on the input polarity selection as well as the registered I/O output polarity configuration.

COMBINATORIAL MODE

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O).

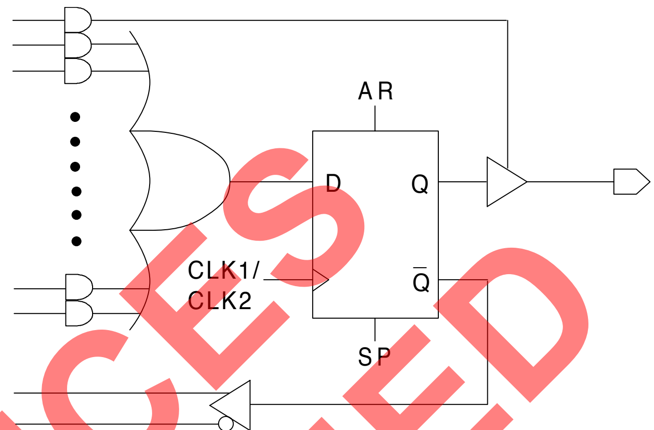
In combinatorial mode there are also two options for the feedback. The first feedback option into the AND array is from the I/O pin side of the output buffer. Both polarities (true and inverted) of the pin are fed back into the AND array. The second option is to drive the feedback from /Q of the buried register. This option provides the combinatorial output with the ability to register the feedback of the same combinatorial output.



ACTIVE LOW REGISTERED OUTPUT WITH BURIED FEEDBACK

S0 = 0
S1 = 0
S3 = 1

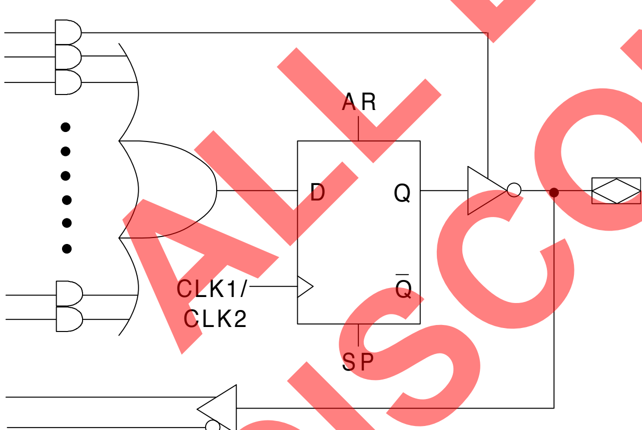
S2 = 1 Selects CLK1
S2 = 0 Selects CLK2



ACTIVE HIGH REGISTERED OUTPUT WITH BURIED FEEDBACK

S0 = 1
S1 = 0
S3 = 1

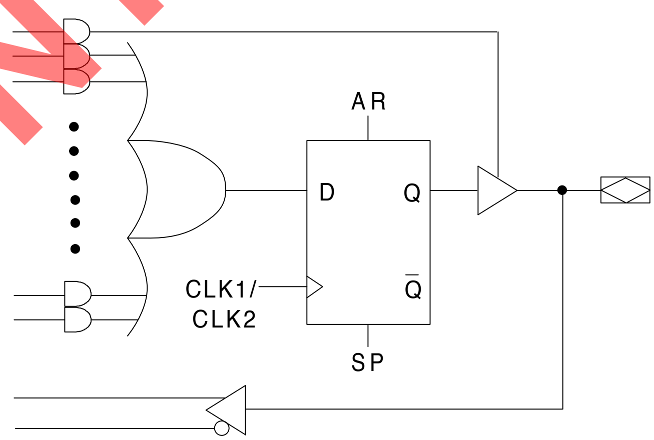
S2 = 1 Selects CLK1
S2 = 0 Selects CLK2



ACTIVE LOW REGISTERED OUTPUT WITH I/O FEEDBACK

S0 = 0
S1 = 0
S3 = 0

S2 = 1 Selects CLK1
S2 = 0 Selects CLK2

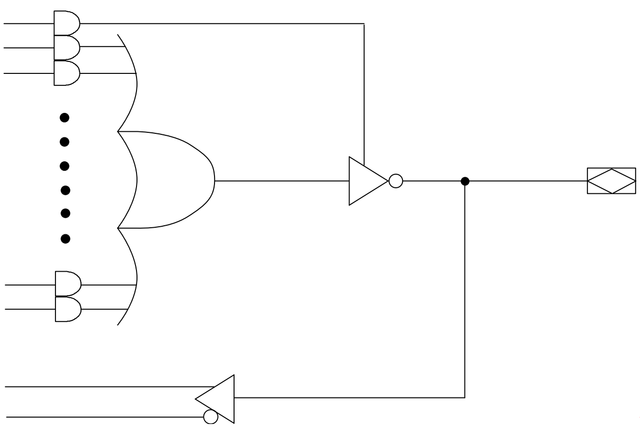


ACTIVE HIGH REGISTERED OUTPUT WITH I/O FEEDBACK

S0 = 1
S1 = 0
S3 = 0

S2 = 1 Selects CLK1
S2 = 0 Selects CLK2

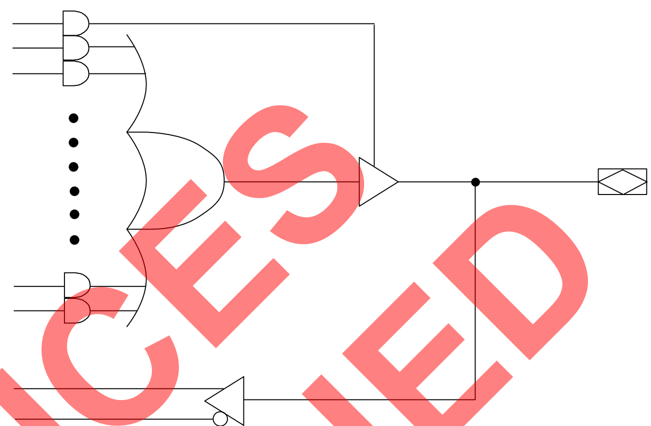
COMBINATORIAL MODE



ACTIVE LOW COMBINATORIAL OUTPUT
WITH I/O FEEDBACK

S0 = 0
S1 = 1
S3 = 1

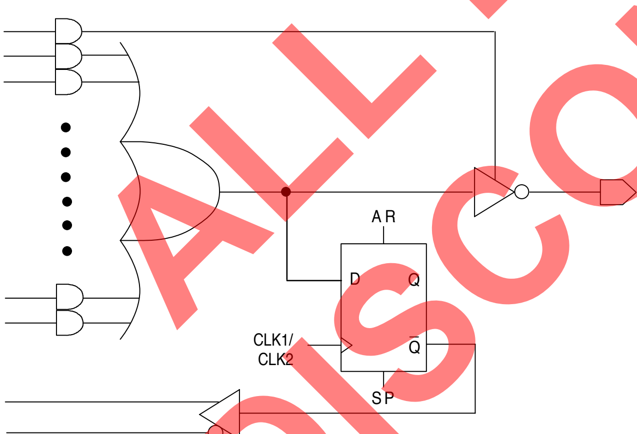
S2 = 1 Selects CLK1
S2 = 0 Selects CLK2



ACTIVE HIGH COMBINATORIAL OUTPUT
WITH I/O FEEDBACK

S0 = 1
S1 = 1
S3 = 1

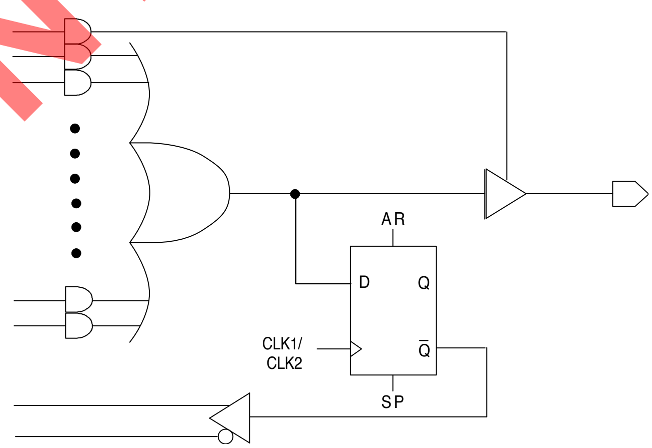
S2 = 1 Selects CLK1
S2 = 0 Selects CLK2



ACTIVE LOW COMBINATORIAL OUTPUT
WITH BURIED REGISTER FEEDBACK

S0 = 0
S1 = 1
S3 = 0

S2 = 1 Selects CLK1
S2 = 0 Selects CLK2

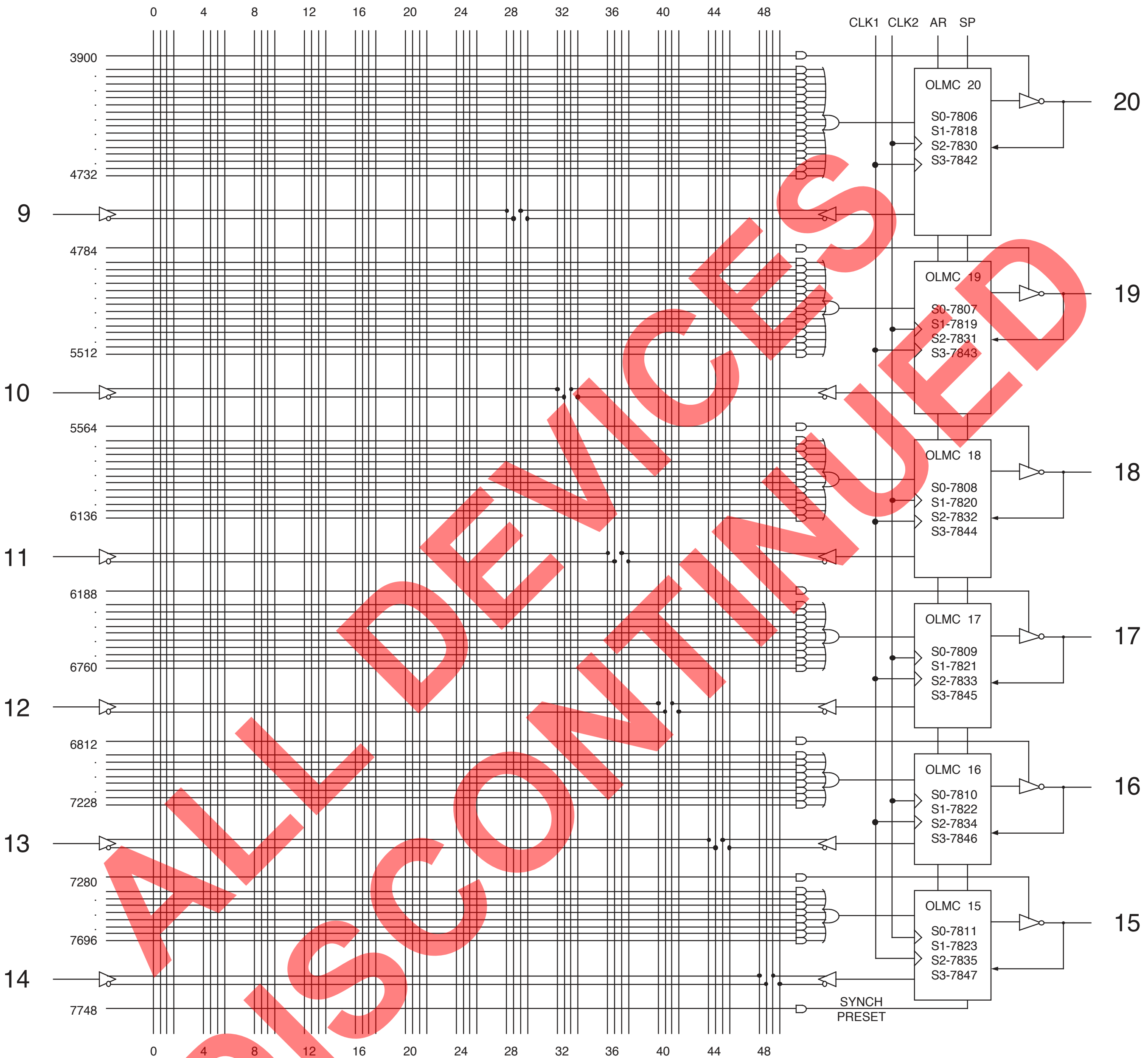


ACTIVE HIGH COMBINATORIAL OUTPUT
WITH BURIED REGISTER FEEDBACK

S0 = 1
S1 = 1
S3 = 0

S2 = 1 Selects CLK1
S2 = 0 Selects CLK2

1
2
3
4
5
6
7
VCC
8
0 4 8 12 16 20 24 28 32 36 40 44 48
0000
0052
0468
0520
0936
0988
1508
1560
2184
2236
2964
3016
3848
ASYNCH
RESET
OLMC 27
S0-7800
S1-7812
S2-7824
S3-7836
OLMC 26
S0-7801
S1-7813
S2-7825
S3-7837
OLMC 25
S0-7802
S1-7814
S2-7826
S3-7838
OLMC 24
S0-7803
S1-7815
S2-7827
S3-7839
OLMC 23
S0-7804
S1-7816
S2-7828
S3-7840
OLMC 22
S0-7805
S1-7817
S2-7829
S3-7841
28
27
26
25
24
23
22
21
CLK1 CLK2 AR SP



B0	B1	L S B	M S B	B3	B4	B5	B6	B7
7848	7849...			Electronic Signature			...7910	7911

[redacted]

Supply voltage V_{CC} .... -0.5 to +7V

Input voltage applied .... -2.5 to V_{CC} +1.0V
Off-state output voltage applied........... -2.5 to V_{CC} +1.0V
Storage Temperature................................. -65 to 150°C
Ambient Temperature with
Power Applied .... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

[redacted]

Commercial Devices:
Ambient Temperature (T_A) .... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground .... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) .... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground .... +4.5 to +5.5V

[redacted]

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[4]	MAX.	UNITS
VIL	Input Low Voltage		Vss – 0.5	—	0.8	V
VIH	Input High Voltage		2.0	—	Vcc+1	V
IIL[1]	Input or I/O Low Leakage Current	0V ≤ VIN ≤ VIL (MAX.)	—	—	–10	µA
IIH	Input or I/O High Leakage Current	3.5V ≤ VIN ≤ VCC	—	—	10	µA
VOL	Output Low Voltage	IOL = MAX. Vin = VIL or VIH	—	—	0.5	V
VOH	Output High Voltage	IOH = MAX. Vin = VIL or VIH	2.4	—	—	V
IOL	Low Level Output Current		—	—	16	mA
IOH	High Level Output Current		—	—	–3.2	mA
IOS[2]	Output Short Circuit Current	VCC = 5V VOUT = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

ICC[3]	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	-7/-10	—	90	130	mA
			-15/-20	—	75	105	mA

INDUSTRIAL

ICC[3]	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	-10/-15/-20	—	110	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Icc specified for a ten-bit binary counter pattern.
4) Typical values are at Vcc = 5V and T_A = 25 °C

Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	-7 MIN.	-7 MAX.	-10 MIN.	-10 MAX.	-15 MIN.	-15 MAX.	-20 MIN.	-20 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	—	7.5	—	10	—	15	—	20	ns
tco	A	Clock to Output Delay	—	4.5	—	7	—	8	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	2	—	2.5	—	2.5	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	6	—	7	—	10	—	12	—	ns
tsu2	—	Synch. Preset before Clk↑	5.5	—	6.5	—	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	95.2	—	71.4	—	55.5	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	125.0	—	105.2	—	80.0	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	142.8	—	125	—	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	3.5	—	4	—	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	3.5	—	4	—	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	7.5	—	10	—	15	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	7.5	—	10	—	15	—	20	ns
tar	A	Input or I/O to Asynch. Reset of Register	—	9	—	13	—	20	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	6	—	8	—	10	—	15	—	ns
tarr	—	Asynch. Reset to Clock Recovery Time	5	—	8	—	10	—	15	—	ns
tspr	—	Synch. Preset to Clock Recovery Time	5	—	8	—	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

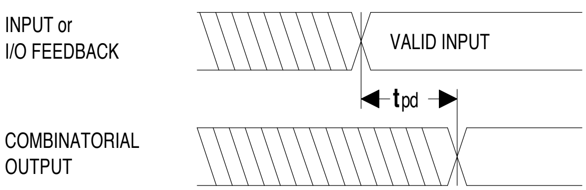
Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	-10		-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	—	10	—	15	—	20	ns
tco	A	Clock to Output Delay	—	7	—	8	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	7	—	10	—	12	—	ns
tsu2	—	Synch. Preset before Clk↑	6.5	—	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	71.4	—	55.5	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	105.2	—	80.0	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	125.0	—	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	4	—	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	10	—	15	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	10	—	15	—	20	ns
tar	A	Input or I/O to Asynch. Reset of Register	—	13	—	20	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	8	—	10	—	15	—	ns
tarr	—	Asynch. Reset to Clock Recovery Time	8	—	10	—	15	—	ns
tspr	—	Synch. Preset to Clock Recovery Time	8	—	10	—	12	—	ns

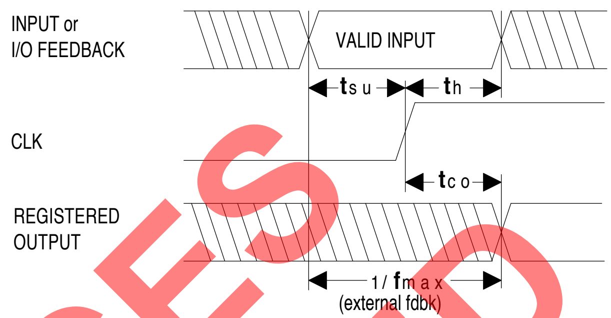
1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V$, $V_I = 2.0V$
$C_{I/O}$	I/O Capacitance	8	pF	$V_{CC} = 5.0V$, $V_{I/O} = 2.0V$

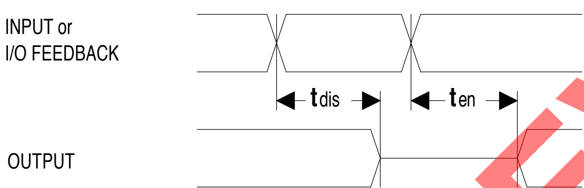
*Guaranteed but not 100% tested.



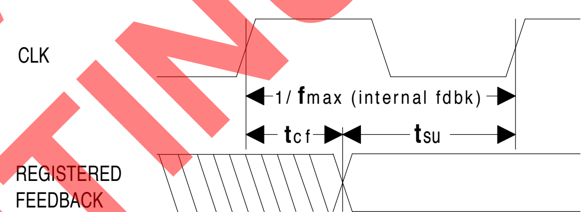
Combinatorial Output



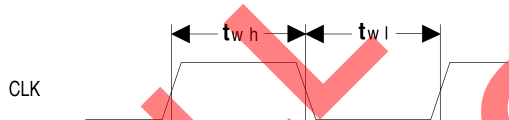
Registered Output



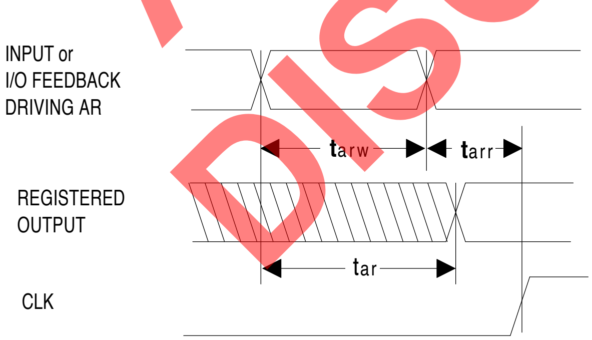
Input or I/O to Output Enable/Disable



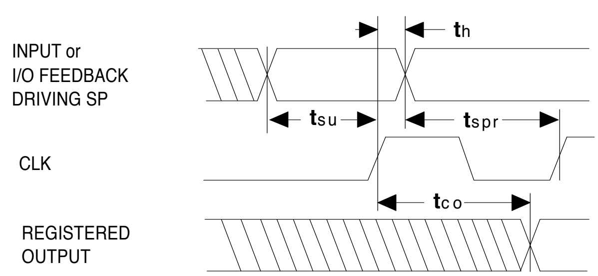
fmax with Feedback



Clock Width

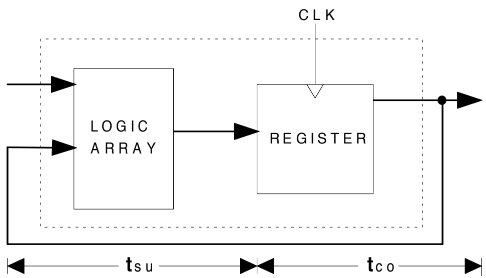


Asynchronous Reset



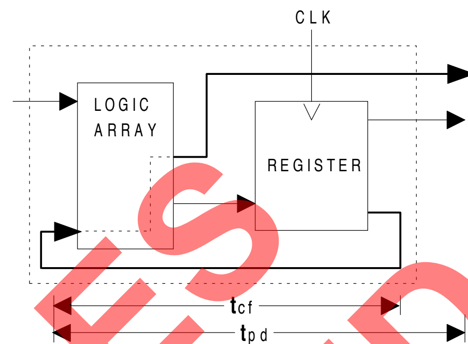
Synchronous Preset

fmax DESCRIPTIONS



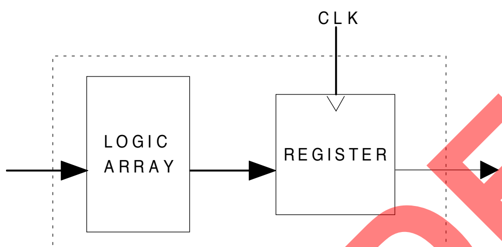
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.



fmax With No Feedback

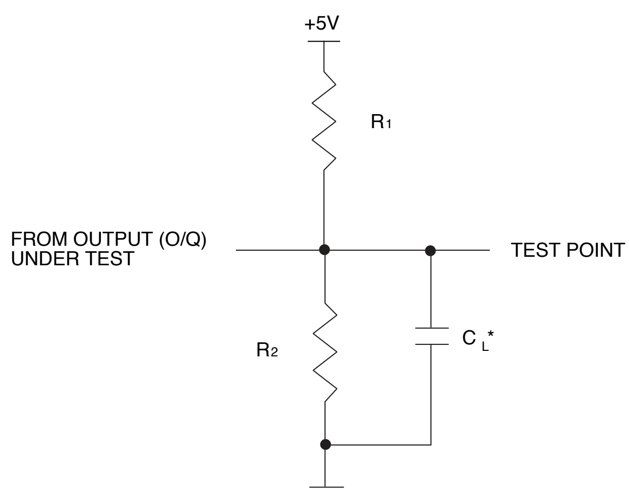
Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

An electronic signature is provided in every GAL26V12 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

A security cell is provided in every GAL26V12 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

GAL26V12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential for latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

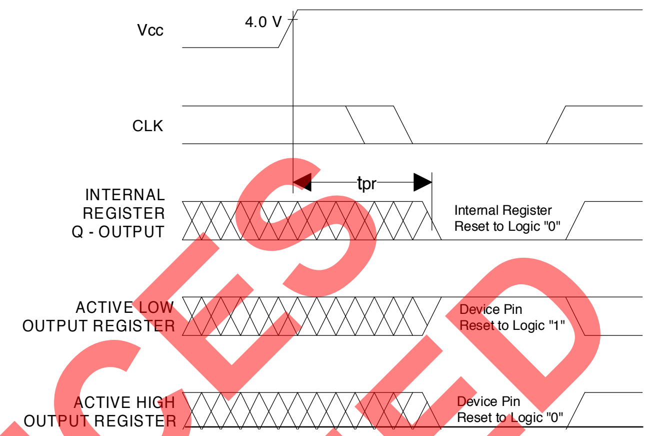
GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

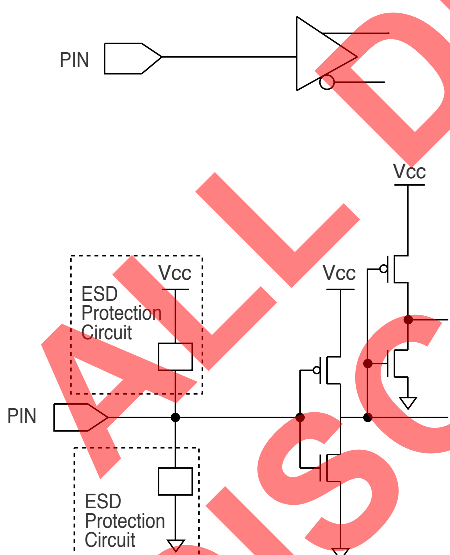
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL26V12 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

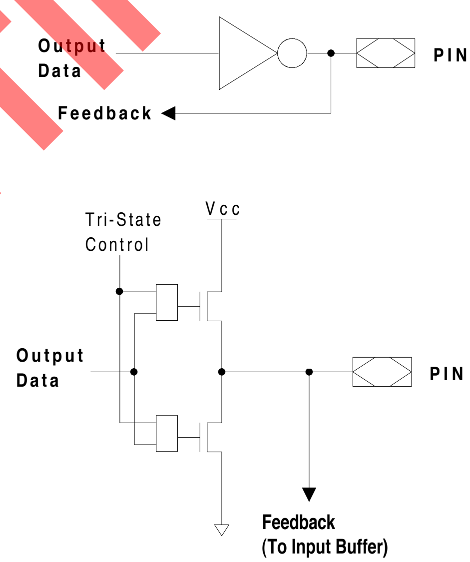
GAL26V12 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

Circuitry within the GAL26V12 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL26V12. First, the VCC rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.





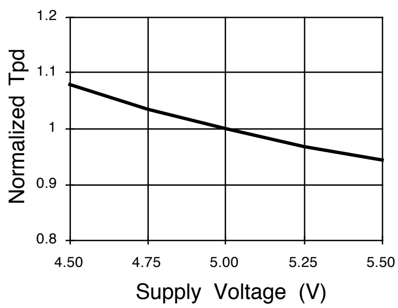
Input



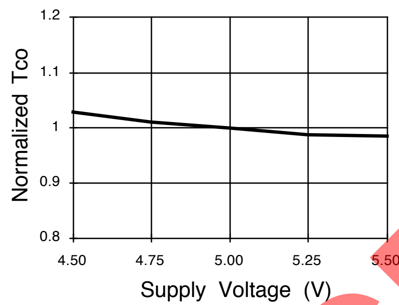
Output

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

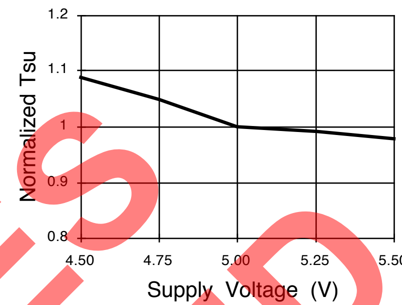
Normalized Tpd vs Vcc



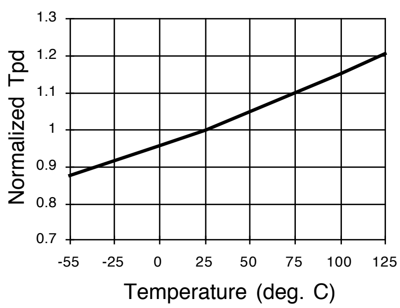
Normalized Tco vs Vcc



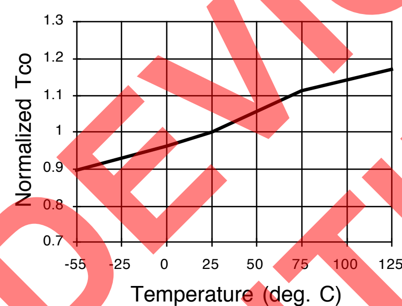
Normalized Tsu vs Vcc



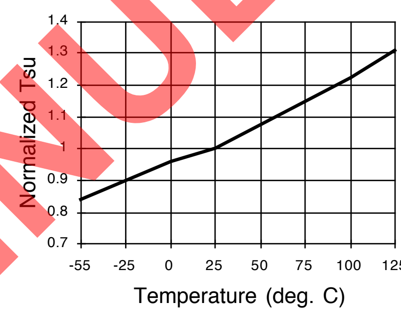
Normalized Tpd vs Temp



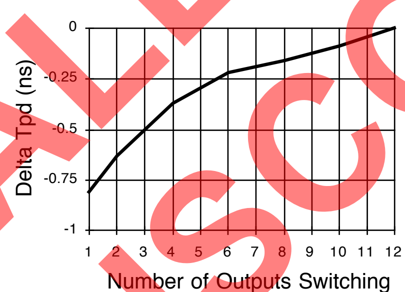
Normalized Tco vs Temp



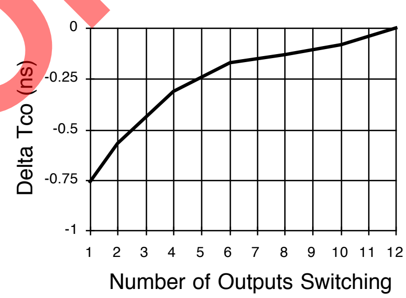
Normalized Tsu vs Temp



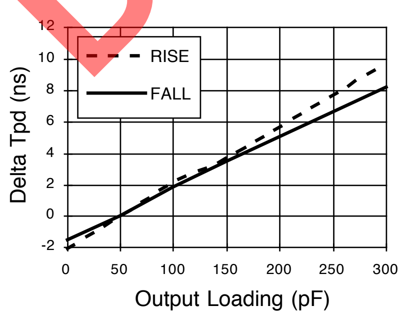
Delta Tpd vs # of Outputs Switching



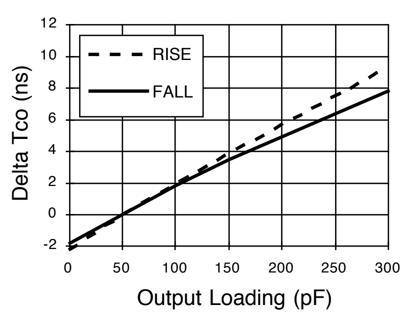
Delta Tco vs # of Outputs Switching



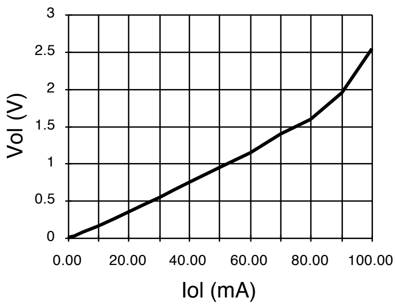
Delta Tpd vs Output Loading



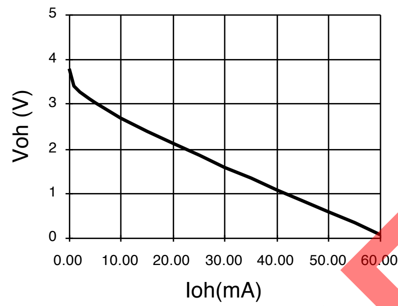
Delta Tco vs Output Loading



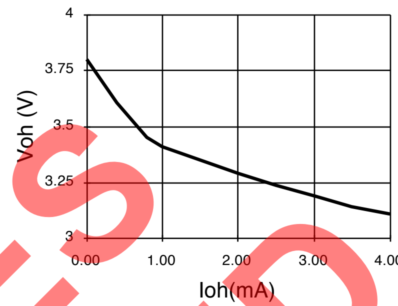
Vol vs Iol



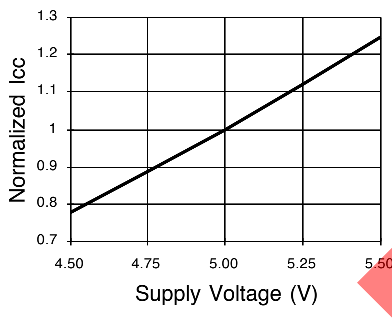
Voh vs Ioh



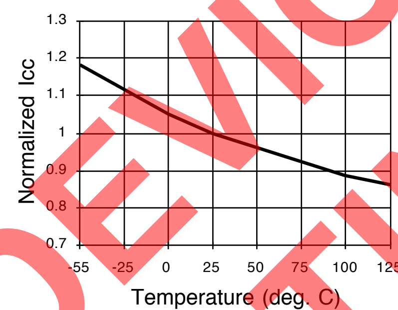
Voh vs Ioh



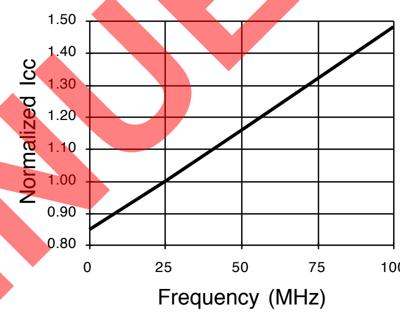
Normalized Icc vs Vcc



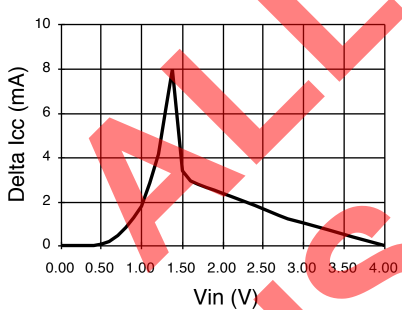
Normalized Icc vs Temp



Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)