RENESAS

3.3V CMOS 16-BIT BUS TRANSCEIVER WITH 3 STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCHR162245A

FEATURES:

- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

DRIVE FEATURES:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems
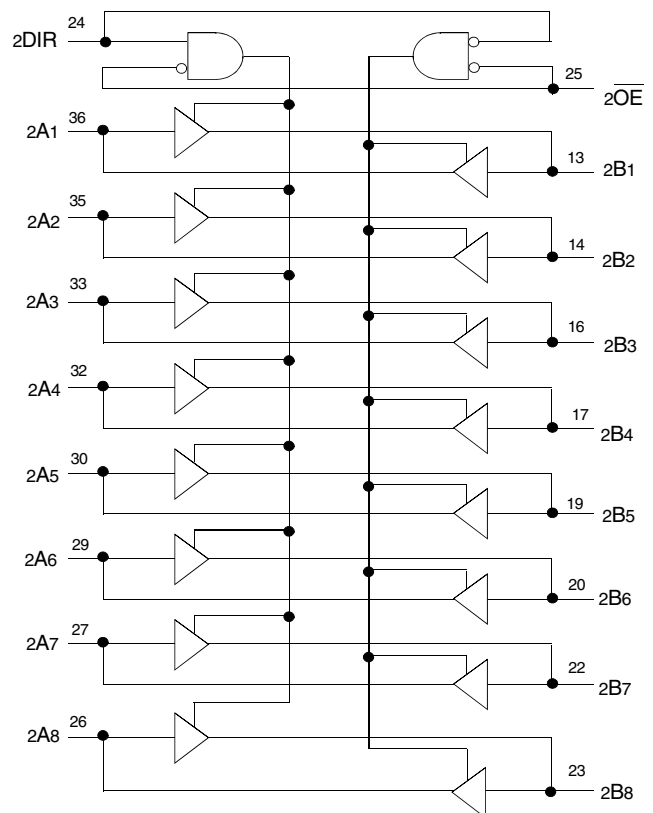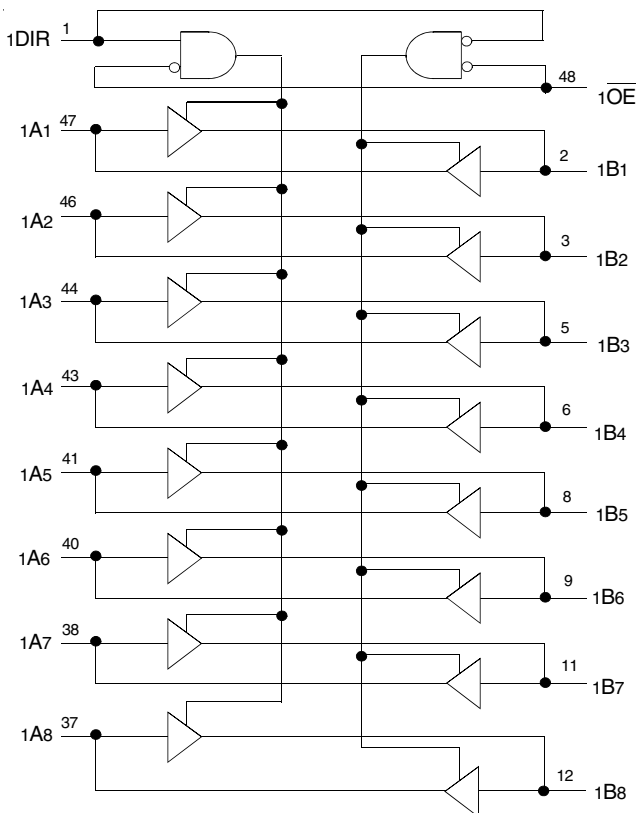
DESCRIPTION:

This 16-bit bus transceiver is built using advanced dual metal CMOS technology. This high-speed, low power device is ideal for asynchronous communication between two buses (A and B). The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (DIR) controls the direction of data flow. The output enable pin (OE) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.
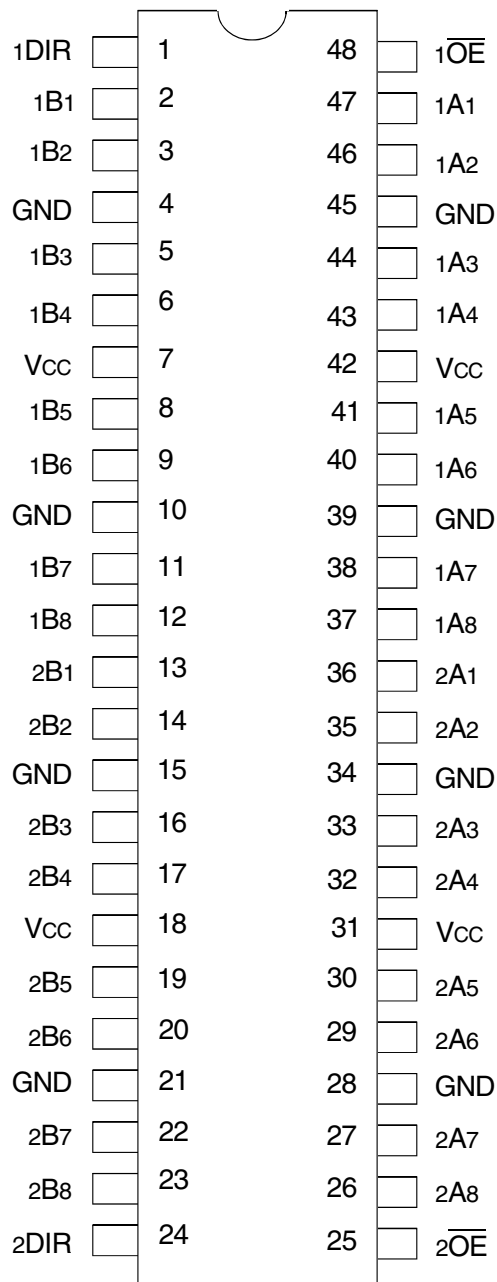
The LVCHR162245A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been designed to drive ±12mA at the designated threshold levels.

The LVCHR162245A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

INDUSTRIAL TEMPERATURE RANGE

OCTOBER 2015

DSC-4598/6

PIN CONFIGURATION

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
VCC	7	42	VCC
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
VCC	18	31	VCC
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$

TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T$_A$ = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	6.5	8	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Output
xAx	Side A Inputs or 3-State Outputs[1]
xBx	Side B Inputs or 3-State Outputs[1]

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH 8-BIT SECTION)[1]

Inputs		Outputs
x$\overline{OE}$	xDIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Z State

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40°C$ to $+85°C$

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \le 5.5V$		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			$3.6 \le V_{IN} \le 5.5V$[2]	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = − 0.1mA	V_{CC} − 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = − 4mA	1.9	—	
			I_{OH} = − 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = − 4mA	2.2	—	
			I_{OH} = − 8mA	2	—	
		V_{CC} = 3V	I_{OH} = − 6mA	2.4	—	
			I_{OH} = − 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = − 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

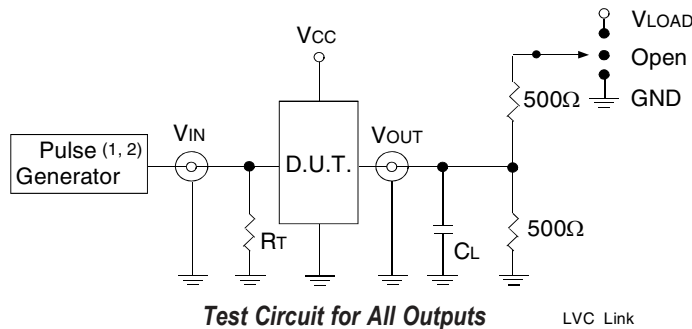| Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	39	pF
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs disabled		4	

SWITCHING CHARACTERISTICS[1]

Symbol	Parameter	V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	—	5.7	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xAx or xBx	—	7.9	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xAx or xBx	—	8.3	2.2	7.4	ns
$t_{SK(o)}$	Output Skew[2]	—	—	—	500	ps

NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T_A = − 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc[(1)]=3.3V±0.3V	Vcc[(1)]=2.7V	Vcc[(2)]=2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

Test Circuit for All Outputs   LVC Link

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open
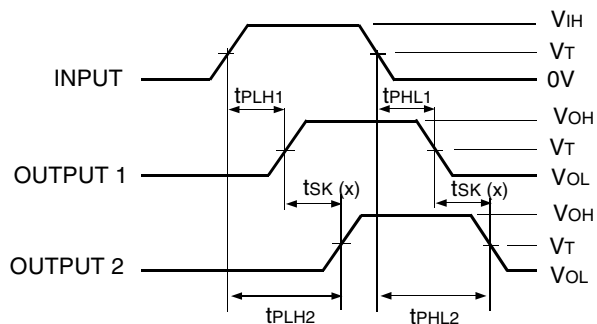
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|\ or\ |t_{PHL2} - t_{PHL1}|$$

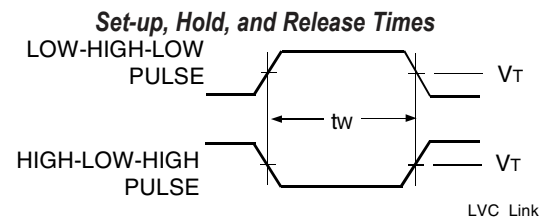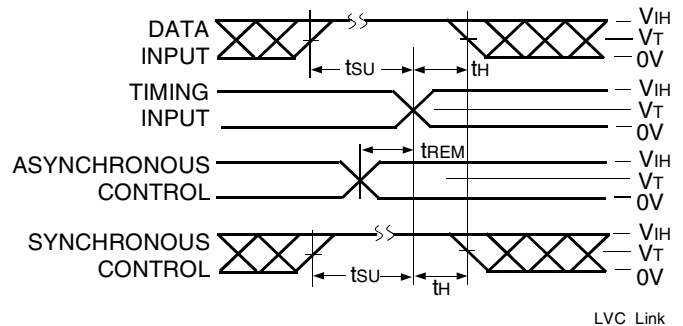*Output Skew - $t_{SK}(x)$*   LVC Link

NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

Propagation Delay
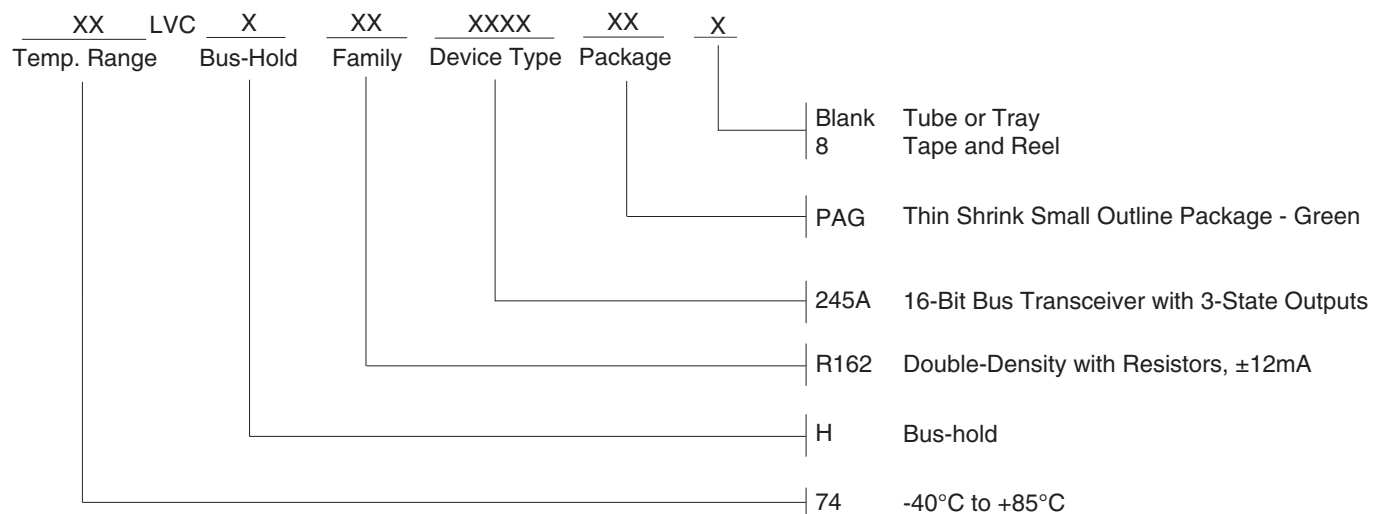

Enable and Disable Times
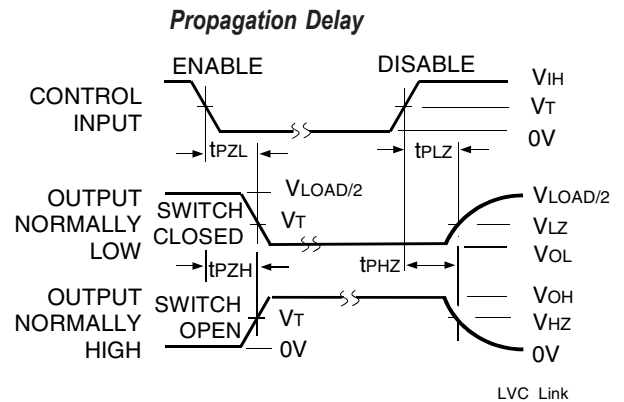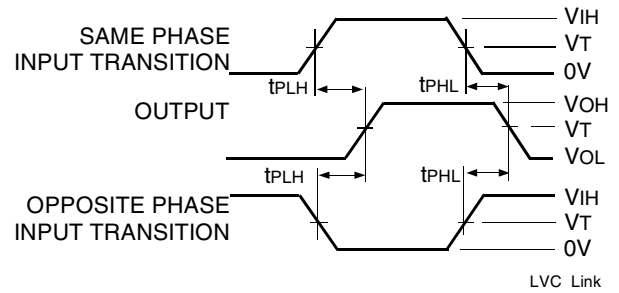
NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Set-up, Hold, and Release Times

Pulse Width

ORDERING INFORMATION

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  XX    LVC    X      XX      XXXX      XX     X
Temp. Range  Bus-Hold  Family  Device Type  Package
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Blank	Tube or Tray
8	Tape and Reel
PAG	Thin Shrink Small Outline Package - Green
245A	16-Bit Bus Transceiver with 3-State Outputs
R162	Double-Density with Resistors, ±12mA
H	Bus-hold
74	-40°C to +85°C

DATASHEET DOCUMENT HISTORY

10/06/2015   Pg. 6   Updated the ordering information by removing non RoHS part and adding Tape and Reel information.

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