

CDCM6208 Evaluation Board

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1 Features

- Easy-to-use evaluation module generating low-phase noise clocks up to 800 MHz
- Easy device programming via host-powered USB port or control pins
- Rapid configuration with provided EVM Control Software
- Powered from the USB port, or by an external 3.3-, 2.5-, or 1.8-V power supply
- Single-ended or differential input; external crystal for use with on-chip oscillator

Words shown in ***bold italics*** in this document show the same name and label on the EVM board itself.



Figure 1. CDCM6208 Evaluation Board

2 General Description

The CDCM6208 is a highly-versatile, low-jitter, low-power frequency synthesizer generating up to eight clock outputs, selectable between LVPECL-like high-swing CML, normal-swing CML, LVDS-like low-power CML, HCSL, or LVCMOS, from one of two inputs that can feature a low frequency crystal or CML, LVPECL, LVDS, or LVCMOS signals. It also features an innovative fractional divider architecture for four of its outputs generating any frequency with better than 1 ppm frequency accuracy. The device is easily configured through I²C or SPI programming interfaces. In the absence of serial interface, pin-programming mode is available and can set the device in many distinct preprogrammed configurations using control pins. Two versions are available, (CDCM6208V1 and CDCM6208V2) depending on the VCO frequency ranges.

The CDCM6208 is programmed through an SPI or I²C interface using the supplied EVM programming graphical user interface (GUI).

The CDCM6208 evaluation module (EVM) demonstrates the electrical performance of the device. This fully-assembled, factory-tested evaluation board allows complete validation of all device functions. For optimum performance, the board is equipped with 50-Ω SMA connectors and well-controlled 50-Ω impedance micro strip transmission lines.

3 Signal Path and Control

The CDCM6208 provides two selectable inputs – PRI_REF and SEC_REF. The PRI_REF and SEC_REF accept either differential- (CML, LVDS) or single-ended LVCMOS signals, up to 250 MHz. Besides the external clocks, SEC_REF allows the use of an external crystal in the frequency range of 10 MHz to 50 MHz. The EVM provides a PC-board footprint for mounting a 3.2 mm × 2.5 mm SMD crystal. If the SEC_REF is driven through the SMA connector, the on-board crystal and **R72** and **R73** must be removed and **R87** must be populated with a 0-Ω resistor (**R89** must also be populated with a 0-Ω resistor for a differential input signal). The device does not have any internal termination or biasing, therefore, proper biasing and termination options are available on the EVM, if needed.

The CDCM6208 provides up to eight differential signals. Out of eight outputs, four differential outputs can convert into eight singled LVCMOS signals. A maximum of eight differential or 4 differential and eight singled LVCMOS clocks or any of the various combinations are possible.

The device operates as a jitter cleaner or as a frequency synthesizer. The CDCM6208 requires a partially-external loop filter. The EVM provides four loop filter options – two filters are for synthesizer mode and the other two for jitter-cleaning mode. The loop-filter selection affects the phase noise and loop stability of the PLL.

In pin mode, the device option is selected by five control pins. In programming mode, options are selected by programming the on-chip registers. The [CDCM6208](#) data sheet provides the detailed information needed for configuration and use of this device.

Four outputs (Y0-Y3) are configurable as an LVDS, CML, or LVPECL and another four outputs (Y4-Y7) are configurable as LVDS, HCSL, or LVCMOS. All outputs are connected to SMA with AC coupling. Y4-Y7 outputs provide the options of 50 Ω to ground (for HCSL outputs).

The LVCMOS outputs can operate at frequencies up to 200 MHz. The HS-CML and NS-CML outputs operate at up to 800 MHz. The LP-CML and HCSL outputs operate at up to 400 MHz.

4 Software-Selectable Option

The EVM control software communicates with the CDCM6208 through a USB interface and the CDCM6208 SPI or I²C port. The USB controller is normally powered over the USB cable. When the USB/SPI or USB/I²C programming interface is available for use, the on-board LED, D3, is illuminated.

The CDCM6208 GUI can save device configurations into a configuration file (.INI), which are loaded at a later time restoring the saved settings.

5 Installing the EVM Control Software and USB Driver

Start the EVM software installation by double-clicking on the file named *CDCM6208_Installer.exe*. The Microsoft .NET Framework 4.0 is automatically downloaded and installed on the computer, if it is not already installed. The installer attempts installation of the EVM hardware driver.

5.1 CDCM6208 Control User Interface

The following represents the initial screen of the GUI:

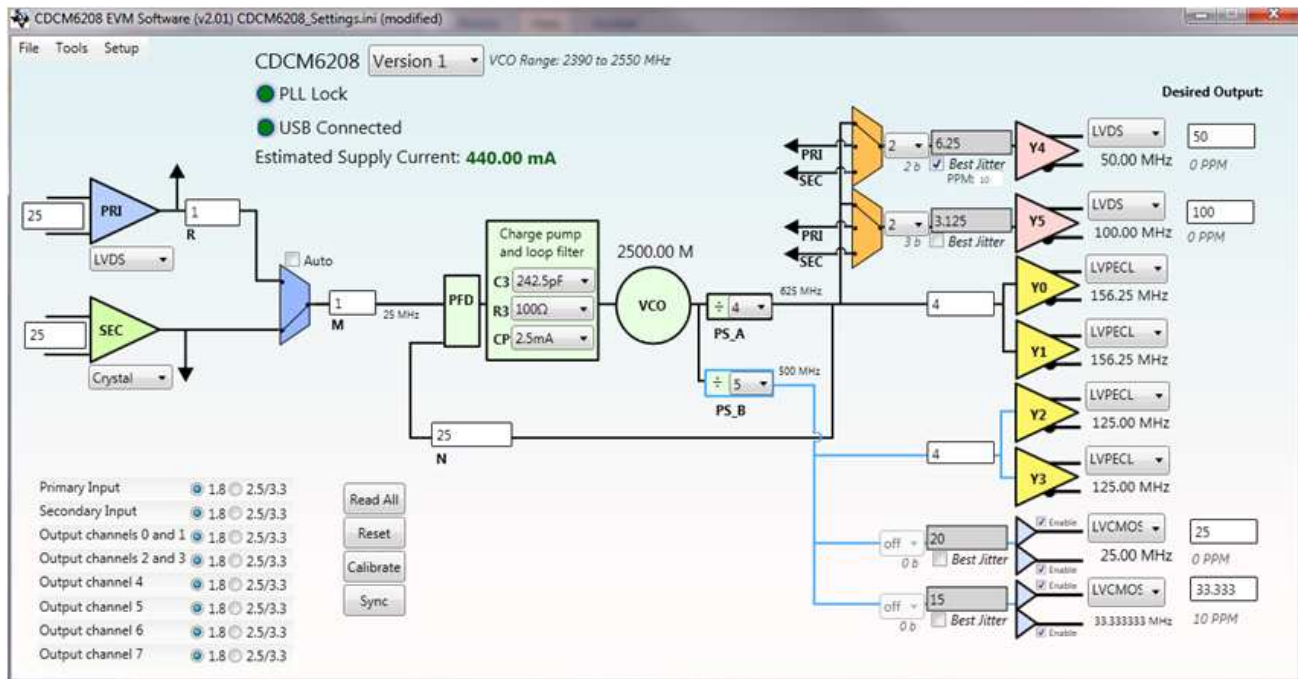


Figure 2. Initial GUI Screen

6 Using the EVM Control Software

The graphical layout of the programming software is based on the functional structure of the CDCM6208. The following settings are changed with this tool:

- Input frequency
- Input divider
- Input type
- Input selection to the PLL
- Charge-pump current
- Internal loop filter components (3rd Pole)
- Pre-scalar and feedback divider
- Output MUX selection
- Output divider or frequency
- Output type

This software also sets input and output buffer supply voltage bits (1.8 V or 2.5/3.3 V)..

6.1 Primary and Secondary Reference Signal Type Selection

Using the pull-down menu, input clock type is selected or input buffer is disabled. The input signal type for *Primary* clock and *Secondary* clock are set to either LVDS, CML, or LVC MOS. Additionally, crystal input is selectable for *Secondary* input.

6.2 Input Divider For Primary Reference ®) Selection

The primary reference has a 4-bit divider ®), therefore, up to 16 appropriate divider values are available.

6.3 Input MUX Selection

The CDCM6208 employs a smart MUX selecting the input clock for the PLL. The input clock is either primary reference only, secondary reference only, or in automatic selection mode. Toggling the connection line, the proper reference input is selected. If the *Auto* box is selected, automatic input selection mode is activated.

6.4 Input Divider (M) For the PLL Selection

The input (M) divider is a continuous 14-b counter (1–16384) that is present after the Smart Input MUX. The output of the M divider sets the PFD frequency to the PLL and must be in the range of 8 kHz to 100 MHz.

6.5 Charge Pump Current Selection

The charge-pump current value is chosen from the pull-down menu. The allowable range of the charge-pump current is from 500 μ A to 4 mA.

6.6 Loop Filter (3rd Pole only) Selection

C1, R2, and C2 are external loop filter components connected to the ELF pin, but the 3rd pole of the loop filter is internal to the device with R3 and C3 register-selectable. Appropriate C3 and R3 values are selected using the pull-down menu.

6.7 Feedback Divider Selection

The feedback divider (N) is made up of a cascaded 8-b counter divider (1–256) and a 10-b counter divider (1–1024) present on the feedback path of the PLL. If the divider value is available, the software automatically selects the proper combination from the two cascaded dividers. The output of the N divider sets the PFD frequency to the PLL and must be in the range of 8 kHz to 100 MHz.

6.8 Prescaler Dividers (PS_A and PS_B) Selection

The prescaler (PS) dividers are fed by the output of the VCO and are distributed to the output dividers (PS_A to the dividers for outputs Y0, Y1, Y4, and Y5. PS_B to the dividers for outputs Y2, Y3, Y6, and Y7). PS_A also completes the PLL, driving the input of the feedback divider (N). Appropriate values are set for each prescaler using the pull-down menu.

6.9 VCO Frequency Selection

The VCO frequency value depends on the selection of reference input frequency and input dividers, prescaler (PS_A), and feedback dividers. The software automatically calculates the VCO frequency, based on the selection, and provides the value. If the calculated VCO frequency is outside of the range, it flashes red.

6.10 Output MUX Selection

Both Y4 and Y5 outputs have multiplexers which select one of the three inputs (PRI_REF, SEC_REF, or PS_A) for the outputs. The proper input is selected for the outputs by dragging the connection line.

6.11 Output Dividers

Outputs Y0 and Y1 share one 8-bit continuous integer divider and outputs Y2 and Y3 share another 8-bit continuous integer divider; therefore, these pairs of outputs have the same frequency. Each of the outputs Y4, Y5, Y6, and Y7 have 8-bit continuous integer dividers and in addition, 20-bit fractional dividers. The software automatically chooses the right divider values for Y4–Y7 outputs from the integer and fractional dividers, if the expected output frequency in the desired output box is provided.

6.12 Output Signal Type Selection

Outputs Y0–Y3 offer LP-CML (LVDS like), CML or HS-CML (LVPECL like) signaling types. Using the pull-down menu, one of the signal types is selected for each output or can disable the output channel completely. Outputs Y4–Y7 offer LP-CML (LVDS like), HCSL or LVCMOS signaling types. Using the pull-down menu, one of the signal types is selected for each output or can disable the output channel completely. If the LVCMOS signal type is selected, check *Enable* boxes, enabling the outputs individually.

6.13 Additional Features

The EVM software GUI comes with tools that are helpful in optimizing the device settings for best performance. These include a Frequency Planning Tool, the Loop Filter Simulator, and the Phase-Noise Simulator. Each of these tools are described in detail in the Help documentation provided in the GUI.

7 Configuring the Board

The CDCM6208 is a programmable clock driver with many options. The EVM was designed with maximum flexibility so engineers can configure the EVM for operation at its desired mode.

7.1 Selecting the Interface Connection

The CDCM6208 is configurable via the serial interface or control pins. Both SPI and I²C interface options are available for configuring the device. Switch SW1 is dedicated for the SPI interface and switch SW2 is for the I²C interface. The selected interface switch must be turned on and the other switch must be turned off. Both switches must be turned off for Pin control mode.

Header **JMP9** also connects an external host to SPI or I²C.

7.2 Configuring the Power Supply

The device is powered up with an external power supply or on-board regulators powered by an attached USB cable. The EVM has options for 1.8-, 2.5-, and 3.3-V power supplies. These supply voltages are external to, or internal from the regulators. It has five different rails – two for outputs, one for PLL, one for digital logic, and one for reference input power supplies.

The banana jacks (**P2**, **P3**, and **P4**) are external 3.3 V, 2.5 V, and 1.8 V, respectively. Banana jack **P1** is for GND. Low-dropout regulators U6, U7, and U8, generate 3.3 V, 2.5 V, and 1.8 V, respectively. The jumper on header **JP_3_10** selects between an external or internal 3.3 V, the jumper on header **JP_3_11** selects between an external or internal 2.5 V, and the jumper on header **JP_3_12** selects between an external or internal 1.8 V.

The jumpers on the header **JMP5** select for the DVDD power rail, **JMP1** selects for the PLL power rails, **JMP3** selects for the output power rails (Y2, Y3, Y6, and Y7), **JPM2** selects for the output power rails (Y0, Y1, Y4, and Y5) and **JPM4** selects for the reference input power rails from 3.3-, 2.5-, and 1.8-V power supplies. Mixed power supplies for this device are possible, using these headers.

NOTE: A USB cable must be connected for biasing voltage generation of 1.2 V and 0.9 V for the reference inputs. These biasing voltages are generated by the on-board regulators which rely on the USB supply. [Figure 3](#) shows the jumper configuration for a USB power supply. The EVM settings drive the device from the USB with 1.8-V and 3.3-V supplies. Jumpers for the header JP_3_10 are set to 3.3-V regulator and for JP_3_3_12 header to 1.8-V regulator. DVDD (JMP5), VDD_PLL (JMP1), VDD_IN (JMP4), and VDD_OUTB (JMP3) supplies are set to 1.8 V and VDD_OUTA (JMP2) supply is set to 3.3 V. The entire device is running at 1.8 V, except the Y0, Y1, Y4, and Y5 outputs which are running at 3.3 V.

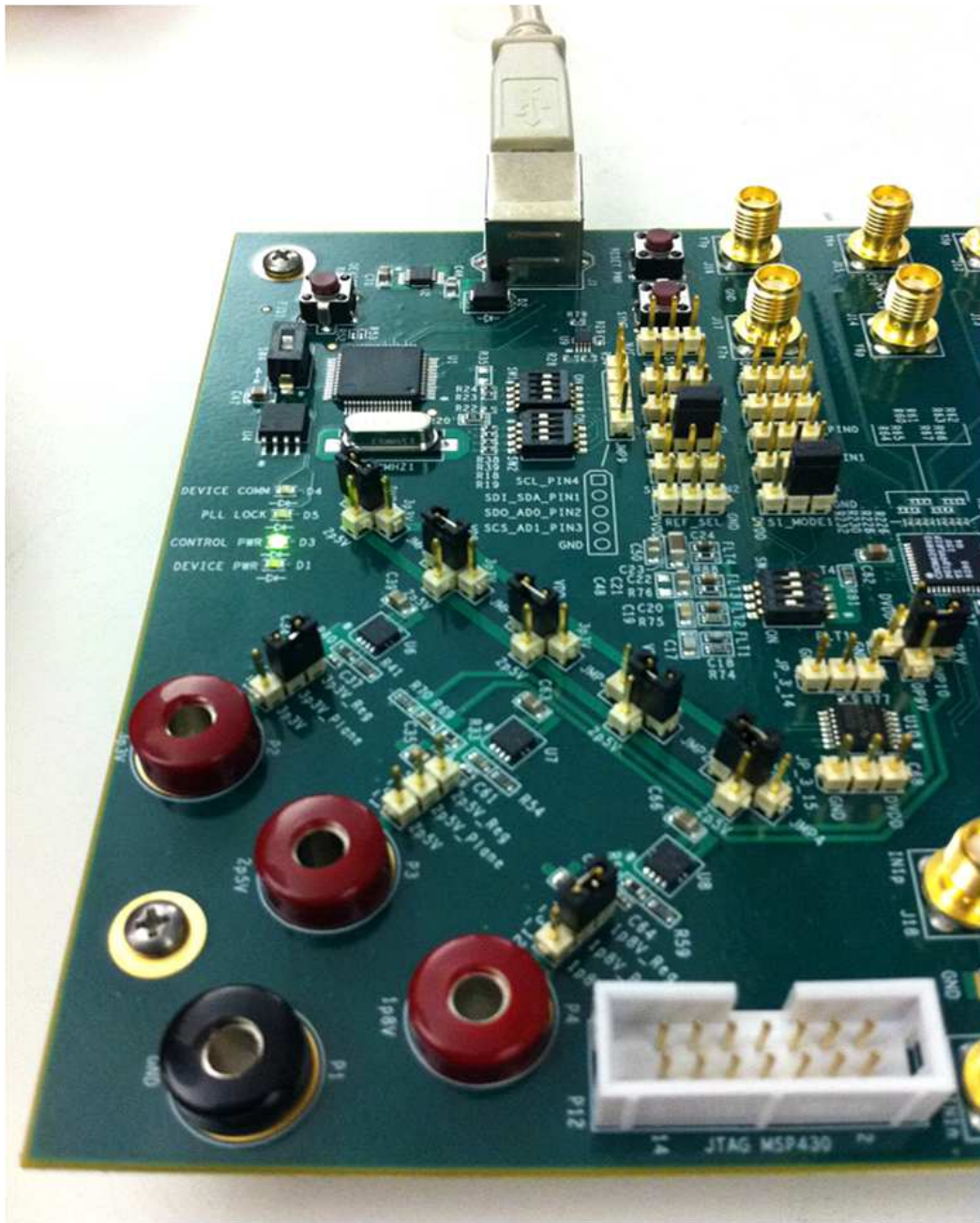


Figure 3. Jumper Configuration For USB Power Supply

7.3 Configuring the Reference Inputs

The CDCM6208 offers two inputs (PRI_REF and SEC_REF). SMA **J18** and **J19** are dedicated for PRI_REF (IN1p and IN1n) and SMA **J20** and **J21** are dedicated for SEC_REF (1N2p and 1N2n). Both inputs in the EVM are AC-coupled, by default, using coupling capacitors (**C25** and **C26** for PRI_REF and **C29** and **C30** for SEC_REF). CDCM6208 does NOT have any internal termination or biasing; so, external biasing is required after AC coupling. Headers **JMP10** and **JMP11** provide the options for PRI_REF input biasing and SEC_REF input biasing, respectively. Depending on the input signaling level and power supply selection, proper biasing must be selected, see [Table 1](#).

Table 1. Input Selection Jumper Settings

Input Signaling Level	Input Supply Voltage	JPM10 and JPM11 Selection
CML	1.8 V/2.5 V/3.3 V	DVDD
LVDS	2.5 V/3.3 V	1P2V
LVDS	1.8 V	0P9V
LVC MOS	1.8 V/2.5 V/3.3 V	GND ⁽¹⁾
Disabled	N.A.	None

⁽¹⁾ This 50 Ω to GND is only required if a signal generator is used.

R83, R84, R85, and R86 resistors (49.9 Ω) provide the termination for 50- Ω trace.

Place 0- Ω resistors in **R87** and **R89** and remove **R72** and **R73** resistors for the external clock to SEC_REF connection.

LVC MOS inputs are single ended and only the positive pins (IN1p for PRI_REF and IN2p for SEC_REF) of the inputs are used and DC terminations are recommended. Replace **C25** with a 0- Ω resistor for PRI_REF and **C29** with a 0- Ω resistor for SEC_REF.

SEC_REF accepts crystal input. SEC_REF input is configured for crystal input by default and a 25-MHz crystal is placed in **Y1**. **C27** and **C28** provide the load capacitance options for the crystal.

7.4 Configuring the Control Pins

The device has multiple dedicated pins controlling and configuring the operation. These pins must be set as instructed for correct device operation.

Power Down Pin (PDN): This pin has an internal 50-k Ω pull-up resistor. For normal operation, the PDN pin should be left open or connect the jumper (header **PDN**) to **DVDD**. For power-down mode, connect the jumper to **GND**.

Synchronization Pin (SYN CN): This pin has an internal 50-k Ω pull-up resistor. For normal operation, the SYN CN pin should be left open or connect the jumper (header **SYN C**) to DVDD. An external signal uses this header to synchronize the outputs. In addition to the header, button **SW7** toggles the SYN CN pin.

Mode Selection Pins (SI_MODE0 and SI_MODE1): These two pins select the mode of device configuration. The SI_MODE1 pin has an internal pull-up resistor and the SI_MODE0 pin has an internal pull-down resistor. The jumpers on the header, **SI_MODE0** and **SI_MODE1**, must be set as shown in [Table 2](#).

Table 2. Mode Selection Jumper Settings

Jumper On SI_MODE1 Header	Jumper On SI_MODE0 Header	Mode of Configuration
GND	Open or GND	SPI mode
GND	DVDD	I ² C mode
Open or DVDD	Open or GND	Pin mode

Reset or Supply Control Pin (RESETN_PWR): This pin has dual functions, depending on the mode selection. This pin acts as a RESETN pin in Interface-programming mode or controls the device core and output supply voltage setting. Button **SW6** and **RESET_PWR** header are dedicated for this pin. This pin has an internal 50-k Ω pull-up resistor. In Interface-programming mode, the header (**RESET_PWR**) is left open or connects the jumper to **DVDD**. Connecting the jumper to **GND** or pressing the button (**SW6**) puts the device in reset mode. In Pin mode, set the jumper to **GND** for a 1.8-V power supply and to **DVDD** for a 2.5-V/3.3-V power supply.

Reference Select Pin (REF_SEL): This pin has an internal 50-k Ω pull-up resistor. Connect the header **REF_SEL** to **GND** for PRI_REF input and leave open or connect to **DVDD** for SEC_REF input selection. See Table 34 in the data sheet ([CDCM6208](#)) for a detailed description.

Status Pin (STATUS1/PIN0): Depending on the operation mode, this is either an input or output pin. In Interface-programming mode, this pin (header **STATUS1_PIN0**) provides the indication of a particular reference clock selection to the PLL or PLL lock and/or unlock or loss of references depending on Register 3 Bit 10-12 settings. See [Table 3](#) for a full description:

Table 3. STATUS1 Functional Description

Status Signal Name	Signal Type	Register Bit	Description
SEL_REF	LVC MOS	R3.12	Indicates reference selected for PLL: "0" → Primary "1" → Secondary
LOSS_REF	LVC MOS	R3.11	Loss of reference input observed at input, Smart MUX output in observation window for PLL: "0" → Reference input present "1" → Loss of reference inputs
PLL_UNLOCK	LVC MOS	R3.10	Indicates unlock status for PLL: "0" → PLL locked "1" → PLL unlocked

In pin mode, this becomes an input pin and the header *pin*, **STATUS1_PIN0**, is controlled by PIN0 which connects to **GND** or **DVDD**.

Device Control Pins (SDI/SDA/PIN1, SDO/AD0/PIN2, SCS/AD1/PIN3 and SCL/PIN4): These four pins have multiple functions depending on the device's programming interface (SPI or I²C) and pin-control modes. See the data sheet ([CDCM6208](#)) for detailed descriptions and see [Table 4](#) for jumper connections.

Table 4. Device Control Pin Functions

Programming Mode	Header SDI_SDA_PIN1	Header SDO_ADO_PIN2	Header SCS_ADI_PIN3	Header SCL_PIN4	Remarks
SPI	Open	Open	Open	Open	Jumpers must not be connected in this mode
I ² C	Open	GND ⁽¹⁾	GND ⁽¹⁾	Open	Header SDO_ADO_PIN2 and SCS_ADI_PIN3 provide the I ² C address option
Pin Mode	DVDD or GND	DVDD or GND	DVDD or GND	DVDD or GND	The pin selections determine the predefined device's functional condition

⁽¹⁾ The control software assumes the default address bit settings for AD[1:0] is 00.

7.5 Selecting the Loop Filter

The CDCM6208 includes an on-chip PLL with a partially-integrated loop filter. External loop components (C1, C2 and R2) are required to complete the PLL. The external loop filter is chosen by selecting one from the four available options on the CDCM6208EVM using the dip switch, **SW5**. Depending upon the device's operation mode, synthesizer or jitter cleaning, selecting appropriate loop filter values is critical. Two loop filters, 1 and 2, are for synthesizer mode and the other two filters, 3 and 4, are for jitter cleaning mode. If different RC components are required based on the customer's PLL configuration, these components must be replaced by appropriate resistor and capacitors.

7.6 Configuring the Outputs

All eight outputs are connected to SMA through AC-coupling. Output Y4-Y7 can provide HCSL clocks. These outputs have 50 Ω-to-GND (not populated) and series-resistors (0-Ω populated) options. Placing 50-Ω resistors and possibly adjusting the series resistor values (up to 33 Ω) improves ringing if the outputs are configured as HCSL.

7.7 Using the MSP430 as a Bootloader

The onboard MSP430G2001 is a bootloader for the CDCM6208. A separate application note describes how to generate, debug, and load the needed software for the MSP430.

SW1 and **SW2** must be in the OFF position while **SW3** must be in the ON position for communication with the MSP430 (**U10**) via JTAG (**P12**) and for communication of the MSP430 with the CDCM6208. Also note that the MSP430 requires a minimum of 1.8 V for nominal operation. Once the program is loaded to the MSP430, resetting power to the MSP430 makes the bootloader execute again – after this occurs, the MSP430 enters a low-power mode.

8 A Step by Step Guide on Updating the TUSB3210 Firmware for I2C communication on the CDCM6208 EVM

Older EVM revisions might require to update the TUSB3210 firmware to enable the correct I²C communication between CDCM6208 and TUSB3210. The following steps explain how to update the firmware.

8.1 Required Software and Hardware

In order to update the TUSB3210 Firmware on the CDCM6208 EVM, the following items are required:

- TI USB EEPROM Burner Utility for the TUSB2136 and TUSB3210
- PC with Windows XP
- USB Cable (Male A to Male B)
- Latest version of TUSB3210 Firmware for the CDCM6208 EVM ([SLAC550](#))

8.2 Installing TI USB EEPROM Burner Software

The TI USB EEPROM Burner software is available on TI's product page for the TUSB3210 for free. This download is available at the following URL. The file is located under Software & Development Tools section. <http://www.ti.com/product/tusb3210>

Once the .ZIP file is successfully downloaded and extracted, setup and installation can begin by opening the "DISK1" directory and running the "setup.exe" program. The program will prompt the user upon successful installation.

8.3 Programming the CDCM6208 EVM's TUSB3210

Step 1 – Powering Up the EVM

The TUSB3210 chip is interfaced with an external EEPROM on the EVM. To ensure proper communication between the Burner software and the TUSB3210, turn Switch 4 (SW4) to the OFF position before connecting the USB cable to the EVM. SW4 is circled below and is shown in the ON position (see [Figure 4](#)).

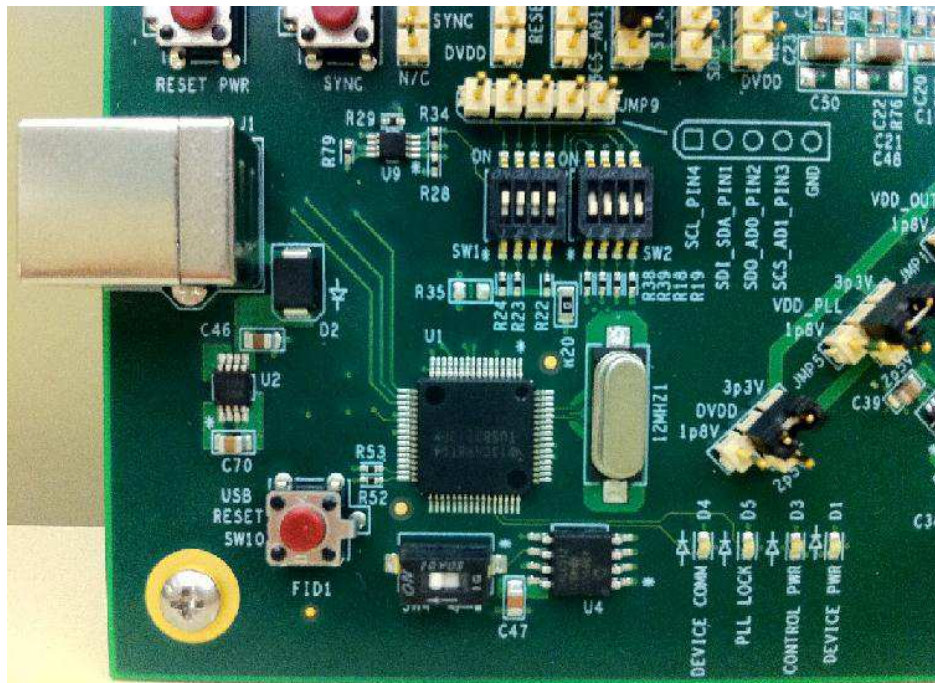


Figure 4. EVM SW4 Location

NOTE: Once the board is powered up, turn SW4 back to the ON position to enable communication between the EEPROM and the TUSB3210 chip. The board is now ready for programming.

Step 2 – Using the TI EEPROM Burner Software

To use the EEPROM Burner Software, simply boot up the program and appropriately fill out the pull down menus. If the CDCM6208 EVM is recognized by the Burner software and driver, an option under the “Select the USB Device:” should appear named “TI TUSB3210 EEPROMBurner”. This indicates the driver has successfully connected to the TUSB3210 on the CDCM6208 EVM.

The EVM features 512kbits of EEPROM, so select this option on the “Select EEPROM Size:” drop down menu. Finally, locate the location of the new firmware .BIN file. Use the Browse button near the “Select EEPROM Image:” to locate the .BIN file location. A screenshot of the Burner software is provided in [Figure 5](#).

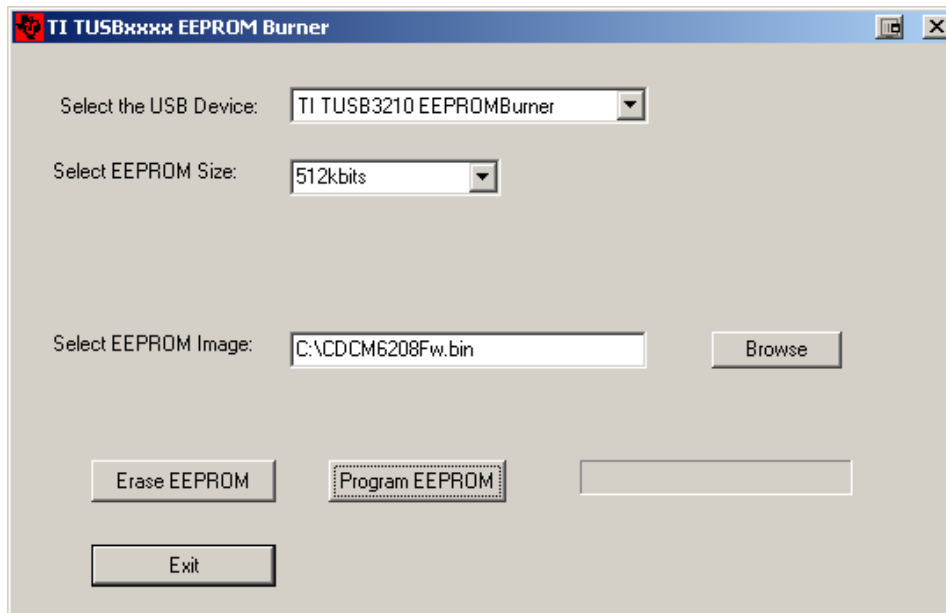


Figure 5. TUSB3210 EEPROM Burner Software

To begin the programming sequence, press the Program EEPROM button. The status of the process is shown below the progress bar. Once the programming is complete, a dialog box will appear reading "EEPROM Programmed Successfully!". This completes upgrading the CDCM6208 EVM Firmware.

9 CDCM6208V2 EVM Board Schematic

CDCM6208 EVM Control Modes

- 1) Pin Control - Use Pin jumpers (Group 2)
- 2) SPI - Set SW1 to On position
- 3) I2C - Set SW2 to On position
- 4) Bootloader - Set SW3 to On position (page 7)

(Select only one control mode at a time - Turn switches off or remove jumpers for non-selected modes)

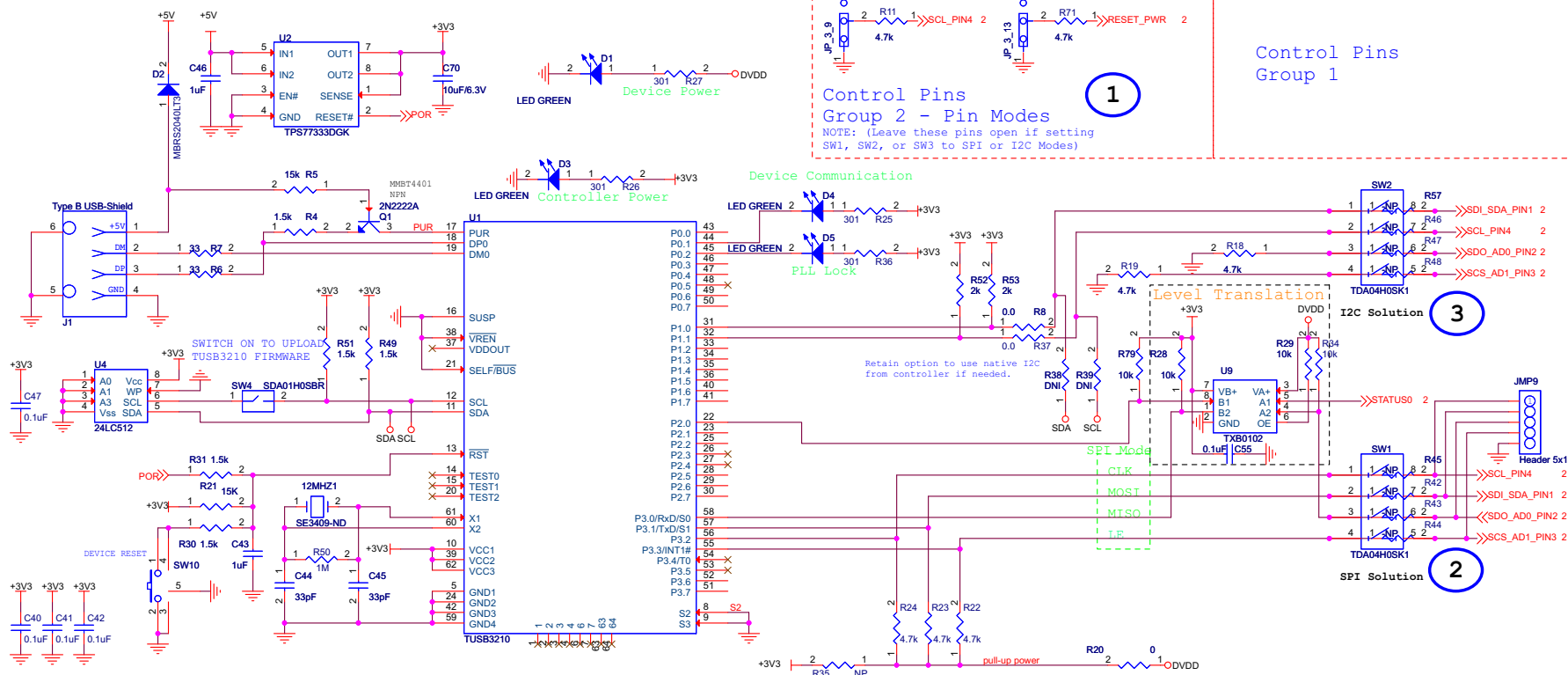


Figure 6. CDCM6208V1/CDCM6208V2 EVM Control Modes

Device Pins and Bypassing

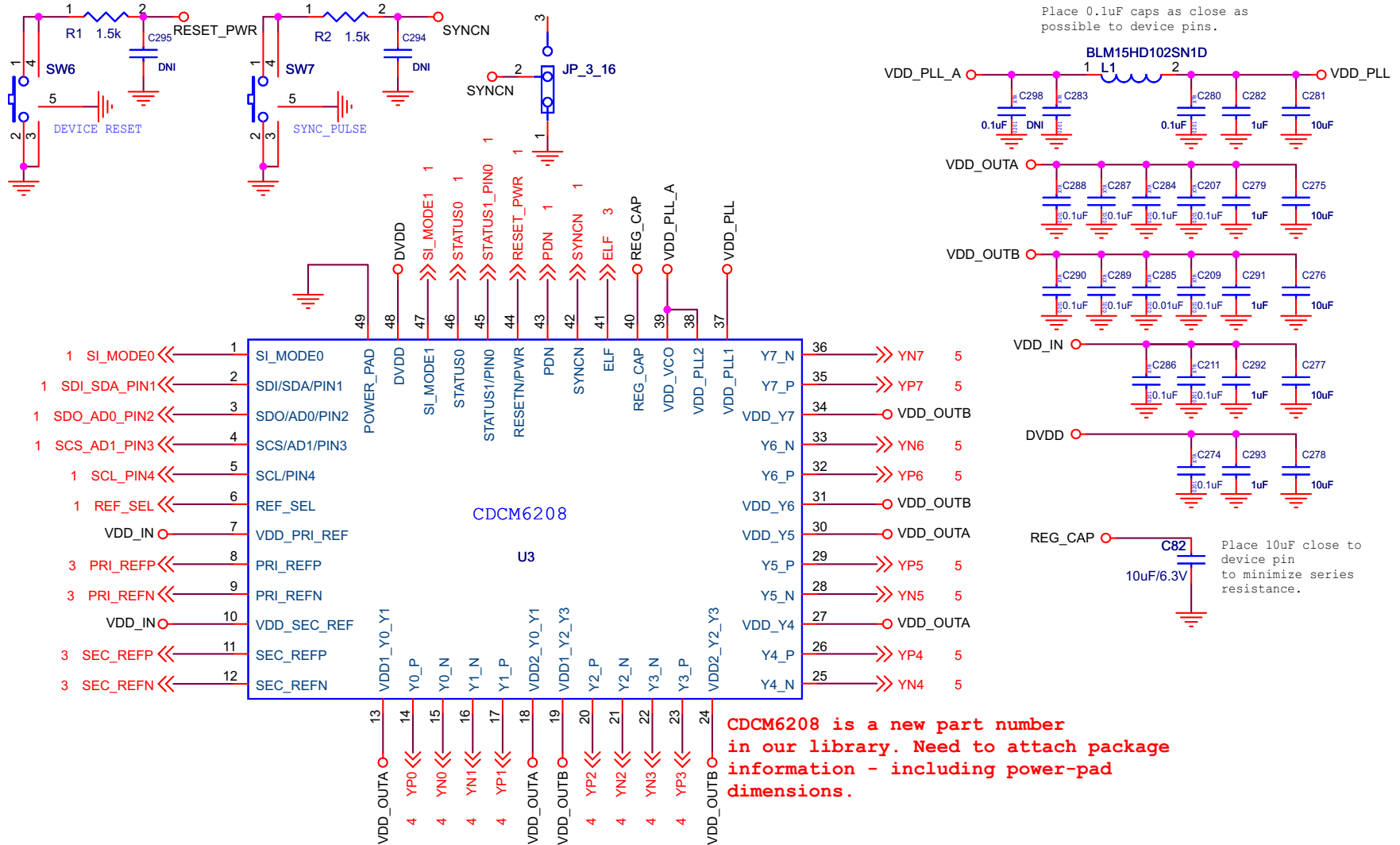
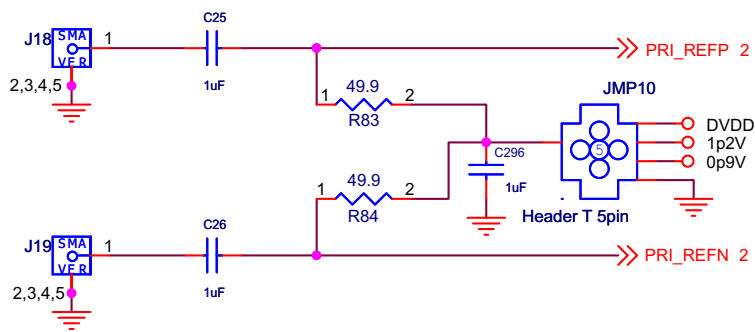


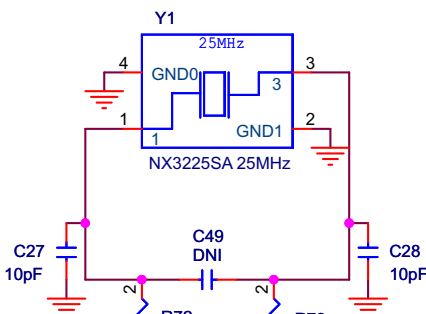
Figure 7. CDCM6208V1/CDCM6208V2 EVM Device Pins and Bypassing

PRIMARY REFERENCE INPUT

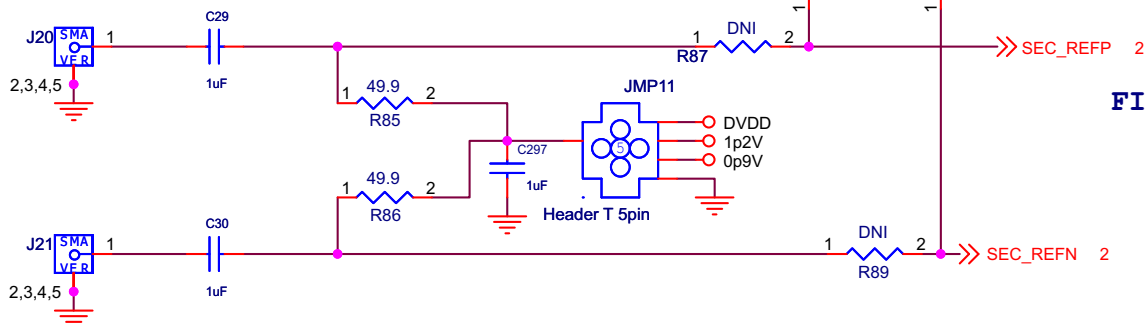


Input jumpers
 Connect center pin to
 * 0.9V for 1.8V LVDS
 * 1.2V for LVDS
 * GND for LVCMOS
 * DVDD for CML - also replace series caps with 0 ohms

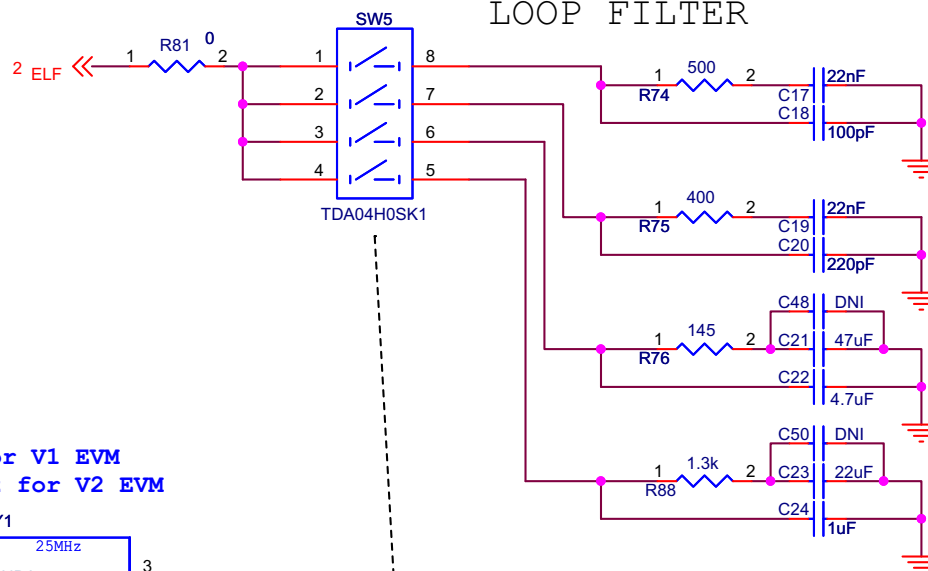
25MHz for V1 EVM
 30.72MHz for V2 EVM



SECONDARY REFERENCE INPUT



LOOP FILTER



FILTER 1

V1: C1=100pF, R2=500, C2=22nF (BW = 300kHz when PFD=25MHz, ICP=2.5mA, R3=100, C3=242.5pF)
 V2: C1=470pF, R2=560, C2=100nF (BW = 300kHz when PFD=30.72MHz, ICP=2.5mA, R3=100, C3=242.5pF)

FILTER 2

V1: C1=220pF, R2=400, C2=22nF (BW = 300kHz when PFD=30.72MHz, ICP=2.5mA, R3=100, C3=242.5pF)
 V2: C1=200pF, R2=400, C2=22nF (BW = 300kHz when PFD=25MHz, ICP=2.5mA, R3=100, C3=242.5pF)

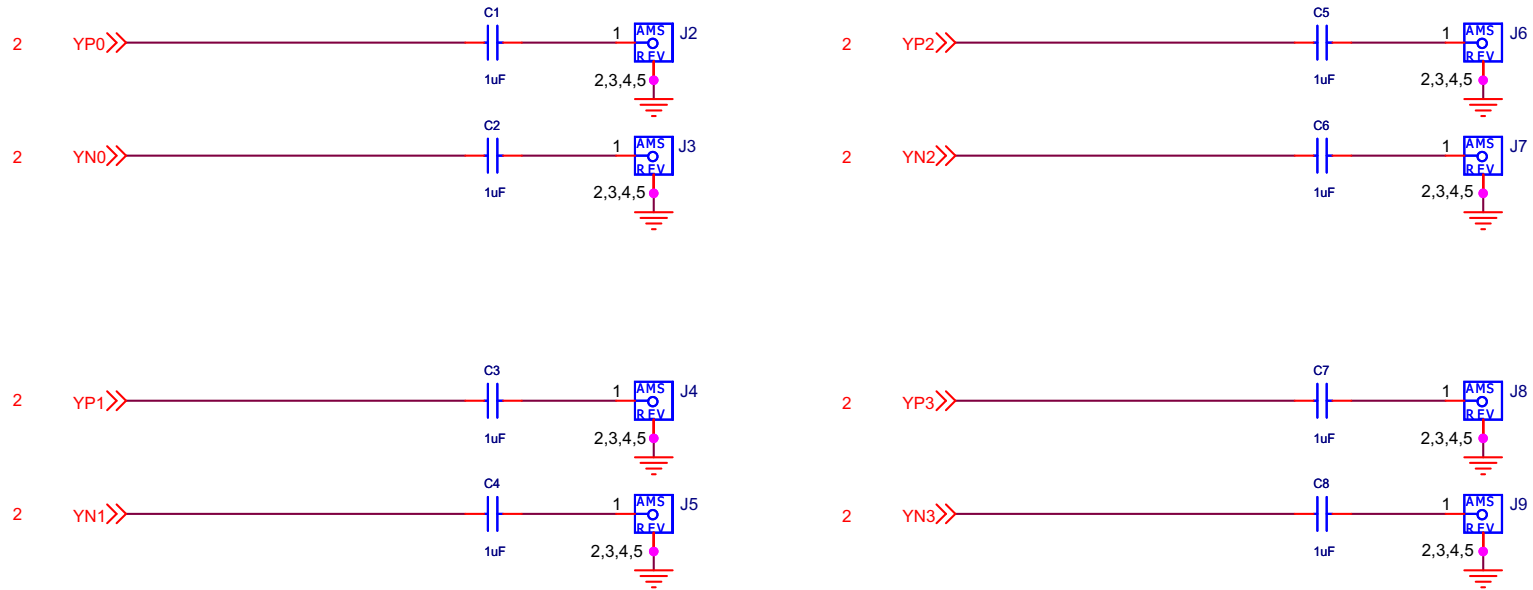
FILTER 3

V1: C1=4.7uF, R2=145, C2=47uF (BW = 40Hz when PFD=40kHz, ICP=500uA, R3=4010, C3=562.5pF)
 V2: C1=4.7uF, R2=10, C2=100uF (BW = 600Hz when PFD=9.6MHz, ICP=500uA, R3=4010, C3=562.5pF)

FILTER 4

V1: C1=1uF, R2=1.3k, C2=22uF (BW = 50Hz when PFD=8kHz, ICP=500uA, R3=4010, C3=562.5pF)
 V2: C1=5uF, R2=100, C2=100uF (BW = 100Hz when PFD=80kHz, ICP=500uA, R3=4010, C3=562.5pF)

Figure 8. CDCM6208V1/CDCM6208V2 EVM Reference Inputs

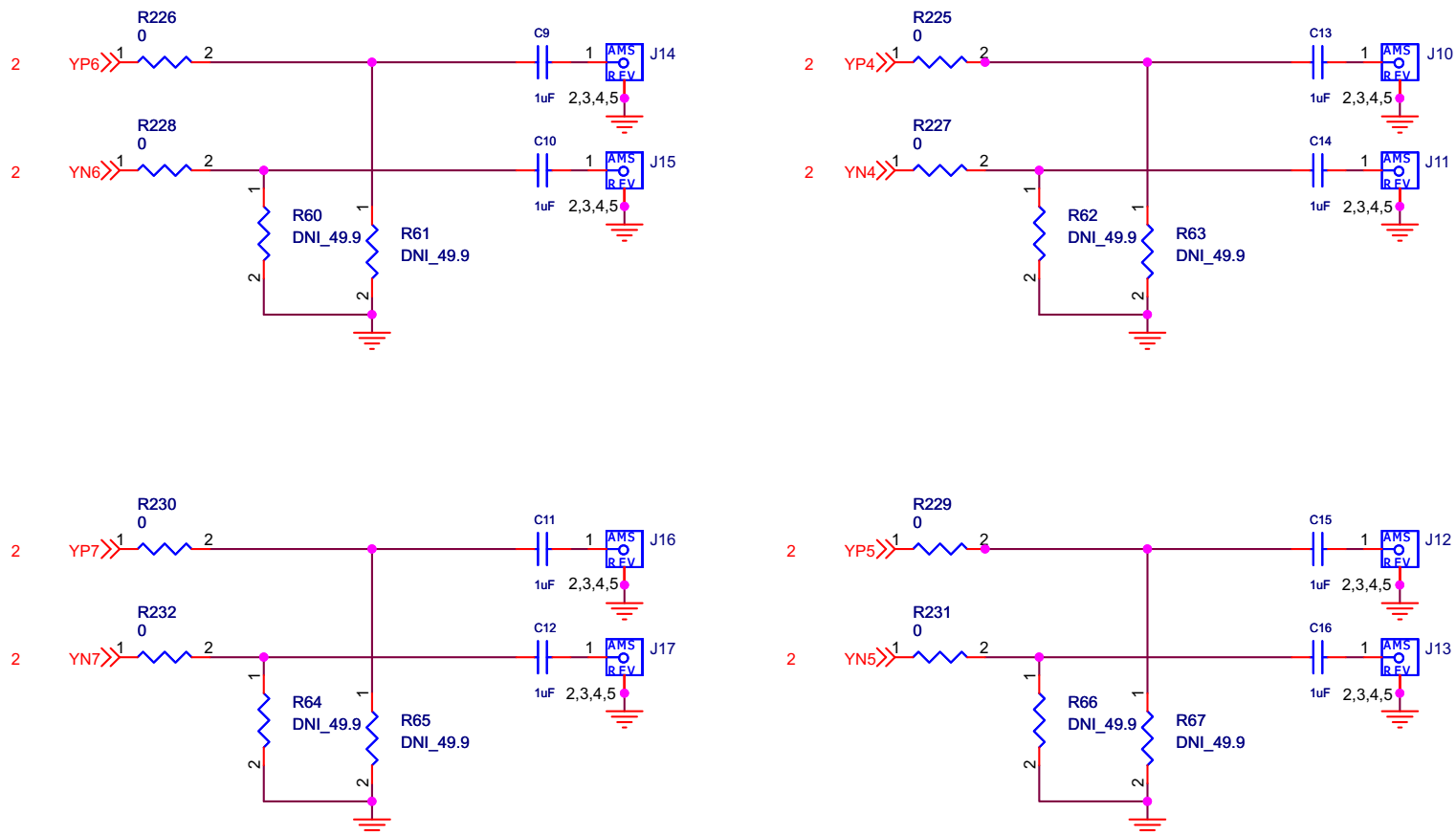


Outputs 0 to 3

Outputs 0 to 3 have option for LP_CML, CML, and HS_CML

Figure 9. CDCM6208V1/CDCM6208V2 EVM Outputs 0 to 3

Outputs 4 to 7



Outputs 4 to 7 have option for HCSL, LVCMOS, LPCML
 For HCSL, install 50 ohm termination resistors and adjust
 series resistor between 0 and 33 ohms to improve ringing.

Figure 10. CDCM6208V1/CDCM6208V2 EVM Outputs 4 to 7

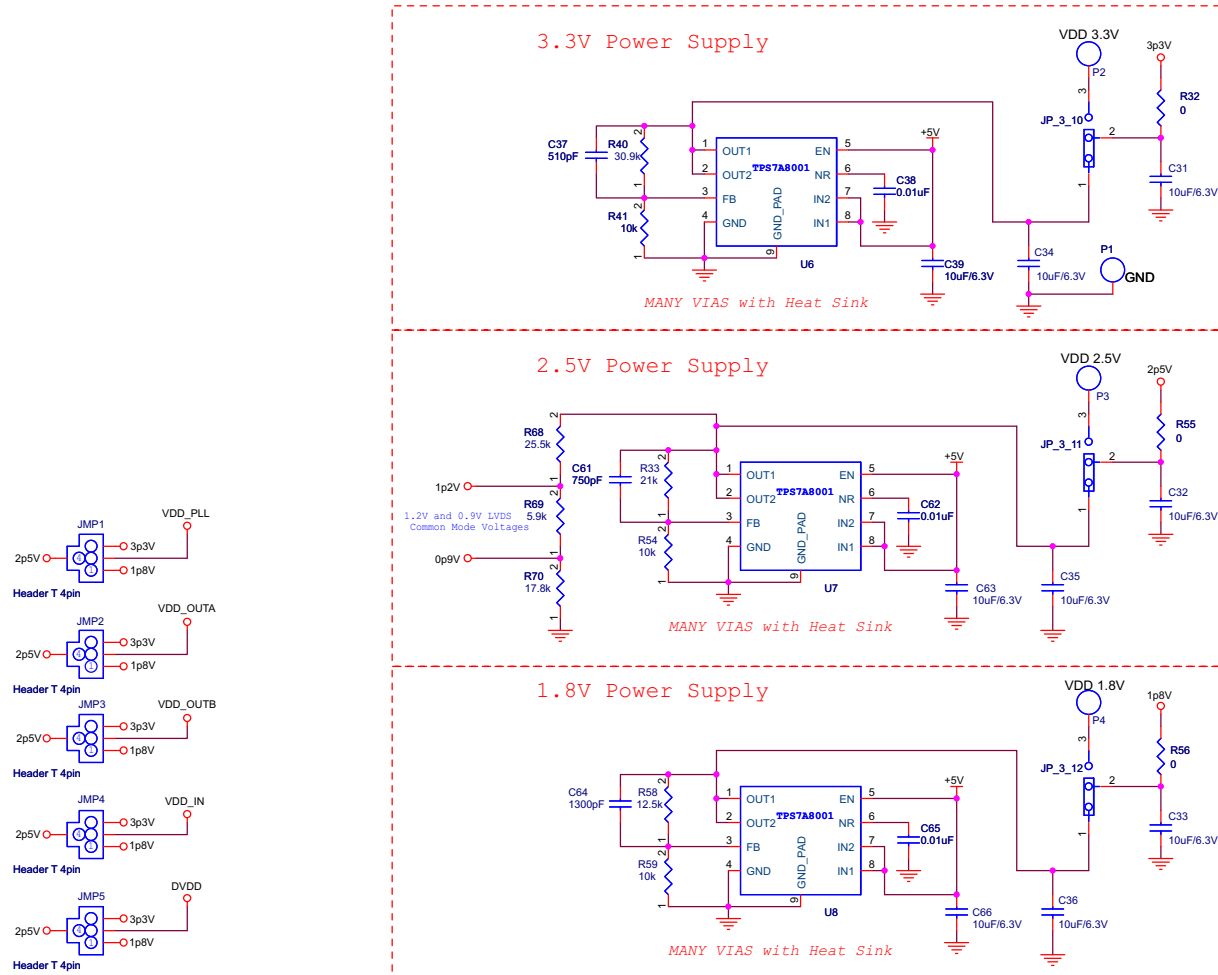


Figure 11. CDCM6208V1/CDCM6208V2 EVM Power Supplies

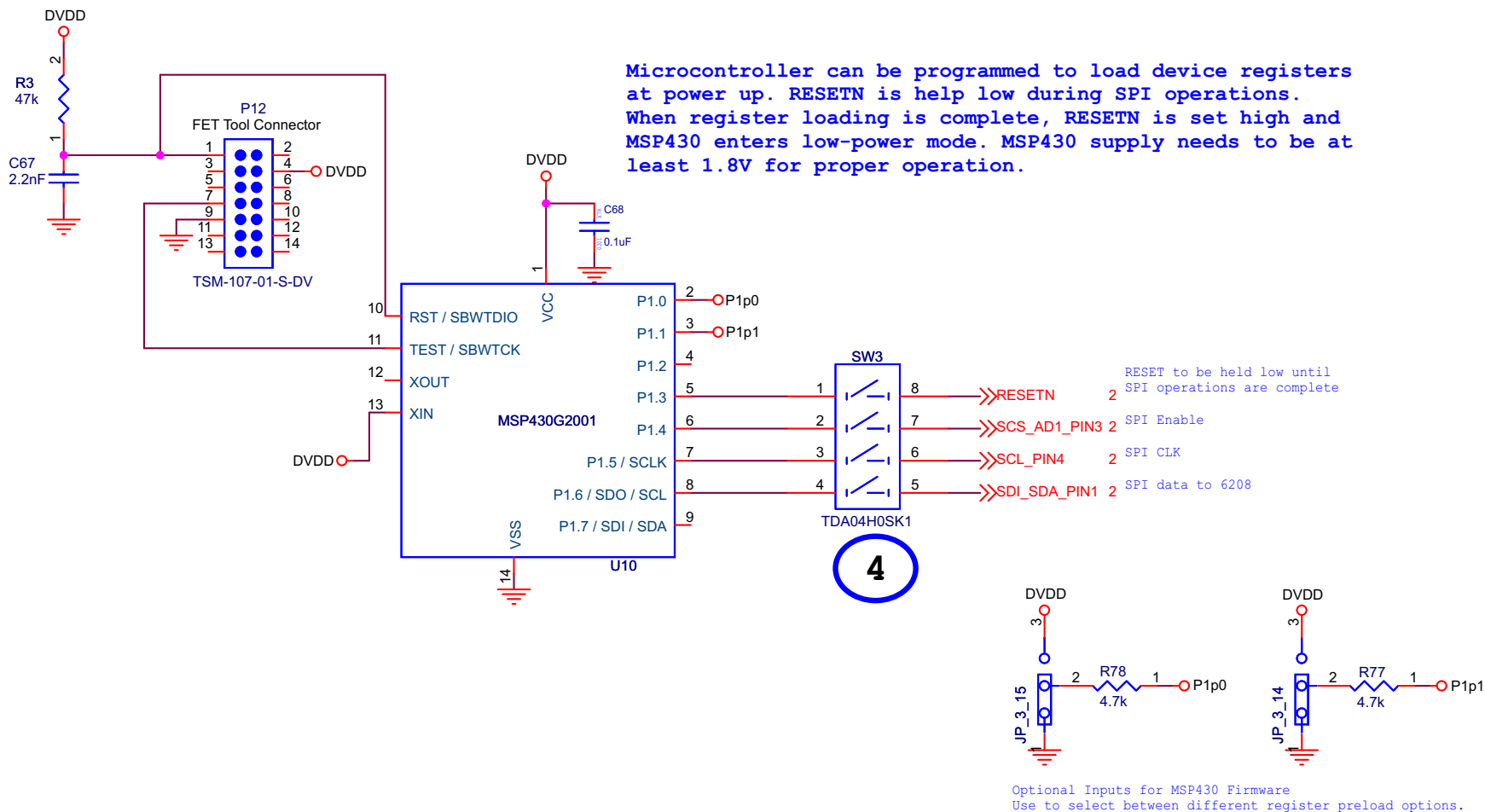


Figure 12. Onboard MSP430G2001

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As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

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