

General Description

The MX875BB0022 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise. The device operates from a 2.5V or 3.3V power supply.

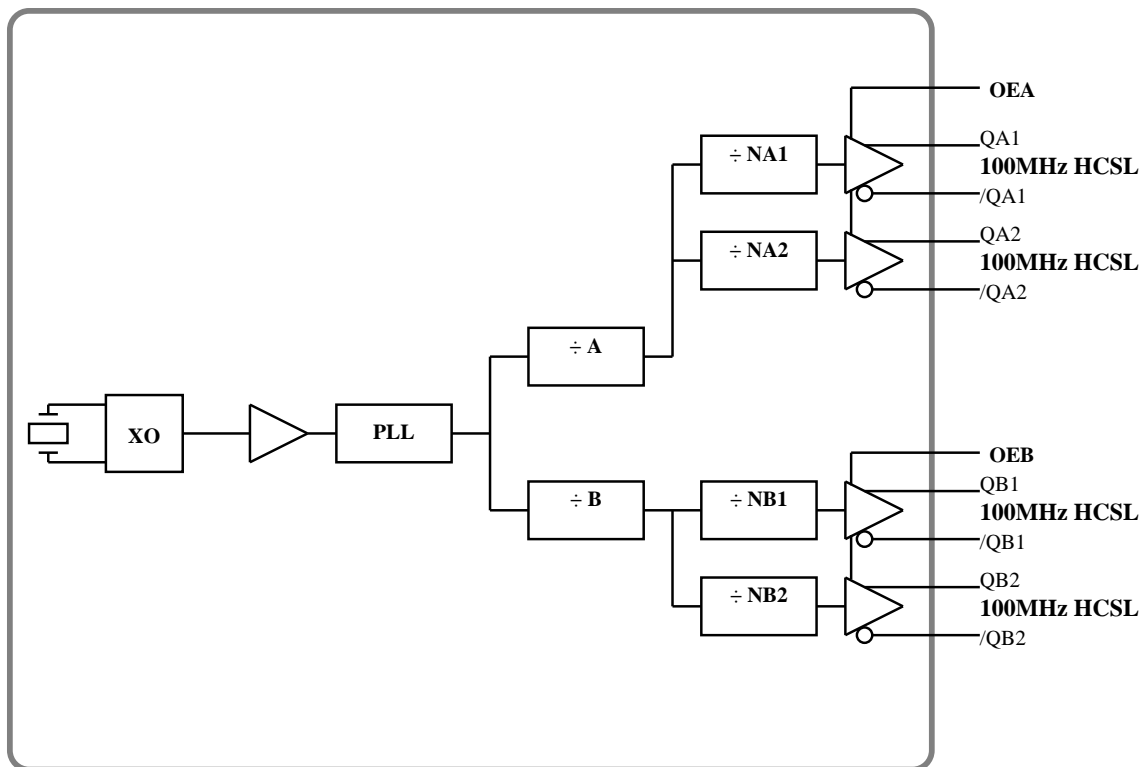
Applications

- PCI Express
- Storage

Features

- Generates 4 output clocks
- Frequency and output logic:
 - 100MHz HCSL x 4
- PCIe Gen 1/2/3/4/5 Compliant
- Integrated Quartz Crystal for Superior Noise/Jitter Performance
- OE on banks A and B
- Typical phase noise:
 - 85fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- 2.5V or 3.3V operating power supply
- Industrial temperature range: -40°C to +85°C
- 48-pin 7x7x1.15mm TQFN

Block Diagram



ClockWorks is a registered trademark of Microchip Technology Inc.

Microchip Technology Inc.

<http://www.microchip.com>

June 10, 2020
MX87-9031-Rev 0.7

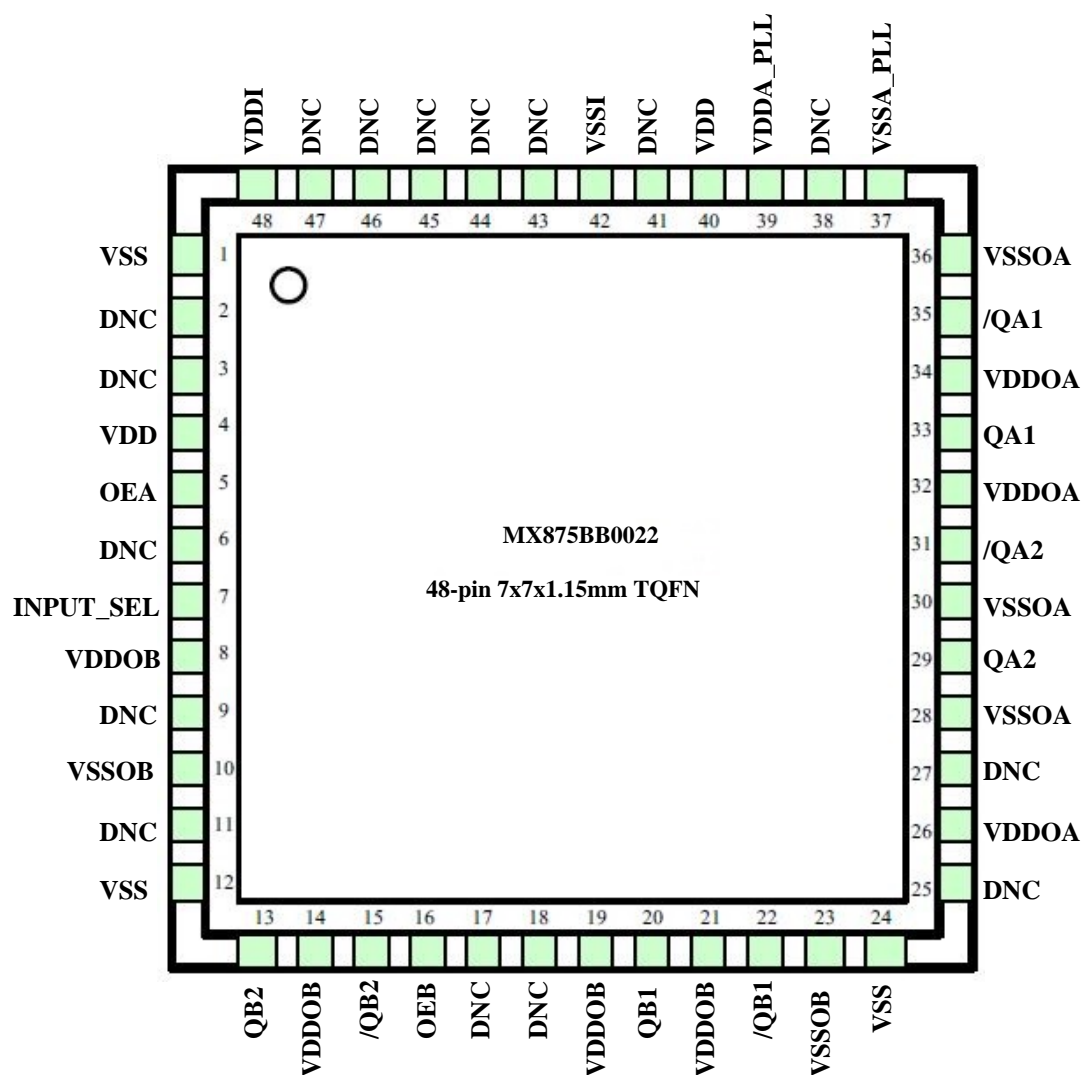
M9999-061020-A
tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking	Shipping	Ambient Temperature Range	Package
MX875BB0022	MX875BB	Tube	-40°C to +85°C	48-pin 7x7x1.15mm TQFN
MX875BB0022 TR	MX875BB	Tape and Reel	-40°C to +85°C	48-pin 7x7x1.15mm TQFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 12, 24	VSS	PWR		Power Supply Ground
2, 3, 6, 38, 41, 44	DNC			Do not connect anything to these pins
4	VDD	PWR		Power Supply
5	OEA	I, SE	LVC MOS	Output Enable, QA outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
7	INPUT_SEL	I, SE	LVC MOS	Internal 75k Ohms Pull-Up 0 = REF_IN, 1 = XTAL
8, 14, 19, 21	VDDOB	PWR		Power Supply for Outputs QB
9, 11	DNC, DNC			Do not connect
10, 23	VSSOB	PWR		Ground Return Path for the Bank B Output Drivers
13, 15	QB2, /QB2	O, Diff	HCSL	Clock Output QB2 Frequency = 100MHz
16	OEB	I, SE	LVC MOS	Output Enable, QB outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
17	DNC			Do not connect
18	DNC			Do not connect
20, 22	QB1, /QB1	O, Diff	HCSL	Clock Output QB1 Frequency = 100MHz
25, 27	DNC, DNC			Do not connect
26, 32, 34	VDDOA	PWR		Power Supply for Outputs QA
28, 30, 36	VSSOA	PWR		Ground Return Path for the Bank A Output Drivers
29, 31	QA2, /QA2	O, Diff	HCSL	Clock Output QA2 Frequency = 100MHz
33, 35	QA1, /QA1	O, Diff	HCSL	Clock Output QA1 Frequency = 100MHz
37	VSSA_PLL	PWR		Analog Power Return for PLL
39	VDDA_PLL	PWR		Analog Power Supply for PLL
40	VDD	PWR		Power Supply
42	VSSI	PWR		Ground for Reference Input Circuits and Crystal Oscillator
43, 45	DNC			Do not connect
46, 47	DNC			Do not connect
48	VDDI	PWR		Power Supply for Reference Input Circuits and Crystal Oscillator

Absolute Maximum Ratings¹

Supply Voltage (VDD, VDDA, VDDI, VDDO).....+4.6V
 Input Voltage (VIN).....-0.50V to +4.6V
 ESD Machine Model.....200V
 ESD Human Body Model.....2kV

Operating Ratings²

Supply Voltage (VDD, VDDO)....+2.375V to +3.465V

Electrical Characteristics

Typical values are TA = 25°C, min/max across -40°C <= TA <= +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDD, VDDO	Supply Voltage	2.5V Operation 3.3V Operation	2.375 3.135	2.5 3.3	2.625 3.465	V
VDDI	Analog & I/O Supply		2.375		3.465	V
VDDA	PLL Core		2.375		3.465	V
IDDA	PLL Core Current Consumption				60	mA
IDDI	Analog & I/O Current				20	mA
IDDO	Output Stage Current Consumption	Per output bank, unloaded			70	mA
IDD	SPI and Miscellaneous Logic				8	mA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

HCSL DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V \pm 5% or 2.5V \pm 5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 50 Ohms to VSS.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage		660	700	850	mV
VOL	Output Low Voltage		-150	0	27	mV
Vcross	Crossing Point Voltage			350		V

AC Electrical Characteristics

VDD = VDDO½ = 3.3V ±5% or 2.5V ±5%

VDD = 3.3V ±5%, VDDO½ = 3.3V ±5% or 2.5V ±5%

TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FOUT	Output Frequency	HCSL		100 x 4		MHz
TR/TF	Output Rise/Fall time ³	HCSL output	175	200	400	ps
ODC	Output Duty Cycle	<400MHz output frequencies	48	50	52	%
Tpd	Input-to-Input Propagation Delay	ZDB mode Generator/Bypass mode	-100	4	100	ps ns
Tskew	Output-to-Output Skew	Notes 4, 5 Same output bank			50	ps
Tlock	PLL Lock Time			5	20	ms
Tjit(Ø)	RMS Phase Noise	Notes 6, 7 Integration range (12kHz-20MHz)		85		fs

Temperature Specifications

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	Ta	-40		+85	°C	
Lead Temperature				+260	°C	Soldering, 20s
Case Temperature				+115	°C	
Storage Temperature Range	Ts	-65		+150	°C	
Package Thermal Resistances (Note 8)						
Junction Thermal Resistance, 7 x 7 TQFN-48Ld	Tja		26		°C/W	

Notes:

- See Figure 'All Outputs Rise/Fall Time'
- Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.
- Output-to-output skew is only defined for outputs in the same PLL bank [A:B] with the same output logic type setting.
- All phase noise measurements were taken with an Agilent 5052B phase noise system.
- If using an external reference input, use a low phase noise source as the phase noise will follow the input source phase noise up to about 1MHz. reference input, use a low phase noise source. The output phase noise will follow the input source phase noise up to about 1.5 MHz.
- The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., TA, TJ, Tja). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Filtering Recommendations

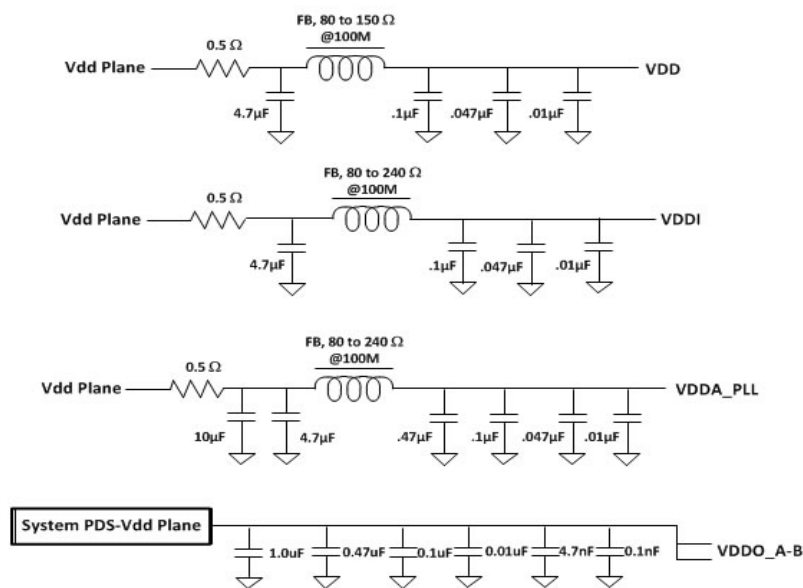


Figure 1. Recommended Power Supply Filtering

- Use the power supply filtering shown in above figure for VDD, VDDA_PLL, VDDI.
- Connect the VDDO pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 80 Ohms to 240 Ohms @100MHz impedance and >250mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Microchip's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in below figure and can be used for any of the above VDD sections.
- Do not use Y5V or Z5U capacitors.

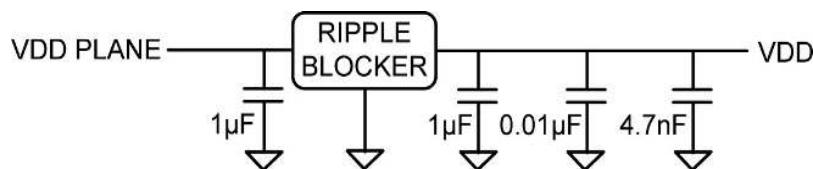


Figure 2. Power Supply Filtering with Ripple Blocker

Timing Diagrams

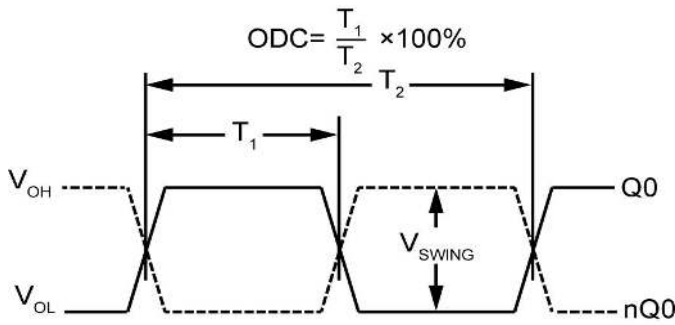


Figure 3. Duty Cycle Timing

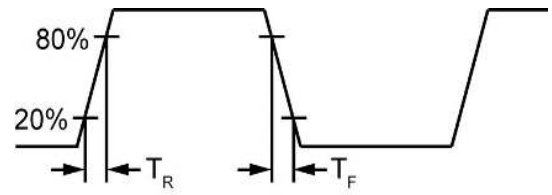


Figure 4. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

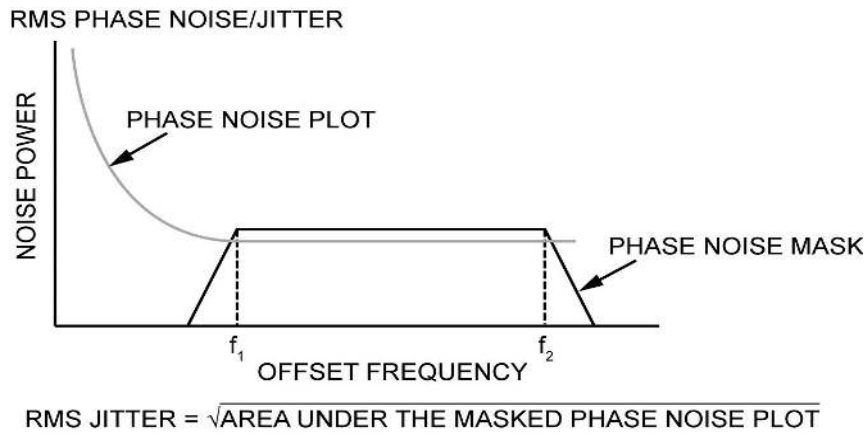


Figure 5. RMS Phase/Noise/Jitter

Crystal Input Interface

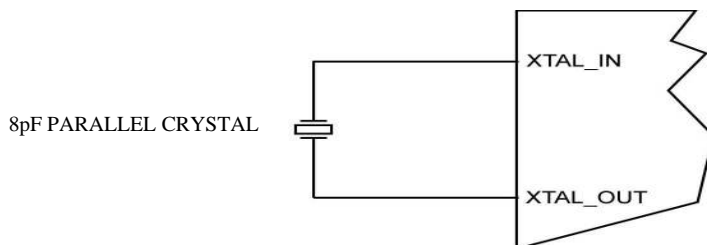


Figure 6. Crystal Input Interface

Output Termination

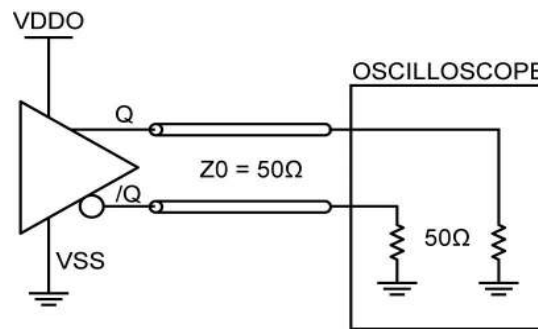


Figure 7. HCSL Output Load and Test Circuit

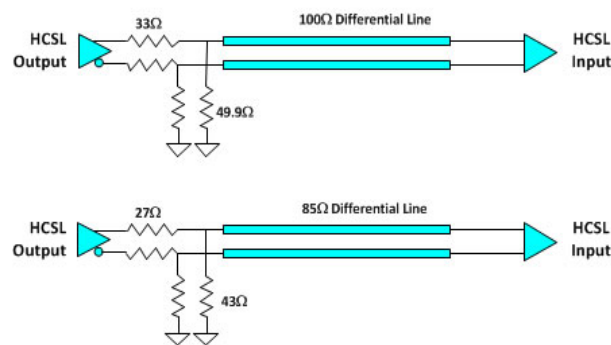
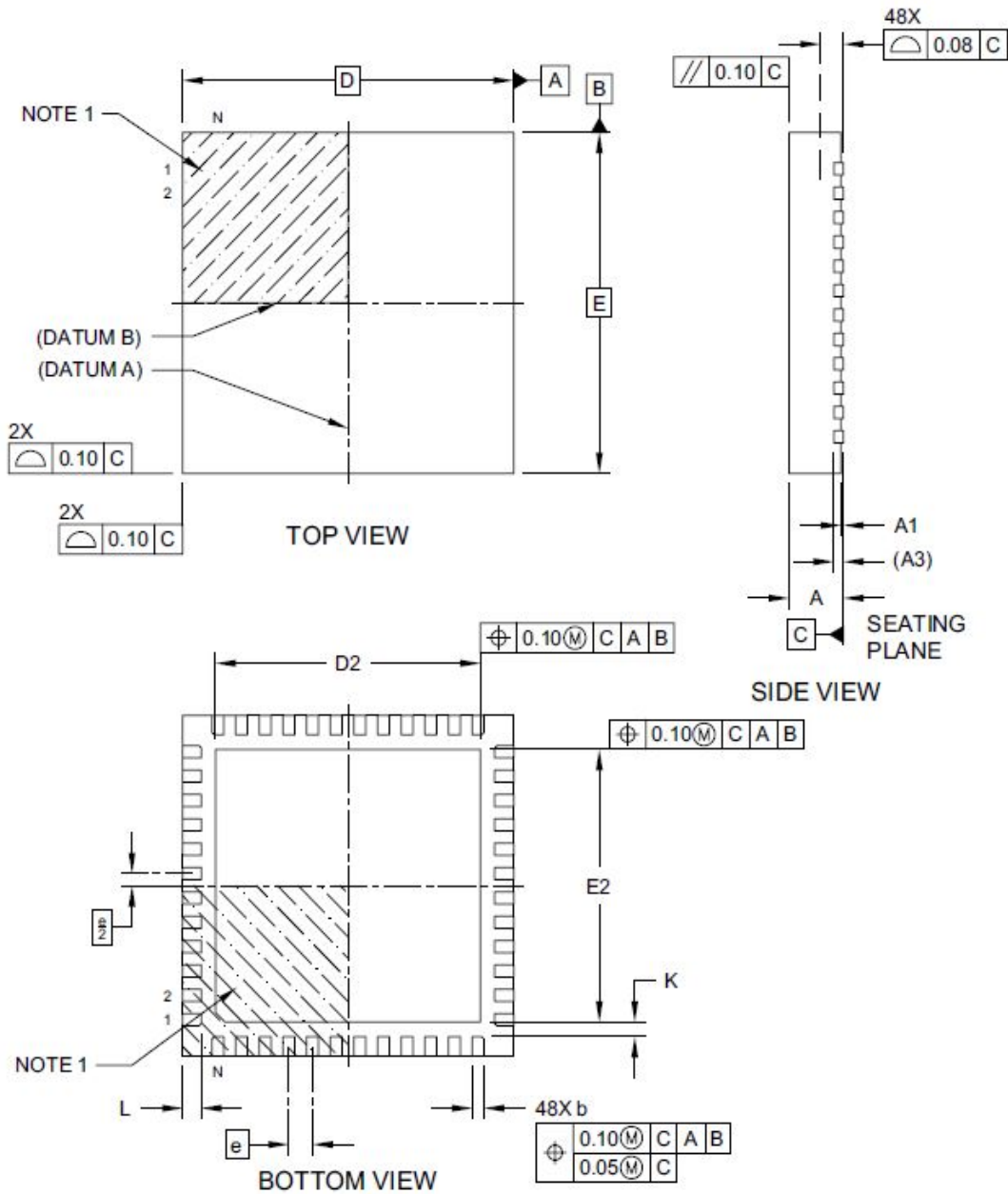


Figure 8. Recommended HCSL Output Termination Circuit

Packaging Information

48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

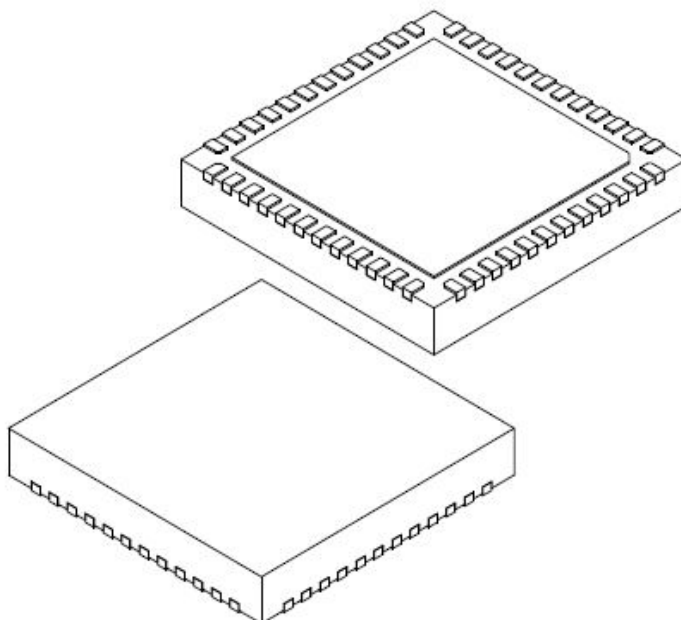
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-466 Rev A Sheet 1 of 2

48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	48		
Pitch	e	0.50 BSC		
Overall Height	A	1.05	1.10	1.15
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	7.00 BSC		
Exposed Pad Length	D2	5.50	5.60	5.70
Overall Width	E	7.00 BSC		
Exposed Pad Width	E2	5.50	5.60	5.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

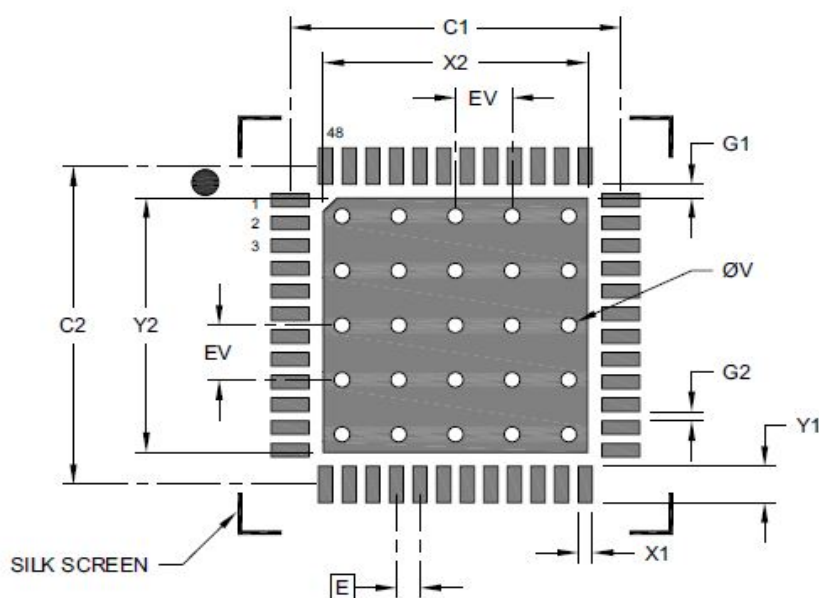
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-466 Rev A Sheet 1 of 2

48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			5.60
Center Pad Length	Y2			5.60
Contact Pad Spacing	C1		7.00	
Contact Pad Spacing	C2		7.00	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.80
Contact Pad to Center Pad (X48)	G1	0.20		
Contact Pad to Contact Pad (X44)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2466 Rev A

Microchip makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Microchip does not assume responsibility for its use. Microchip reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Microchip's terms and conditions of sale for such products, Microchip assumes no liability whatsoever, and Microchip disclaims any express or implied warranty relating to the sale and/or use of Microchip products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Microchip products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Microchip Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Microchip for any damages resulting from such use or sale.

© 2020 Microchip Technology Inc.