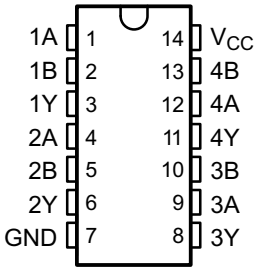
# QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

Check for Samples: SN54AHC86, SN74AHC86

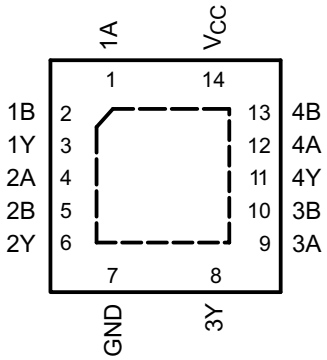
## FEATURES

- Operating Range 2-V to 5.5-V $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

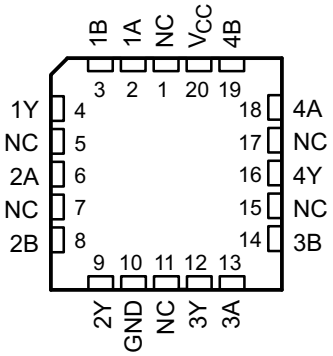
SN54AHC86 . . . J OR W PACKAGE
SN74AHC86 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)




SN74AHC86 . . . RGY PACKAGE
(TOP VIEW)




SN54AHC86 . . . FK PACKAGE
(TOP VIEW)




NC − No internal connection

## DESCRIPTION

The ’AHC86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

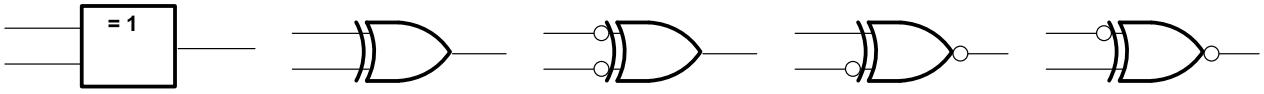
**FUNCTION TABLE**
**(EACH GATE)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

## EXCLUSIVE–OR LOGIC

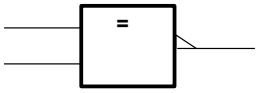
An exclusive-OR gate has many applications, some of which can be represented better by alternativelogic symbols.

**EXCLUSIVE OR**



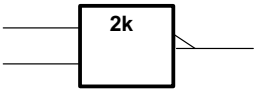

These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



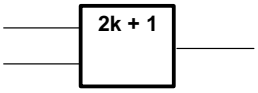

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage range, $V_{CC}$ | | –0.5 to 7 | V |
| Input voltage range, $V_I$(2) | | –0.5 to 7 | V |
| Output voltage range, $V_O$(2) | | –0.5 to $V_{CC}$ + 0.5 | V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | | –20 | mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| Continuous current through $V_{CC}$ or GND | | ±50 | mA |
| Package thermal impedance, $\theta_{JA}$ | D package(3) | 86 | °C/W |
| | DB package(3) | 96 | |
| | DGV package(3) | 127 | |
| | N package(3) | 80 | |
| | NS package(3) | 76 | |
| | PW package(3) | 113 | |
| | RGY package(4) | 47 | |
| Storage temperature range, $T_{stg}$ | | –65 to 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) The package thermal impedance is calculated in accordance with JESD 51-5

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | SN54AHC86 | | SN74AHC86 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$= 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$= 3V | 2.1 | | 2.1 | | |
| | | $V_{CC}$= 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level Input voltage | $V_{CC}$= 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$= 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$= 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$= 2 V | | –50 | | –50 | mA |
| | | $V_{CC}$= 3.3 V ± 0.3 V | | –4 | | –4 | |
| | | $V_{CC}$= 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$= 2 V | | 50 | | 50 | mA |
| | | $V_{CC}$= 3.3 V ± 0.3 V | | 4 | | 4 | |
| | | $V_{CC}$= 5 V ± 0.5 V | | 8 | | 8 | |
| Δt/Δv | Input Transition rise or fall rate | $V_{CC}$= 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$= 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | SN54AHC86 | | SN74AHC86 | | Recommended SN74AHC86 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OH}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | | 0.5 | |
| | $I_{OH}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | | 0.5 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 (1) | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | | 20 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | SN54AHC86 | | SN74AHC86 | | Recommended SN74AHC86 | | |
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | 7 (1) | 11 (1) | 1 (1) | 13 (1) | 1 | 13 | 1 | 13 | ns |
| $t_{PHL}$ | | | | 7 (1) | 11 (1) | 1 (1) | 13 (1) | 1 | 13 | 1 | 13 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | 1 | 16.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | SN54AHC86 | | SN74AHC86 | | Recommended SN74AHC86 | | |
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | 4.8 (1) | 6.8 (1) | 1 (1) | 8 (1) | 1 | 8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | 4.8 (1) | 6.8 (1) | 1 (1) | 8 (1) | 1 | 8 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | 6.3 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$ | | | | 6.3 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## NOISE CHARACTERISTICS

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | | SN74AHC86 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

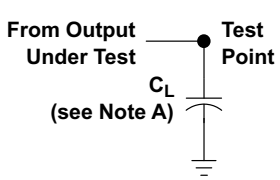
(1) Characteristics are for surface-mount packages only.

## OPERATING CHARACTERISTICS

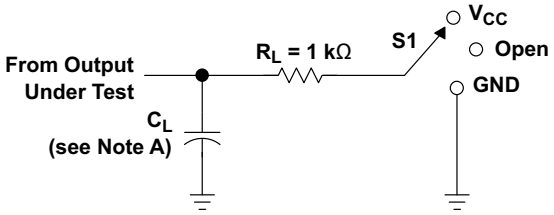
$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION

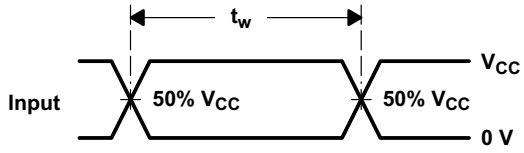



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

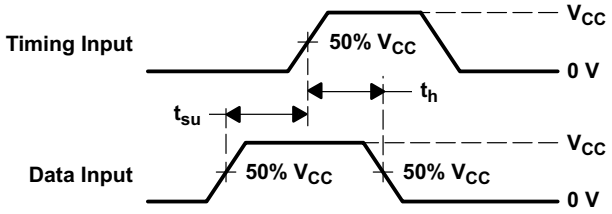



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

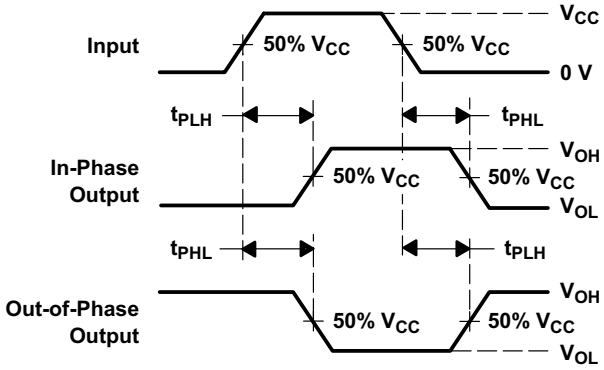
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



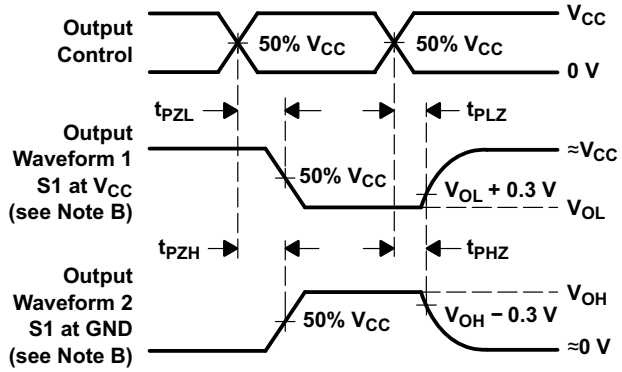

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## REVISION HISTORY

**Changes from Revision I (July 2003) to Revision J** **Page**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9681601Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9681601Q2A SNJ54AHC86FK | Samples |
| 5962-9681601QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681601QCA SNJ54AHC86J | Samples |
| 5962-9681601QDA | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681601QDA SNJ54AHC86W | Samples |
| SN74AHC86D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC86 | Samples |
| SN74AHC86DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA86 | Samples |
| SN74AHC86DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA86 | Samples |
| SN74AHC86DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC86 | Samples |
| SN74AHC86N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHC86N | Samples |
| SN74AHC86NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC86 | Samples |
| SN74AHC86PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA86 | Samples |
| SN74AHC86PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA86 | Samples |
| SN74AHC86PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA86 | Samples |
| SN74AHC86RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HA86 | Samples |
| SNJ54AHC86FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9681601Q2A SNJ54AHC86FK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54AHC86J | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681601QC A SNJ54AHC86J | Samples |
| SNJ54AHC86W | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681601QD A SNJ54AHC86W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

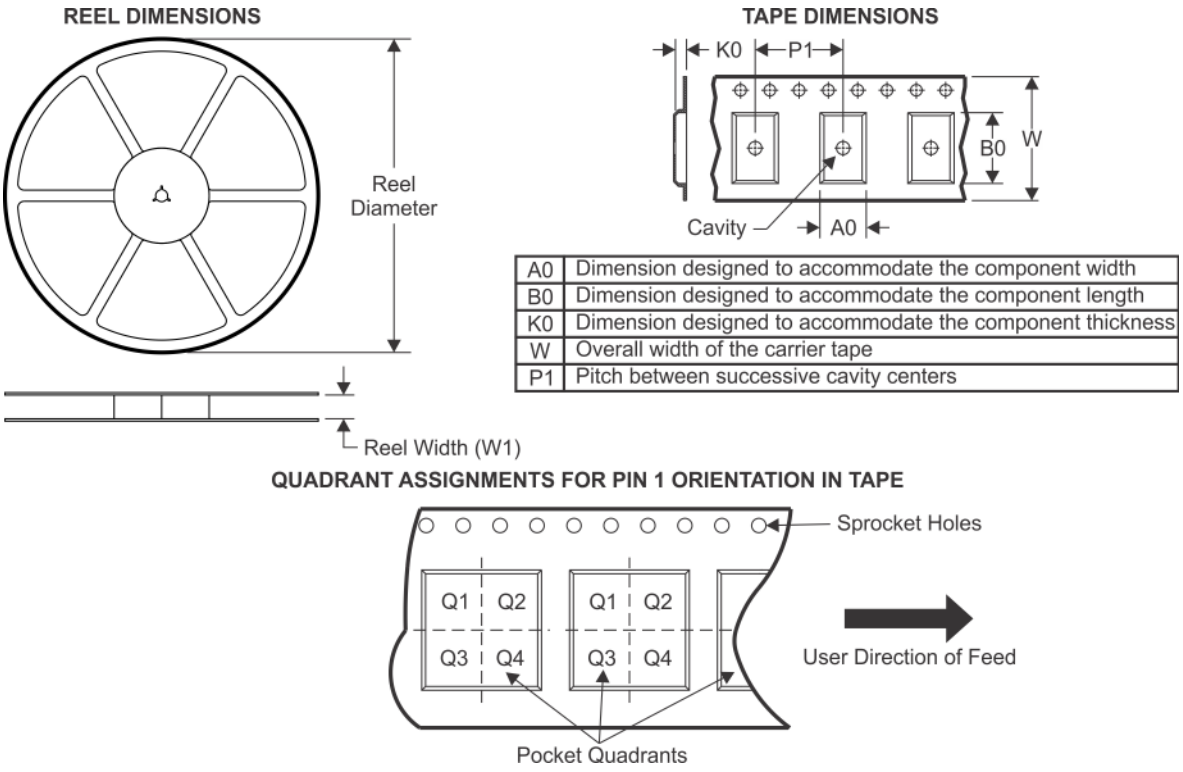
**OTHER QUALIFIED VERSIONS OF SN54AHC86, SN74AHC86 :**

- Catalog: SN74AHC86
- Military: SN54AHC86

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

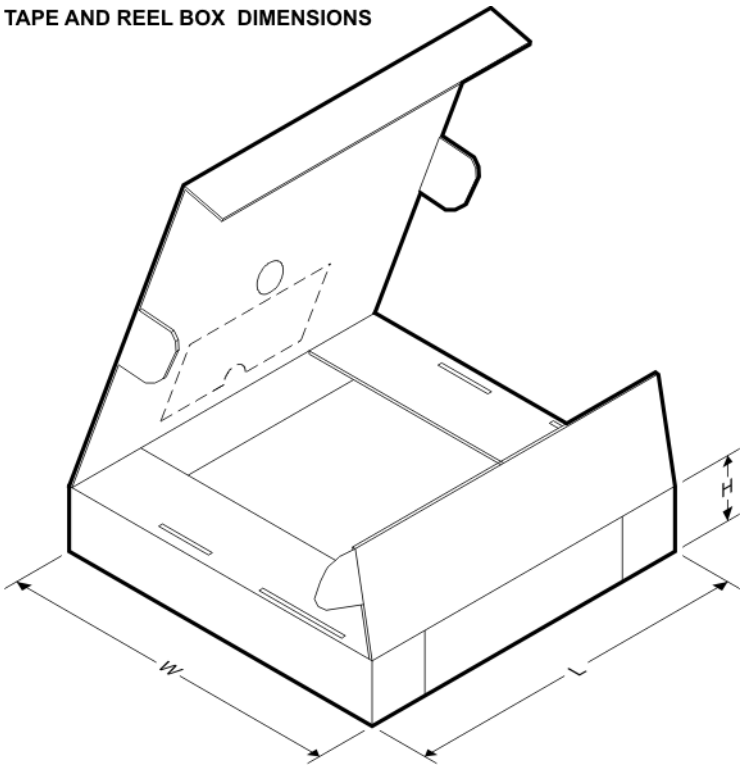



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC86DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC86DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHC86NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC86PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC86RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

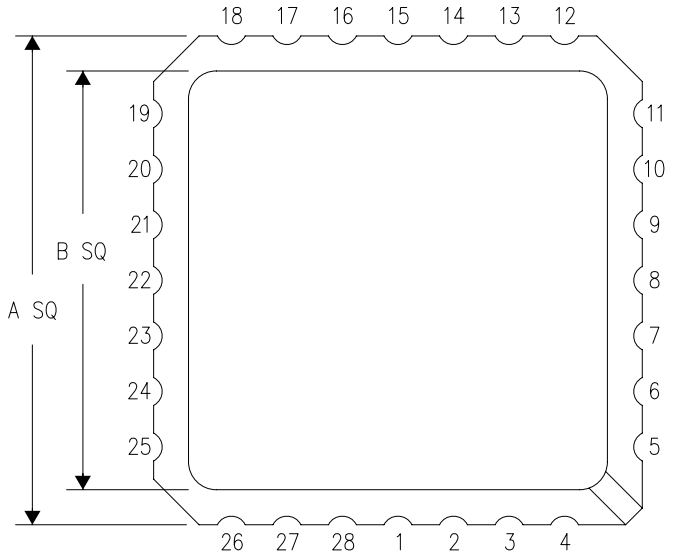



*All dimensions are nominal

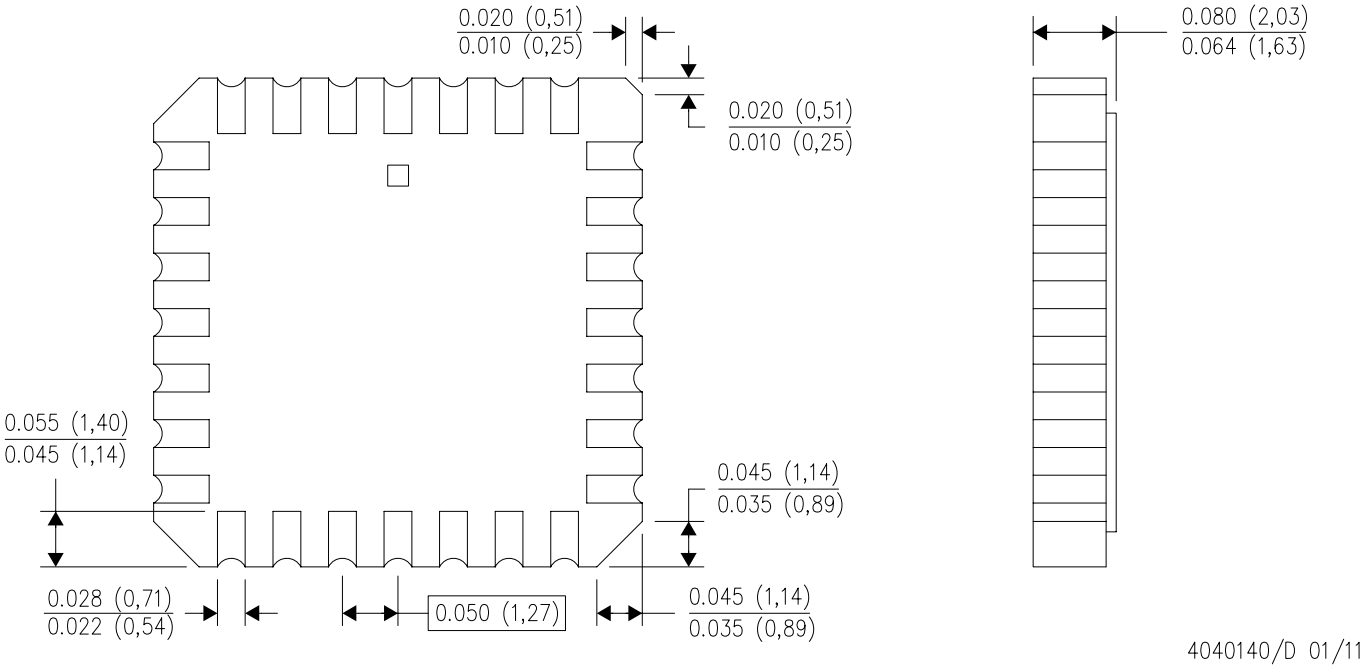
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC86DGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHC86DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74AHC86NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHC86PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHC86RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



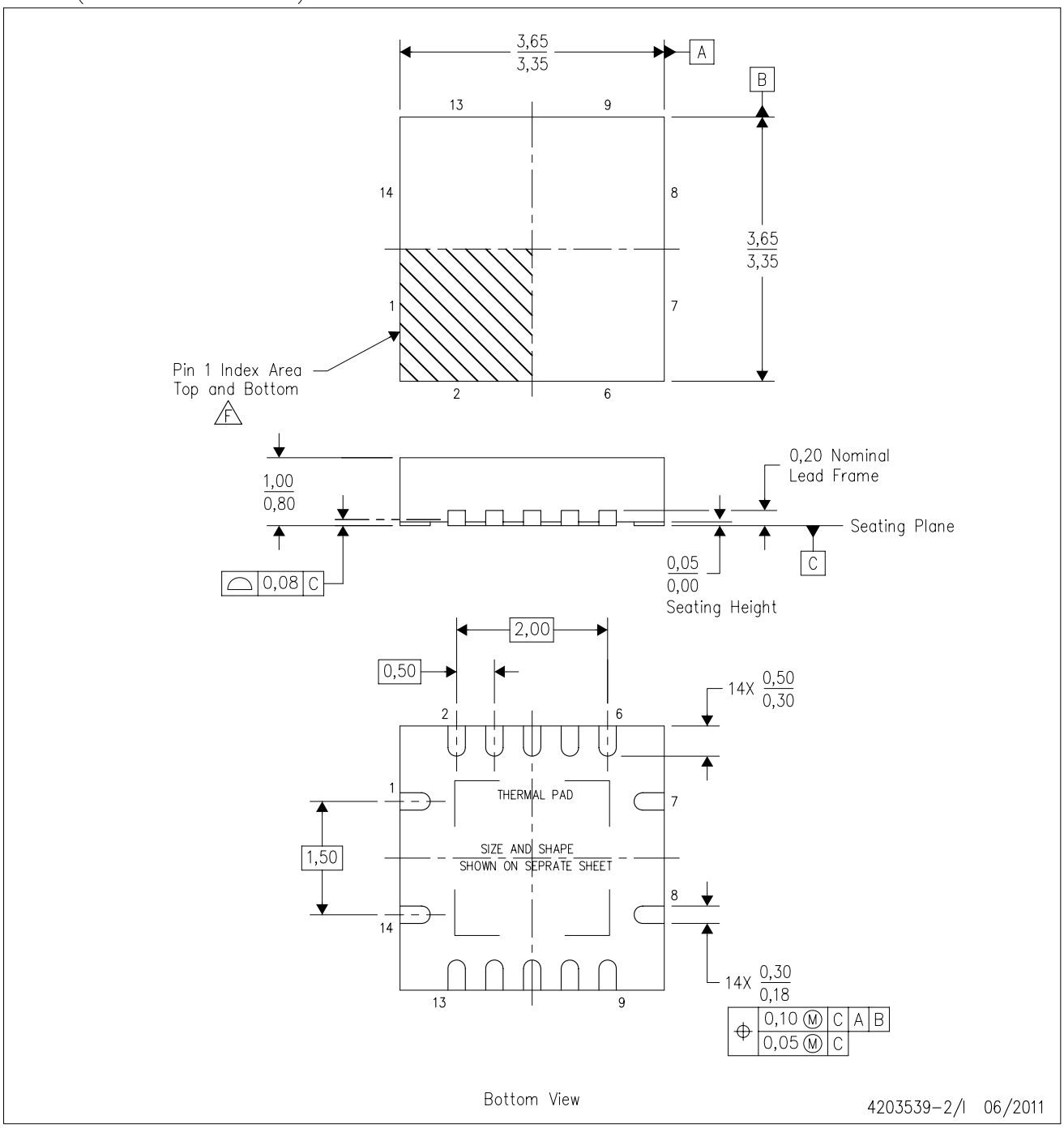

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

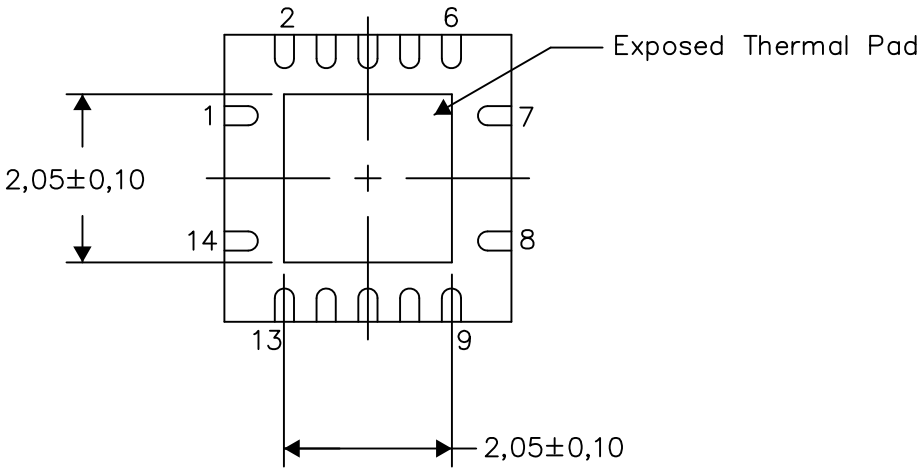
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



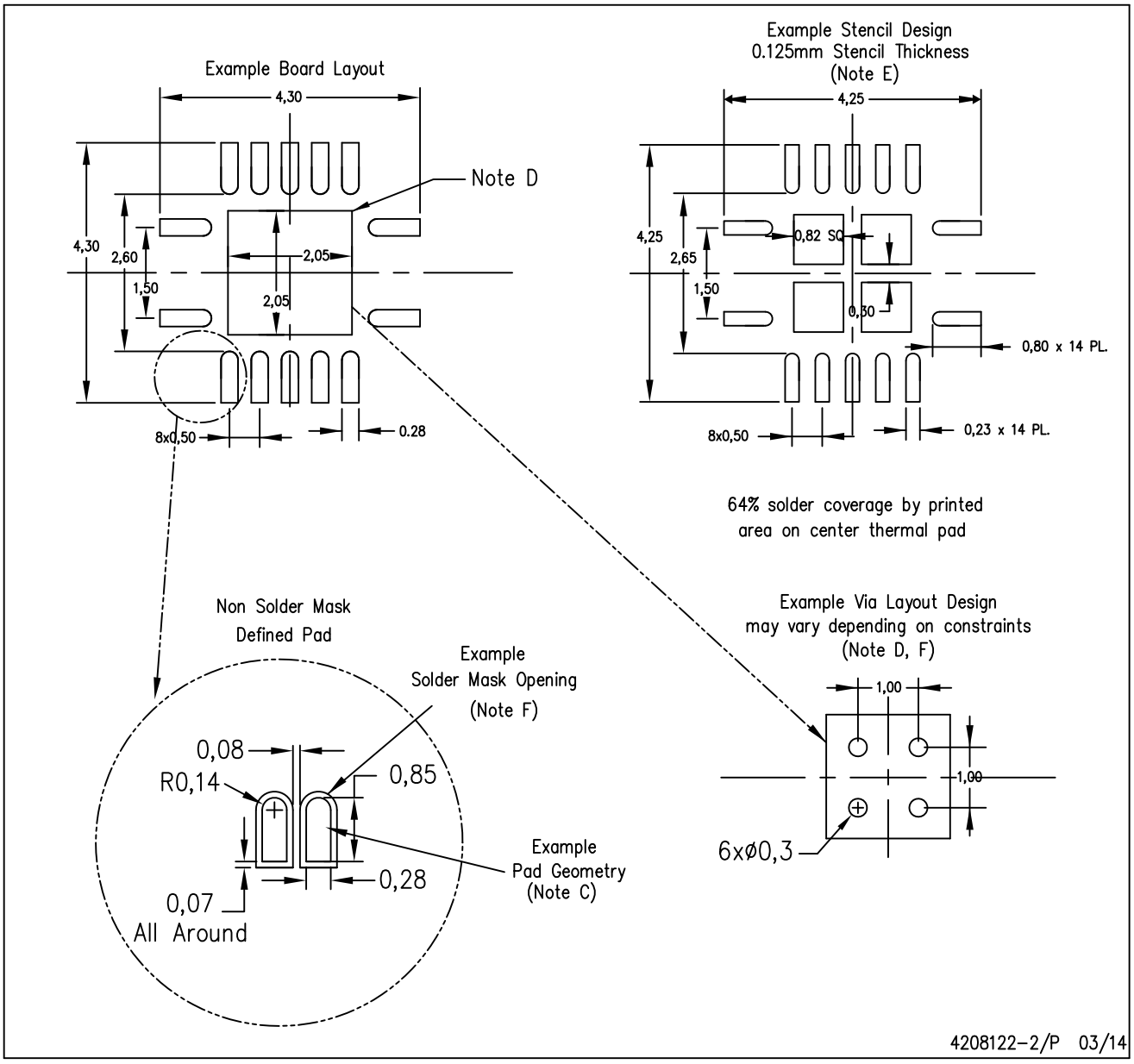

Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

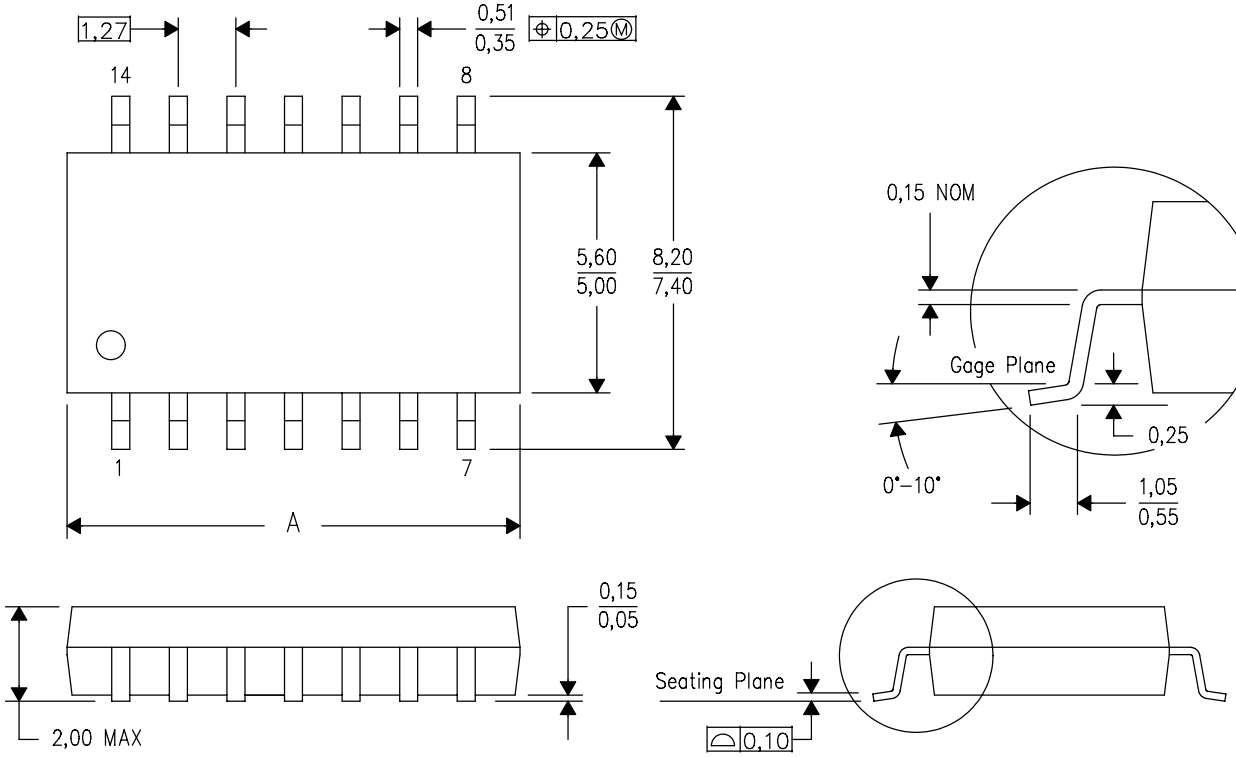



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

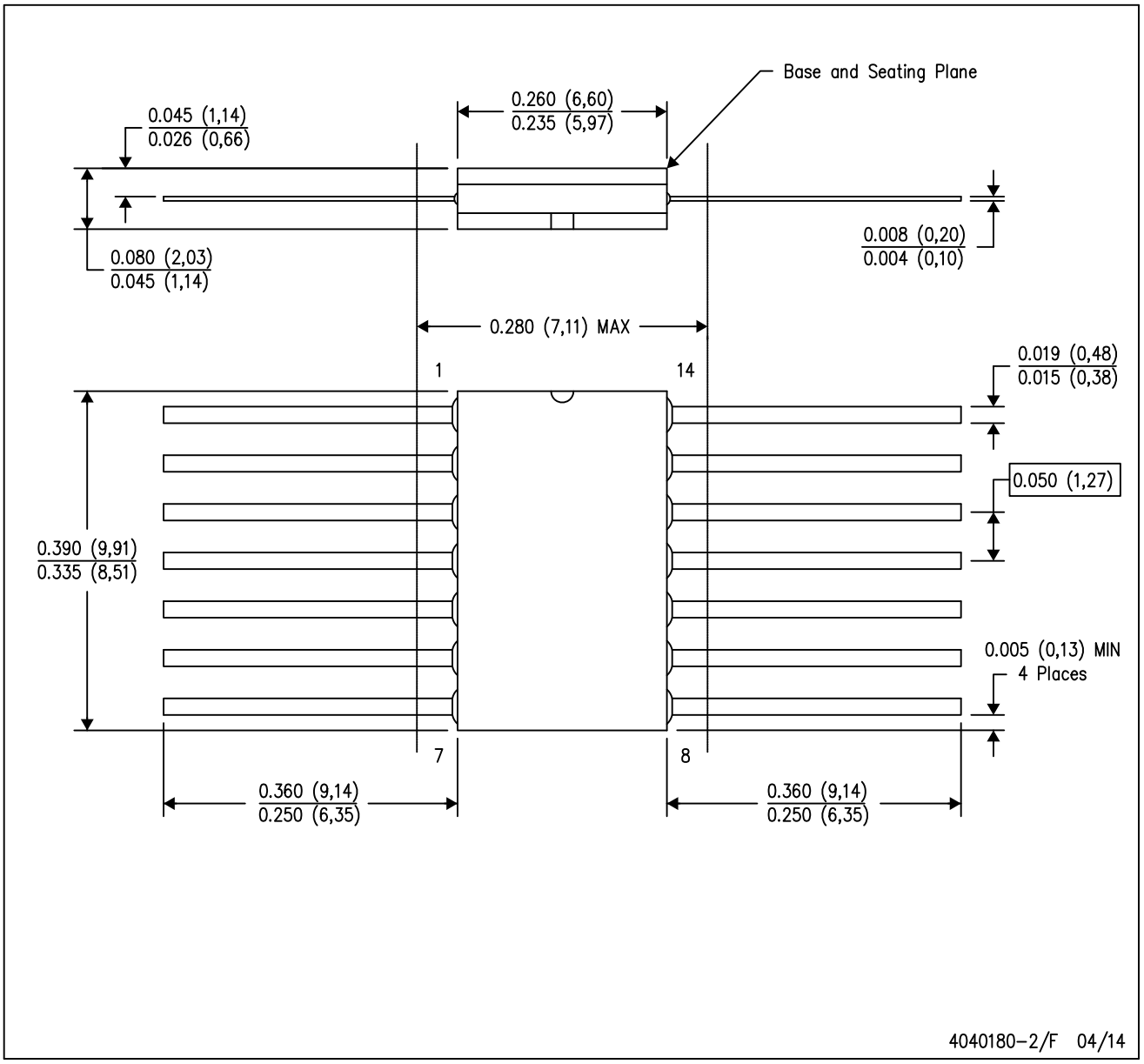



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

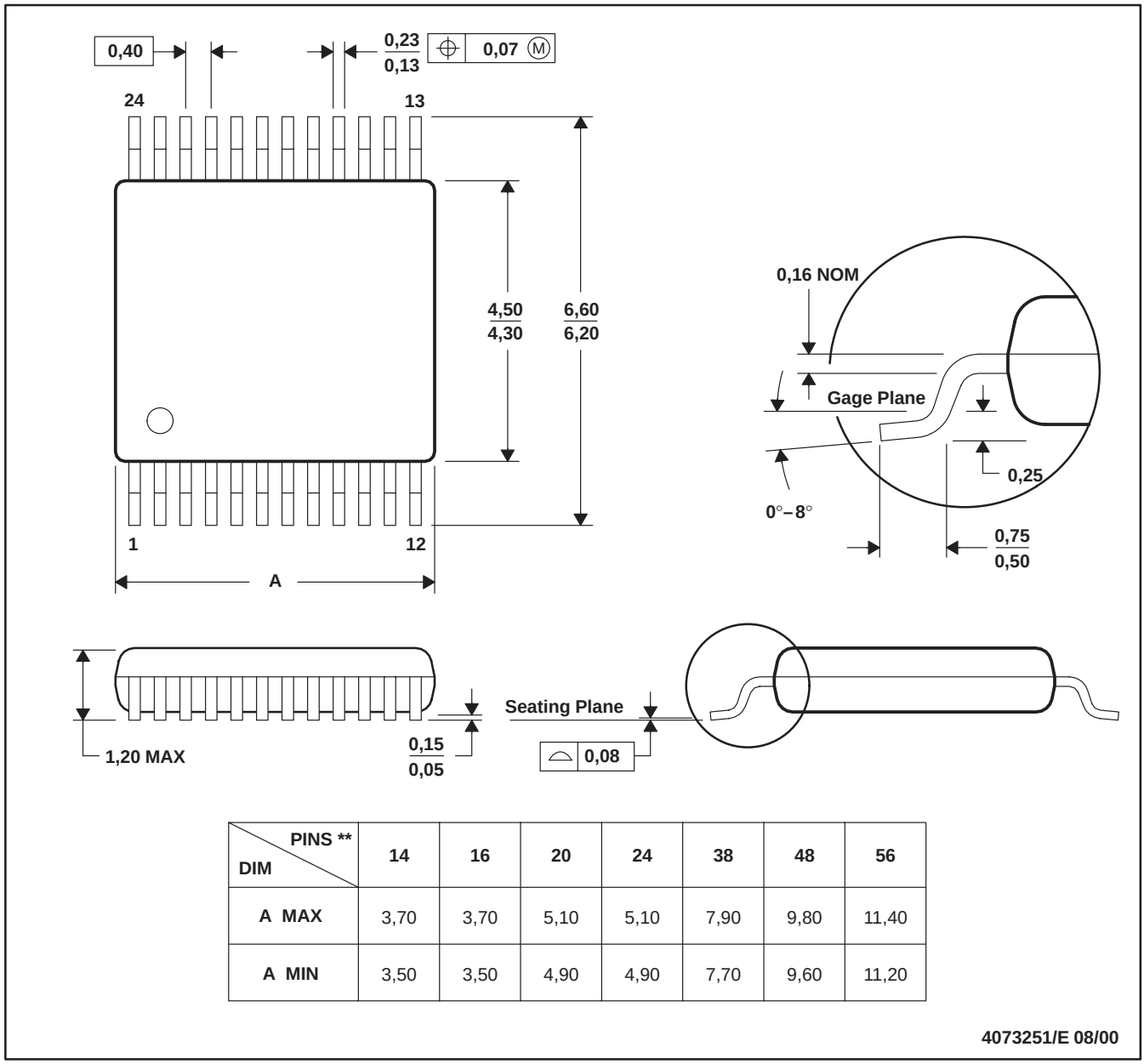



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

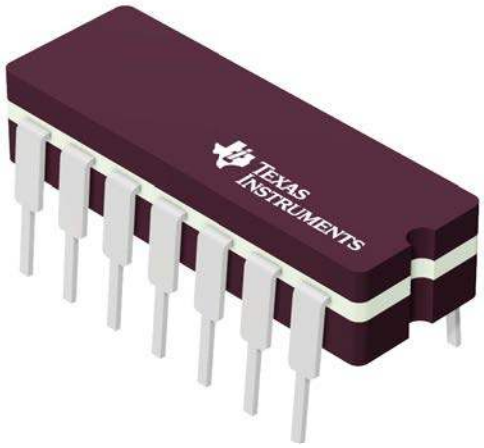
**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

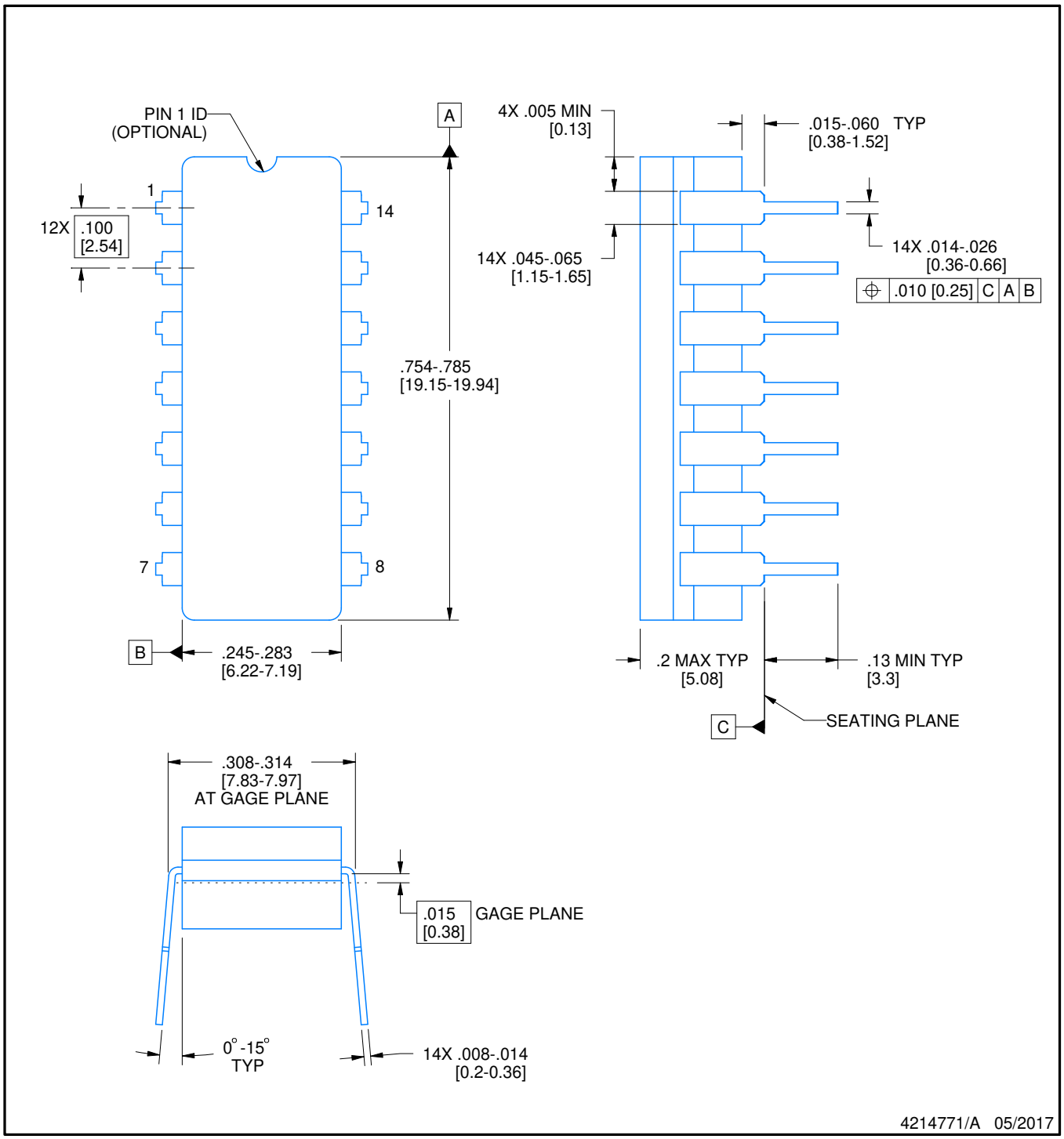
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

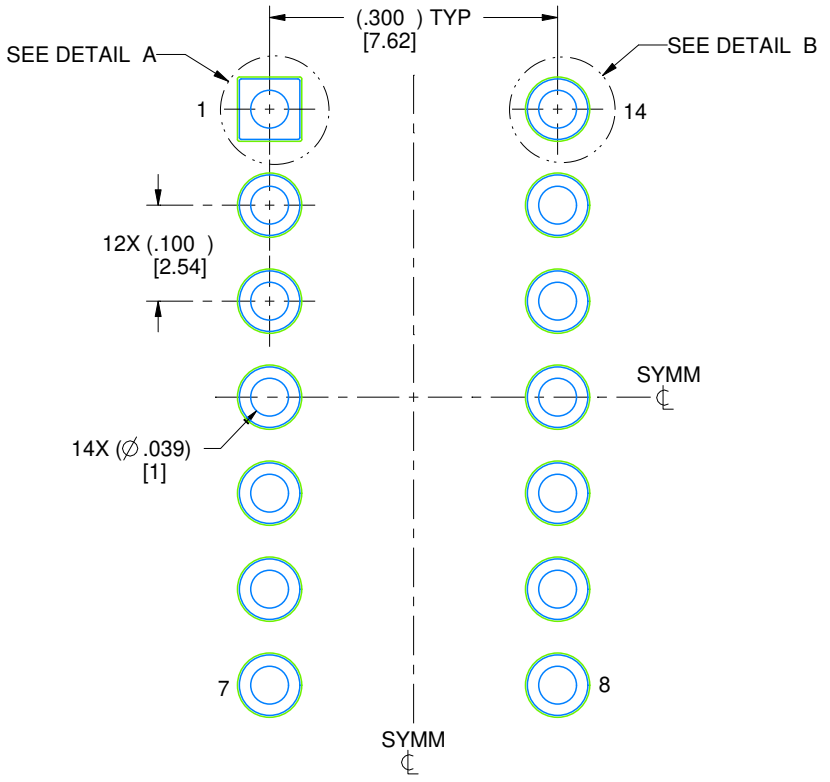
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

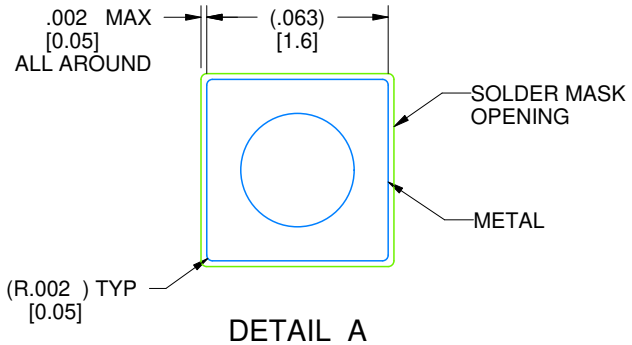
## J0014A

## CDIP - 5.08 mm max height

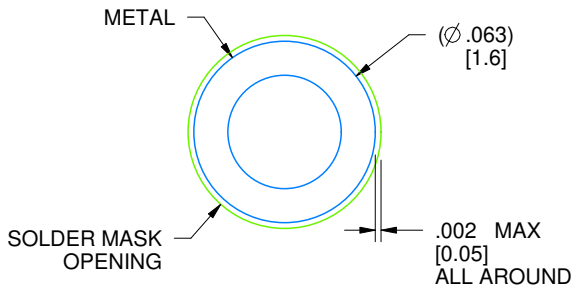
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



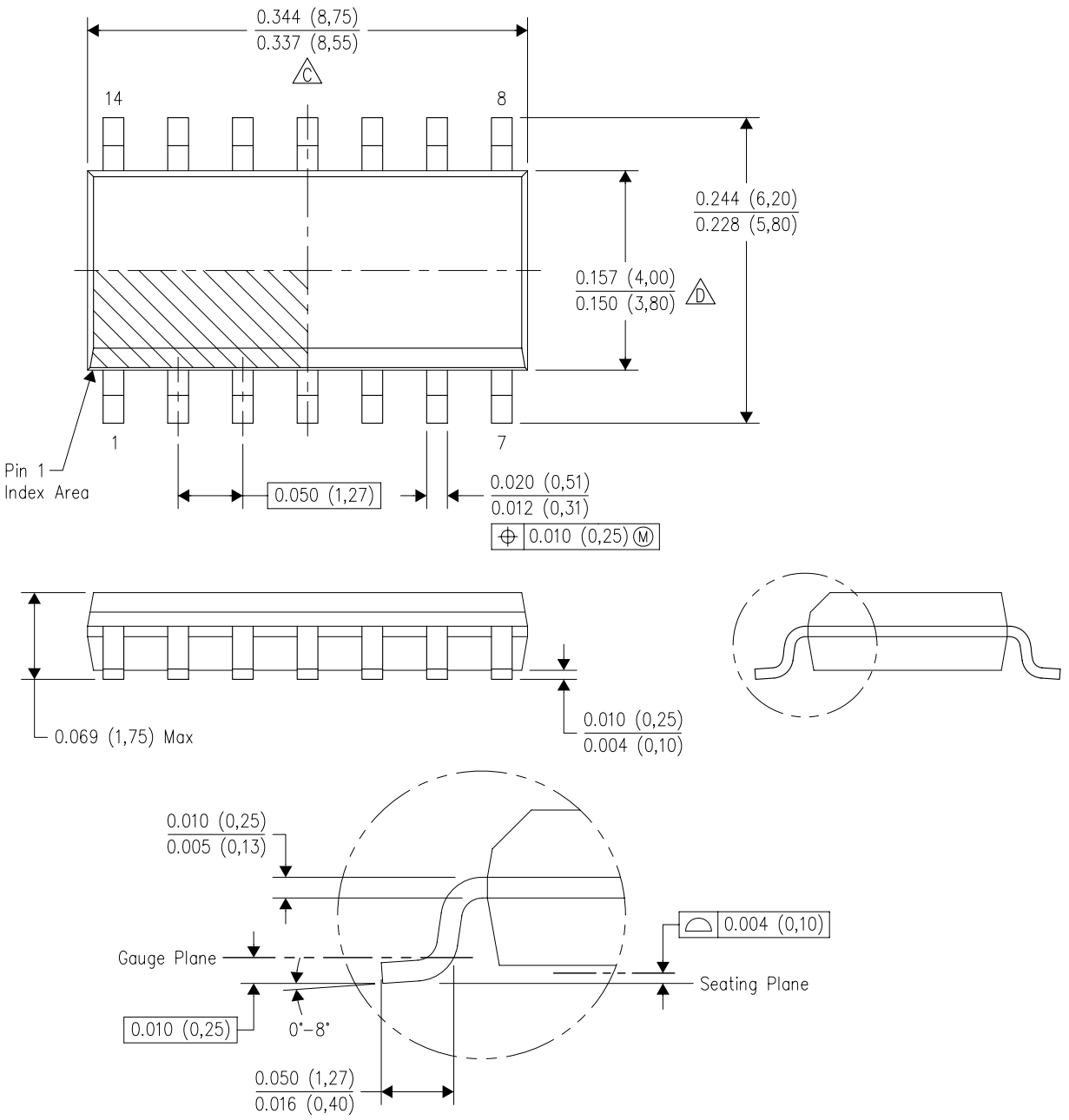

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

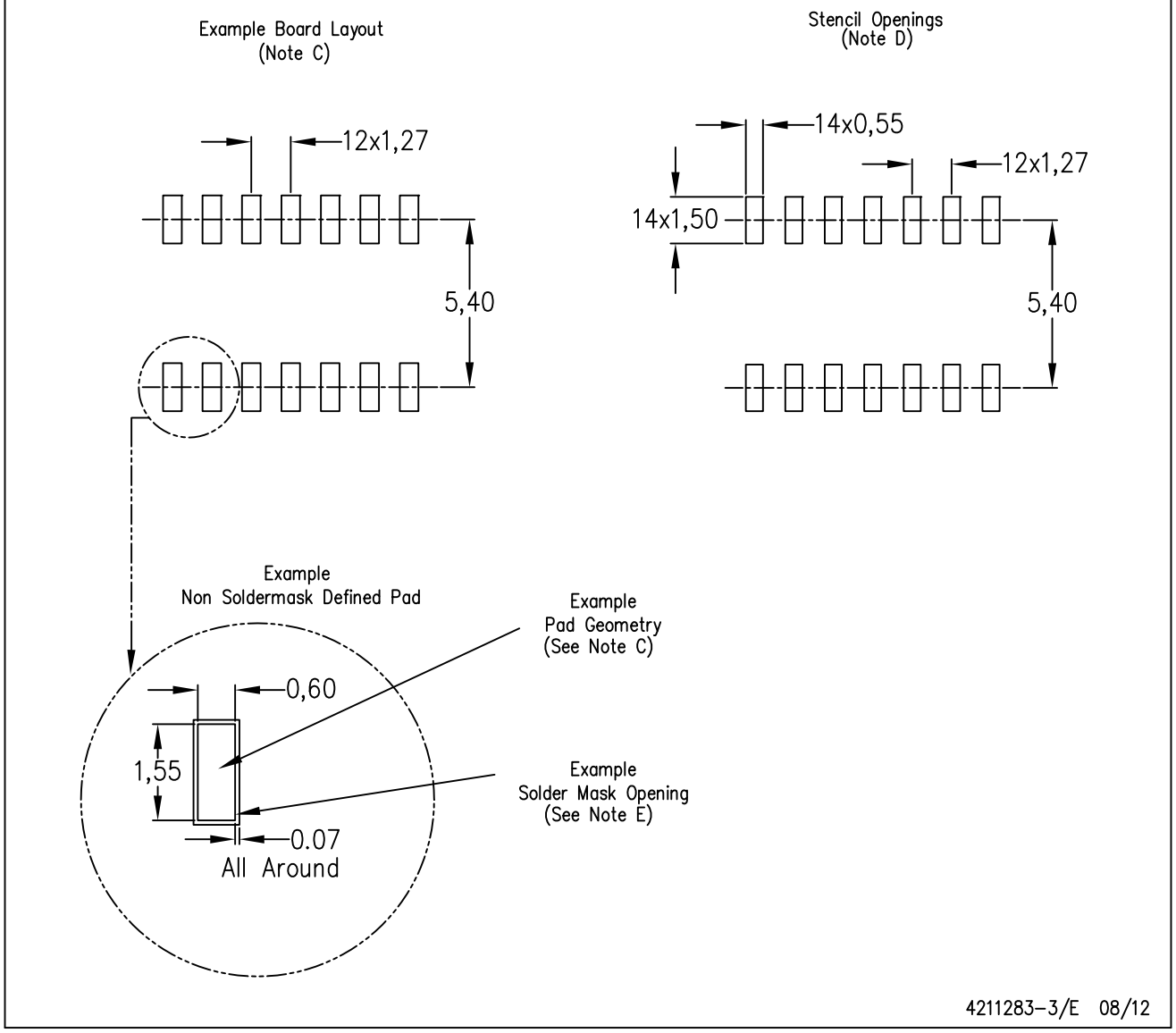
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

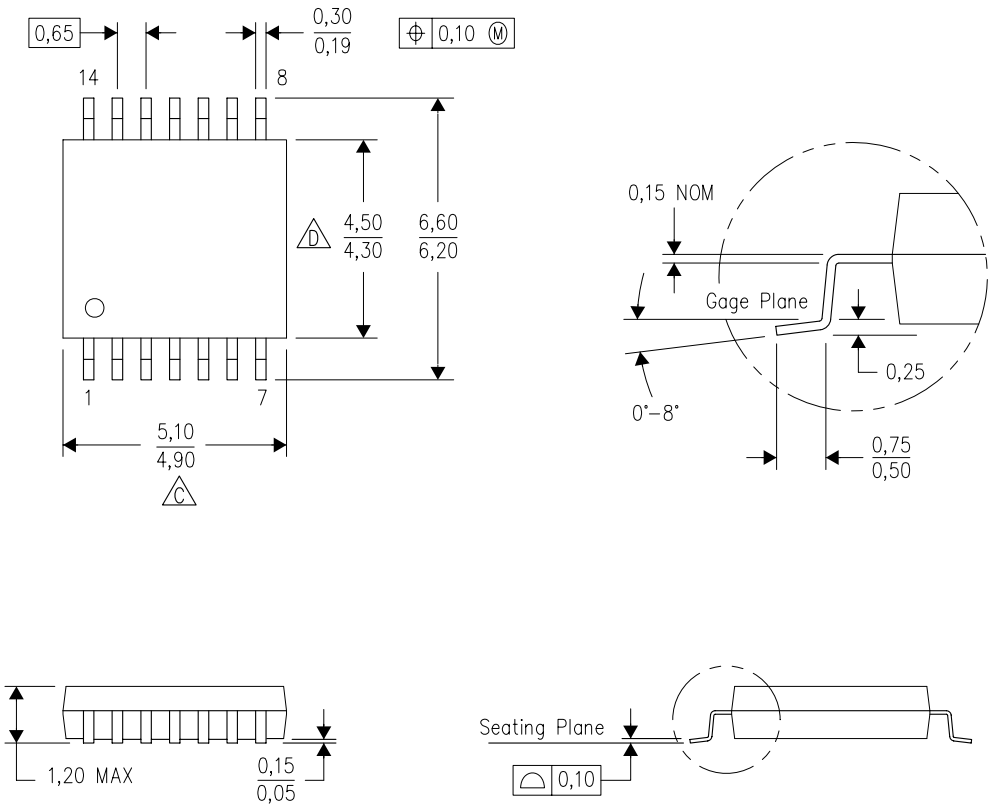
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

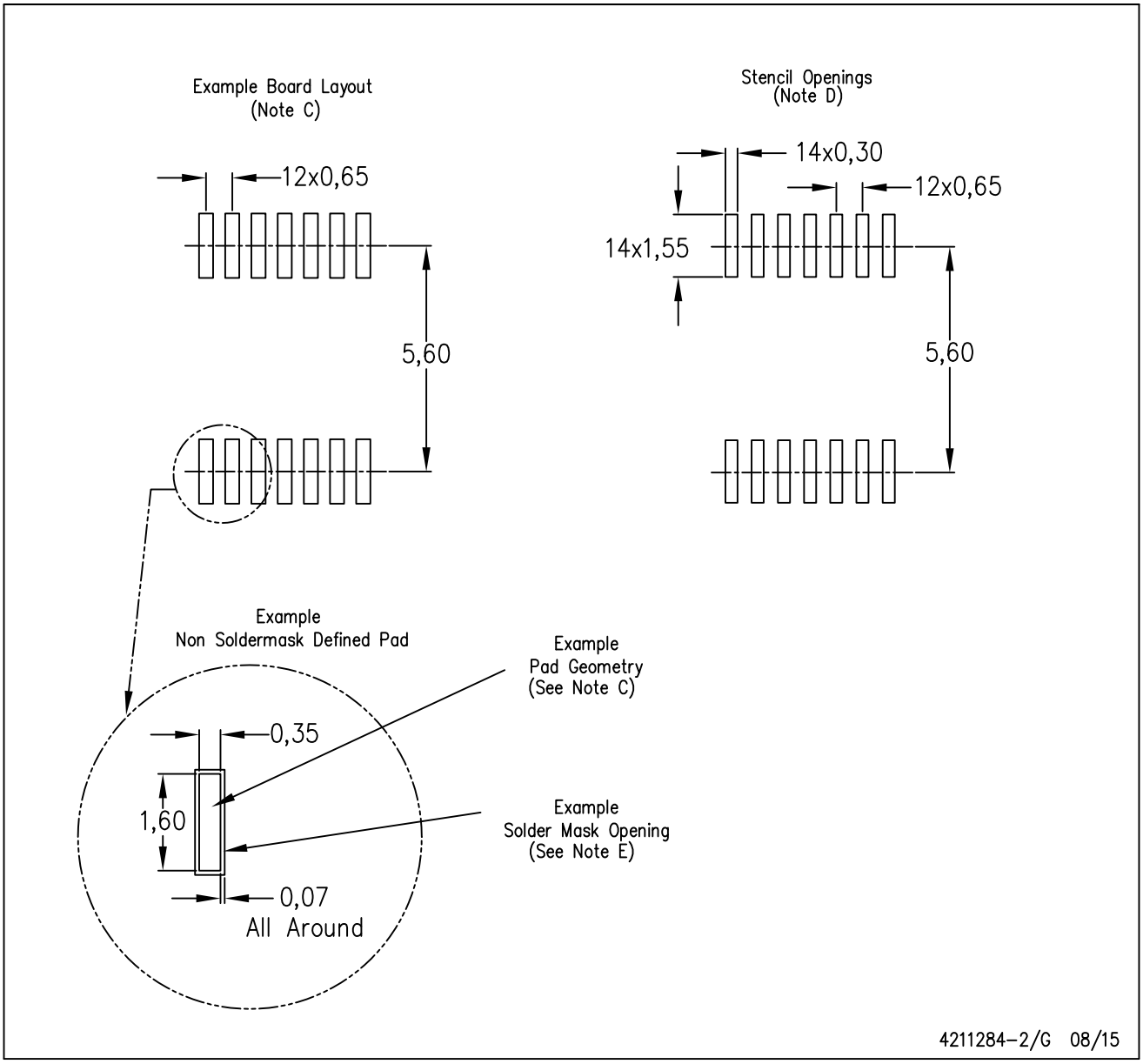
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

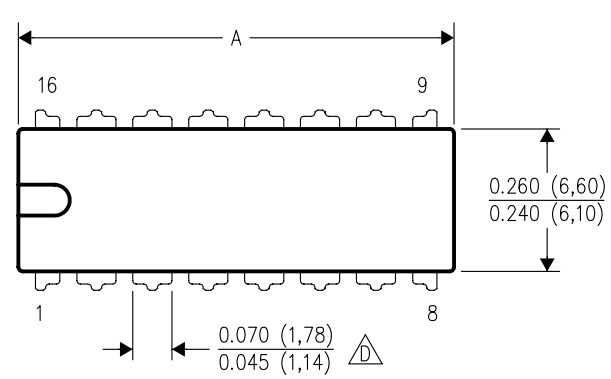



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

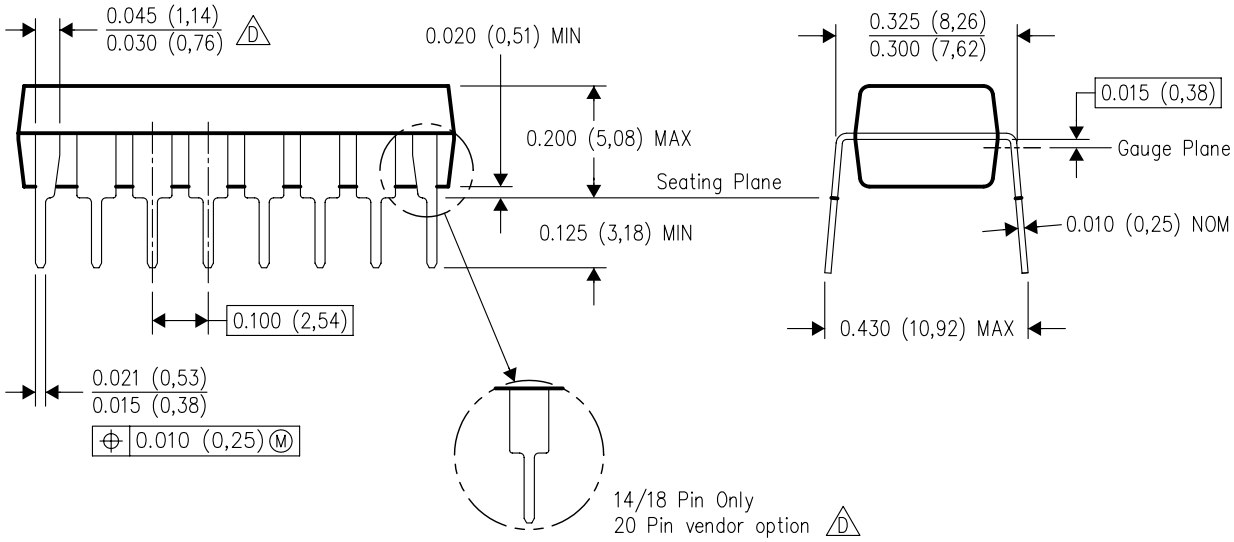
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |



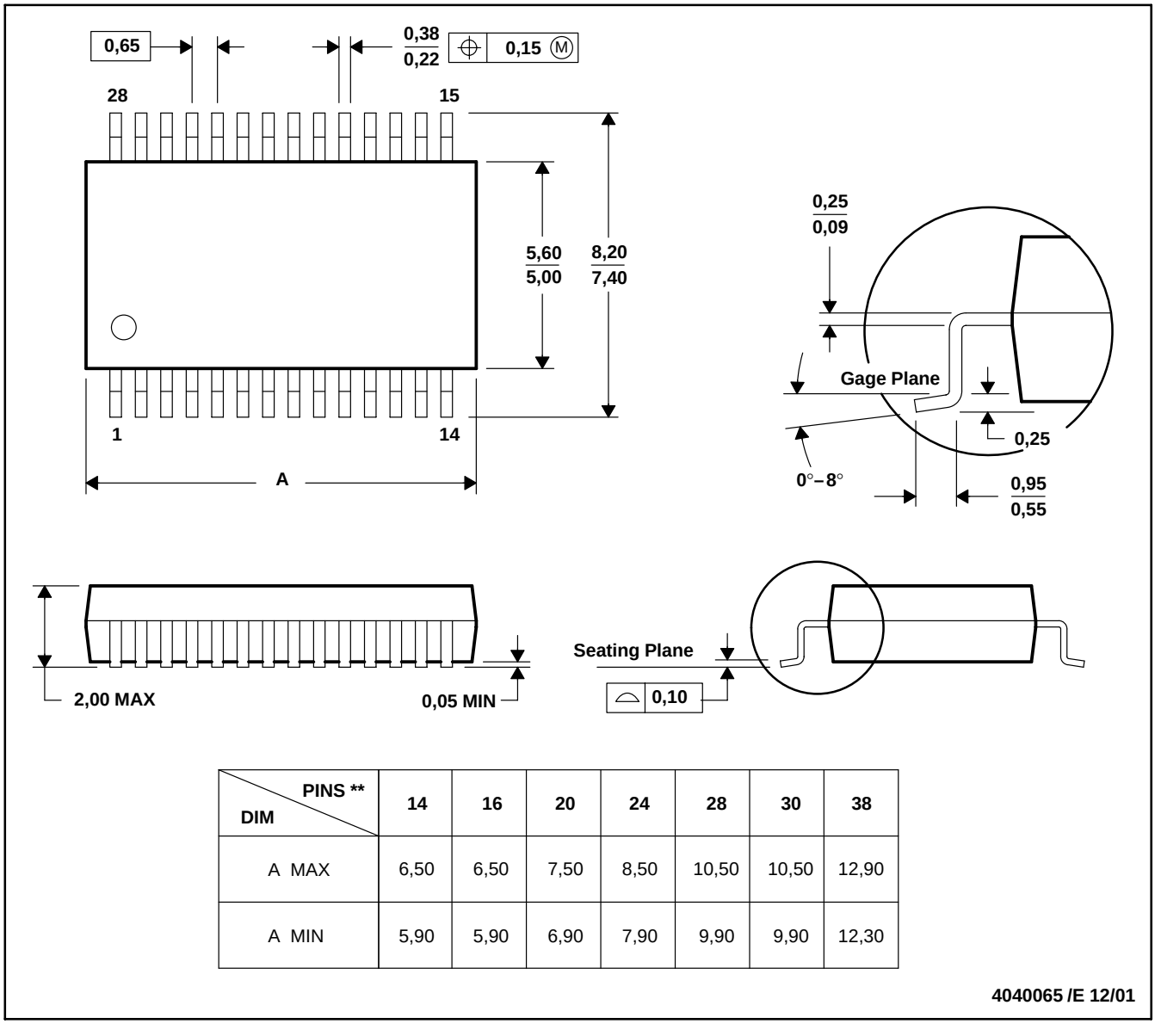

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265