Rochester Electronics®

Datasheet

74AC11175

Quadruple D-Type Flip-Flops with Clear

These positive-edge-triggered flip-flops implement D-type flip-flop logic with a direct clear input. Information at the D inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 54AC11175 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11175 is characterized for operation from -40°C to 85°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

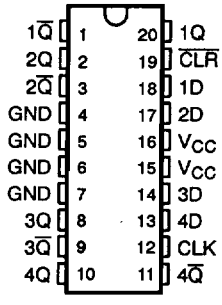
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

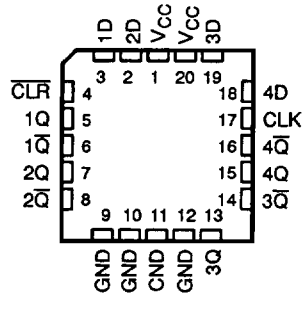
FOR REFERENCE ONLY

- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11175 . . . J PACKAGE
74AC11175 . . . DW or N PACKAGE
(TOP VIEW)



54AC11014 . . . FK PACKAGE
(TOP VIEW)



description

These positive-edge-triggered flipflops implement D-type flip-flop logic with a direct clear input. Information at the D inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

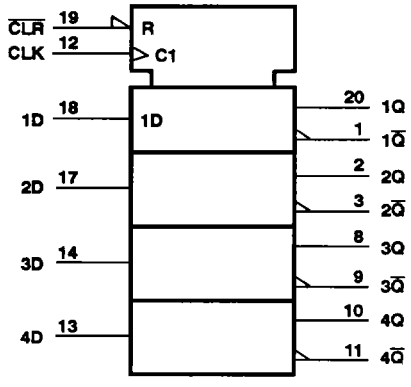
The 54AC11175 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11175 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

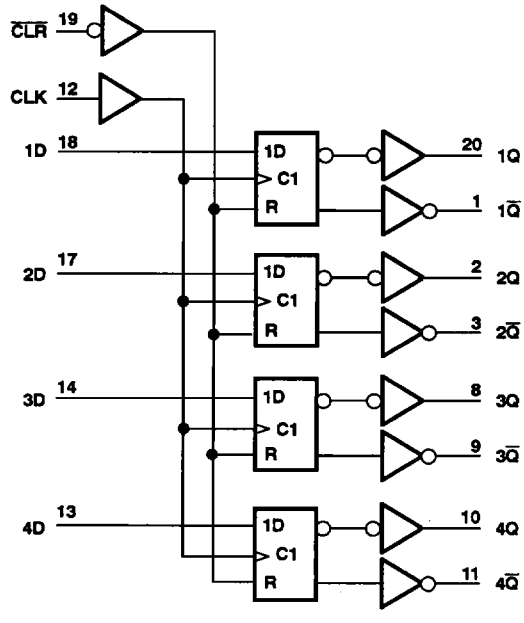
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11175			74AC11175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		VCC = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = − 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = − 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = − 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = − 50 mA†	5.5 V				3.85				
	I_{OH} = − 75 mA†	5.5V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5.5		5.5		5.5		ns
		CLK high or low	5.5		5.5		5.5		
t_{su}	Setup time before CLK↑	Data	8		8		8		ns
		$\overline{CLR}$ inactive	8		8		8		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high or low	4				4		
t_{su}	Setup time before CLK↑	Data	5.5				5.5		ns
		$\overline{CLR}$ inactive	5.5		5.5		5.5		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90	120		90		90		MHz
t_{PLH}	$\overline{CLR}$	Any Q	2.6	7	8.7	2.6	9	2.6	9.3	ns
		Any $\overline{Q}$	2.6	7	8.7	2.6	9.9	2.6	9.3	
t_{PHL}	$\overline{CLR}$	Any Q	2.5	10	11.6	2.5	13	2.5	12.4	ns
		Any $\overline{Q}$	2.5	10	11.6	2.5	13	2.5	12.4	
t_{PLH}	CLK	Any Q	2.4	6.8	8.7	2.4	9.4	2.4	9.1	ns
		Any $\overline{Q}$	2.4	6.8	8.7	2.4	9.4	2.4	9.1	
t_{PHL}	CLK	Any Q	1.7	9.4	11.7	1.7	13	1.7	12.5	ns
		Any $\overline{Q}$	1.7	9.4	11.7	1.7	13	1.7	12.5	

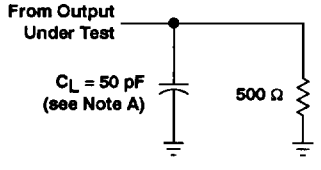
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	150		125		125		MHz
t_{PLH}	$\overline{CLR}$	Any Q	2.2	4.5	6.3	2.2		2.2	6.8	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.1	2.2	6.8	
t_{PHL}	$\overline{CLR}$	Any Q	2.4	6.7	8.5	2.4	9.7	2.4	9.3	ns
		Any $\overline{Q}$	2.4	6.7	8.5	2.4	9.7	2.4	9.3	
t_{PLH}	CLK	Any Q	2.2	4.5	6.3	2.2	7.2	2.2	6.9	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.2	2.2	6.9	
t_{PHL}	CLK	Any Q	1.9	6.4	8.5	1.9	9.7	1.9	9.3	ns
		Any $\overline{Q}$	1.9	6.4	8.5	1.9	9.7	1.9	9.3	

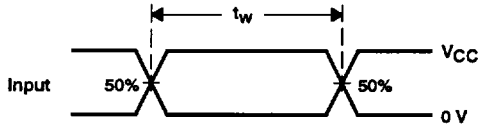
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	48	pF

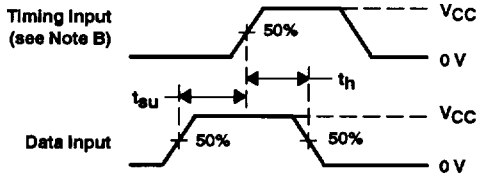
PARAMETER MEASUREMENT INFORMATION



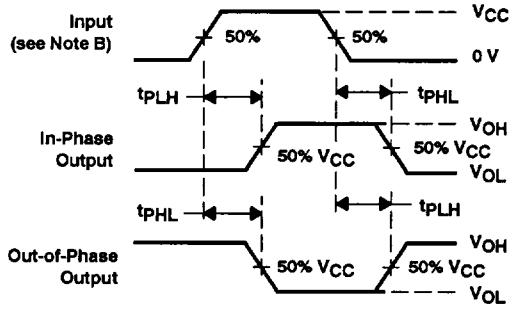
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms