NCP1380

Quasi-Resonant Current-Mode Controller for High-Power Universal Off-Line Supplies

The NCP1380 hosts a high−performance circuitry aimed to powering quasi−resonant converters. Capitalizing on a proprietary valley−lockout system, the controller shifts gears and reduces the switching frequency as the power loading becomes lighter. This results in a stable operation despite switching events always occurring in the drain−source valley. This system works down to the 4^{th} valley and toggles to a variable frequency mode beyond, ensuring an excellent standby power performance.

To improve the safety in overload situations, the controller includes an Over Power Protection (OPP) circuit which clamps the delivered power at high−line. Safety−wise, a fixed internal timer relies on the feedback voltage to detect a fault. Once the timer elapses, the controller stops and stays latched for option A and C or enters auto−recovery mode for option B and D.

Particularly well suited for adapter applications, the controller features a pin to implement either a combined overvoltage / overtemperature protection (Version A and B) or a combined brown−out/overvoltage protection (Version C and D).

Features

- Quasi−Resonant Peak Current−Mode Control Operation
- Valley Switching Operation with Valley−Lockout for Noise−Immune Operation
- Frequency Foldback at Light Load to Improve the Light Load Efficiency
- Adjustable Over Power Protection
- Auto−Recovery or Latched Internal Output Short−Circuit Protection
- Fixed Internal 80 ms Timer for Short−Circuit Protection
- Combined Overvoltage and Overtemperature Protection (A and B Versions)
- Combined Overvoltage Protection and Brown−Out (C and D Versions)
- +500 mA/−800 mA Peak Current Source/Sink Capability
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- Extended V_{CC} Range Operation Up to 28 V
- Extremely Low No−Load Standby Power
- SO−8 Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- High Power ac−dc Converters for TVs, Set−Top Boxes etc.
- Offline Adapters for Notebooks

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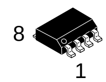
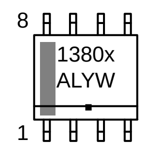
QUASI−RESONANT PWM CONTROLLER FOR HIGH POWER AC−DC WALL ADAPTERS



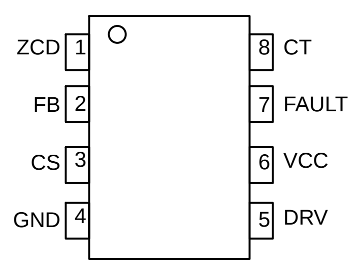
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAMS



1380x	= Specific Device Code
x	= Device Option (A, B, C, or D)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

TYPICAL APPLICATION EXAMPLE

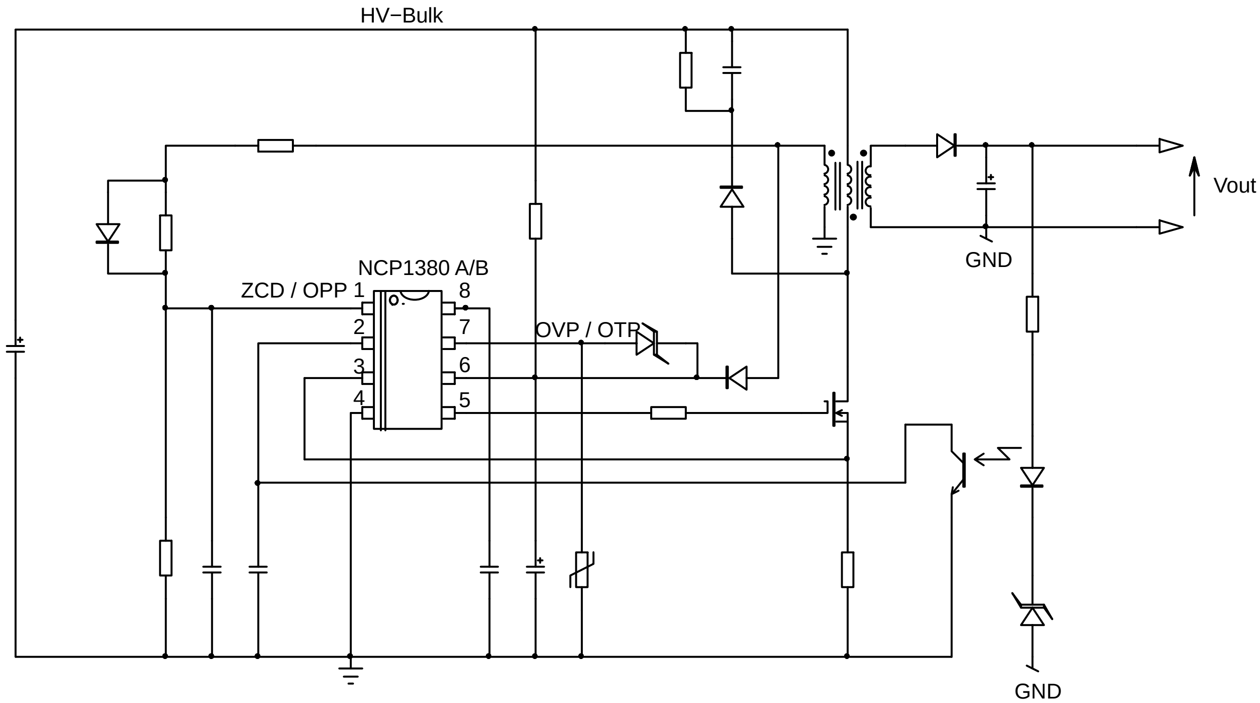


Figure 1. Typical Application Schematic for A and B Versions

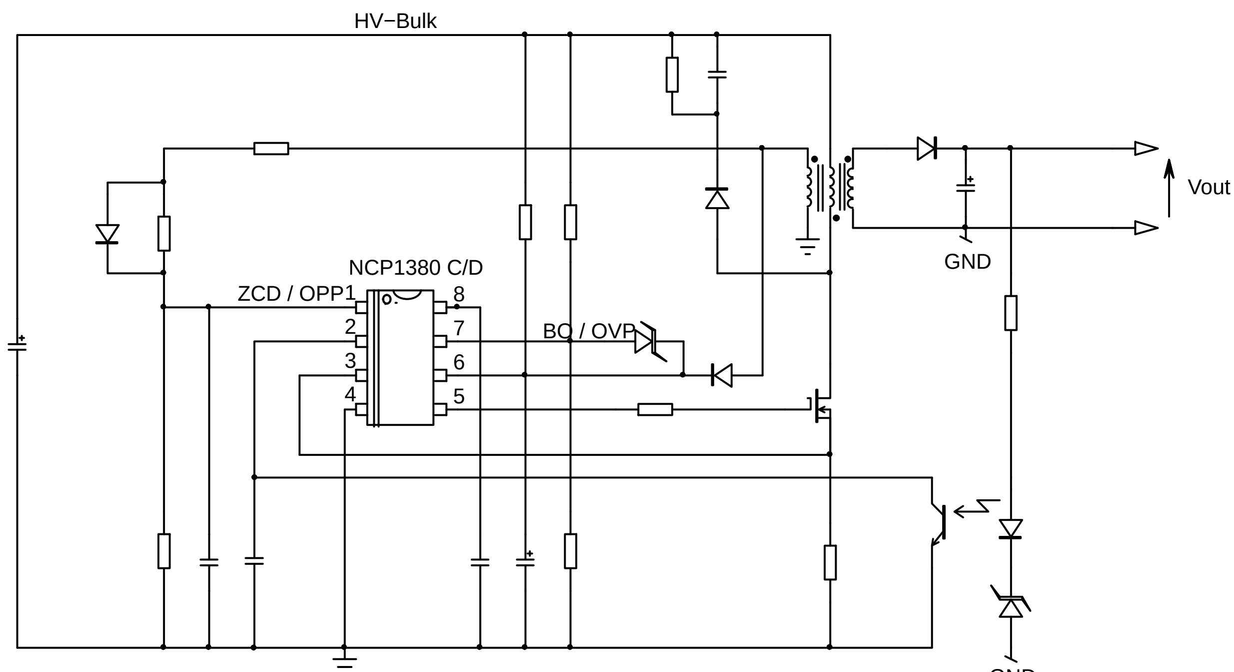


Figure 2. Typical Application Schematic for C and D Versions

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	ZCD	Zero Crossing Detection Adjust the over power protection	Connected to the auxiliary winding, this pin detects the core reset event. Also, injecting a negative voltage smaller than 0.3 V on this pin will perform over power protection.
2	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
3	CS	Current sense	This pin monitors the primary peak.
4	GND	−	The controller ground
5	DRV	Driver output	The driver’s output to an external MOSFET
6	V_{CC}	Supplies the controller	This pin is connected to an external auxiliary voltage.
7	Fault	Over voltage and Over temperature protection (A and B versions) Over−voltage and Brown−out protection (C and D versions)	Pulling this pin down with an NTC or up with a zener diode allows to latch the controller. This pin observes the HV rail and protects the circuit in case of low main conditions. It also offers a way to latch the circuit in case of over voltage event.
8	C_T	Timing capacitor	A capacitor connected to this pin acts as the timing capacitor in foldback mode.

NCP1380 OPTIONS

	OTP	OVP	Brown−Out	Auto−Recovery Overcurrent Protection	Latched Overcurrent Protection
NCP1380 / A	Yes	Yes			Yes
NCP1380 / B	Yes	Yes		Yes	
NCP1380 / C		Yes	Yes		Yes
NCP1380 / D		Yes	Yes	Yes	

INTERNAL CIRCUIT ARCHITECTURE

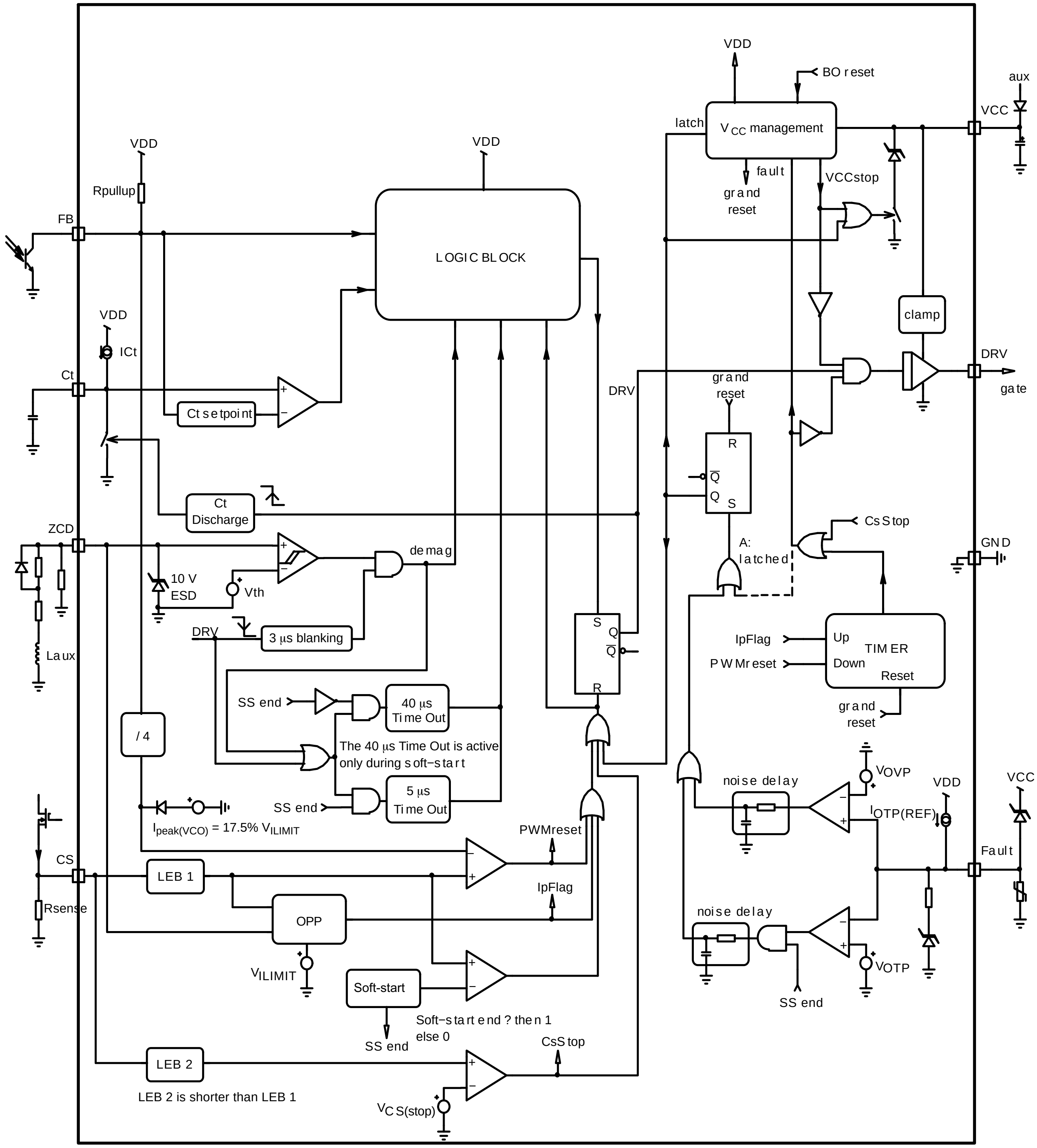


Figure 3. Internal Circuit Architecture for Versions A and B

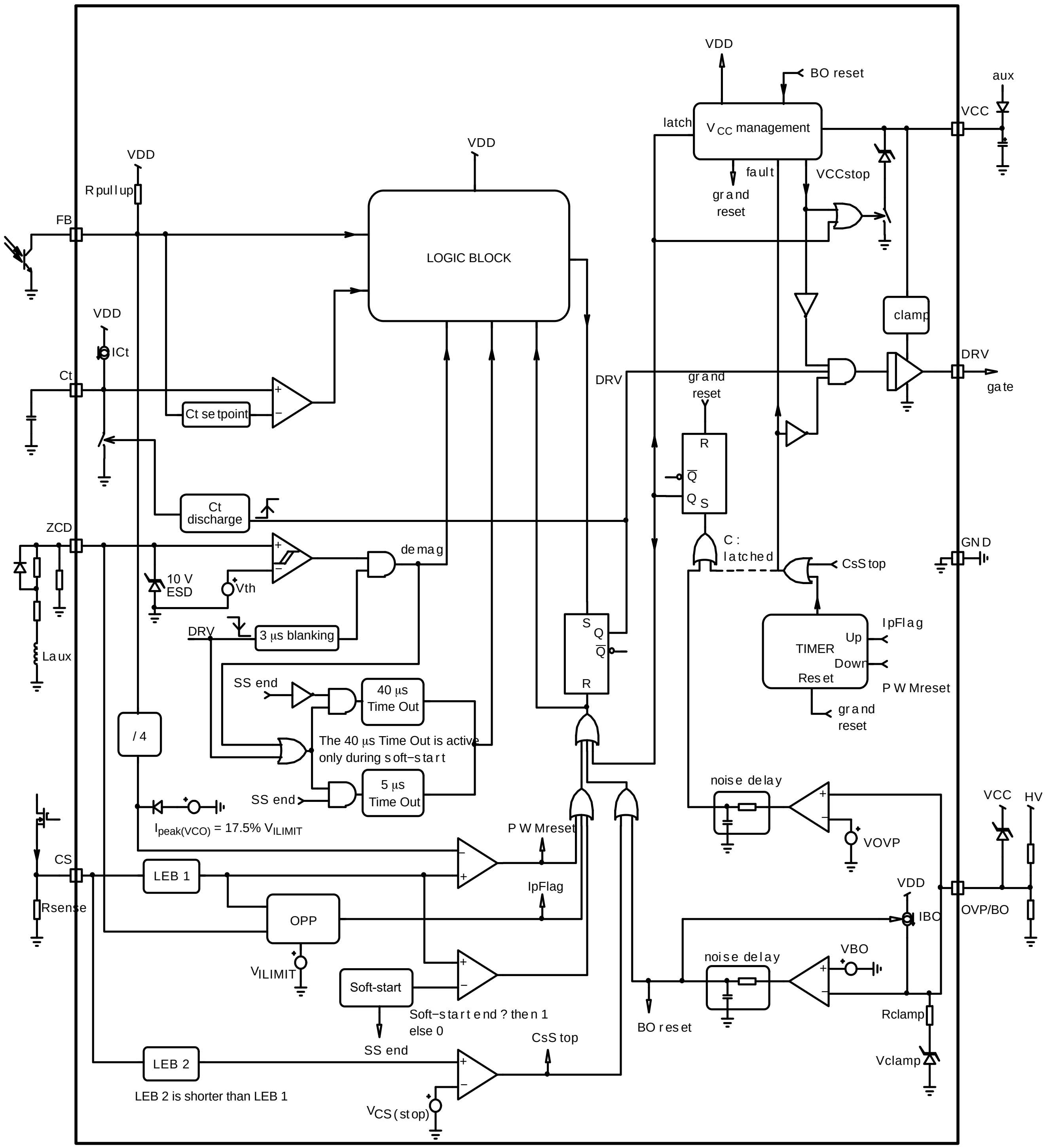


Figure 4. Internal Circuit Architecture for Versions C and D

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, V_{CC} pin, continuous voltage Maximum current for V_{CC} pin	−0.3 to 28 ±30	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3 to 20 ±1000	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins DRV and V_{CC}) Current range for low power pins (except pins ZCD, DRV and V_{CC})	−0.3 to 10 ±10	V mA
$I_{ZCD(MAX)}$	Maximum current for ZCD pin	+3 / −2	mA
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	120	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM Model (Note 1)	4	kV
	ESD Capability, MM Model (Note 1)	200	V
	ESD Capability, CDM Model (Note 1)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC Standard JESD22, Method A114E
   Machine Model 200 V per JEDEC Standard JESD22, Method A115A
   Charged Device Model 2000 V per JEDEC Standard JESD22−C101D.
2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{FB} = 3 V, V_{CS} = 0 V, V_{fault} = 1.5 V, C_T = 680 pF) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Symbol		Condition	Min	Typ	Max	Unit
SUPPLY SECTION − STARTUP AND SUPPLY CIRCUITS						
 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(latch)}$ $V_{CC(reset)}$	Supply Voltage Startup Threshold Minimum Operating Voltage Hysteresis $V_{CC(on)} - V_{CC(off)}$ Clamped V_{CC} when latched−off Internal logic reset	 V_{CC} increasing V_{CC} decreasing V_{CC} decreasing, I_{CC} = 30 μA 	 16 8.3 7.2 6.2 6	 17 9 8.0 7.2 7	 18 9.4 9.2 8.2 8	V
$t_{VCC(off)}$ $t_{VCC(reset)}$	$V_{CC(off)}$ noise filter $V_{CC(reset)}$ noise filter		− −	5 20	− −	μs
$I_{CC(start)}$	Startup current	FB pin open $V_{CC} = V_{CC(on)}$ − 0.5 V	−	10	20	μA
$I_{CC(disch)}$	Current that discharges V_{CC} when the controller gets latched	V_{CC} = 12 V	3.0	4.0	5.0	mA
$I_{CC(latch)}$	Current into V_{CC} that keeps the controller latched (Note 3)	$V_{CC} = V_{CC(latch)}$	30	−	−	μA
 I_{CC1} I_{CC2} I_{CC3A} I_{CC3B}	Supply Current Device Disabled/Fault (Note 3) B, C, and D only Device Enabled/No output load on pin 5 Device Switching (F_{SW} = 65 kHz) Device Switching VCO mode	 $V_{CC} > V_{CC(off)}$ F_{sw} = 10 kHz C_{DRV} = 1 nF, F_{SW} = 65 kHz C_{DRV} = 1 nF, V_{FB} = 1.25 V	 − − − −	 1.7 1.7 2.65 2.0	 2.0 2.0 3.0 −	mA
CURRENT COMPARATOR − CURRENT SENSE						
V_{ILIM}	Current Sense Voltage Threshold	V_{FB} = 4 V, V_{CS} increasing	0.76	0.8	0.84	V
t_{LEB}	Leading Edge Blanking Duration for V_{ILIM}	Minimum on time minus t_{ILIM}	210	275	330	ns
I_{bias}	Input Bias Current (Note 3)	DRV high	−2	−	2	μA
t_{ILIM}	Propagation Delay	$V_{CS} > V_{ILIM}$ to DRV turn−off	−	125	175	ns
$I_{peak(VCO)}$	Percentage of maximum peak current level at which VCO takes over (Note 4)	V_{FB} = 0.4 V, V_{CS} increasing	15.4	17.5	19.6	%

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{FB} = 3 V, V_{CS} = 0 V, V_{fault} = 1.5 V, C_T = 680 pF) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Symbol		Condition	Min	Typ	Max	Unit
CURRENT COMPARATOR − CURRENT SENSE						
$V_{OPP(MAX)}$	Setpoint decrease for V_{ZCD} = −300 mV (Note 5)	V_{ZCD} = −300 mV, V_{FB} = 4 V, V_{CS} increasing	35	37.5	40	%
$V_{CS(stop)}$	Threshold for immediate fault protection activation		1.125	1.200	1.275	V
t_{BCS}	Leading Edge Blanking Duration for $V_{CS(stop)}$		−	120	−	ns
DRIVE OUTPUT − GATE DRIVE						
 R_{SNK} R_{SRC}	Drive Resistance DRV Sink DRV Source	 V_{DRV} = 10 V V_{DRV} = 2 V	 − −	 12.5 20	 − −	Ω
 I_{SNK} I_{SRC}	Drive current capability DRV Sink DRV Source	 V_{DRV} = 10 V V_{DRV} = 2 V	 − −	 800 500	 − −	mA
t_r	Rise Time (10% to 90%)	C_{DRV} = 1 nF, V_{DRV} from 0 to 12 V	−	40	75	ns
t_f	Fall Time (90% to 10%)	C_{DRV} = 1 nF, V_{DRV} from 0 to 12 V	−	25	60	ns
$V_{DRV(low)}$	DRV Low Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V C_{DRV} = 1 nF, R_{DRV} = 33 kΩ	8.4	9.1	−	V
$V_{DRV(high)}$	DRV High Voltage (Note 6)	V_{CC} = $V_{CC(MAX)}$ C_{DRV} = 1 nF	10.5	13.0	15.5	V
DEMAGNETIZATION INPUT − ZERO VOLTAGE DETECTION CIRCUIT						
$V_{ZCD(TH)}$	ZCD threshold voltage	V_{ZCD} decreasing	35	55	90	mV
$V_{ZCD(HYS)}$	ZCD hysteresis	V_{ZCD} increasing	15	35	55	mV
 V_{CH} V_{CL}	Input clamp voltage High state Low state	 I_{pin1} = 3.0 mA I_{pin1} = −2.0 mA	 8 −0.9	 10 −0.7	 12 −0.3	V
t_{DEM}	Propagation Delay	V_{ZCD} decreasing from 4 V to −0.3 V	−	150	250	ns
C_{PAR}	Internal input capacitance		−	10	−	pF
t_{BLANK}	Blanking delay after on−time		2.30	3.15	4.00	μs
t_{outSS} t_{out}	Timeout after last demag transition	During soft−start After the end of soft−start	28 5.0	41 5.9	54 6.7	μs
$R_{ZCD(pdown)}$	Pulldown resistor (Note 3)		140	320	700	kΩ
TIMING CAPACITOR						
$V_{CT(MAX)}$	Maximum voltage on C_T pin	V_{FB} < $V_{FB(TH)}$	5.15	5.40	5.65	V
I_{CT}	Source current	V_{CT} = 0 V	18	20	22	μA
$V_{CT(MIN)}$	Minimum voltage on C_T pin, discharge switch activated		−	−	90	mV
C_T	Recommended timing capacitor value			220		pF
FEEDBACK SECTION						
$R_{FB(pullup)}$	Internal pullup resistor		15	18	22	kΩ
I_{ratio}	Pin FB to current setpoint division ratio		3.8	4.0	4.2	
$V_{FB(TH)}$	FB pin threshold under which C_T is clamped to $V_{CT(MAX)}$		0.26	0.3	0.34	V

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{FB} = 3 V, V_{CS} = 0 V, V_{fault} = 1.5 V, C_T = 680 pF) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Symbol		Condition	Min	Typ	Max	Unit
FEEDBACK SECTION						
	Valley threshold					V
V_{H2D}	FB voltage where 1st valley ends and 2nd valley starts	V_{FB} decreases	1.316	1.4	1.484	
V_{H3D}	FB voltage where 2nd valley ends and 3rd valley starts	V_{FB} decreases	1.128	1.2	1.272	
V_{H4D}	FB voltage where 3rd valley ends and 4th valley starts	V_{FB} decreases	0.846	0.9	0.954	
V_{HVCOD}	FB voltage where 4th valley ends and VCO starts	V_{FB} decreases	0.732	0.8	0.828	
V_{HVCOI}	FB voltage where VCO ends and 4th valley starts	V_{FB} increases	1.316	1.4	1.484	
V_{H4I}	FB voltage where 4th valley ends and 3rd valley starts	V_{FB} increases	1.504	1.6	1.696	
V_{H3I}	FB voltage where 3rd valley ends and 2nd valley starts	V_{FB} increases	1.692	1.8	1.908	
V_{H2I}	FB voltage where 2nd valley ends and 1st valley starts	V_{FB} increases	1.880	2.0	2.120	
FAULT PROTECTION (ALL VERSIONS)						
T_{SHDN}	Thermal Shutdown	Device switching (F_{SW} around 65 kHz)	140	−	170	°C
$T_{SHDN(HYS)}$	Thermal Shutdown Hysteresis		−	40	−	°C
t_{OVLD}	Overload Timer	V_{FB} = 4 V, V_{CS} > V_{ILIM}	75	85	95	ms
t_{SSTART}	Soft−start duration	V_{FB} = 4 V, V_{CS} ramping up, measured from 1st DRV pulse to $V_{CS(peak)}$ = 90% of V_{ILIM}	2.8	3.8	4.8	ms
$R_{Fault(clamp)}$	Clamp series resistor		1.3	1.55	1.8	kΩ
V_{OVP}	Fault detection level for OVP	V_{Fault} increasing	2.35	2.5	2.65	V
$t_{latch(delay)}$	Delay before latch confirmation		22.5	30	37.5	μs
FAULT PROTECTION A & B VERSIONS						
$I_{OTP(REF)}$	Reference current for direct connection of an NTC (Note 7)	V_{Fault} = V_{OTP} + 0.2 V	85	91	97	μA
V_{OTP}	Fault detection level for OTP	V_{Fault} decreasing	0.744	0.8	0.856	V
$V_{Fault(clamp)}$	Clamped voltage (Fault pin left open)	Fault pin open	1.13	1.35	1.57	V
FAULT PROTECTION C & D VERSIONS						
V_{BO}	Brown−Out level	V_{Fault} decreasing	0.744	0.8	0.856	V
I_{BO}	Sourced hysteresis current V_{Fault} > V_{BO}	V_{Fault} = V_{BO} + 0.2 V	9	10	11	μA
$t_{BO(delay)}$	Delay before entering and exiting Brown−out		22.5	30	37.5	μs
$V_{Fault(clamp)}$	Clamped voltage (Fault pin left open)	Fault pin open	1.0	1.2	1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.
4. The peak current setpoint goes down as the load decreases. It is frozen below $I_{peak(VCO)}$ (I_{peak} = cst)
5. If negative voltage in excess to −300 mV is applied to ZCD pin, the current setpoint decrease is no longer guaranteed to be linear
6. Minimum value for T_J = 125°C
7. NTC with R_{110} = 8.8 kΩ.

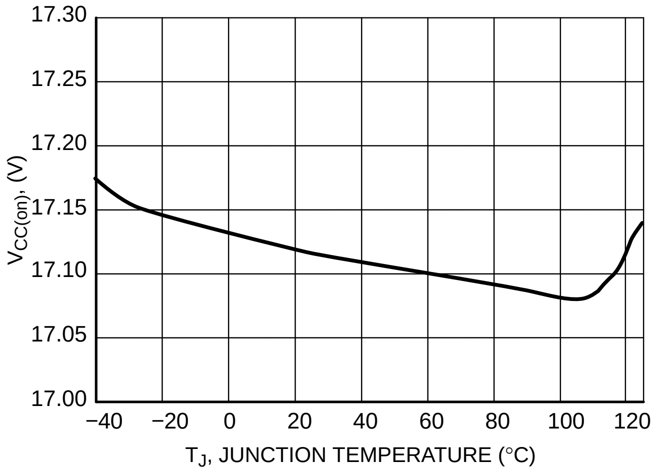


Figure 5. $V_{CC(on)}$ vs. Junction Temperature

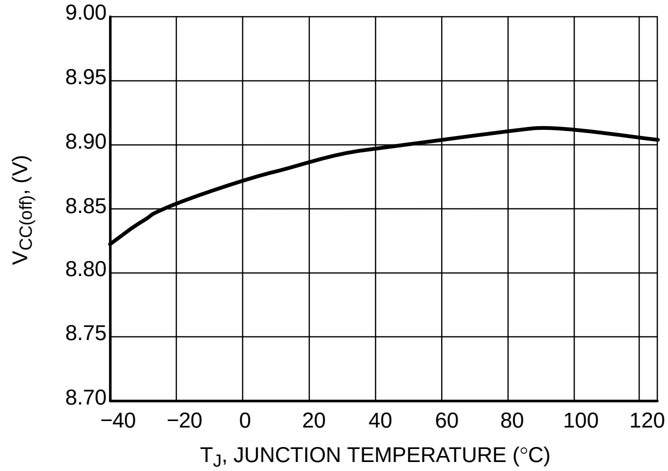


Figure 6. $V_{CC(off)}$ vs. Junction Temperature

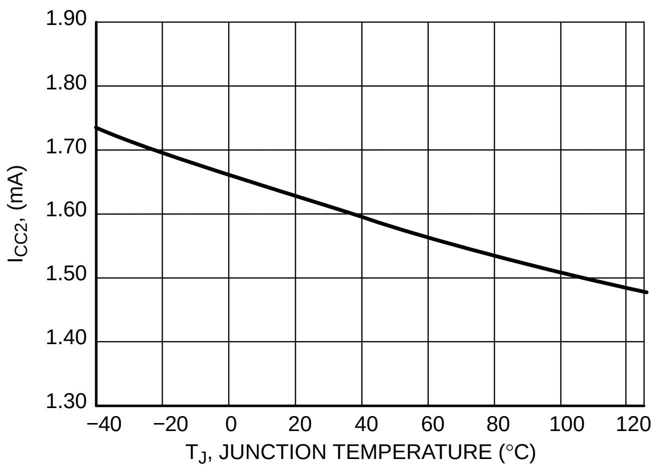


Figure 7. I_{CC2} vs. Junction Temperature

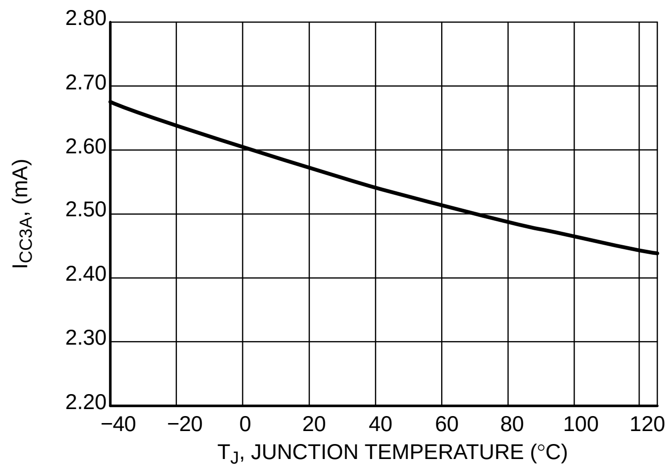


Figure 8. I_{CC3A} vs. Junction Temperature

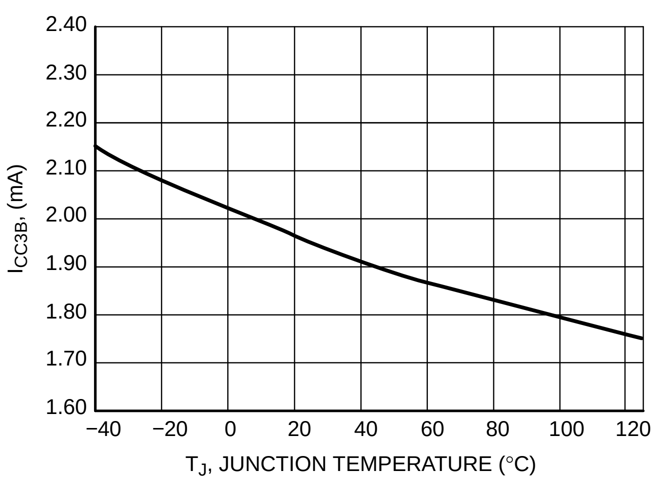


Figure 9. I_{CC3B} vs. Junction Temperature

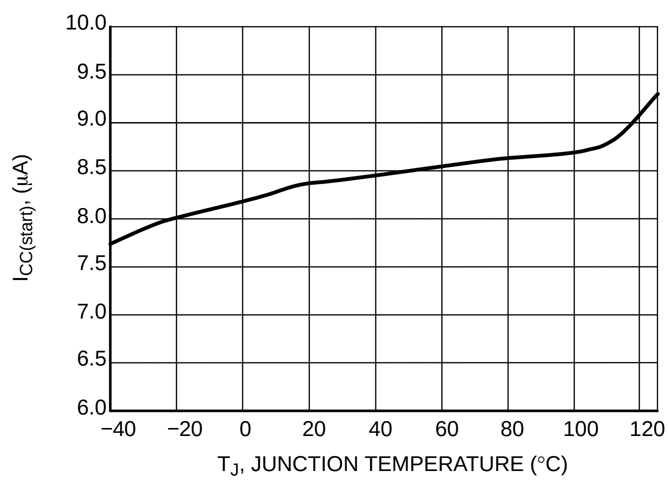


Figure 10. $I_{CC(start)}$ vs. Junction Temperature

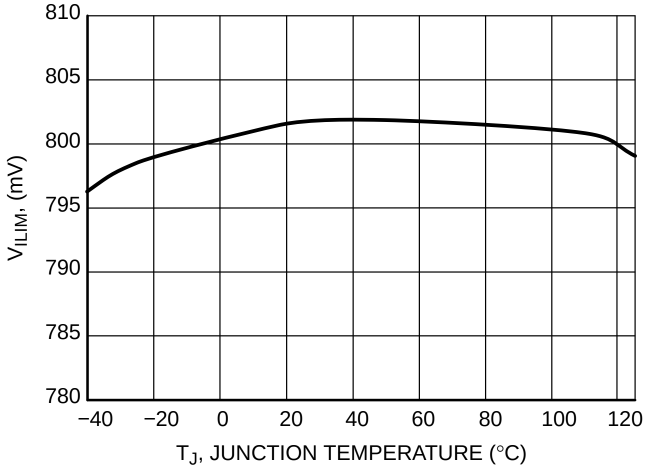


Figure 11. V_{ILIM} vs. Junction Temperature

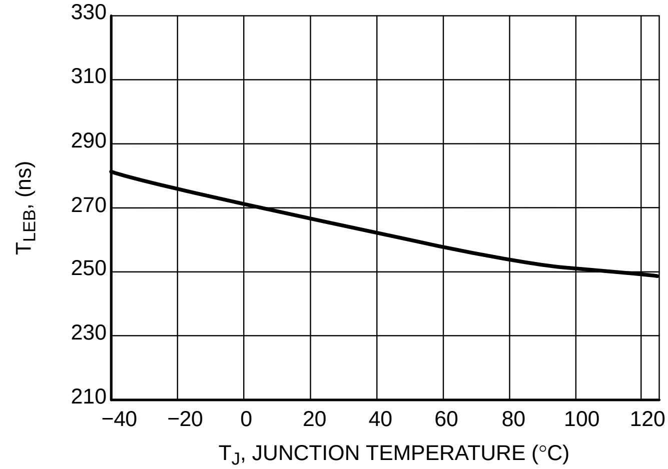


Figure 12. T_{LEB} vs. Junction Temperature

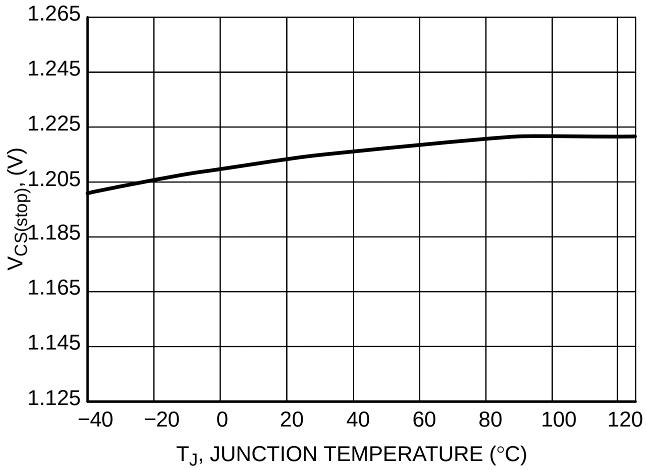


Figure 13. $V_{CS(stop)}$ vs. Junction Temperature

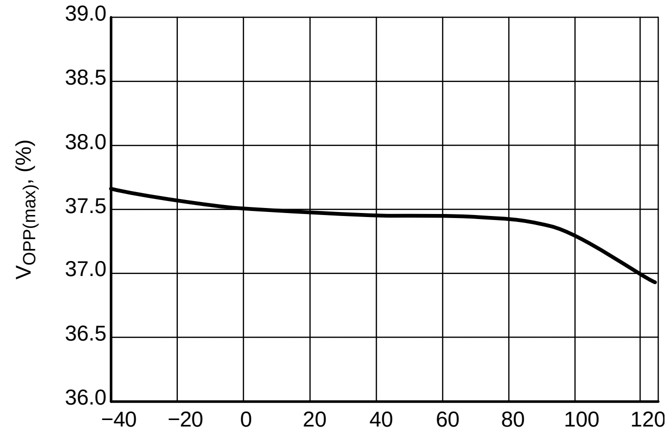


Figure 14. $V_{OPP(MAX)}$ vs. Junction Temperature

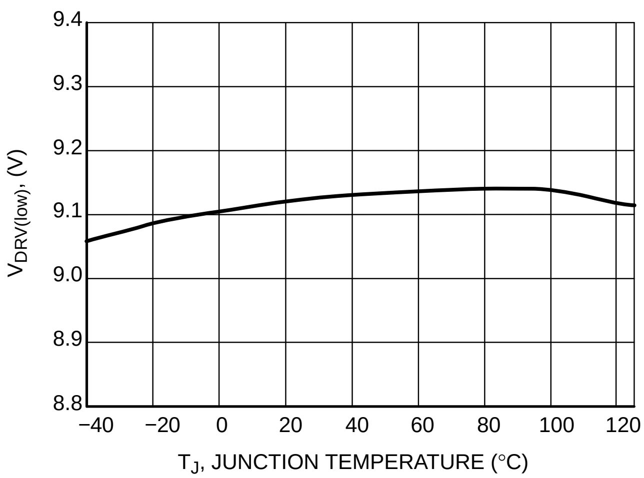


Figure 15. $V_{DRV(low)}$ vs. Junction Temperature

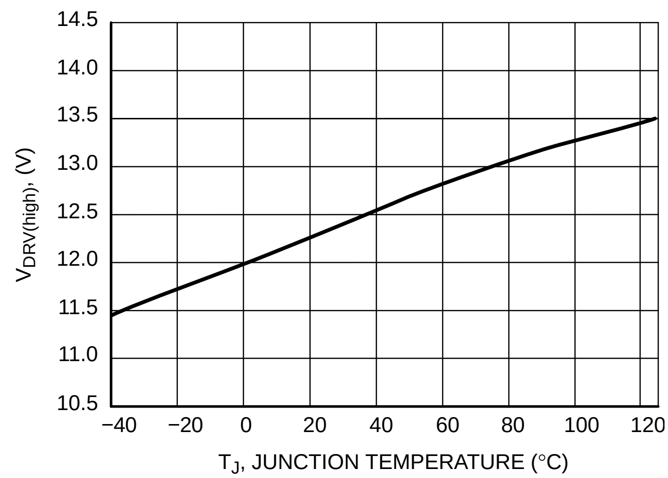


Figure 16. $V_{DRV(high)}$ vs. Junction Temperature

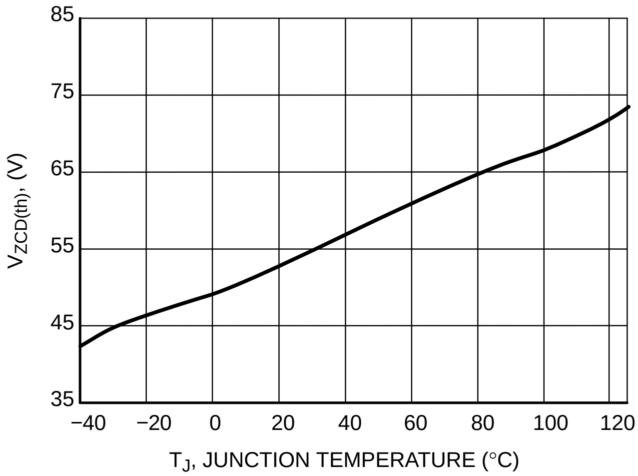


Figure 17. $V_{ZCD(th)}$ vs. Junction Temperature

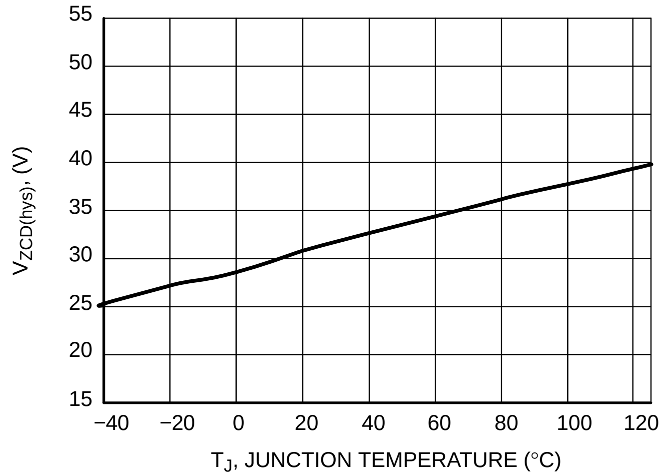


Figure 18. $V_{ZCD(hys)}$ vs. Junction Temperature

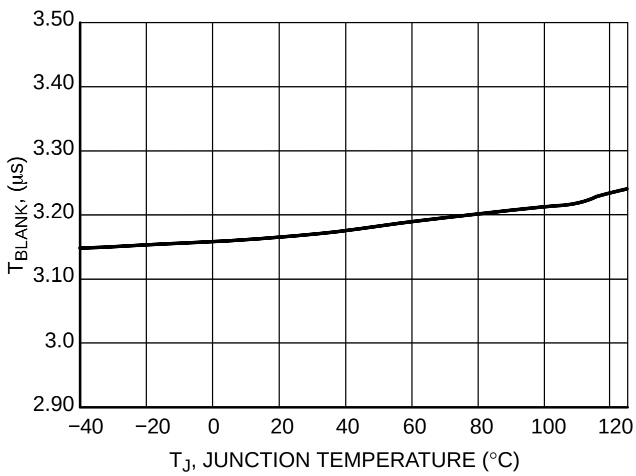


Figure 19. T_{BLANK} vs. Junction Temperature

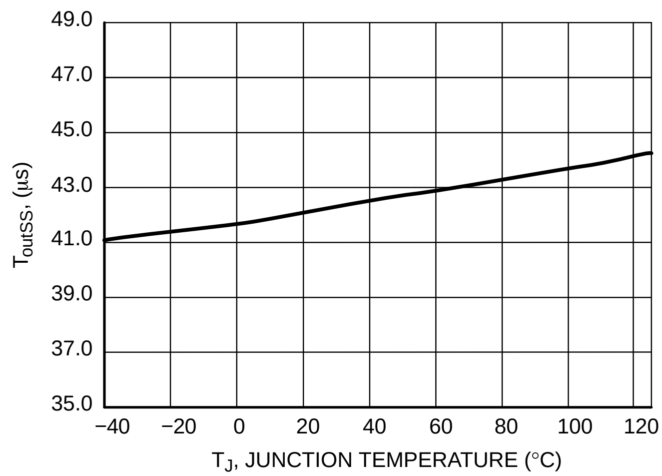


Figure 20. T_{outSS} vs. Junction Temperature

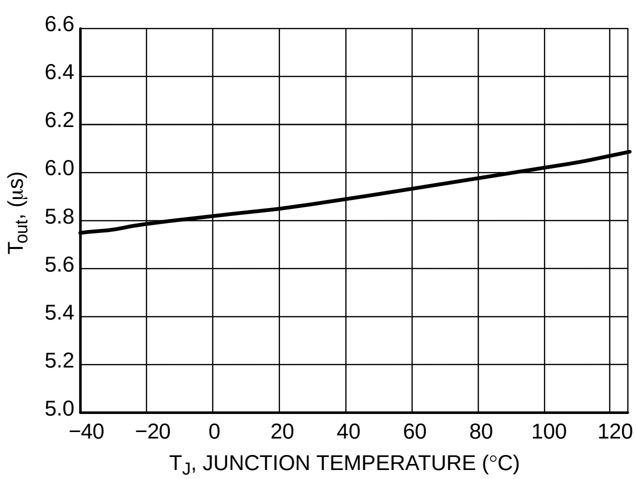


Figure 21. T_{out} vs. Junction Temperature

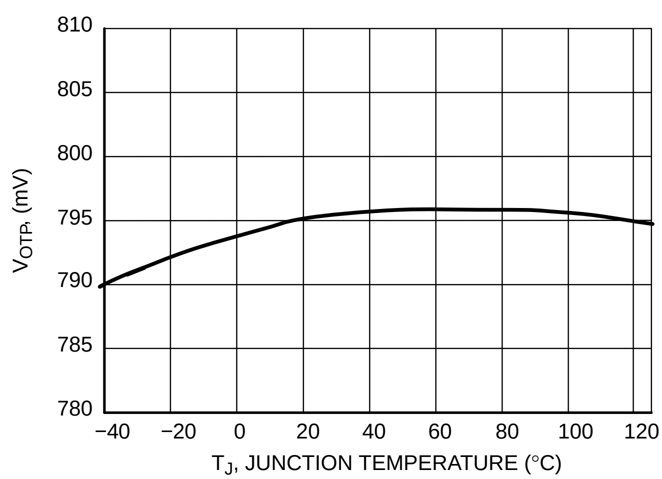


Figure 22. V_{OTP} vs. Junction Temperature

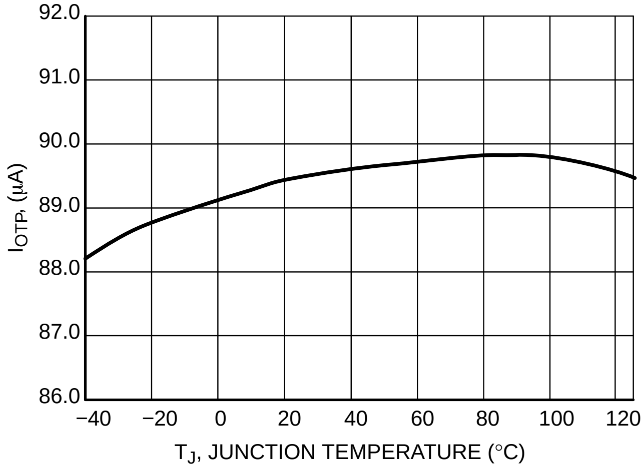


Figure 23. I_{OTP} vs. Junction Temperature

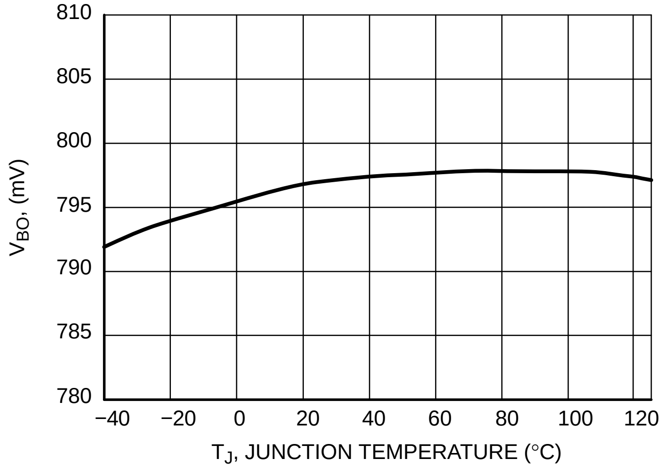


Figure 24. V_{BO} vs. Junction Temperature

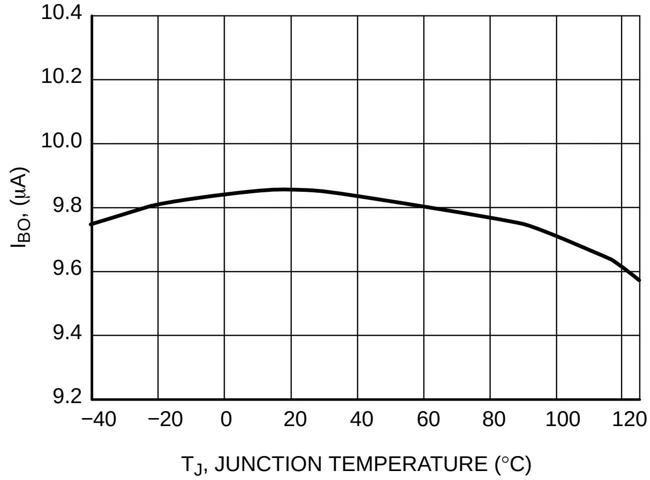


Figure 25. I_{BO} vs. Junction Temperature

APPLICATION INFORMATION

The NCP1380 implements a standard current−mode architecture operating in quasi−resonant mode. Due to a proprietary circuitry, the controller prevents valley−jumping instability and steadily locks out in selected valley as the power demand goes down. Once the fourth valley is reached, the controller continues to reduce the frequency further down, offering excellent efficiency over a wide operating range. Thanks to a fault timer combined to an OPP circuitry, the controller is able to efficiently limit the output power at high−line.

- **Quasi−Resonance Current−mode operation**: implementing quasi−resonance operation in peak current−mode control, the NCP1380 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to a proprietary circuitry, the controller locks−out in a selected valley and remains locked until the output loading significantly changes. When the load becomes lighter, the controller jumps into the next valley. It can go down to the 4^{th} valley if necessary. Beyond this point, the controller reduces its switching frequency by freezing the peak current setpoint. During quasi−resonance operation, in case of very damped valleys, a 5.5 μs timer emulates the missing valleys.
- **Frequency reduction in light−load conditions**: when the 4^{th} valley is left, the controller reduces the switching frequency which naturally improves the standby power by a reduction of all switching losses.
- **Overpower protection (OPP)**: When the voltage on ZCD pin swings in flyback polarity, a direct image if the input voltage is applied on ZCD pin. We can thus reduce the peak current depending of V_{ZCD} during the on−time.
- **Internal soft−start**: A soft−start precludes the main power switch from being stressed upon startup. Its duration is fixed and equal to 4 ms.
- **Fault input (A and B versions)**: By combining a dual threshold on the Fault pin, the controller allows the direct connection of an NTC to ground plus a zener diode to a monitored voltage. In case the pin is brought below the OTP threshold by the NTC or above the OVP threshold by the zener diode, the circuit permanently latches−off and V_{CC} is clamped to 7.2 V.
- **Fault input (C and D versions)**: The C and D versions of NCP1380 include a brown−out circuit which safely stops the controller in case the input voltage is too low. Restart occurs via a complete startup sequence (latch reset and soft−start). During normal operation, the voltage on this pin is clamped to V_{clamp} to give enough room for OVP detection. If the voltage on this pin increases above 2.5 V, the part latches−off.
- **Short−circuit protection**: Short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (where the auxiliary winding level does not properly collapse in presence of an output short). Here, when the internal 0.8 V maximum peak current limit is activated, the timer starts counting up. If the fault disappears, the timer counts down. If the timer reaches completion while the error flag is still present, the controller stops the pulses. This protection is latched on A and C version (the user must unplug and re−plug the power supply to restart the controller) and auto−recovery on B and D versions (if the fault disappears, the SMPS automatically resumes operation). In addition, all versions feature a winding short−circuit protection, that senses the CS signal and stops the controller if V_{CS} reaches 1.5 x V_{ILIM} (after a reduced LEB of t_{BCS}). This additional comparator is enabled only during the main LEB duration t_{LEB}, for noise immunity reason.

NCP1380 OPERATING MODES

NCP1380 has two operating mode: quasi−resonant operation and VCO operation for the frequency foldback.

The operating mode is fixed by the FB voltage as portrayed by Figure 26:

- Quasi−resonant operation occurs for FB voltage higher than 0.8 V (FB decreasing) or higher than 1.4 V (FB increasing) which correspond to high output power and medium output power. The peak current is variable and is set by the FB voltage divided by 4.
- Frequency foldback or VCO mode occurs for FB voltage lower than 0.8 V (FB decreasing) or lower than 1.4 V (FB increasing). This corresponds to low output power.

During VCO mode, the peak current decreases down to 17.5% of its maximum value and is then frozen. The switching frequency is variable and decreases as the output load decreases.

The switching frequency is set by the end of charge of the capacitor connected to the C_T pin. This capacitor is charged with a constant current source and the capacitor voltage is compared to an internal threshold fixed by FB voltage. When this capacitor voltage reaches the threshold the capacitor is rapidly discharged down to 0 V and a new period start.

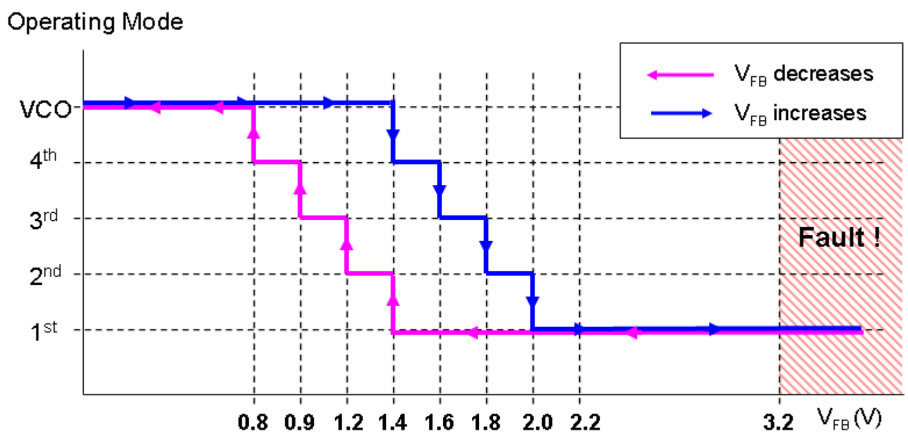


Figure 26. Operating Valley According to FB Voltage

VALLEY DETECTION AND SELECTION

The valley detection is done by monitoring the voltage of the auxiliary winding of the transformer. A valley is detected when the voltage on pin 1 crosses down the 55 mV internal threshold. When a valley is detected, an internal counter is incremented. The operating valley (1st, 2nd, 3rd or 4th) is determined by the FB voltage as shown by Figure 26.

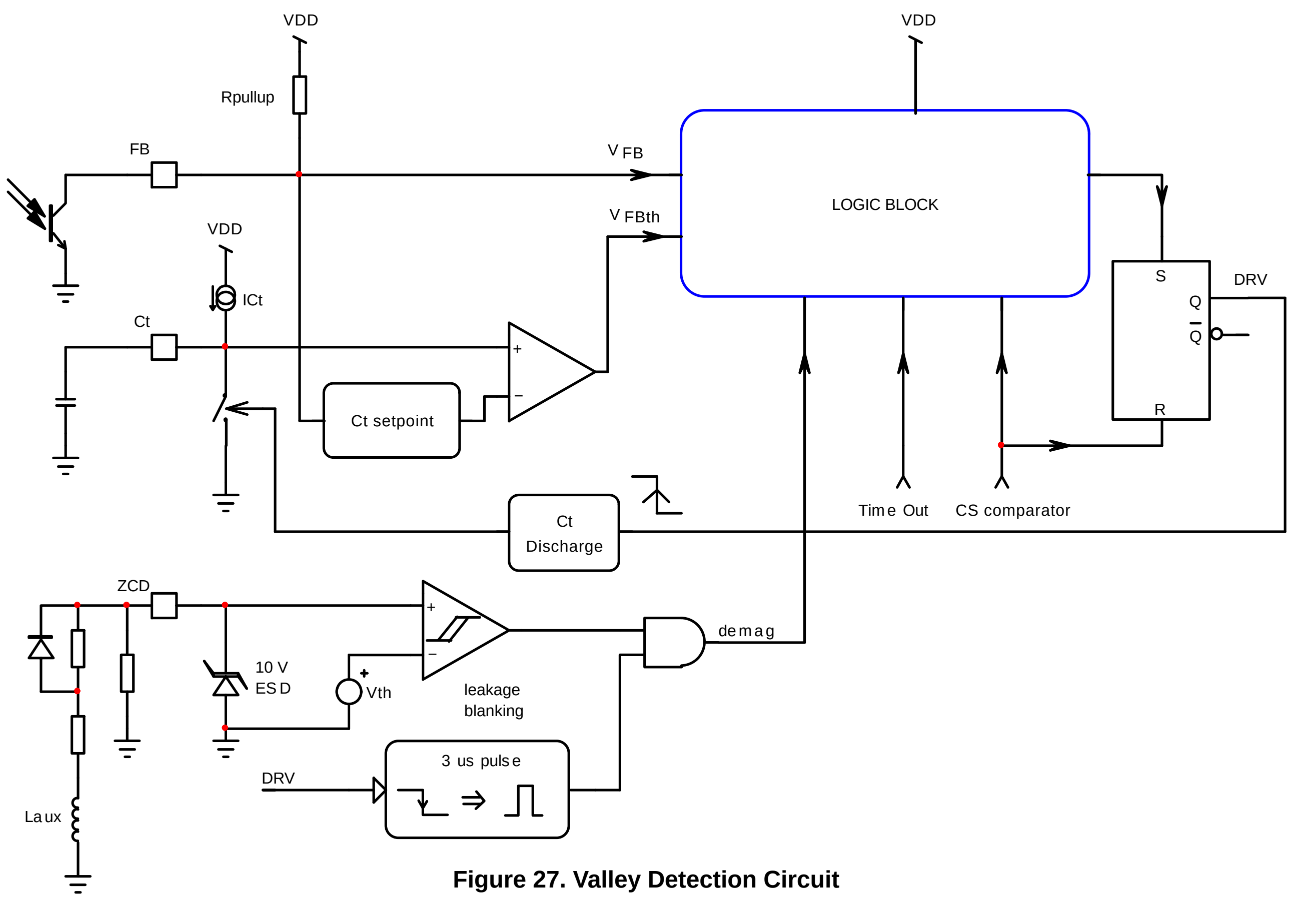


Figure 27. Valley Detection Circuit

As the output load decreases (FB voltage decreases), the valleys are incremented from the first to the fourth. When the fourth valley is reached, if FB voltage further decreases below 0.8 V, the controller enters VCO mode.

During VCO operation, the peak current continues to decrease until it reaches 17.5% of the maximum peak current: the switching frequency expands to deliver the necessary output power. This allows achieving very low standby power consumption.

The Figure 28 shows a simulation case where the output current of a 19 V, 60 W adapter decreases from 2.8 A to 0.1 A. No instability is seen during the valley transitions (Figures 29, 30, 31 and 32)

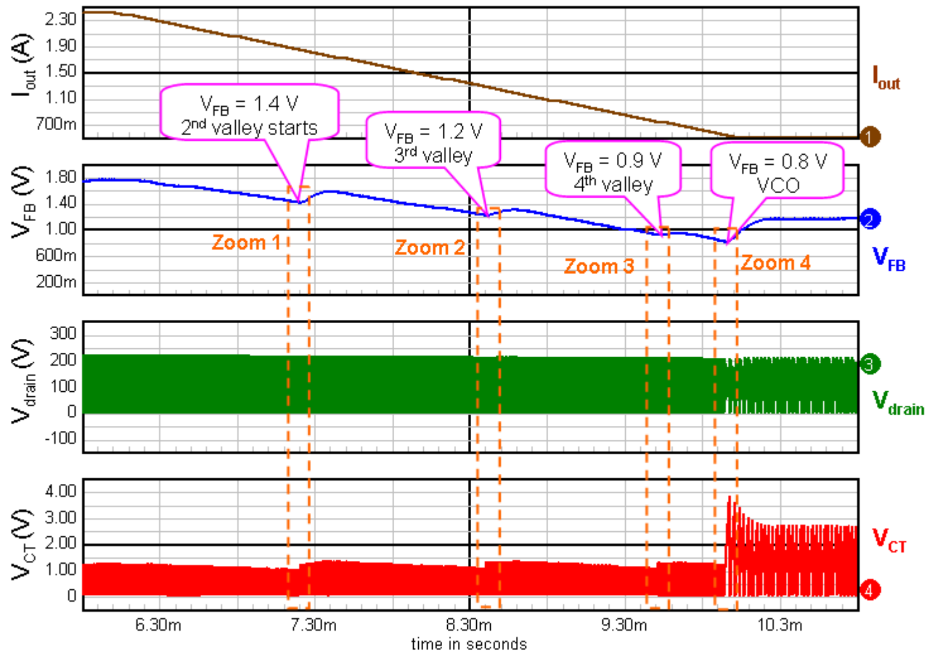


Figure 28. Output Load is Decreased from 2.8 A Down to 100 mA at 120 Vdc Input Voltage

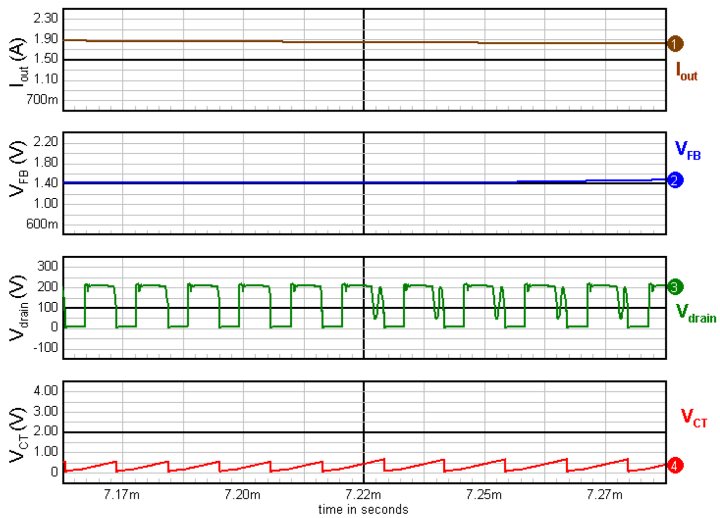


Figure 29. Zoom 1: 1st to 2nd Valley Transition

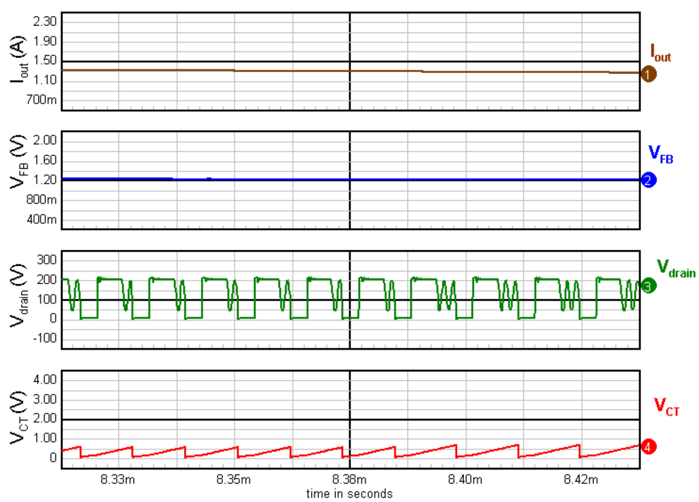


Figure 30. Zoom 2: 2nd to 3rd Valley Transition

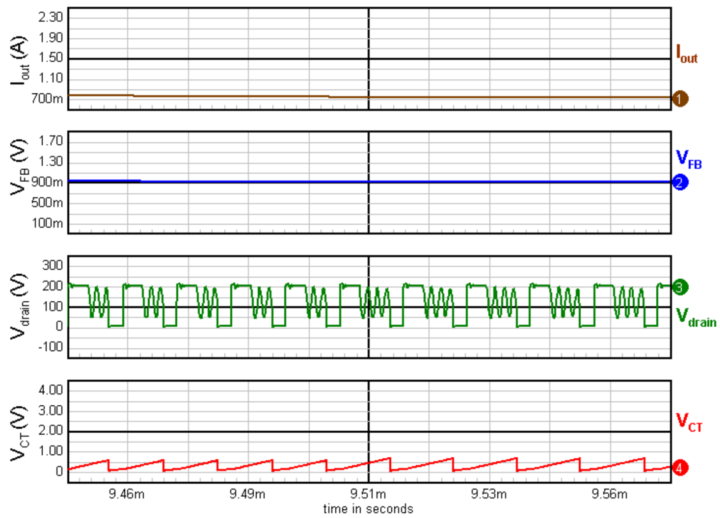


Figure 31. Zoom 3: 3rd to 4th Valley Transition

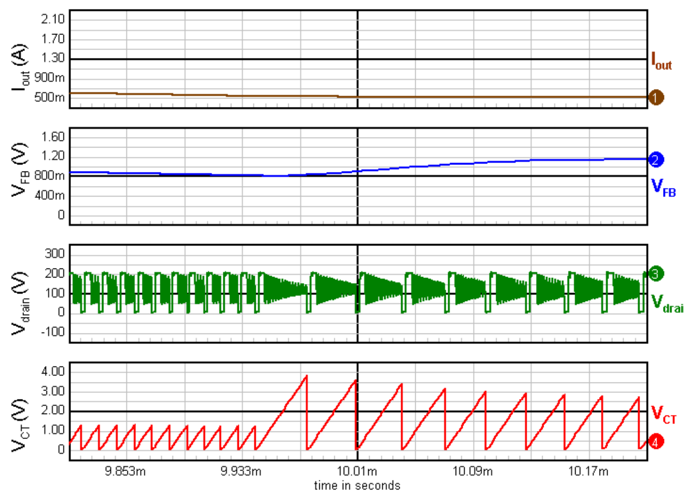


Figure 32. Zoom 4: 4th Valley to VCO Mode Transition

Time Out

In case of extremely damped free oscillations, the ZCD comparator can be unable to detect the valleys. To avoid such situation, NCP1380 integrates a Time Out function that acts as a substitute clock for the decimal counter inside the logic bloc. The controller thus continues its normal operation. To avoid having a too big step in frequency, the time out duration is set to 5.5 μs. Figures 34 and 35 detail the time out operation.

The NCP1380 also features an extended time out during the soft−start.

Indeed, at startup, the output voltage reflected on the auxiliary winding is low. Because of the voltage drop introduced by the Over Power Compensation diode (Figure 40), the voltage on the ZCD pin is very low and the ZCD comparator might be unable to detect the valleys. In this condition, setting the DRV Latch with the 5.5 μs time−out can lead to a continuous conduction mode operation (CCM) at the beginning of the soft−start. This CCM operation only last a few cycles until the voltage on ZCD pin becomes high enough to be detected by the ZCD comparator. To avoid this, the time−out duration is extended to 40 μs during the soft−start in order to ensure that the transformer is fully demagnetized before the MOSFET is turned−on.

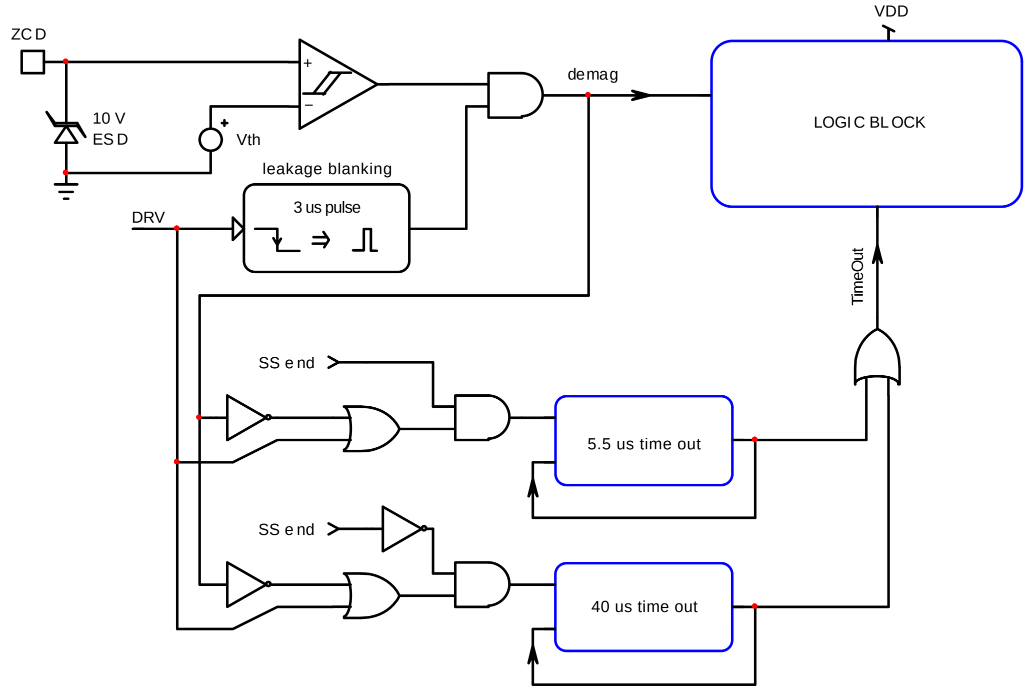


Figure 33. Time Out Circuit

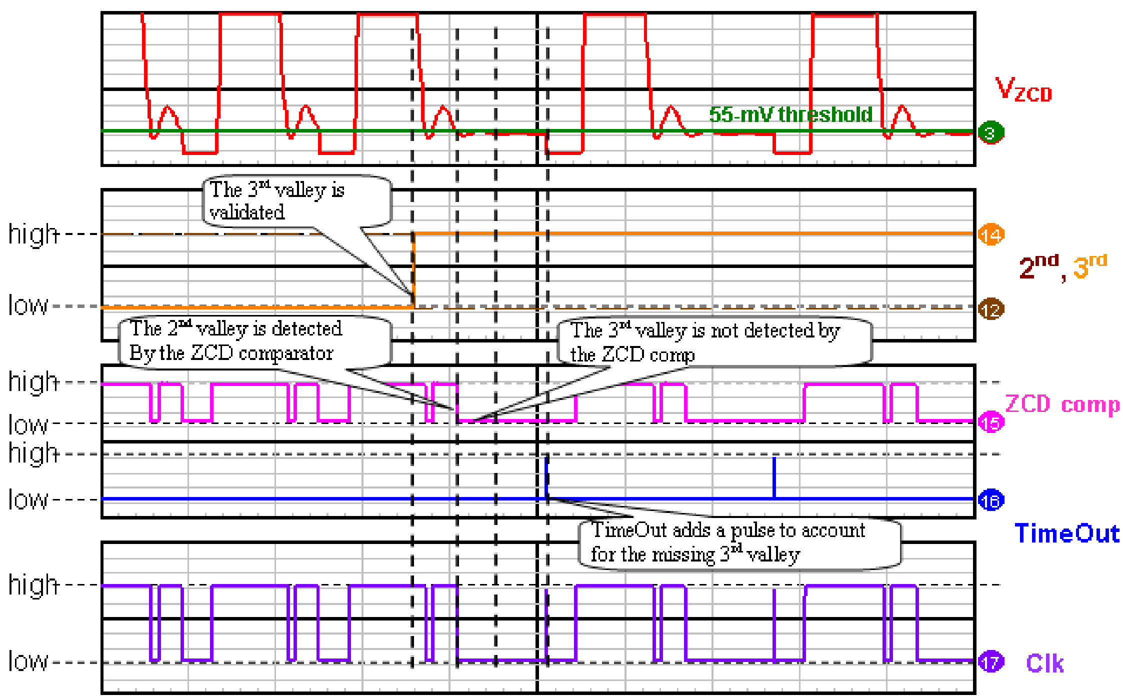


Figure 34. Time Out Case n°1: the 3rd Valley is Missing

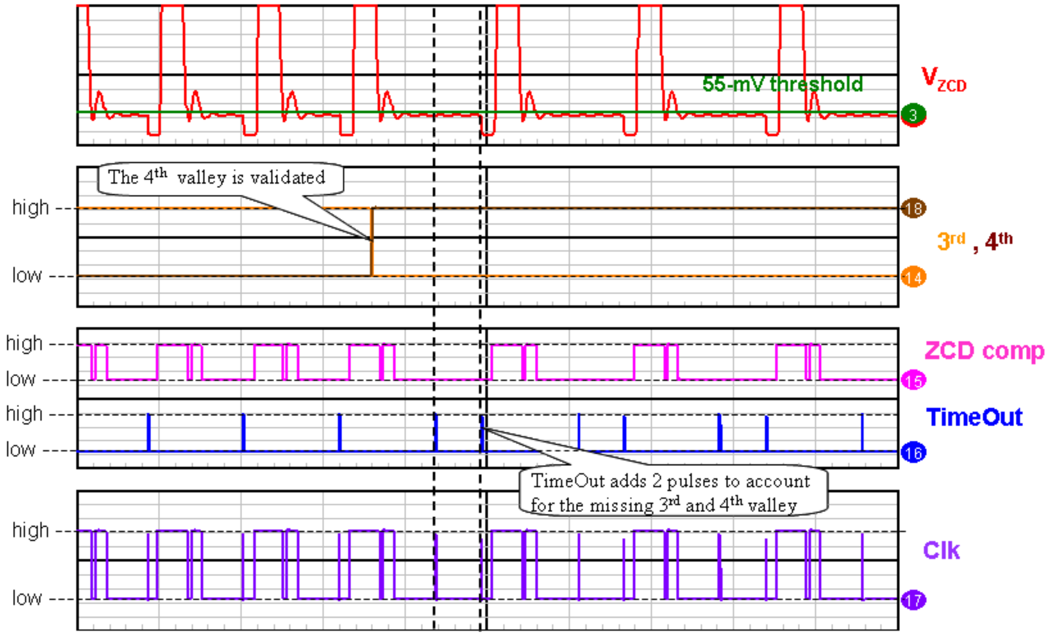


Figure 35. Time Out Case n°2: the 3rd and 4th Valley are Missing

VCO MODE OR FREQUENCY FOLDBACK

VCO operation occurs for FB voltage lower than 0.8 V (FB decreasing), or lower than 1.4 V (FB increasing). This corresponds to low output power.

During VCO operation, the peak current is fixed to 17.5% of his maximum value and the frequency is variable and expands as the output power decreases.

The frequency is set by the end of charge of the capacitor connected to the C_T pin. This capacitor is charged with a constant current source and its voltage is compared to an internal threshold (V_{FBth}) fixed by FB voltage (see Figure 27). When this capacitor voltage reaches the threshold, the capacitor is rapidly discharged down to 0 V and a new period start. The internal threshold is inversely proportional to FB voltage. The relationship between V_{FB} and V_{FBth} is given by Equation 1.

$$V_{FBth} = 6.5 - (10/3)V_{FB} \qquad \text{(eq. 1)}$$

When V_{FB} is lower than 0.3 V, V_{CT} is clamped to $V_{CT(MAX)}$ which is typically 5.5 V. Figure 36 shows the VCO mode at works.

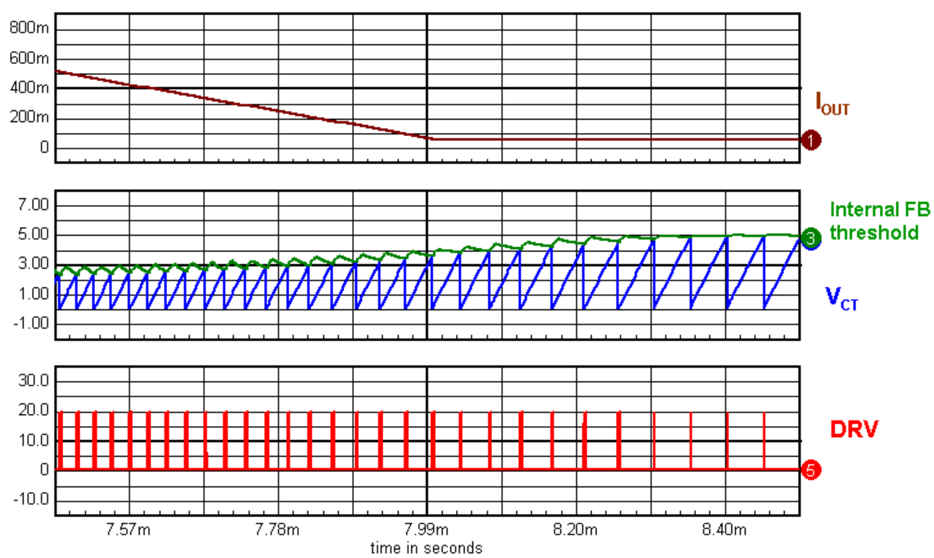


Figure 36. In VCO Mode, as the Power Output Decreases, the Frequency Expands

SHORT−CIRCUIT OR OVERLOAD MODE

Figure 37 shows the implementation of the fault timer.

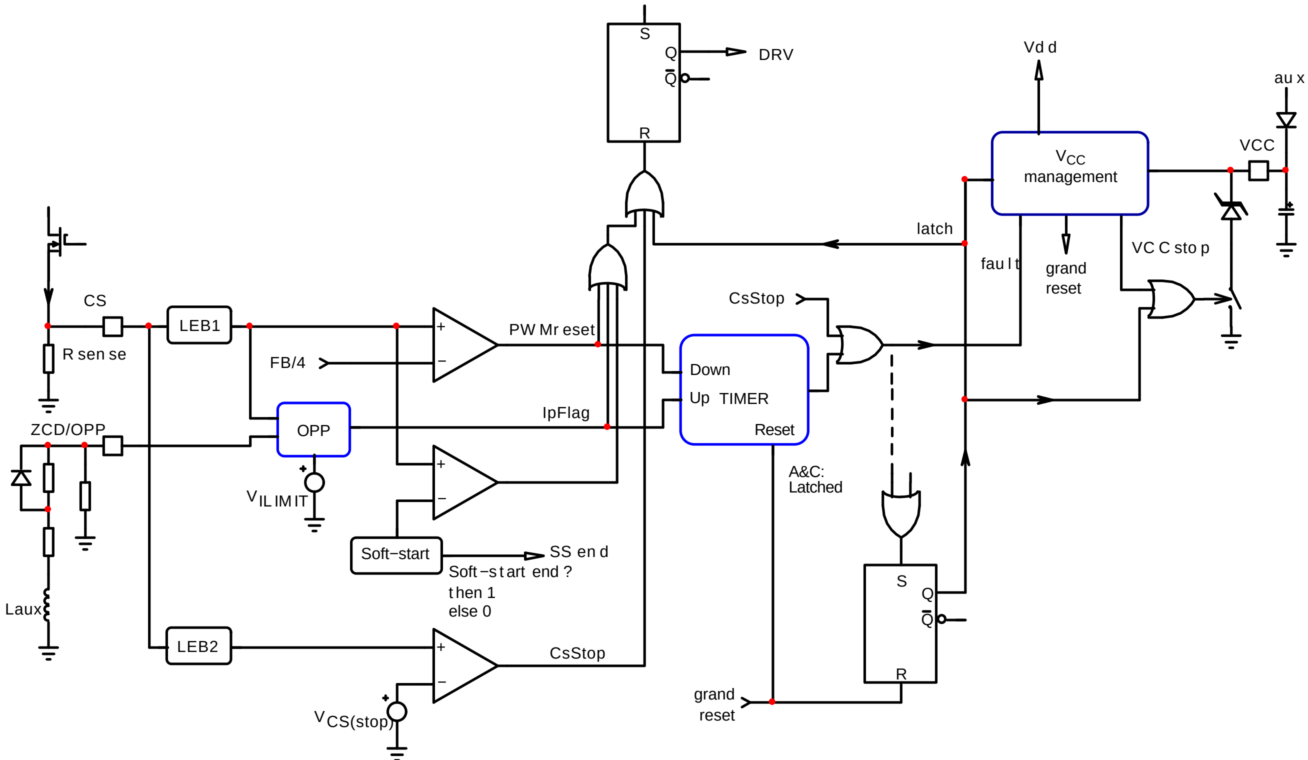


Figure 37. Overload Detection Schematic

When the current in the MOSFET is higher than V_{ILIM} / R_{sense}, “Max Ip” comparator trips and the digital timer starts counting: the timer count is incremented each 10 ms. When the current comes back within safe limits, “Max Ip” comparator becomes silent and the timer count down: the timer count is decremented each 10 ms. In normal overload conditions the timer reaches its completion when it has counted up 8 times 10 ms.

On B and D version, when the timers reaches its completion, the circuit enter auto−recovery mode: the circuit stops all operations and V_{CC} decreases via the circuit own consumption (I_{CC1}). When V_{CC} reaches $V_{CC(off)}$, the circuit goes in startup mode and restart switching. (see Figure 38) This ensures a low duty−cycle burst operation in fault mode.

On A and C versions, when the timers finishes counting 80 ms, the circuit goes in latch mode (Figure 39): the DRV pulses stop and V_{CC} is pulled down to $V_{CC(latch)}$ which is 7.2 V typically. The circuit un−latches when the current circulating in V_{CC} pin drops below $I_{CC(latch)}$.

In parallel to the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a threshold of 1.2 V is able to sense winding short−circuit and immediately shut down the controller. Depending on the version, this additional protection is either latched or auto−recovery, according to the overload protection behavior.

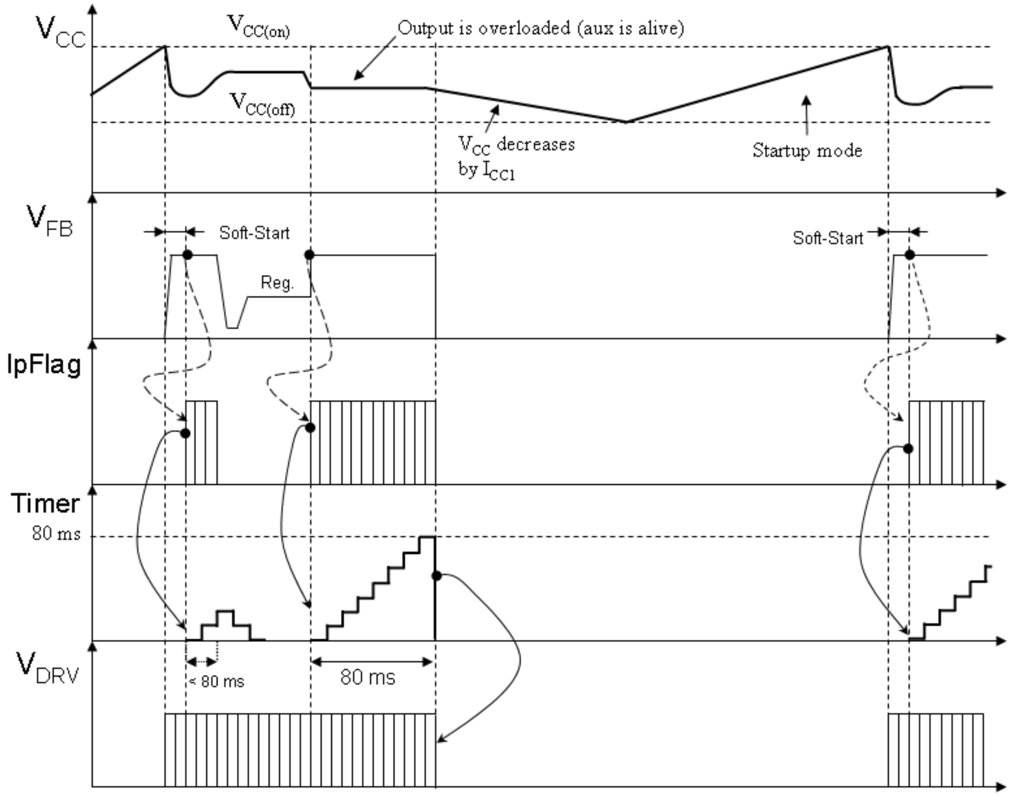


Figure 38. Auto−Recovery Short−Circuit Protection on B and D Versions

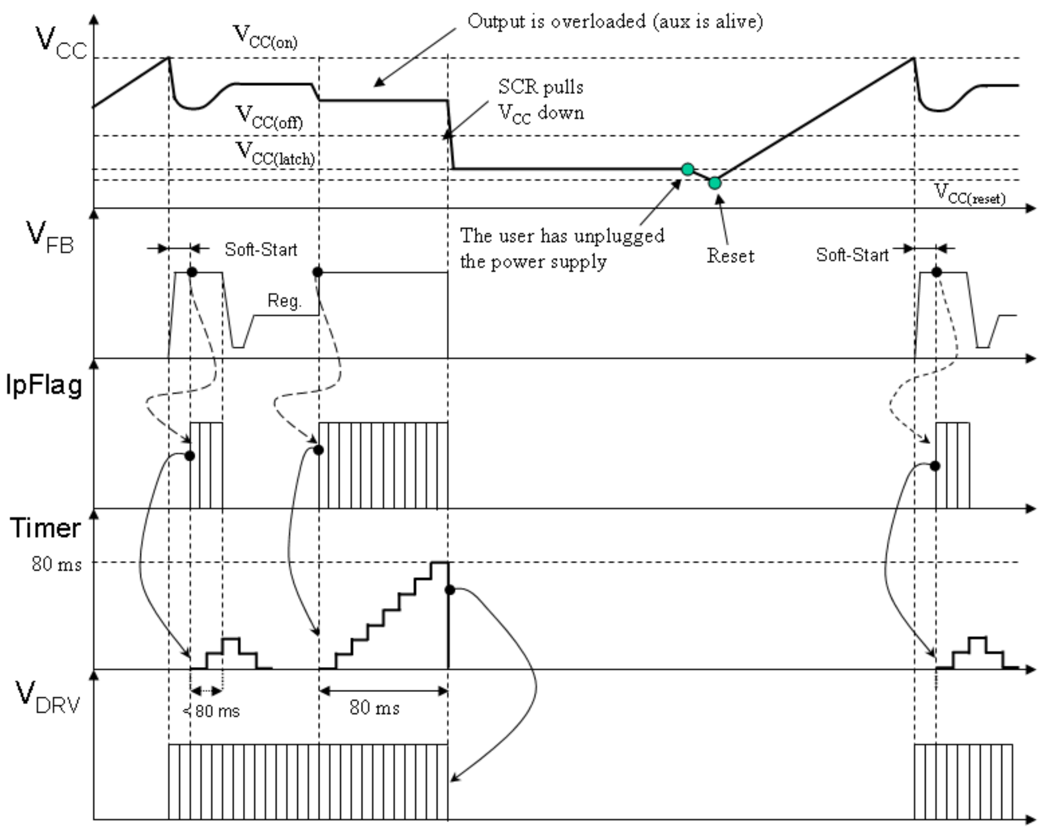


Figure 39. Latched Short−Circuit Protection on A and C Versions

OVER POWER COMPENSATION

The over power compensation is achieved by monitoring the signal on ZCD pin (pin 1). Indeed, a negative voltage applied on this pin directly affects the internal voltage reference setting the maximum peak current (Figure 40).

When the power MOSFET is turned−on, the auxiliary winding voltage becomes a negative voltage proportional to the input voltage. As the auxiliary winding is already connected to ZCD pin for the valley detection, by selecting the right values for R_{opu} and R_{opl}, we can easily perform over power compensation.

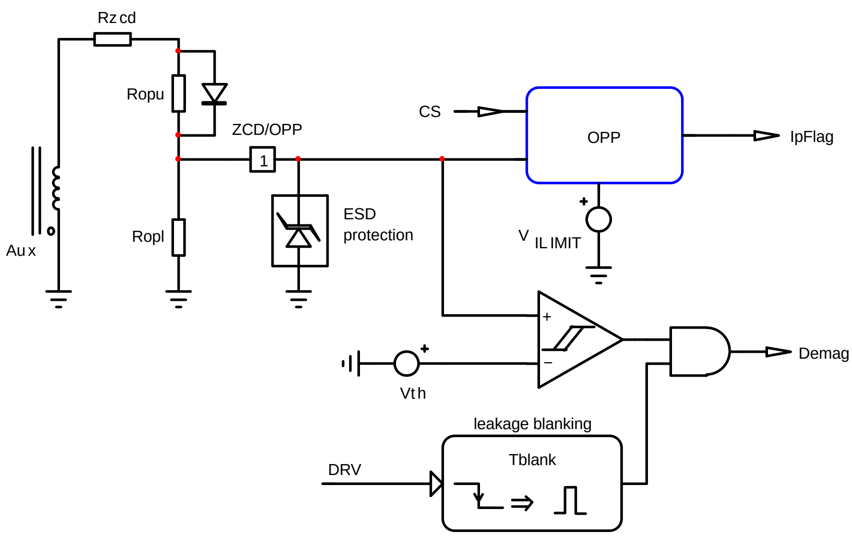


Figure 40. Over Power Compensation Circuit

To ensure optimal zero−crossing detection, a diode is needed to bypass R_{opu} during the off−time.

If we apply the resistor divider law on the pin 1 during the on−time, we obtain the following relationship:

$$\frac{R_{ZCD} + R_{opu}}{R_{opl}} = -\frac{N_{p,aux}V_{in} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 2)}$$

Where:

$N_{p,aux}$ is the auxiliary to primary turn ration: $N_{p,aux} = N_{aux} / N_p$

V_{in} is the DC input voltage

V_{OPP} is the negative OPP voltage

By selecting a value for R_{opl}, we can easily deduce R_{opu} using Equation 2. While selecting the value for R_{opl}, we must be careful not choosing a too low value for this resistor in order to have enough voltage for zero−crossing detection during the off−time. We recommend having at least 8 V on ZCD pin, the maximum voltage being 10 V.

During the off−time, ZCD pin voltage can be expressed as follows:

$$V_{ZCD} = \frac{R_{opl}}{R_{ZCD} + R_{opl}}\left(V_{aux} - V_d\right) \quad \text{(eq. 3)}$$

We can thus deduce the relationship between R_{opl} and R_{ZCD}:

$$\frac{R_{ZCD}}{R_{opl}} = \frac{V_{aux} - V_d - V_{ZCD}}{V_{ZCD}} \quad \text{(eq. 4)}$$

Design example:

$V_{aux} = 18$ V

$V_d = 0.6$ V

$N_{p,aux} = 0.18$

If we want at least 8 V on ZCD pin, we have:

$$\frac{R_{ZCD}}{R_{opl}} = \frac{V_{aux} - V_d - V_{ZCD}}{V_{ZCD}} = \frac{18 - 0.6 - 8}{8} \approx 1.2 \quad \text{(eq. 5)}$$

We can choose: $R_{ZCD} = 1$ kΩ and $R_{opl} = 1$ kΩ.

For the over power compensation, we need to decrease the peak current by 37.5% at high line (370 Vdc). The corresponding OPP voltage is:

$$V_{OPP} = 0.375 \times V_{ILIM} = -300\text{ mV} \quad \text{(eq. 6)}$$

Using Equation 2, we have:

$$\frac{R_{ZCD} + R_{opu}}{R_{opt}} = -\frac{N_{p,aux}V_{lin} - V_{OPP}}{V_{OPP}} = \frac{-0.18 \times 370 - (-0.3)}{(-0.3)} = 221 \quad \text{(eq. 7)}$$

Thus,

$$R_{opu} = 221_{Ropl} - R_{ZCD} = 221 \times 1k - 1k = 220\text{ k}\Omega \quad \text{(eq. 8)}$$

OVERVOLTAGE/OVERTEMPERATURE DETECTION (A AND B VERSIONS)

Overvoltage and overtemperature detection is achieved by reading the voltage on pin 7 (See Figure 41).

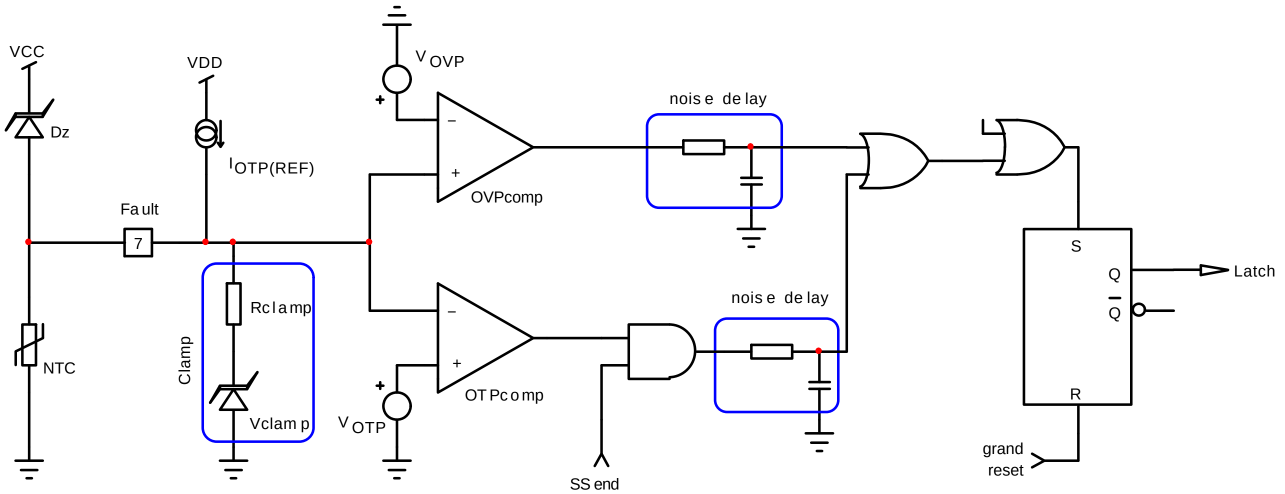


Figure 41. OVP/OTP Circuitry

The $I_{OTP(REF)}$ current (91 μA typ.) biases the Negative Temperature Coefficient sensor (NTC), naturally imposing a dc voltage on the OTP pin. An internal clamp limit the pin 7 voltage to 1.2 V when the NTC resistance is high (For example, at 25°C, R_{NTC} > 100 kΩ). When the temperature increases, the NTC's resistance reduces bringing the pin 7 voltage down until it reaches a typical value of 0.8 V: the comparator trips and latches−off the controller (see Figure 42).

In case of overvoltage, the zener diode starts to conduct and inject current inside the internal clamp resistor R_{clamp} thus causing the pin 7 voltage to increase. When this voltage reaches the OVP threshold (2.5 V typ), the controller is latched−off: all the DRV pulses stops and V_{CC} is pulled−down to $V_{CC(latch)}$ (7.2 V typ). The circuit un−latches when the current circulating in V_{CC} pin drops below $I_{CC(latch)}$, thus the user must unplug and replug the power supply.

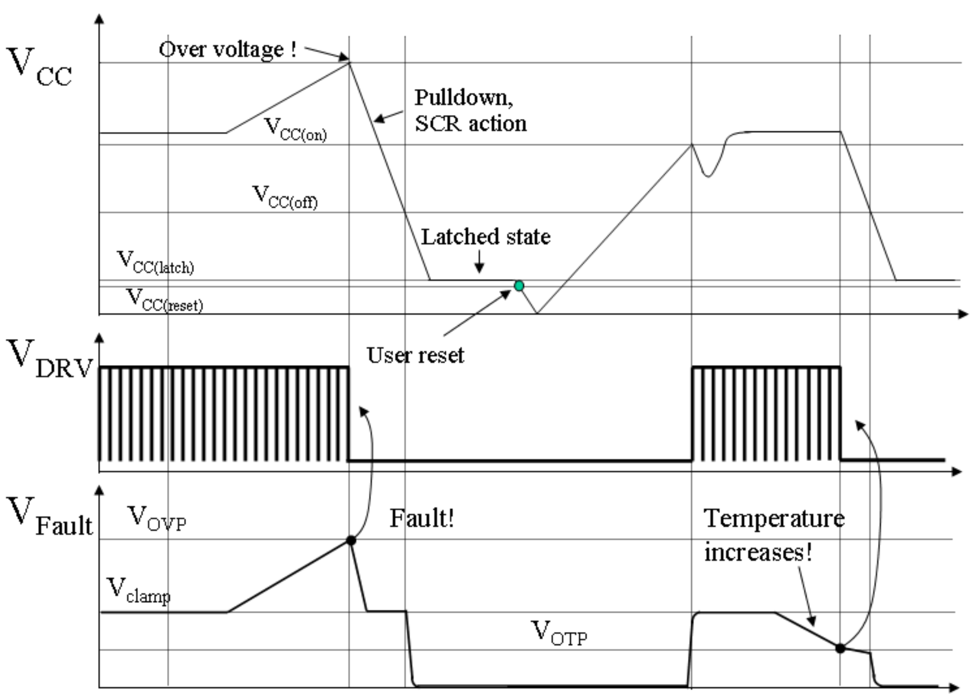


Figure 42. Overvoltage and Overtemperature Chronograms

OVERVOLTAGE PROTECTION/BROWN−OUT (C AND D VERSIONS)

The C and D versions of NCP1380 combine brown−out and overvoltage detection on pin 7.

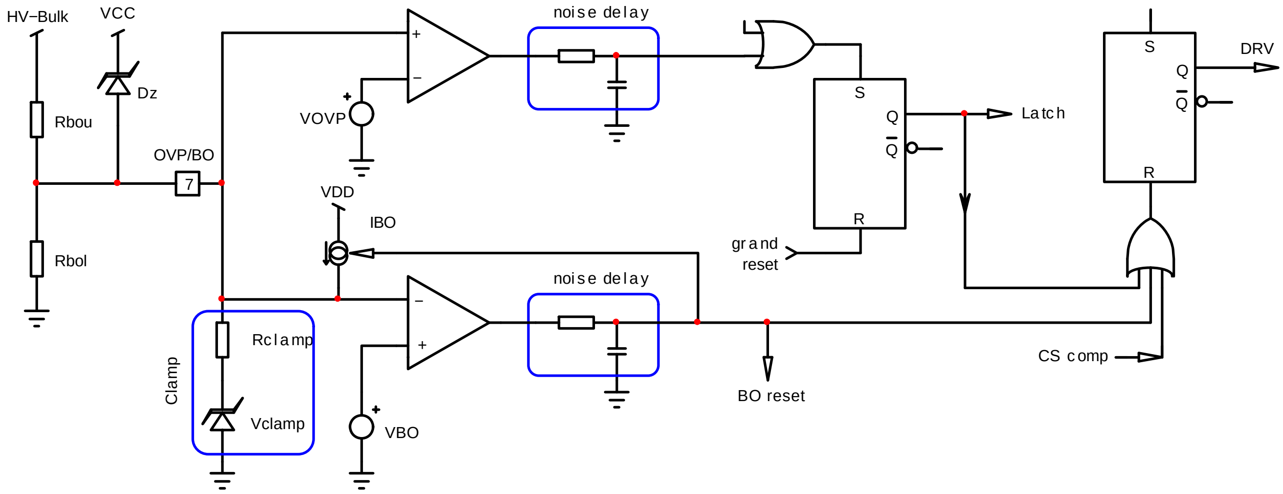


Figure 43. Brown−out and Overvoltage Protection

In order to protect the power supply against low input voltage condition, the pin 7 permanently monitors a fraction of the bulk voltage through a voltage divider. When this image of bulk voltage is below the V_{BO} threshold, the controller stops switching. When the bulk voltage comes back within safe limits, the circuit will restart pulsing only when V_{CC} reaches $V_{CC(on)}$ (Figure 44): this ensures a clean startup sequence with soft−start. The hysteresis for the brown−out function is implemented with a high side current source sinking 10 μA when the brown−out comparator is high ($V_{bulk} < V_{bulk(on)}$)

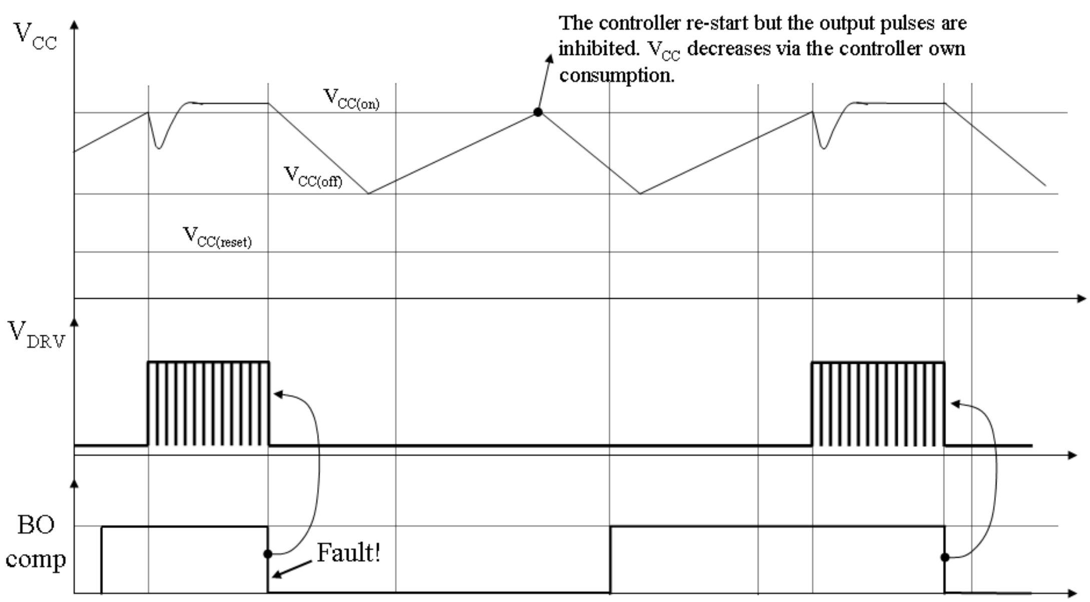


Figure 44. Brown−out Operating Chronograms

In order to avoid having a too high voltage on pin 7 if the bulk voltage is high, an internal clamp limits the voltage.

In case of overvoltage, the zener diode will start to conduct and inject current inside the internal clamp resistor R_{clamp} thus causing pin 7 voltage to increase. When this voltage reaches V_{OVP}, the controller latches−off and stays latched until the user cycles down the power supply (Figure 45).

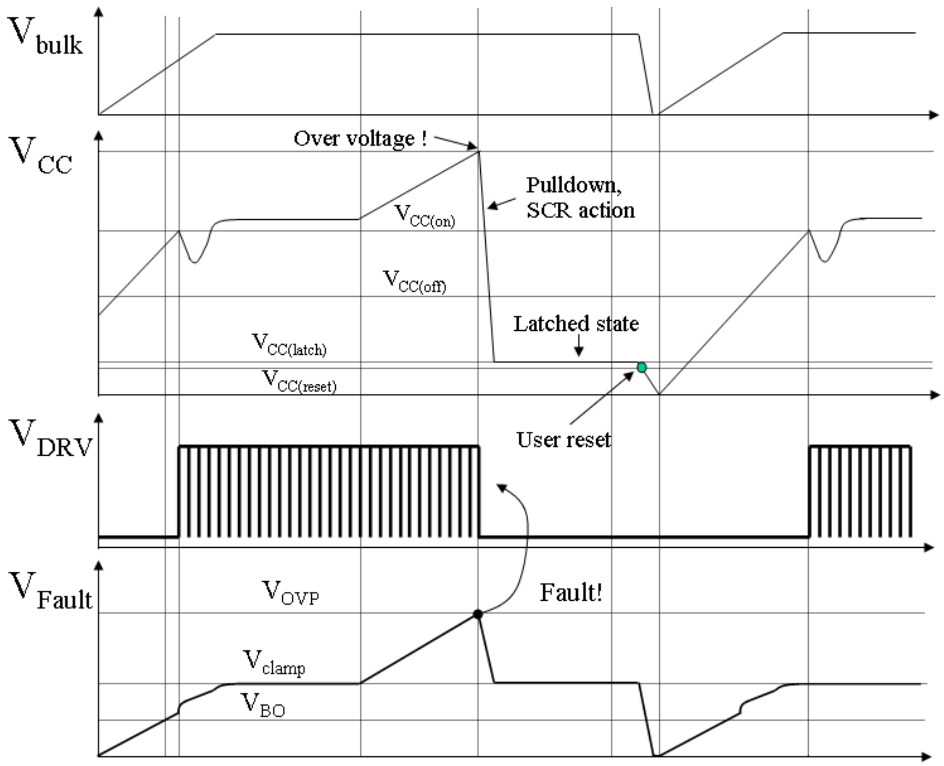


Figure 45. Operating Chronograms in Case of Overvoltage

The following equations show how to calculate the brownout resistors.

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulk(on)}$) and the bulk voltage for shutdown ($V_{bulk(off)}$). Then use the following equation to calculate R_{bou} and R_{bol}.

$$R_{bol} = \frac{V_{BO}\left(V_{bulk(on)} - V_{bulk(off)}\right)}{I_{BO}\left(V_{bulk(on)} - V_{BO}\right)} \qquad \text{(eq. 9)}$$

$$R_{bou} = \frac{R_{bol}\left(V_{bulk(on)} - V_{BO}\right)}{V_{BO}} \qquad \text{(eq. 10)}$$

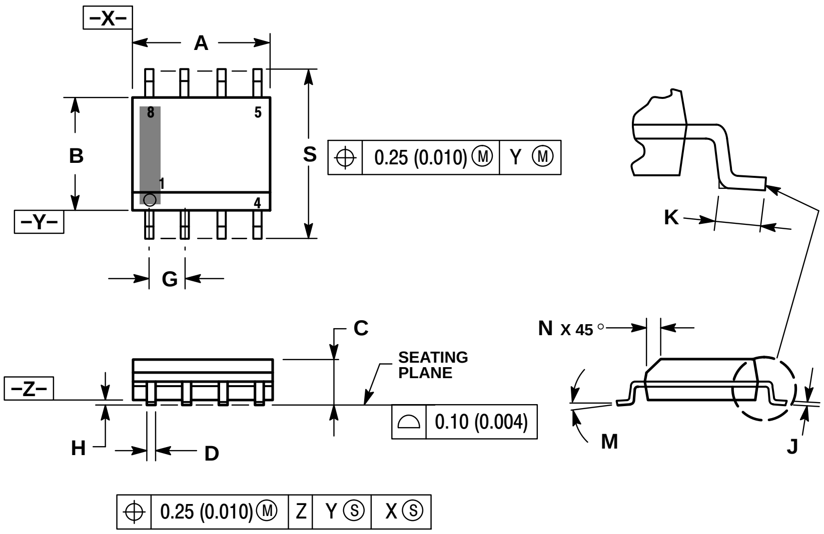
ORDERING INFORMATION

Device	Package	Shipping†
NCP1380ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1380BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1380CDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1380DDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

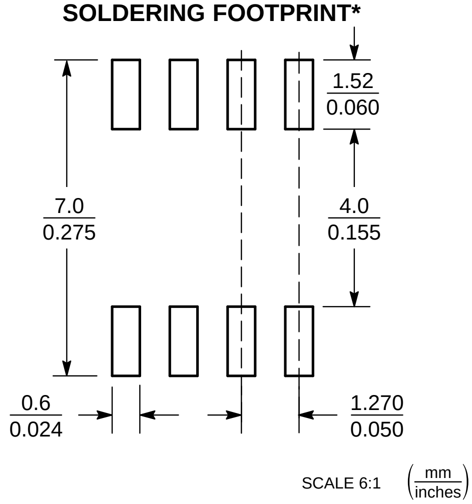
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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