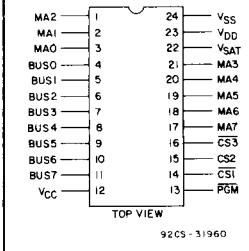


TERMINAL ASSIGNMENT

256-Word x 8-Bit Static EPROM (Erasable/ Programmable Read-Only Memory)

Features:

- *Static silicon-gate CMOS circuitry—CD4000-series compatible*
- *Compatible with CDP1800-series microprocessors*
- *Single voltage supply (during READ): 4-6.5 V*
- *Low power dissipation (READ): 20 mW typ.*
- *Fast access time: 1 μs max.*
- *Fast programming time: 5 sec. typ.*
- *Data retention (125°C): 17.3 years typ.*
- *Write/erase endurance > 300 cycles*
- *3-state outputs, TTL compatible*
- *Functional replacement for 1700-series UV erasable PROMs*

The RCA-CDP18U42C is a static CMOS, 2048-bit programmable read-only memory, organized as 256 words by 8 bits. It is compatible with the CDP1802 microprocessor and will interface directly with the CDP1802 as shown in the system diagram (Fig. 1). The CDP18U42C has common data inputs and data outputs and utilizes a single power supply during read operations. RCA ion-implanted, silicon-gate, CMOS technology is employed in the CDP18U42C. Three CHIP-SELECT signals ($\overline{CS1}$, CS2, CS3) are provided. The device is designed for systems where simplicity and low power are desirable.

The CDP18U42C is ultraviolet erasable and electrically programmable, making it ideally suited for experimentation and other uses where rapid design changes are necessary. Complete programming and functional testing are performed on each device prior to shipment.

The CDP18U42C is supplied in a 24-lead hermetic dual-in-line ceramic package (D suffix) having a window in the lid which is transparent to ultraviolet light.

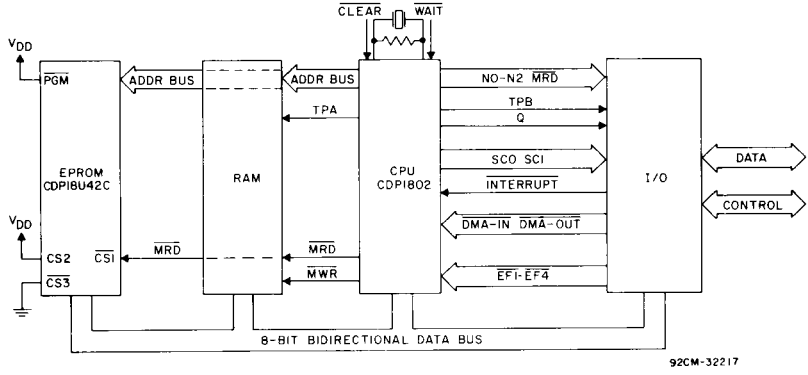


Fig. 1 — Typical CDP1802 microprocessor system using the CDP18U42CD.

Printed in USA/11-79

Erasing Procedure

The CDP18U42CD may be erased when exposed to high-intensity short-wave ultraviolet light at a wavelength of 2537 Angstroms. An example of an ultraviolet light source which will erase a CDP18U42CD in 5 to 20 minutes is the Ultra Violet Products Model S-52T lamp, which should be used without short-wave filters and with the PROM placed within 1 inch of the lamp tubes.

The erase procedure is a bulk erase in which all 2048 bits (256 x 8) assume a 0 state (OUTPUTS = LOW), allowing the user to program a new bit pattern.

The erase characteristics of the CDP18U42CD are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. It should be noted that light from the sun and from certain types of fluorescent lamps contains wavelengths in the 3000-4000 Angstrom range. Extended exposure of the CDP18U42CD to these types of lighting conditions will require opaque labels to be placed over the transparent lid to prevent unintentional erasure.

Programming Procedure

After being erased, the CDP18U42C exhibits a zero state (OUTPUT = LOW) in all locations. Programming is accomplished by introducing a 1 state (OUTPUT = HIGH) in the desired bit locations. Programming is done on a byte basis, in which any previously erased bits may be selectively programmed to a 1 state. This feature allows the user to change any 0 bits to 1's within a particular byte in an already programmed CDP18U42C without having to do a bulk program or a bulk erase. The program procedure consists of addressing a word, selecting the CDP18U42C, with the PGM (PROGRAM) input at a logic 0 (V_{SS}), and raising the V_{DD} and V_{SAT} inputs to the proper program voltage (22 V typ.). The data to be programmed is applied to the BUS0-BUS7 inputs. See Fig. 3.

Read Procedure

During a read operation, the CDP18U42C functions as a normal CMOS ROM. The read procedure consists of addressing a word and selecting the CDP18U42C, with the PGM input at a logic 1 (V_{DD},V_{SAT} = V_{CC}). Data is read at the BUS0-BUS7 outputs. See Fig. 4.

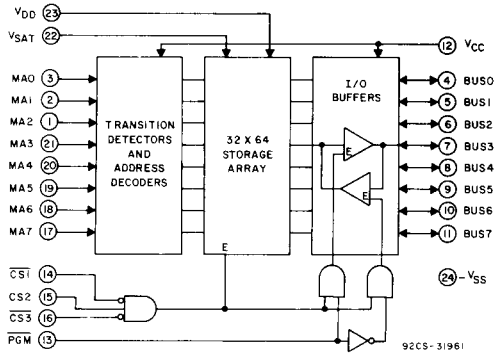


Fig. 2 — Block diagram for CDP18U42CD.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE
(All voltage values referenced to V_{SS} terminal)

V_{CC} (READ, PROGRAM)	−0.5 to 7 V
V_{DD} (READ)	−0.5 to 7 V
V_{DD} (PROGRAM)	−0.5 to 25 V
V_{SAT} (READ)	−0.5 to 7 V
V_{SAT} (PROGRAM)	−0.5 to 25 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
OPERATING-TEMPERATURE RANGE (T_A)	−40 to +85 °C
STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, unless otherwise noted.

CHARACTERISTIC	CONDITIONS					LIMITS			UNITS
	V_O (V)	V_{IN} (V)	V_{CC} (V)	V_{DD} (V)	V_{SAT} (V)	CDP18U42CD			
						Min.	Typ.*	Max.	
Quiescent Device Current: Read Operation									μA
I_{CC}	—	0,5	5	5	5	—	10	100	
I_{DD}	—	0,5	5	5	5	—	10	100	
I_{SAT}	—	0,5	5	5	5	—	1	10	
Program Operation									
I_{CC}	—	0,5	5	22	22	—	10	100	
I_{DD}	—	0,5	5	22	22	—	10	100	
I_{SAT}	—	0,5	5	22	22	—	1	10	
Output Low Drive (Sink Current) I_{OL}	0.4	0,5	5	—	—	1.6	2	—	mA
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	—	—	−1.6	−2	—	
Output Voltage (Low Level) V_{OL}	—	0,5	5	—	—	—	0	0.05	V
Output Voltage (High Level) V_{OH}	—	0,5	5	—	—	4.95	5	—	
Input Voltage (Low Level) V_{IH}	0.5,4.5	—	5	—	—	—	—	1.5	V
Input Voltage (High Level) V_{IL}	0.5,4.5	—	5	—	—	3.5	—	—	
Input Leakage Current I_{IN}	0.5,4.5	Any Input	5	—	—	—	—	±1	μA
3-State Output Leakage Current I_{OUT}	—	0,5	5	—	—	—	±1	±5	
Input Capacitance C_{IN}	Any Input					—	5	7.5	pF
Output Capacitance C_{OUT}	Any Output					—	5	7.5	

*Typical values are for $T_A = 25$ °C.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS	UNITS
Read Operation:		
Supply Voltage Range V_{CC}, V_{DD}, V_{SAT}	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{CC}	
Program Operation:		
Supply Voltage Range V_{CC}	4 to 6.5	
Supply Voltage Range V_{DD}, V_{SAT}	18 to 22	V
Input Voltage Range	V_{SS} to V_{CC}	
Input Signal Rise Or Fall Times t_r,t_f	⩽ 5	μs

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; V_{CC}, V_{DD}, $V_{SAT} \pm 5\%$; Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC		CONDITIONS V_{CC} (V)	CONDITIONS V_{DD} (V)	CONDITIONS V_{SAT} (V)	TYPICAL VALUES	UNITS
Read Operation						
Read Cycle Time	t_{RC}				1000	ns
Access Time From Address Change	t_M	5	5	5	1000	ns
Access Time From Chip Select	t_{ACS}	5	5	5	1000	ns
Address Setup Time	t_{AS}	5	5	5	0	ns
Address Hold Time	t_{AH}	5	5	5	0	ns
Bus Contention Delay	t_D	5	5	5	50	ns
Output Hold Time From Address Change	t_{OHA}	5	5	5	50	ns
Output 3-State From Deselection	t_{OTD}	5	5	5	50	ns
Access Time From $\overline{PGM}$	t_{AP}	5	5	5	1000	ns
Program Operation						
Program Cycle Time	t_{PC}	5	18	18	10	ms
		5	22	22	0.1	
Address Setup Time	t_{AS}	5	18,22	18,22	0	ns
Address Hold Time	t_{AH}	5	18,22	18,22	0	ns
PGM To Outputs Inactive	t_{PX}	5	18,22	18,22	200	ns
Chip Select To Program Setup Time	t_{CS}	5	18,22	18,22	500	ns
Chip Select To Program Hold Time	t_{CH}	5	18,22	18,22	200	ns
$\overline{PGM}$ To Program Voltage Setup Time	t_{PS}	5	18,22	18,22	500	ns
$\overline{PGM}$ To Program Voltage Hold Time	t_{PH}	5	18,22	18,22	200	ns
Data Setup Time	t_{DS}	5	18,22	18,22	200	ns
Data Hold Time	t_{DH}	5	18,22	18,22	200	ns
Program Voltage Pulse Width	t_{PVW}	5	18	18	10	ms
		5	22	22	0.1	
Program Voltage Rise Or Fall Time	t_{PR}, t_{PF}	5	18,22	18,22	2	μs

TABLE I - OPERATING MODES FOR CDP18U42CD

OPERATING MODE	V_{SS} (V)	V_{CC} (V)	V_{DD} (V	V_{SAT} (V)	$\overline{CS1}$ (V)	CS2 (V)	$\overline{CS3}$ (V)	$\overline{PGM}$ (V)	BUS 0-BUS 7
READ	0	5	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{CC}	OUTPUT
PROGRAM	0	5	18-22 	18-22 	V_{SS}	V_{CC}	V_{SS}	V_{SS}	INPUT
DESELECT	0	5	V_{CC}	V_{CC}	X	X	V_{CC}	V_{CC}	3-STATE
DESELECT	0	5	V_{CC}	V_{CC}	X	V_{SS}	X	V_{CC}	3-STATE
DESELECT	0	5	V_{CC}	V_{CC}	V_{CC}	X	X	V_{CC}	3-STATE

X = DON'T CARE

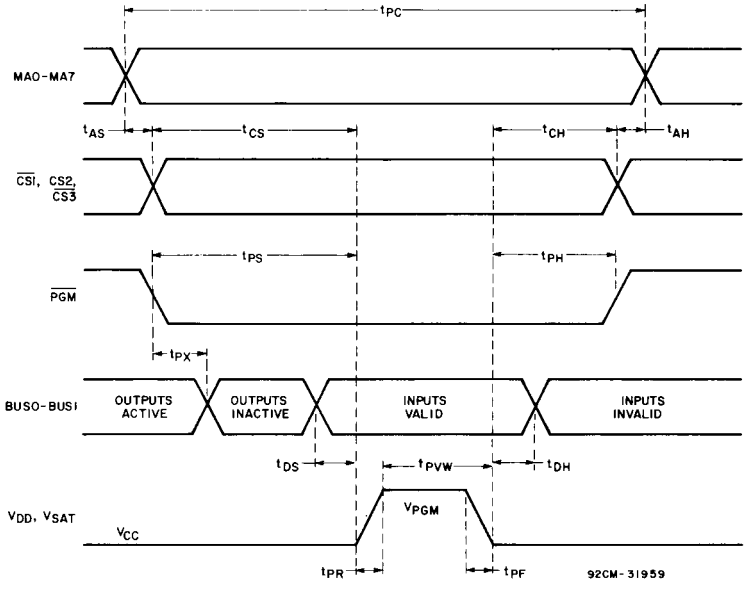


Fig. 3 — Program timing diagram.

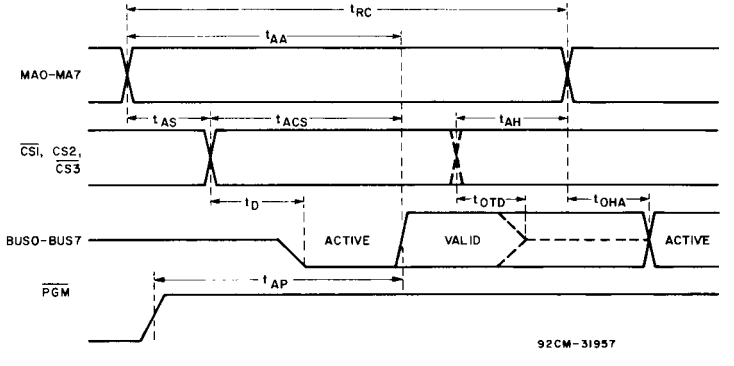


Fig. 4 — READ timing diagram.

TABLE II - POWER DISSIPATION FOR CDP18U42CD

OPERATION	CONDITIONS			TYPICAL VALUES*	UNITS
	V_{CC} (V)	V_{DD} (V)	V_{SAT} (V)		
READ QUIESCENT	5	5	5	0.05	mW
READ UNSELECTED (1 MHz)	5	5	5	10	mW
READ SELECTED (1 MHz)	5	5	5	20	mW
WRITE ALL 0'S	5	18	18	0.1	mW
	5	22	22	0.2	
WRITE ALL 1'S	5	18	18	120	mW
	5	22	22	300	

*Typical values are for $T_A = 25°C$.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

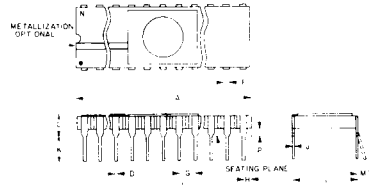
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

(D) SUFFIX
24-Lead Dual-In-Line Side-Brazed Ceramic Package
(With Transparent Window)



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.115	0.175		2.93	4.44
D	0.015	0.023		0.39	0.58
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.77	1.77
J	0.008	0.012	3	0.21	0.30
K	0.125	0.175		3.18	4.44
L	0.580	0.620	2	14.74	15.74
M	–	7		–	7
P	0.025	0.050		0.64	1.27
N	24			24	

92CM-32216

NOTES:

1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.