RENESAS

LOW-VOLTAGE 24-BIT BUS SWITCH

74CBTLV16211

FEATURES:

- + 5 Ω A/B bi-directional switch
- Isolation Under Power-Off Conditions
- Over-voltage tolerant
- Latch-up performance exceeds 100mA
- VCC = 2.3V 3.6V, normal range
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in TSSOP package

DESCRIPTION:

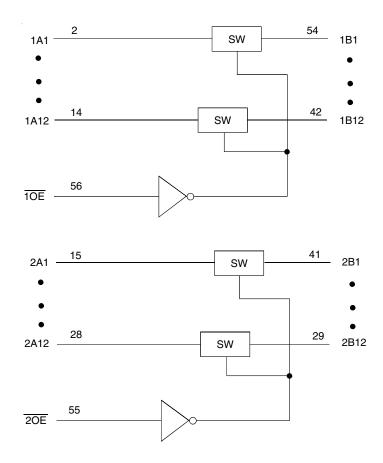
The CBTLV16211 operates as a single 24-bit bus switch or as a dual 12-bit bus switch, which provides high speed switching. This device has very low ON resistance, resulting in under 250ps propagation delay throughout the switch. When Output Enable (\overline{OE}) is low, the corresponding 12-bit bus switch is on and port A is connected to Port B. When \overline{OE} is high, the switch is off and a high impedance exists between Port A and Port B. To ensure the high-impedance state during power up or power down,

OE should be tied to Vcc through a pullup resistor.

APPLICATIONS:

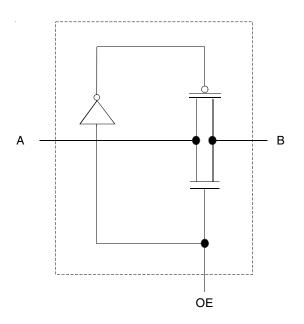
3.3V High Speed Bus Switching and Bus Isolation

FUNCTIONAL BLOCK DIAGRAM



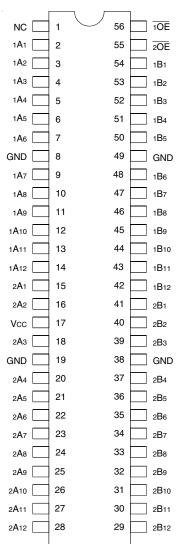
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SIMPLIFIED SCHEMATIC, EACH SWITCH



JUNE 2019

PIN CONFIGURATION



TOP VIEW

PackageType	Package Code	Order Code
TSSOP	PAG56	PAG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
Vcc	Supply Voltage Range	-0.5 to 4.6	V
Vi	Input Voltage Range	-0.5 to 4.6	V
	Continuous Channel Current	128	mA
Ік	Input Clamp Current, VI/O < 0	-50	mA
Тѕтс	Storage Temperature Range	-65 to +150	°C

NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description	
XOE	Output Enable (Active LOW)	
хАх	Port A Inputs or Outputs	
хВх	Port B Inputs or Outputs	

FUNCTION TABLE (EACH 12-BIT BUS SWITCH)⁽¹⁾

Input OE	Operation
L	A-Port = B-Port
Н	Disconnect

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

OPERATING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vcc	Supply Voltage		2.3	3.6	V
Vін	High-Level Control Input Voltage	Vcc = 2.3V to 2.7V	1.7	—	V
		Vcc = 2.7V to 3.6V	2	_	
VIL	Low-Level Control Input Voltage	Vcc = 2.3V to 2.7V	—	0.7	V
		Vcc = 2.7V to 3.6V	—	0.8	
TA	Operating Free-Air Temperature		40	+85	°C

NOTE:

1. All unused control inputs of the device must be held at Vcc or GND to ensure proper device operation.



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $TA = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
Vik	Control Inputs, Data I/O	Vcc = 3V, li = -18mA		_	—	-1.2	V
li	Control Inputs	Vcc = 3.6V, VI = Vcc or GNE)	_	—	±1	μA
loz	Data I/O	Vcc = 3.6V, Vo = 0V or 3.6V	switch disabled	—	—	5	μA
IOFF		Vcc = 0V, VI or Vo = 0V or 3	.6V	_	—	10	μA
lcc		Vcc = 3.6V, Io = 0, VI = Vcc or GND		_	—	10	μA
$\Delta lcc^{(2)}$	Control Inputs	Vcc = 3.6V, one input at 3V, other inputs at Vcc or GND		_	—	300	μA
Сі	Control Inputs	VI = 3V or 0		_	4	—	pF
CIO(OFF)		Vo = 3V or 0, \overline{OE} = Vcc		—	6.5	—	pF
	Max. at Vcc = 2.3V	VI = 0 IO = 64mA		—	5	8	
	Typ. at Vcc = 2.5V		lo = 24mA	_	5	8]
Ron ⁽³⁾		VI = 1.7V	lo = 15mA	—	27	40	Ω
		VI = 0	lo = 64mA	_	5	7	
	Vcc = 3V		lo = 24mA		5	7	
		VI = 2.4V	lo = 15mA	_	10	15	

NOTES:

1. Typical values are at 3.3V, +25°C ambient.

2. The increase in supply current is attributable to each input that is at the specified voltage level rather than Vcc or GND.

3. This is measured by the voltage drop between the A and B terminals at the indicated current through the switch.

SWITCHING CHARACTERISTICS

		$V_{CC} = 2.5V \pm 0.2V$		$Vcc = 3.3V \pm 0.3V$		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tPD ⁽¹⁾	Propagation Delay	—	0.15	—	0.25	ns
	A to B or B to A					
ten	Output Enable Time	1	7	1	6.2	ns
	OE to A or B					
tois	Output Disable time	1	7.2	1	7.7	ns
	OE to A or B					

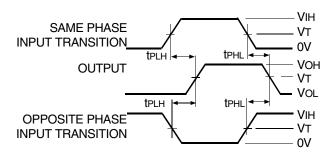
NOTE:

1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impededance).

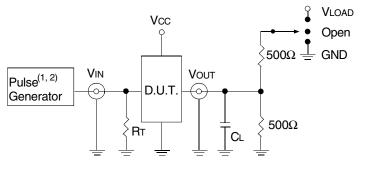
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc ⁽¹⁾ =3.3V±0.3V	Vcc ⁽²⁾ =2.5V±0.2V	Unit
VLOAD	6	2 x Vcc	V
Vін	3	Vcc	V
Vτ	1.5	Vcc / 2	V
Vlz	300	150	mV
Vнz	300	150	mV
CL	50	30	pF



Propagation Delay



Test Circuits for All Outputs

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

 $\mathsf{R}\mathsf{T}$ = Termination resistance: should be equal to $\mathsf{Z}\mathsf{O}\mathsf{U}\mathsf{T}$ of the Pulse Generator.

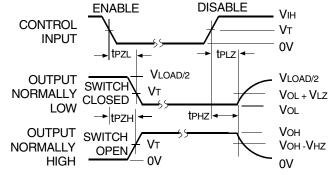
NOTES:

1. Pulse Generator for All Pulses: Rate \leq 10MHz; tF \leq 2.5ns; tR \leq 2.5ns.

2. Pulse Generator for All Pulses: Rate \leq 10MHz; tF \leq 2ns; tR \leq 2ns.

SWITCH POSITION

Test	Switch
tplz/tpzL	VLOAD
tрнz/tрzн	GND
tPD	Open



NOTE:

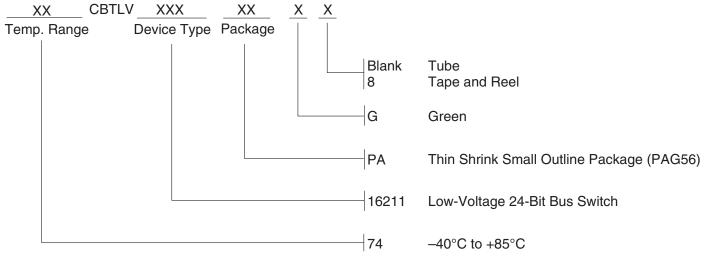
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



74CBTLV16211 LOW-VOLTAGE 24-BIT BUS SWITCH

ORDERINGINFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74CBTLV16211PAG	PAG56	TSSOP	I
	74CBTLV16211PAG8	PAG56	TSSOP	I

Datasheet Document History

 12/01/2014
 Pg. 2, 5
 Updated the ordering information by removing the "IDT" notation, obsolete packages "SSOP/TVSOP" and non RoHS part and by adding Tape and Reel information.

 06/03/2019
 Pg. 2,5
 Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail.

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TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

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