

TLV1117LVxxEVM-714 Evaluation Module

This User's Guide describes operational use of the TLV1117LVxxEVM-714 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TLV1117LVxx, low dropout linear regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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1 Introduction

The Texas Instruments TLV1117LVxxEVM-714 EVM helps design engineers to evaluate the operation and performance of the TLV1117LVxx family of linear regulators for possible use in their own circuit application. This particular EVM configuration contains a single linear regulator with internal thermal and current limit shutdowns circuitry in a small SOT-223 package. The regulator is capable of delivering up to 1A to the load depending on the input-output power dissipation across the part which can be minimized because of the very low dropout voltage. The input and output capacitors for the TLV1117LVxx need be 0.4 μ F (effective minimum) for stability; however, for conservative design practice accounting for widely varying noise environments, and dynamic line/load conditions, a 10- μ F capacitor has been employed at the input and output ports.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup and use the TLV1117LVxxEVM-714.

2.1 Input/Output Connectors and Jumper Descriptions

2.1.1 J1 –VIN

Input power supply voltage connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are greater than six inches. For example, an additional 47 μ F electrolytic capacitor connected from J1 to ground can improve the transient response of the TLV1117LVxx while eliminating unwanted ringing on the input due to long wire connections.

2.1.2 J2 –VOUT

Regulated output voltage connector.

2.1.3 J3 – GND

Ground-return connector for the input power supply.

2.1.4 J4– GND

Output ground-return connector.

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

2.3 Equipment Setup

- Turn off the input power supply after verifying that its output voltage is set to less than 6V. Connect the positive voltage lead from input power supply to V_{IN} , at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J3 connector of the EVM.
- Connect a 0-1A load between the output, V_{OUT} at connector J2, and ground, GND at connector J4.

3 Operation

- Turn on the input power supply. For initial operation it is recommended that the input power supply, V_{IN} – J1, be set to 5 V.
- Vary the respective loads and V_{IN} voltages as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TLV1117LV18EVM-714 printed-circuit board. These tests were performed with the 1.8-V version of the TLV1117LV18EVM-714 evaluation module.

4.1 Turn-on Sequence

Figure 1 shows the turn-on/off characteristic where 3.3V is applied to VIN. The output drives full load (1A). The output voltage startup ramp is not load dependant.

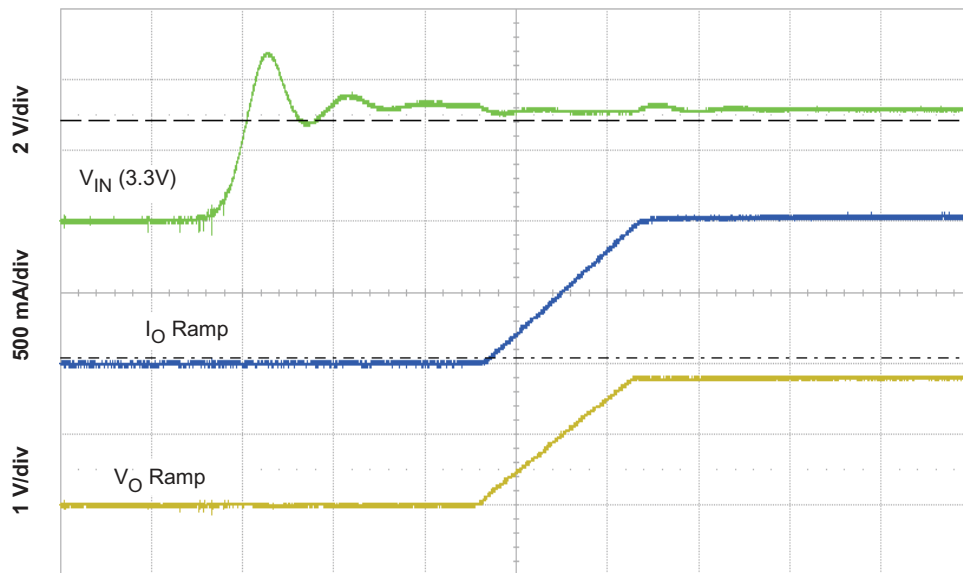


Figure 1. Turn-on Sequence: Green – V_{IN} (3.3 V), Blue – I_O Ramp, Yellow – V_O Ramp

4.2 Output Load Transient

Figure 2 shows the load transient response (V_{OUT} , yellow) for a load step transient from 100 mA to 500 mA (output current, I_O , blue). V_{IN} is set at 3.3 V.

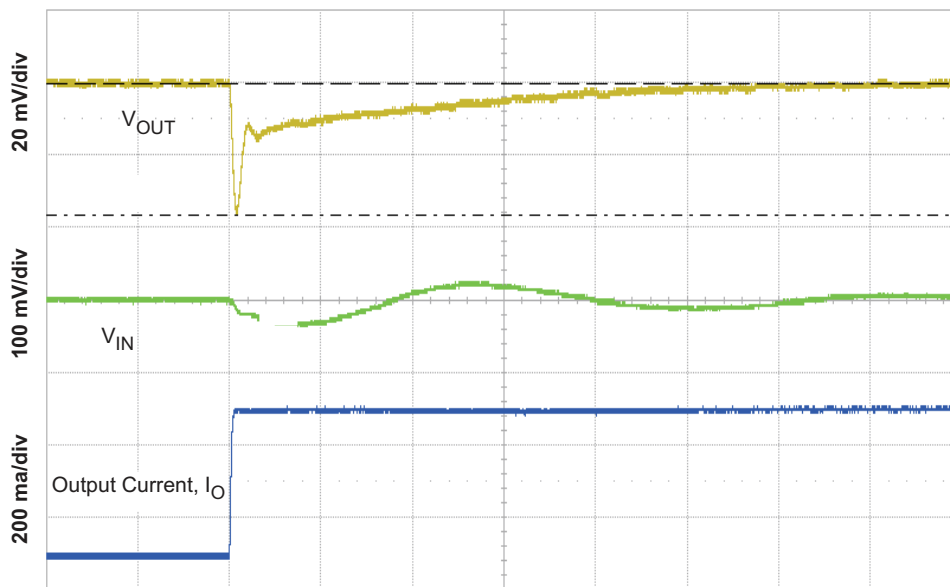


Figure 2. Load step and Transient Response: Yellow – V_{OUT} , Green – V_{IN} , Blue – Output Current, I_O

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \tag{1}$$

Where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device (Watts), and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, T_J , must not be allowed to exceed 150°C. The layout design must use copper trace and plane areas smartly, as thermal sinks, in order not to allow T_J to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The layout should consider carefully the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 4 shows the PCB top V_{OUT} plane has twenty-four 6-mil thermal via connections to the bottom side copper V_{OUT} plane to dissipate heat. The PCB is a two layer board with 2oz. copper on top and bottom layers. The DCY package drawing can be found at the Texas Instruments web site in the product folder for the TLV1117LVxx LDO.

Table 1 repeats information from the Dissipation Ratings Table of the TLV1117LV series data sheet for comparison with the thermal resistance, θ_{JA} , calculated for this EVM layout to show the wide variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC High-K (2s2p) board having dimensions of 3-inch x 3-inch with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_{JA} , and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation Without Derating ($T_A = 25^\circ\text{C}$)	Max Dissipation Without Derating ($T_A = 70^\circ\text{C}$)
High-K	DCY	62.9°C/W	1.59 W	874 mW
TLV1117LVxxEVM-714	DCY	47.8°C/W	2.615 W	1.674 W

6 Board Layout

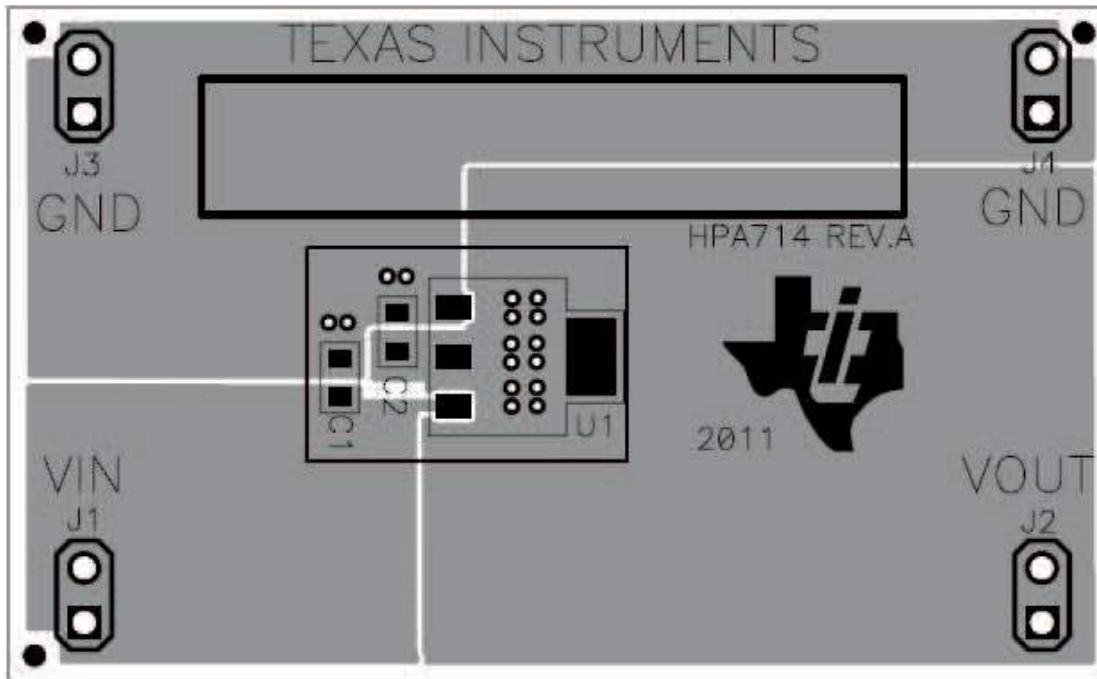


Figure 3. Assembly Layer

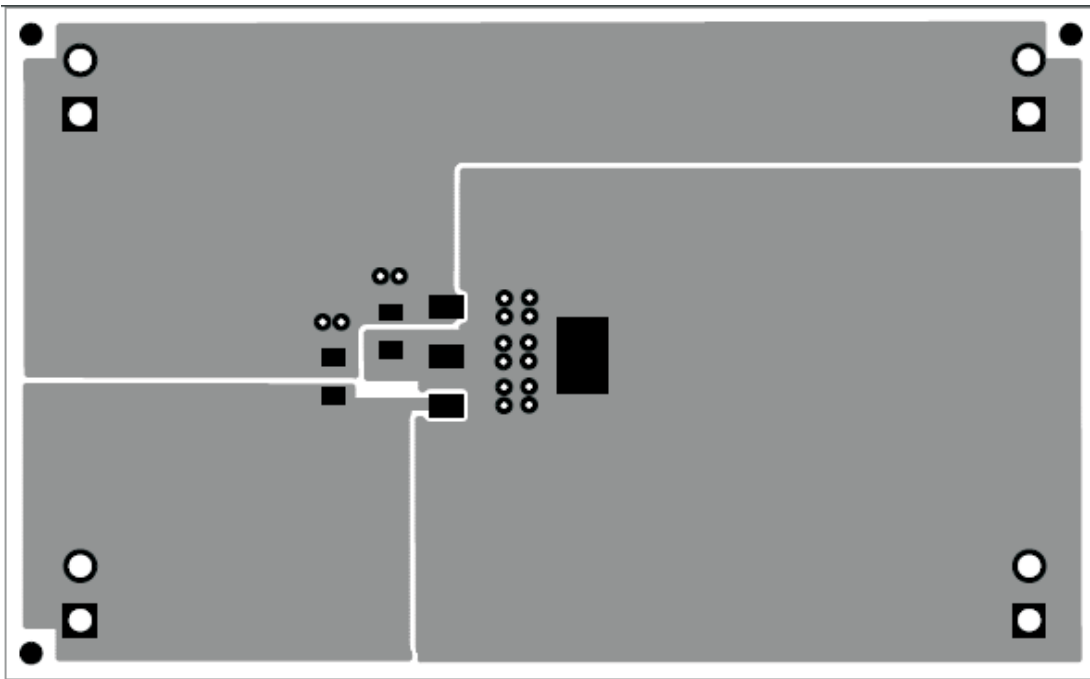


Figure 4. Top Layer Routing

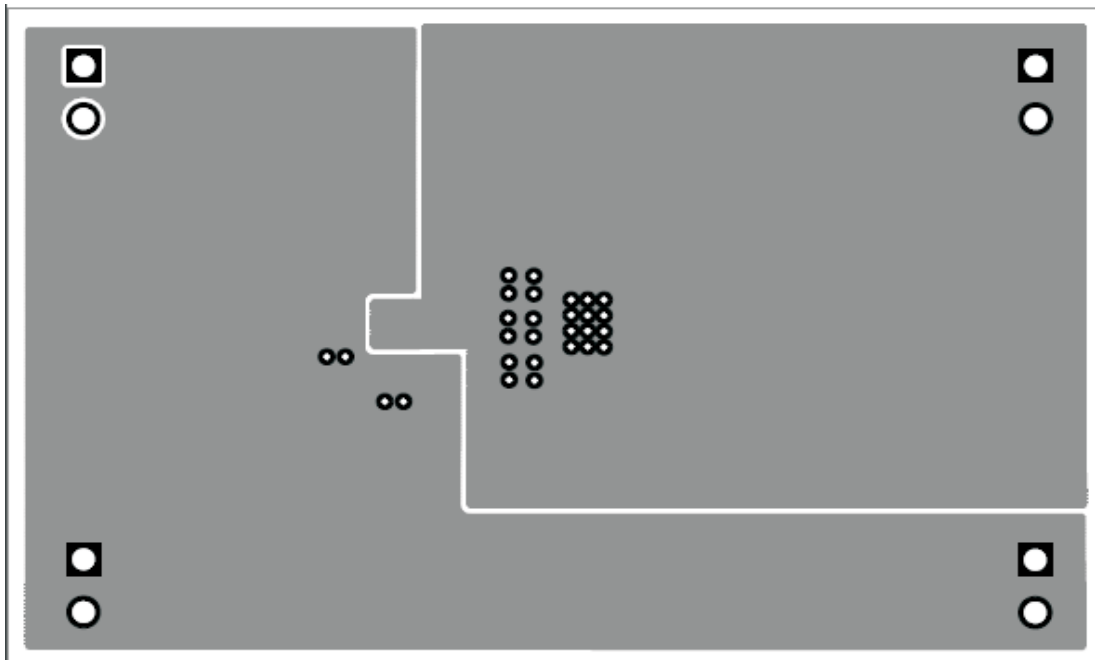
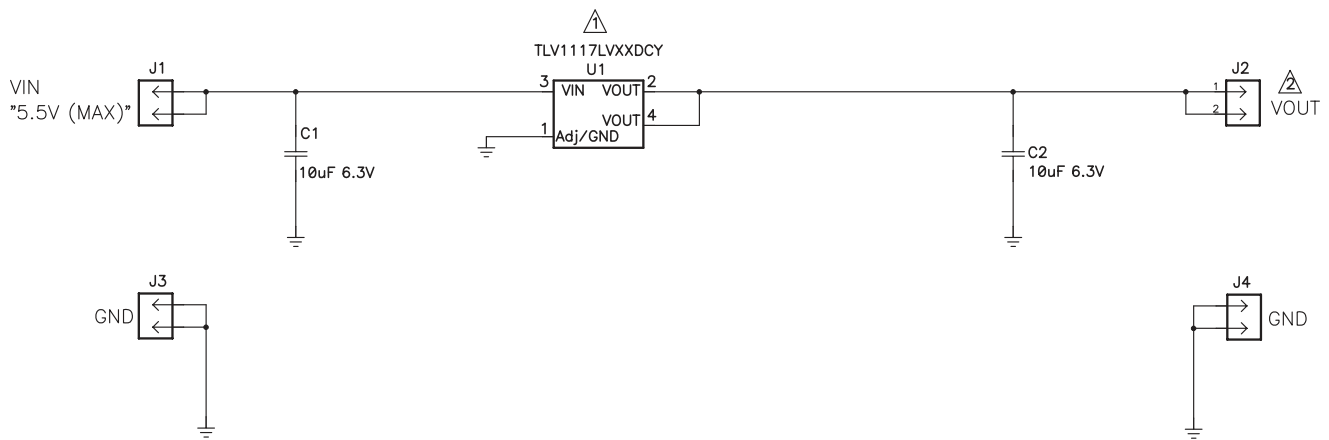


Figure 5. Bottom Layer Routing



NOTES
 ▲ SEE BOM FOR INSTALLE
 ▲ SEE TABLE BELOW

ASSY	U1	VOUT	IOUT MAX
-001	TLV1117LV18DCY	1.8V	1.0A
-002	TLV1117LV33DCY	3.3V	1.0A

Figure 6. TLV1117LVxxEVM-714 Schematic

7 Bill of Material

Table 2. TLV1117LVxxEVM-714 Bill of Materials

Count		RefDes	Value	Description	Size	Part Number	MFR
-001	-002	C1, C2	10uF	Capacitor, Ceramic, Low Inductance, 6.3 V, X5R, 20%	0603	STD	STD
4	4	J1, J2, J3, J4		Header, Male 2-pin, 100 mil spacing	0.100 in. x 2	PEC02SAAN	Sullins
1	0	U1		IC, 1A, Positive Fixed Voltage, LDO Regulator	SOT-223	TLV1117LV18DCY	TI
0	1	U1		IC, 1A, Positive Fixed Voltage, LDO Regulator	SOT-223	TLV1117LV33DCY	TI
1	1	—		2.00 x 1.240 x 0.062 inch 2 layer 2oz. PCB	2.0 x 1.240 inch.	HPA714	Any
1	1	—		Label	1.25 x 0.25 inch	THT-13-457-10	Brady

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2V to 6V and the output voltage range of Not to exceed 6V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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