

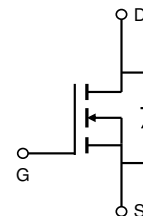
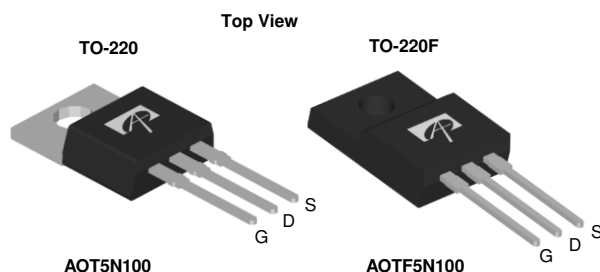
### General Description

The AOT5N100 & AOTF5N100 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability this parts can be adopted quickly into new and existing offline power supply designs.

### Product Summary

$V_{DS}$	1100@150°C
$I_D$ (at $V_{GS}=10V$ )	4A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 4.2Ω

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	AOT5N100	AOTF5N100	Units
Drain-Source Voltage	$V_{DS}$	1000		V
Gate-Source Voltage	$V_{GS}$	±30		V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	4	4*
		$T_C=100^\circ C$	2.5	2.5*
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	15		A
Avalanche Current <sup>C</sup>	$I_{AR}$	2.8		A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	117		mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	235		mJ
Peak diode recovery dv/dt	dv/dt	5		V/ns
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	195	42
		Derate above 25°C	1.6	0.3
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	$T_L$	300		°C

### Thermal Characteristics

Parameter	Symbol	AOT5N100	AOTF5N100	Units
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink <sup>A</sup>	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.64	3	°C/W

\* Drain current limited by maximum junction temperature.

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

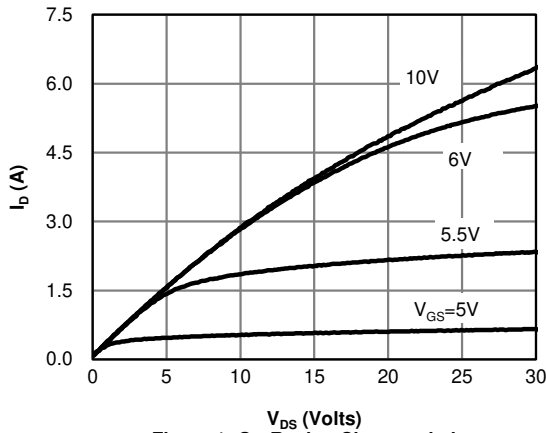
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>STATIC PARAMETERS</b>							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	1000			V	
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C		1100			
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		1.04		V/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =1000V, V <sub>GS</sub> =0V			1	μA	
		V <sub>DS</sub> =800V, T <sub>J</sub> =125°C			10		
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V			±100	nA	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	3.3	3.9	4.5	V	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =2.5A		3.5	4.2	Ω	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =40V, I <sub>D</sub> =2.5A		5		S	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.73	1	V	
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4	A	
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current				15	A	
<b>DYNAMIC PARAMETERS</b>							
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	750	950	1150	pF	
C <sub>oss</sub>	Output Capacitance		40	62	85	pF	
C <sub>riss</sub>	Reverse Transfer Capacitance		3.5	6	9	pF	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	2	4.3	6.5	Ω	
<b>SWITCHING PARAMETERS</b>							
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =800V, I <sub>D</sub> =5A	15	19	23	nC	
Q <sub>gs</sub>	Gate Source Charge				4.6		nC
Q <sub>gd</sub>	Gate Drain Charge				6.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =500V, I <sub>D</sub> =5A, R <sub>G</sub> =25Ω		27		ns	
t <sub>r</sub>	Turn-On Rise Time			40		ns	
t <sub>D(off)</sub>	Turn-Off DelayTime			50		ns	
t <sub>f</sub>	Turn-Off Fall Time			33		ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =5A, di/dt=100A/μs, V <sub>DS</sub> =100V	350	450	550	ns	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =5A, di/dt=100A/μs, V <sub>DS</sub> =100V	4.2	5.5	6.8	μC	

- A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25° C.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C, Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.
- G. L=60mH, I<sub>AS</sub>=2.8A, V<sub>DD</sub>=150V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25° C

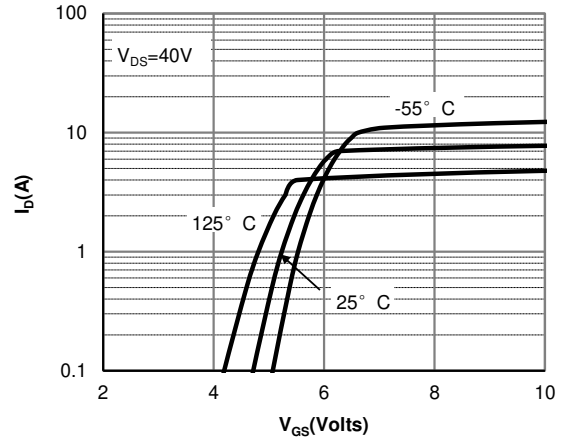
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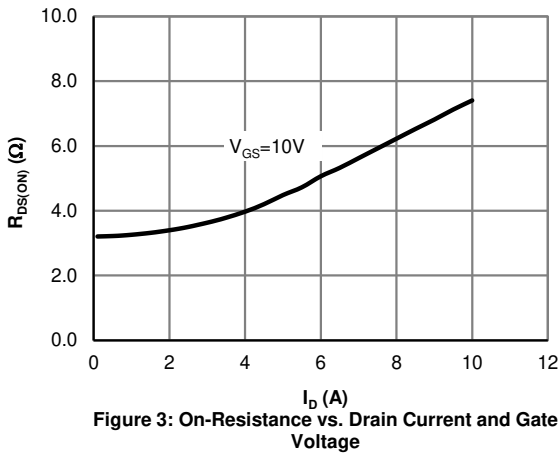
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



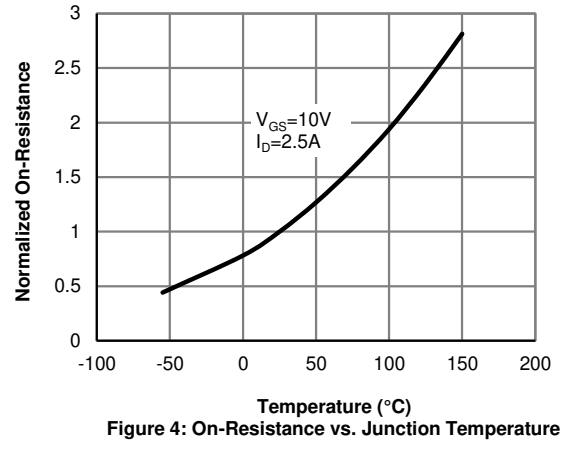
**Figure 1: On-Region Characteristics**



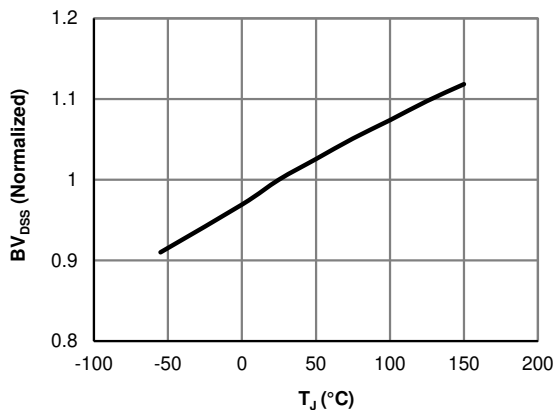
**Figure 2: Transfer Characteristics**



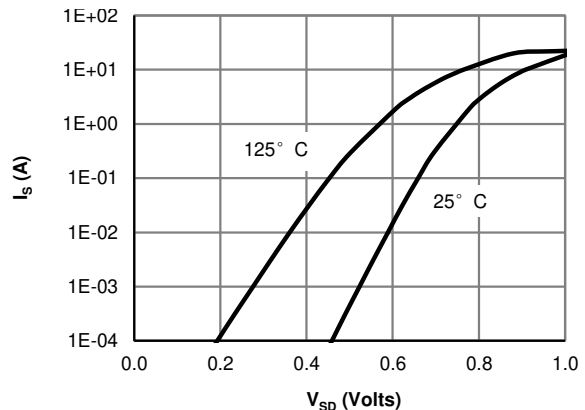
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: Break Down vs. Junction Temperature**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

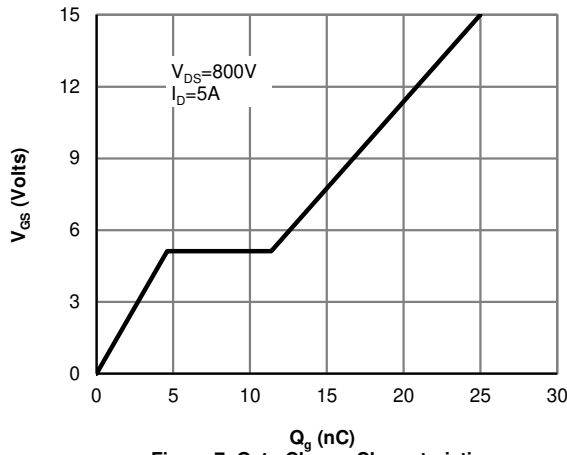


Figure 7: Gate-Charge Characteristics

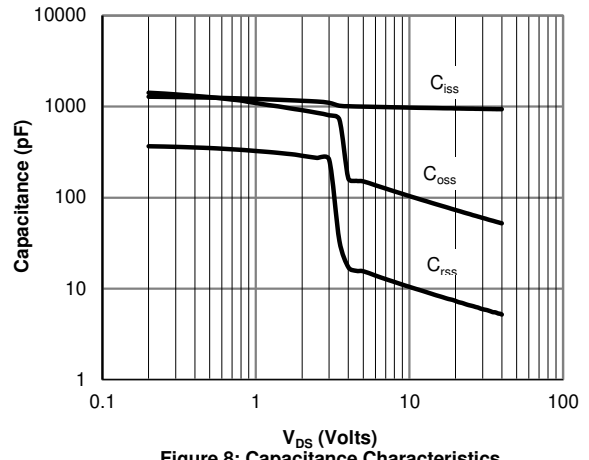


Figure 8: Capacitance Characteristics

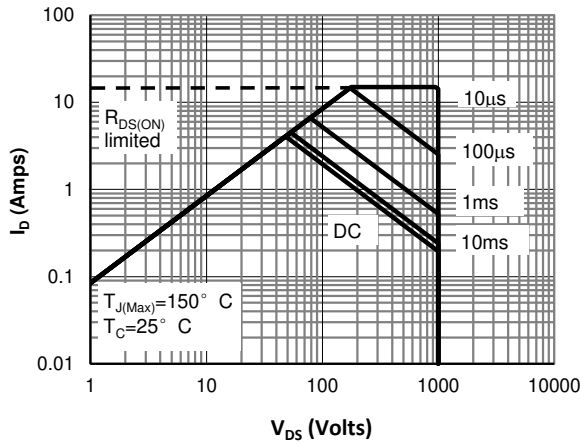


Figure 9: Maximum Forward Biased Safe Operating Area for AOT5N100 (Note F)

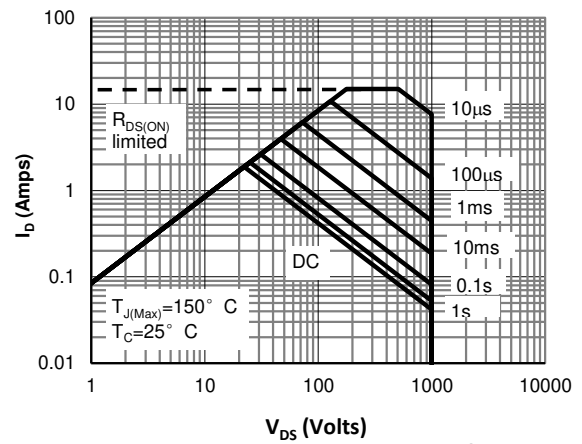


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF5N100 (Note F)

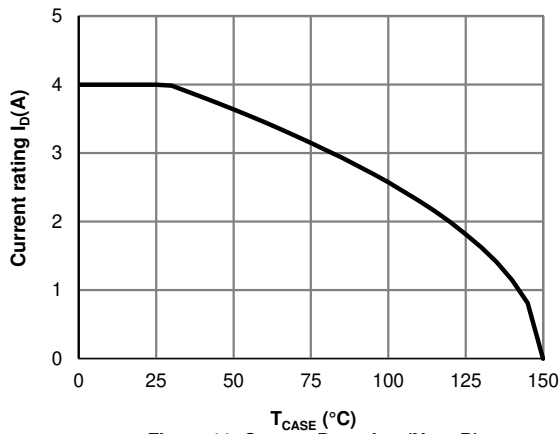


Figure 11: Current De-rating (Note B)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

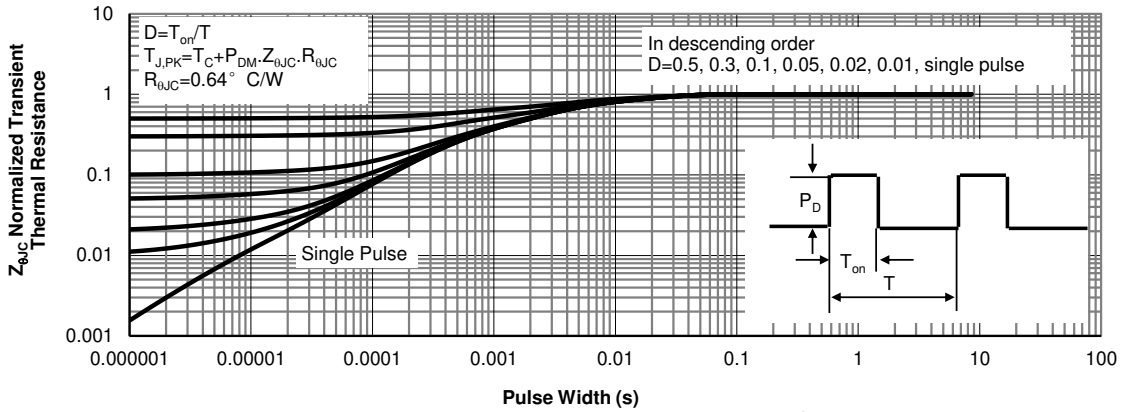


Figure 12: Normalized Maximum Transient Thermal Impedance for AOT5N100 (Note F)

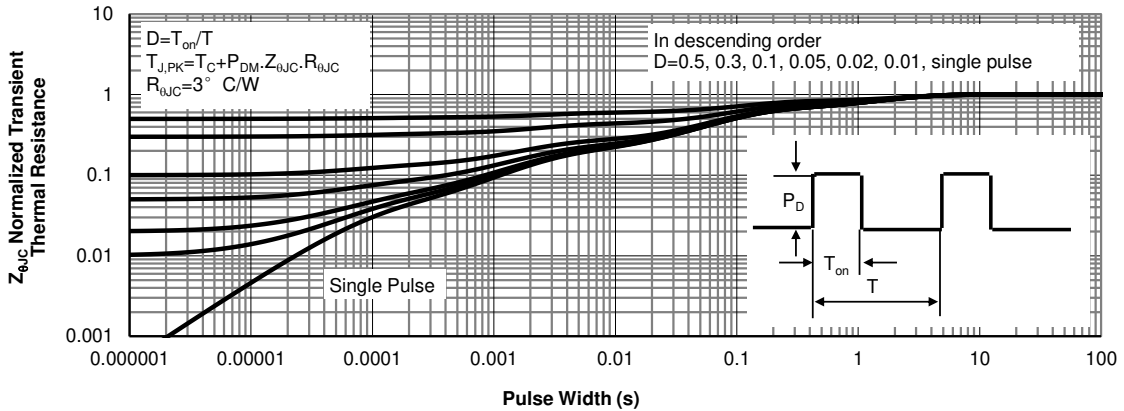
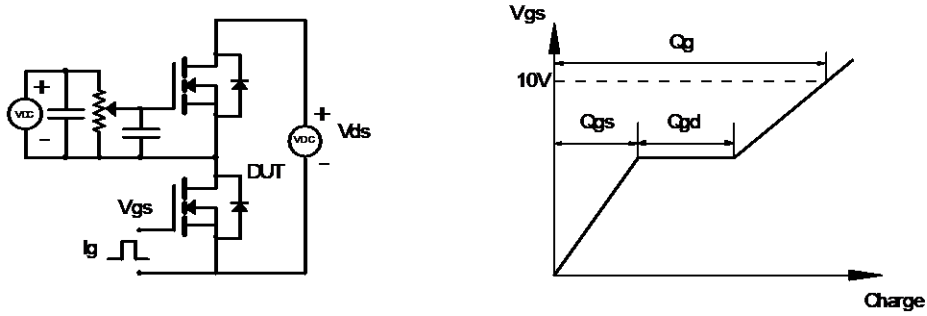
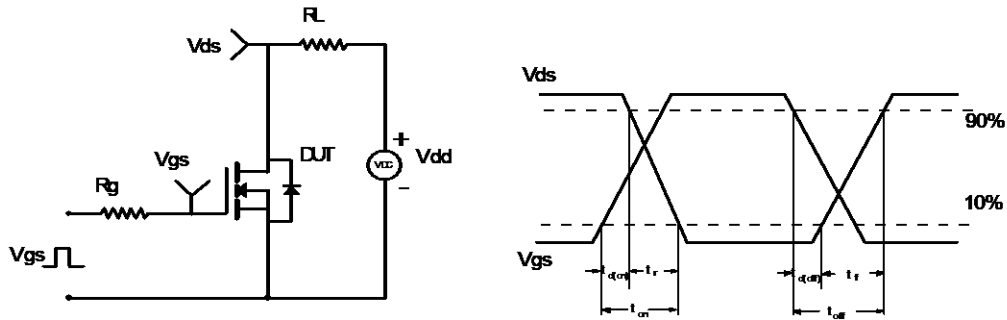


Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF5N100 (Note F)

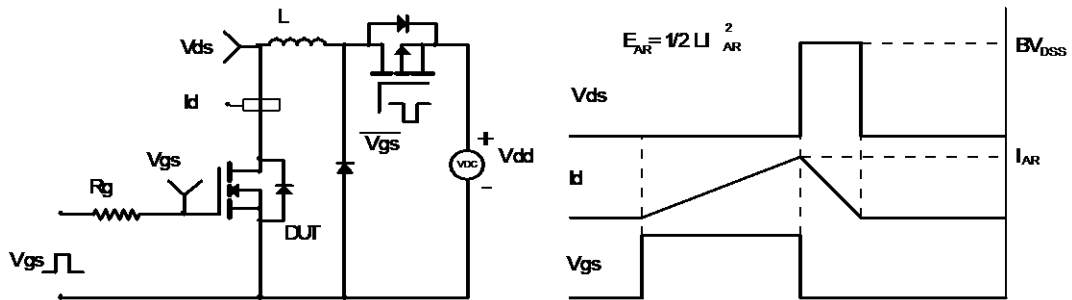
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

