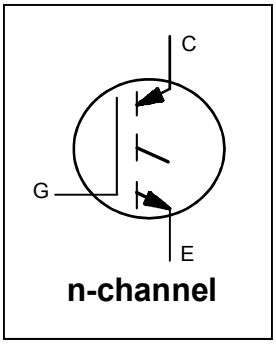
INSULATED GATE BIPOLAR TRANSISTOR

V_{CES} = 1200V
$I_{C(Nominal)}$ = 20A
$T_{J(max)}$ = 175°C
$V_{CE(on)}$ typ = 1.9V @ I_C= 20A



n-channel

Applications

- Medium Power Drives
- UPS
- HEV Inverter
- Welding
- Induction Heating

G	C	E
Gate	Collector	Emitter

Features	→ Benefits
Low $V_{CE(ON)}$ and switching Losses	High efficiency in a wide range of applications and switching frequencies
Square RBSOA and Maximum Junction Temperature 175°C	Improved Reliability due to rugged hard switching performance and higher power capability
Positive $V_{CE\ (ON)}$ Temperature Coefficient	Excellent current sharing in parallel operation

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG7CH35UEF	Die on film	Wafer	1	IRG7CH35UEF

Mechanical Parameter

Die Size	3.937 x 4.826	mm^2
Minimum Street Width	75	µm
Emiter Pad Size (Included Gate Pad)	See Die Drawing	mm^2
Gate Pad Size	0.503 x 0.501	
Area Total / Active	19/10	
Thickness	120	µm
Wafer Size	200	mm
Flat Position	0	Degrees
Maximum-Possible Chips per Wafer	1447 pcs	
Passivation Front side	Silicon Nitride	
Front Metal	Al, Si (4µm)	
Backside Metal	Al- Ti - Ni- Ag (1kA°-1kA°-4kA°-6kA°)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, T_J=25°C	1200	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ②	80	A
V_{GE}	Gate Emitter Voltage	± 30	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	°C

Static Characteristics (Tested on wafers) . T_J=25°C

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 100µA ③
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.35	1.60		V_{GE} = 15V, I_C = 5A, T_J = 25°C
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	3.0	—	6.0		I_C = 600µA , V_{GE} = V_{CE}
I_{CES}	Zero Gate Voltage Collector Current	—	2.0	100	µA	V_{CE} = 1200V, V_{GE} = 0V
I_{GES}	Gate Emitter Leakage Current	—	—	± 100	nA	V_{CE} = 0V, V_{GE} = ±30V

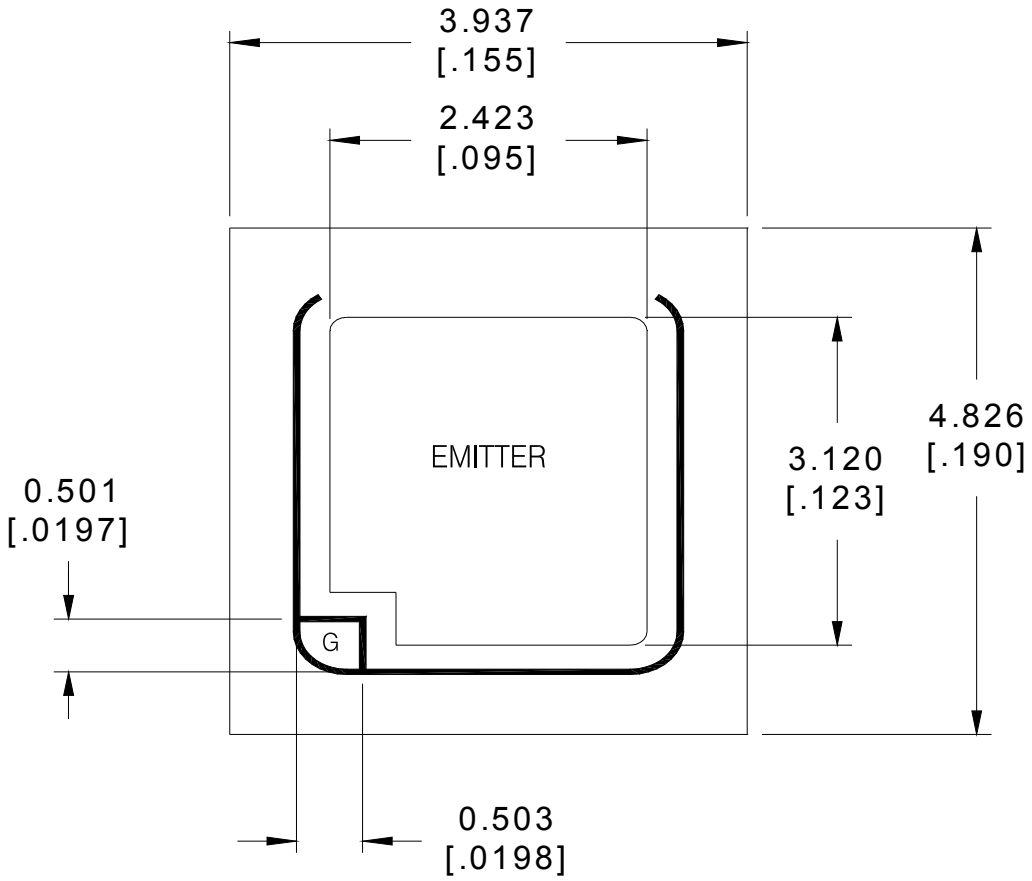
Electrical Characteristics (Not subject to production test- Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.9	2.2	V	V_{GE} = 15V, I_C = 20A , T_J = 25°C ④
		—	2.4	—		V_{GE} = 15V, I_C = 20A , T_J = 175°C④
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 80A V_{CC} = 960V, Vp ≤1200V Rg = 10Ω, V_{GE} = +20V to 0V
C_{iss}	Input Capacitance	—	1905	—	pF	V_{GE} = 0V
C_{oss}	Output Capacitance	—	60	—		V_{CE} = 30V
C_{rss}	Reverse Transfer Capacitance	—	40	—		f = 1.0MHz,
Q_g	Total Gate Charge (turn-on)	—	85	—	nC	I_C = 20A
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	15	—		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	35	—		V_{CC} = 600V

Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions ⑤
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	I_C = 20A, V_{CC} = 600V
t_r	Rise time	—	15	—		R_G = 10Ω, V_{GE}=15V, L=200µH
$t_{d(off)}$	Turn-Off delay time	—	160	—		T_J = 25°C
t_f	Fall time	—	80	—		
$t_{d(on)}$	Turn-On delay time	—	25	—		I_C = 20A, V_{CC} = 600V
t_r	Rise time	—	20	—		R_G = 10Ω, V_{GE}=15V, L= 200µH
$t_{d(off)}$	Turn-Off delay time	—	200	—		T_J = 175°C
t_f	Fall time	—	200	—		

Die Drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: MILLIMETERS
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

5. DIE THICKNESS = 0.120 [.0047]

REFERENCE: IRG7CH35UB
IRG7PH35UPBF
IRG7PH35U-EP
IRG7PH35UDPBF
IRG7PH35UD-EP
IRG7PH35UD1PBF
IRG7PH35UD1-EP

Notes:

①The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
②V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 200µH, R_G = 10Ω.
③Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely
④Die Level Characterization
⑤Values influenced by parasitic L and C in measurement

Additional Testing and Screening
For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

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Further Information

For further information please contact your local IR Sales office or email your enquiry to http://die.irf.com

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 101N. Sepulveda Blvd, El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

