

Structure Silicon Monolithic Integrated Circuit

Product Series 6ch Power Driver for Car Audio

Type **BD8210EFV**

Feature

- The SPINDLE driver and the SLED driver can highly effective drive with PWM drive system.
- The actuator driver and the loading driver are linear BTL drive and are achieving a low noise power.

○ Absolute maximum ratings(Ta=25°C)

Parameter	Symbol	Limits	Unit
POWER MOS power supply voltage	SPVM, SPRNF, SLRNF	15 #1	V
Pre-block / BTL / Loading driver power-block power supply voltage	Vcc, VMFCRNF, VMTKRNF, VM_S	15	V
Input terminal voltage1	VIN1 #2	VCC	V
Input terminal voltage2	VIN2 #3	VM_S	V
Power dissipation	Pd	2.0 #4	W
Operating temperature range	Topr	- 40 ~ 85	°C
Storage temperature	Tstg	- 55 ~ 150	°C
Junction temperature	Tjmax	150	°C

#1 POWER MOS output terminals are contained.

#2 It shows each terminal of CTL1 ,CTL2 ,Vc ,LDVc ,LDIN ,TINN ,and FINN.

#3 It shows each terminal of HU+ ,HU- ,HV+ ,HV- ,HW+ ,HW- ,SL1INN ,SL2INN ,SPIN ,SPVM ,and VM\_S.

#4 Ta=25°C , PCB (70mm× 70mm× 1.6mm,occupied copper foil is less than 3%,glass epoxy standard board) mounting.

Reduce power by 16mW for each degree above 25°C.

○ Operating conditions (Ta=-40 ~ +85°C)

(Set the power supply voltage taking allowable dissipation into considering.)

Parameter	Symbol	MIN	TYP	MAX	Unit
Pre-block / Loading driver power-block power supply voltage	Vcc	6	8	10	V
PWM-part Pre-block power supply voltage	VM_S	6	8	Vcc	V
Spindle driver powerblock power supply voltage	SPVM, SPRNF	6	8	VM_S	V
Sled motor driver powerblock power supply voltage	SLRNF	6	8	VM_S	V
Actuator driver powerblock Power supply voltage	VMFCRNF VMTKRNF	4	8	Vcc	V

Install detect resistance between SPVM, SPRNF, SLRNF and VM\_S, and between VMFCRNF, VMTKRNF and AVM.

Status of this document

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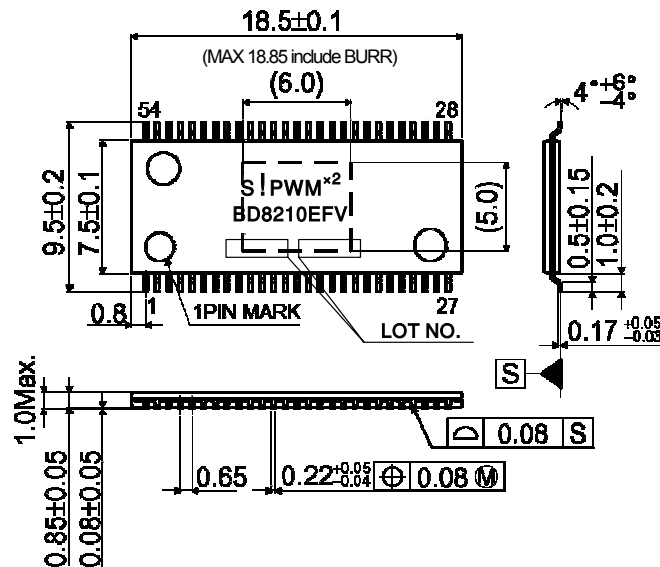
A radiation is not designed.

○ Electrical characteristics

(Unless otherwise noted, Ta=25°C, Vcc=SPVM=SLVM=8V, AVM=5V, Vc=LDVC=1.65V, RL=8Ω, RLSP=2Ω, SPRNF=0.25Ω, SLRNF=0.5Ω)

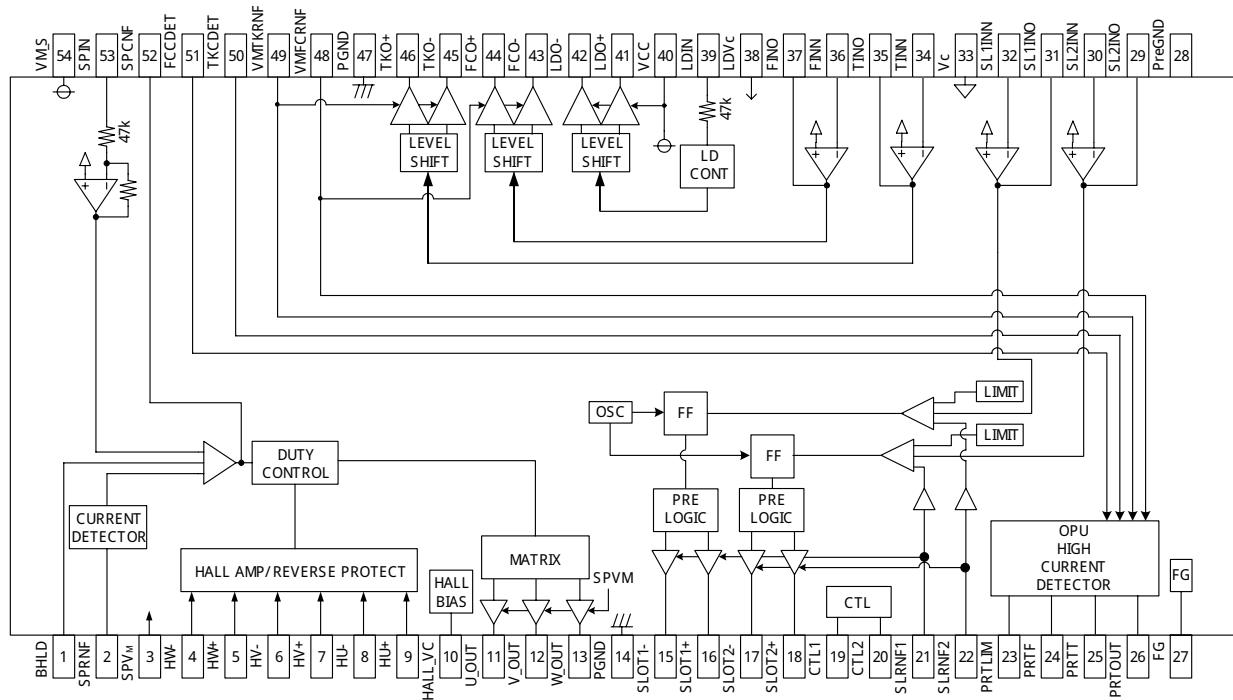
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition		
Circuit current	Quiescent current 1	IQ1	-	18	25	mA	High gain mode	
	Quiescent current 2	IQ2	-	18	25	mA	Low gain mode	
	Standby-on current 1	IST1	-	0.7	1.0	mA	Standby mode	
Spindle driver Block	Hall bias	Voltage of hall bias	VHB	0.45	0.9	1.35	V	IHB = 10mA
		Input bias current	IHB	-5	-	5	μA	
	Hall AMP	Input level	VHIM	50	-	-	mV/pp	
		Common mode input range	VHICM	1	-	6	V	
	Torque instruction I/O	Input dead zone 1 (one side)	VDZSP1	0	10	40	mV	High gain mode
		Input dead zone 2 (one side)	VDZSP2	0	10	40	mV	Low gain mode
		Input output gain 1	grSP1	0.8	1.00	1.20	A/V	High gain mode
		Input output gain 2	grSP2	0.16	0.20	0.24	A/V	Low gain mode
		Output On resistor (Vertical harmony)	RONSP	-	1	1.8	Ω	IL = 500mA
		Output limit current	ILVSP1	1.05	1.32	1.58	A	All mode commonness
		Input impedance	RiSP	35	47	59	kΩ	
	FG output	PWM frequency	fosc	-	100	-	kHz	
		Low voltage	VFGL	-	0.1	0.3	V	10KΩ Pull-up (3.3V)
Stepping motor driver Block	Input dead zone (one side)	VDZSL	5	15	30	mV		
	Input output gain	grSL	425	500	575	mAV		
	Input offset voltage	VOSL	-5	-	5	mV		
	Input bias current	IBASSL	10	50	300	nA		
	Output On resistor (Vertical harmony)	RONSL	-	2.2	3.7	Ω	IL = 500mA	
	Output limit current	ILVSL	672	800	928	mA		
	PWM frequency	fosc	-	100	-	kHz		
Actuator driver Block	Input offset voltage	VIOACT	-5	-	5	mV		
	Input bias current	IBIASACT	10	50	300	nA		
	Output offset voltage	VOFFT	-50	0	50	mV		
	Output saturation voltage (vertical harmony)	VOFT	-	0.9	1.6	V	IL = 500mA	
	Voltage gain	GVFT	105	12	135	dB		
Loading driver Block	Output offset voltage	VOFLD	-50	0	50	mV		
	Output saturation voltage (vertical harmony)	VOLD	-	1.5	2.3	V	IL = 500mA	
	Input impedance	RiLD	35	47	59	kΩ		
	Voltage gain	GVLD	13	15	17	dB		
Picking up protection circuit Block	PRTT/PRTF Default voltage	VPRTREF	1.00	1.06	1.12	V		
	PRTT/PRTF Protection detection voltage	VPRTDET	282	300	318	V		
	PRTLIM Voltage	VPRTLIM	500	530	560	mV		
	DETAMP Input offset voltage	VOFDET	-5	0	5	mV		
Picking up protection reset Block	L output voltage	VOL	-	0.1	0.3	V	33KΩ Pull-up (3.3V)	
	H input voltage	VH	2	-	-	V		
	L input voltage	VL	-	-	0.8	V		
CTL1,CTL2	L input voltage	VIL	-	-	0.8	V		
	H input voltage	VH	2	-	-	V		
	Highlevel input current	IcTH	-	50	100	μA	CTL = 3.3V	
Function	Vc drop muting Voltage of mute	VVMc	0.4	0.7	1	V		
	Vcc drop muting Voltage of mute	VVMcc	3.4	3.8	4.2	V		
	LDVc drop muting Voltage of mute	VMLDVC	0.4	0.7	1	V		
	Vc input current	Ic	-	4	8	μA		
	LDVc input current	ILDVC	-	4	8	μA		

○ Package outlines : HTSSOP-B54



(UNIT : mm)

○ Block diagram



- About input / output polarity, FCO+=L, FCO-=H at FINO > Vc. Same applies to SL1INO, SL2INO, TINO.

○ Pin description

No.	Symbol	Description	No.	Symbol	Description
1	BHLD	Spindle driver current sense bottom hold	54	VM_S	Spindle / Sled control block power supply
2	SPRN	Spindle driver current sense	53	SPIN	Spindle driver input
3	SPVM	Spindle driver power supply	52	SPCNF	Spindle driver loop filter
4	HW-	Hall amp.W negative input	51	FCCDET	Drive current detect for Focus drive
5	HW+	Hall amp.W positive input	50	TKCDET	Drive current detect for Tracking drive
6	HV-	Hall amp.V negative input	49	VMTKRNF	Tracking driver power supply
7	HV+	Hall amp.V positive input	48	VMFCRNF	Focus driver power supply
8	HU-	Hall amp.U negative input	47	PGND	Act / LD driver power ground
9	HU+	Hall amp.U positive input	46	TKO+	Tracking driver positive output
10	HALL_Vc	Hole bias	45	TKO-	Tracking driver negative output
11	U_OUT	Spindle driver output U	44	FCO+	Focus driver positive output
12	V_OUT	Spindle driver output V	43	FCO-	Focus driver negative output
13	W_OUT	Spindle driver output W	42	LDO-	Loading driver negative output
14	PGND	Spindle & SLED driver block power ground	41	LDO+	Loading driver positive output
15	SLO1-	Sled driver 1 negative output	40	Vcc	BTL pre and Loading power supply
16	SLO1+	Sled driver 1 positive output	39	LDIN	Input for Loading driver
17	SLO2-	Sled driver 2 negative output	38	LDVc	Reference voltage input for Loading driver
18	SLO2+	Sled driver 2 positive output	37	FINO	Output for Focus driver pre-op amp
19	CTL1	Driver logic control input 1	36	FINN	Inverted input for Focus driver pre-op amp
20	CTL2	Driver logic control input 2	35	TINO	Output for Tracking driver pre-op amp
21	SLRNF1	Sled driver 1 current sense	34	TINN	Inverted input for Tracking driver pre-op amp
22	SLRNF2	Sled driver 2 current sense	33	Vc	Reference voltage input
23	PRTLIM	Droop current setting for Pick-up protect	32	SL1INN	Inverted input for Sled driver 1 pre-op amp
24	PRTF	Protect Time setting for Focus	31	SL1INO	Output for Sled driver 1 pre-op amp
25	PRTT	Protect Time setting for tracking	30	SL2INN	Inverted input for Sled driver 2 pre-op amp
26	PRTOUT	Protect output	29	SL2INO	Output for Sled driver 2 pre-op amp
27	FG	FG output	28	PreGND	Pre block ground

○ **Cautions in using the IC**

**1. Absolute maximum ratings**

We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum ratings, such as impressed voltages or the operating temperature range, is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.

**2. Reverse polarity connection**

Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line and motor coil line.

**3. Power supply line**

Due to return of regenerative current by reverse electromotive force, using electrolytic and ceramic suppress filter capacitors (0.1μF) close to the IC power input terminals (Vcc and GND) are recommended. Please note the electrolytic capacitor value decreases at lower temperatures and examine to dispense physical measures for safety.

**4. GND line**

Please keep the GND line the lowest potential always, and check the GND voltage when transient voltages are connected to the IC.

**5. Thermal design**

Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins. This product has exposed the frame to the back side of the package, but please note that it is assumed to use heat radiation efficiency by the heat radiation for this part. Please take the heat radiation pattern on not only the surface of the substrate but also the back of the substrate widely.

**6. Short circuit mode between terminals and wrong mounting**

Do not mount the IC in the wrong direction and displacement, and be careful about the reverse-connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GND.

**7. Radiation**

Strong electromagnetic radiation can cause operation failures.

**8. ASO (Area of Safety Operation)**

Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.

**9. TSD (Thermal Shut-Down)**

The TSD is activated when the junction temperature (Tj) exceeds Tjmax, and the output terminal is switched to OPEN.

The guarantee and protection of set are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

**10. Capacitor between output and GND**

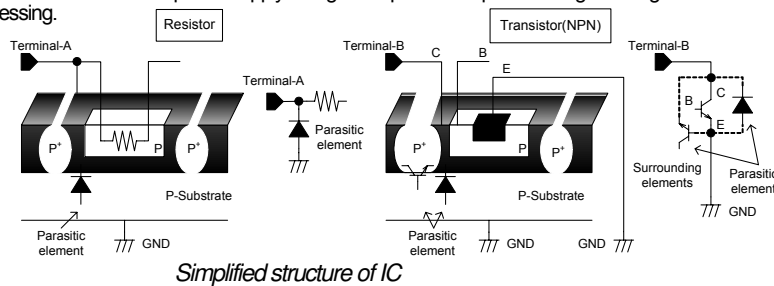
If a large capacitor is connected between the output and GND, this IC might be destroyed when Vcc becomes 0V or GND, because the electric charge accumulated in the capacitor flows to the output. Please set said capacitor to smaller than 0.1μF.

**11. Inspection by the set circuit board**

The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, when attaching or detaching from jig in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC, and vice versa. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

**12. Input terminal**

This IC is a monolithic IC, and has P<sup>+</sup> isolation and P substrate for the element separation. Therefore, a parasitic PN junction is formed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminal A on the resistor, at Terminal B on the transistor, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the interference of circuit operation, then the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND (P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.



**13. Earth wiring pattern**

If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

**14. Reverse-rotation braking**

In the case of reverse-rotation braking from high-speed rotation, pay good attention to reverse electromotive force. Furthermore, fully check output current and consider the revolutions applied to the reverse-rotation brake.

**15. About the capacitor between SPVM and PGND**

The capacitor between SPVM and PGND absorbs the change in a steep voltage and the current because of the PWM drive, as a result, there is a role to suppress the disorder of the SPVM voltage. However, the effect falls by the influence of the wiring impedance etc, if the capacitor becomes far from IC. Please examine the capacitor between SPVM and PGND to arrange it near IC.

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