Si5364-EVB

EVALUATION BOARD FOR Si5364 SONET/SDH PRECISION PORT CARD CLOCK IC

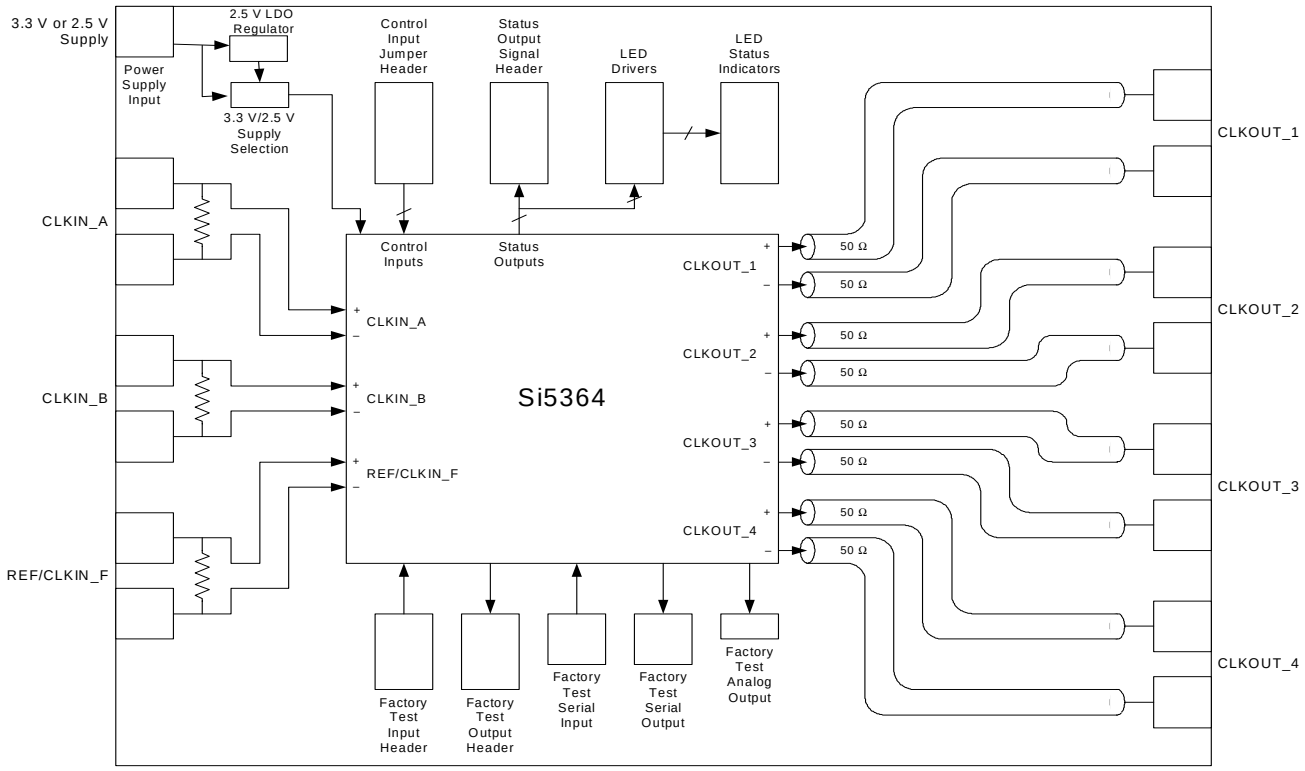
Description

The Si5364-EVB is the evaluation board for the Si5364 SONET/SDH Precision Port Card Clock IC. This evaluation board provides access to all signals associated with normal operation of the device. This circuit board also is designed to provide access to signals that are reserved for factory testing purposes.

Features

- Si5364 device can be powered directly from either a 3.3 or 2.5 V supply
- Differential I/Os ac-coupled on board
- Differential inputs terminated on board
- Control input signals are switch/jumper configurable
- Status outputs brought out to headers for access
- LED status indicators reflect state of status outputs
- LED status indicators can be disabled for device power measurements

Function Block Diagram



Functional Description

The Si5364-EVB is the evaluation board for the Si5364 SONET/SDH Precision Port Card Clock IC. This evaluation board provides access to all signals associated with normal operation of the device. This circuit board also is designed to provide access to signals that are reserved for factory testing purposes.

Power Supply Selection and Connections

The Si5364-EVB board is switch selectable for operation using either a single 3.3 V or a single 2.5 V supply.

For operation using a 3.3 V supply, configure the board as follows:

1. Remove power supply connections from the VDD and GND terminals of the board's power connector, J15.
2. Remove the connection between VDD33 and VDD25 by removing the jumper on header JPI.
3. Set VSEL33 high by sliding the switch on the VSEL33 (JP3) to the side marked "1".
4. Connect the power supply ground lead and 3.3 V supply lead to the GND and VDD terminals of the board's power connector, J15.

For operation using a 2.5 V supply, configure the board as follows:

1. Remove power supply connections from the VDD and GND terminals of the board's power connector, J15.
2. Set VSEL33 low by sliding the switch on the VSEL33 (JP3) to the side marked "0".
3. Connect VDD33 and VDD25 by installing a jumper between one of the 3.3 V pins and one of the 2.5 V pins on header JPI.
4. Connect the power supply ground lead and 2.5 V supply lead to the GND and VDD terminals of the board's power connector, J15.

Power Consumption

Typical supply current draw for the Si5364-EVB with LED indicators disabled and one clock output enabled is 120 mA. Each additional clock output that is enabled adds approximately 15 mA. LED indicators, when enabled, adds approximately 8 mA for each indicator that is illuminated.

Si5364 Control Inputs

Most of the control inputs to the Si5364 are routed to the center post of a SPDT switch located at JP1. The switches are wired with the signal on the center pin, VDD33 on one side pin, and GND on the other side pin. Each input is easily configurable to a high or a low state.

There are three inputs to the Si5364 that are not routed to switches at JP1. Two of these signals are INCDELAY and DECDELAY. They are routed to push button switches SW1 and SW2, respectively, through headers JP4 and JP5. Inverters U6 and U7 condition the action of these switches before being sent to the Si5364 device. Pressing and releasing these switches provides a single pulse to the control input for the Si5364. This is a convenient method for evaluating the operation of the INCDELAY and DECDELAY functions. Resistors R26 and R27 allow the user to disconnect the switches from the device and drive the inputs from another source. JP4 and JP5 are not populated when shipped from the factory. If an external source is required to drive the INCDELAY and DECDELAY inputs, then populate these two headers. This provides the user a convenient location to connect the source.

Each LVTTL input on the Si5364 device has an internal pull-down mechanism. The control inputs default to a low state if no device drives the input.

RSTN/CAL Settings for Normal Operation and Self-Calibration

The RSTN/CAL signal is an LVTTL input to the Si5364 and has an on-chip pull down mechanism. This pin must be set high to enable normal operation of the Si5364 device.

Setting RSTN/CAL low forces the Si5364 into a reset state. A low-to-high transition of RSTN/CAL enables the part and initiates a self-calibration sequence.

The Si5364 device automatically initiates a self-calibration at power-up if the RSTN/CAL signal is held high. A self-calibration of the device also can be manually initiated by pushing the RSTN/CAL switch, SW3, then releasing. Self-calibration must be initiated manually after changing the state of either the BWSEL[1:0] control inputs or the FEC[1:0] inputs.

Whether manually initiated or automatically initiated at power-up, the self-calibration process requires the presence of a valid input clock. If the self-calibration is initiated without a valid clock present, the device waits for a valid clock before completing the self-calibration. The Si5364 clock outputs drift to the lower end of the operating frequency range as the device waits for a valid clock. After the input clock is validated, the calibration process runs to completion, the device locks to the input, and the clock outputs shifts to their target frequencies. Subsequent losses of the input clock do not require re-calibration. If the clock input is lost after self-calibration, the device enters Digital Hold mode. When the input clock returns, the device re-locks to the input clock without performing a self-calibration.

Status Signals

The status outputs from the Si5364 device are each routed to one pin of a two-row header, JP11. The header is wired so that the signals are present on one side of the header and a ground reference is present on the other. The letter S marks the row of signal pins and the row of ground pins is marked with the letter G.

On the Si5364-EVB board, the status outputs are also routed to two buffer/driver ICs (U4 and U5) that drive one LED indicator for each status signal.

Enabling and Disabling the Status Indicator LEDs

The status LED driver outputs can be disabled. The disabled driver outputs are placed into a high impedance state to get a more accurate measurement of the current/ power being consumed by the Si5364 device. The LED drivers are enabled when the switch at JP9 is switched to ON. The driver outputs are disabled when the switch is set to OFF.

Factory Test Headers

Locations for headers JP8 and JP10 are included on the SI5364-EVB for factory testing. For customer evaluation, these locations are not populated.

Differential Clock Input Signals

The differential clock inputs to the Si5364-EVB are terminated on the board at a location near the input SMA connectors. The input SMA connectors are ac coupled to the termination circuit. The termination circuit consists of two 50 Ω resistors and a 0.1 µF capacitor, connected so that the positive and negative inputs of the differential pair each see a 50 Ω termination to "ac ground", and the line-to-line termination impedance is 100 Ω. The signals are then routed to the Si5364 device.

Single-ended operation is accomplished by supplying a signal to one of the differential inputs, typically the positive input. The other input should be shorted to ground with an SMA shorting plug.

Differential Clock Output Signals

The differential clock outputs from the Si5364 device are routed to the perimeter of the circuit board using 50 Ω transmission structures. The capacitors that provide ac-coupling are located near the clock output SMA connectors.

Internal Regulator Compensation

The Si5364-EVB contains pad locations for a resistor and a capacitor between the VDD25 node and ground. The resistor pads are populated with a 0 Ω resistor. The capacitor pads are populated with a low ESR 33 µF tantalum capacitor. This is the suggested compensation circuit for Si5364 devices.

There are two considerations for selecting this combination of compensation resistor and capacitor. First, is the stability of the regulator. The second is noise filtering.

The acceptable range for the time constant at this node is 15 µs to 50 µs. The capacitor used on the board is a 33 µF capacitor with an ESR of .8 Ω. This yields a time constant of 26.4 µs. The designer could decide to use a 330 µF capacitor with an ESR of .15 Ω. This yields a time constant of 49.5 µs. Each of these cases provide a compensation circuit that makes the output of the regulator stable.

The second issue is noise filtering. For this, more capacitance is usually better. For the two cases described above, the 330 µF case provides greater noise filtering. However, the large case size of the 330 µF capacitor might make it impractical for many applications. The Si5364 device is specified with the 33 µF cap.

Default Jumper Settings

The default jumper settings for the Si5364-EVB board are given in Table 1 on page 4. These settings configure the board for operation from a 3.3 V supply.

Table 1. Si5364-EVB Assembly Rev B-01 Default Jumper/Switch Settings

Location	Signal	State	Notes
JP3	VSEL33	1	Si5364 device Internal Regulator enabled
JP12	VDD33	Open	Si5364 device VDD33 pins not connected to 2.5 V supply plane
JP1	VALTIME	0	100 ms Validation Time
	SMC/S3N	1	SONET Minimum Clock criteria selected
	DSBLFOS	0	Frequency Offset alarms enabled
	RVRT	1	Revertive clock switching mode selected
	AUTOSEL	1	Automatic input Selection enabled
	DSBLFSYNC	0	FSYNC output enabled
	MANCNTRL[0]	0	CLKIN_A would be selected if AUTOSEL = 0
	MANCNTRL[1]	1	CLKIN_A would be selected if AUTOSEL = 0
	FEC[0]	0	FEC scaling factor = 1/1 (no FEC scaling)
	FEC[1]	0	FEC scaling factor = 1/1 (no FEC scaling)
	BWSEL[0]	1	Loop Bandwidth = 6400 Hz
	BWSEL[1]	1	Loop Bandwidth = 6400 Hz
	FRQSEL_1[0]	1	CLKOUT_1 = 622 MHz Range
	FRQSEL_1[1]	1	CLKOUT_1 = 622 MHz Range
	FRQSEL_2[0]	1	CLKOUT_2 = 622 MHz Range
	FRQSEL_2[1]	1	CLKOUT_2 = 622 MHz Range
	FRQSEL_3[0]	1	CLKOUT_3 = 622 MHz Range
	FRQSEL_3[1]	1	CLKOUT_3 = 622 MHz Range
	FRQSEL_4[0]	1	CLKOUT_4 = 622 MHz Range
	FRQSEL_4[1]	1	CLKOUT_4 = 622 MHz Range
	FXD_DELAY	0	Fixed Delay mode disabled
JP9	LED ENABLE_N	ON	LED Status Indicators enabled
JP2	SYNCIN	No Jumper Installed	Header for SYNCIN input signal
JP15	FSYNC	No Jumper Installed	Header for FSYNC output signal

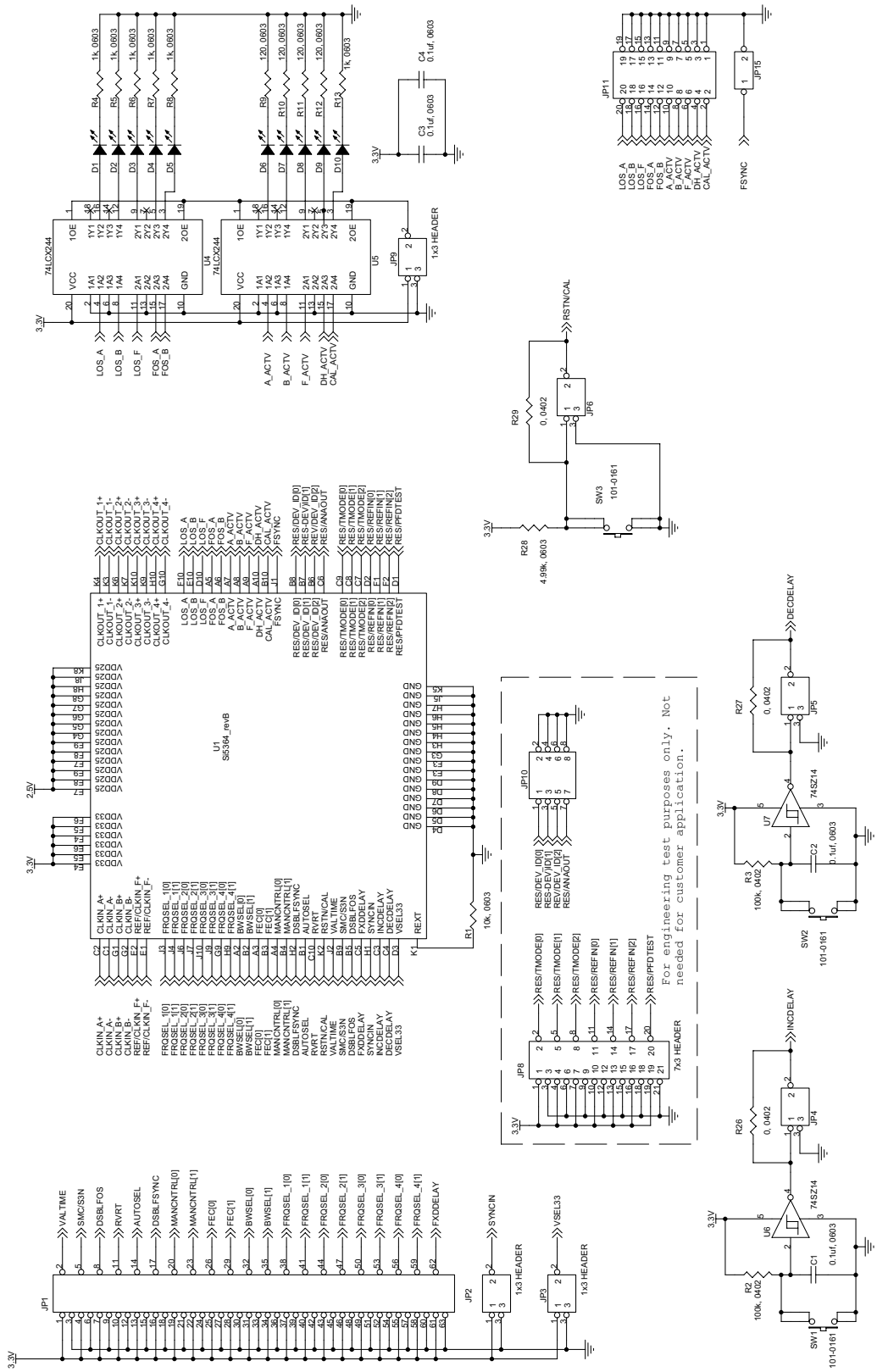


Figure 1. Si5364-EVB Typical Application Schematic (page 1 of 2)

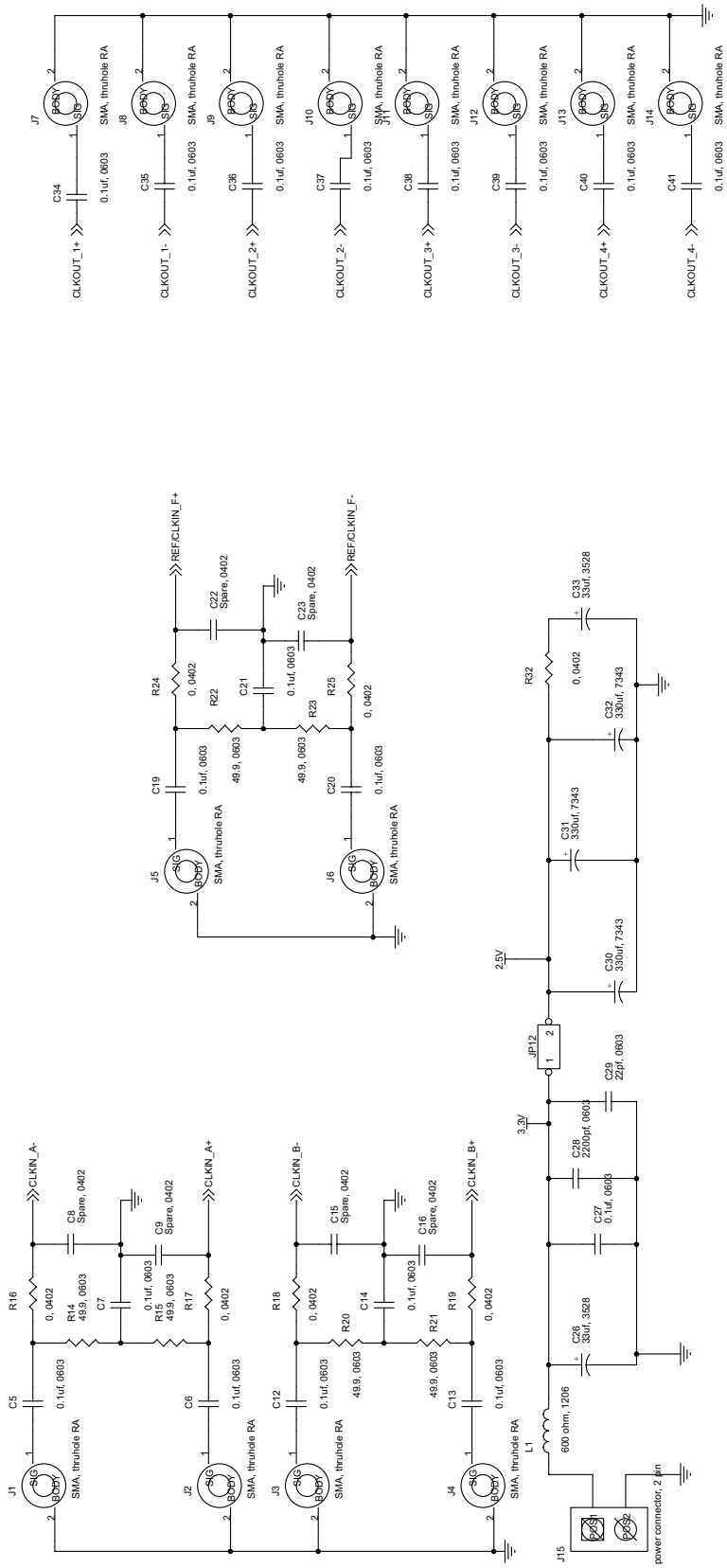


Figure 2. Si5364-EVB Typical Application Schematic (page 2 of 2)

Bill of Materials

Reference	Description	Manufacturer	Part Number
C1-C7,C12-C14,C19-C21	0.1uf, 0603	Venkel	C0603X7R160-104KNE
C27,C34-C41			
C8,C9,C15,C16,C22,C23	Spare, 0402		
C26,C33	33uf, 3528	Venkel	TA6R3TCR336KBR
C28	2200pf, 0603	Venkel	C0603X7R160-222KNE
C29	22pf, 0603	Venkel	C0603C0G500-220KNE
C30,C31,C32	330uf, 7343	Venkel	TA6R3TCR337KER
D1,D2,D3,D4,D5,D10	LED, SM, red, superbright	Panasonic	LN1271RAL
D6,D7,D8,D9	LED, SM, green	Panasonic	LN1371G
JP1	21x3 HEADER		
JP2,JP3,JP4,JP5,JP6,JP9	1x3 HEADER		
JP8	7x3 HEADER		
JP10	4x2 HEADER		
JP11	10x2 Header		
JP12,JP15	HEADER 2X1		
J1,J2,J3,J4,J5,J6,J7,J8,	SMA, thruhole RA	Johnson Components	142-0701-301
J9,J10,J11,J12,J13,J14			
J15	power connector, 2 pin	Phoenix Contact	140-A-111-02 1729018
L1	600 ohm, 1206	MURATA	BLM31A601S
R1	10k, 0603	Venkel	CR0603-16W-1002FT
R2,R3	100k, 0402	Venkel	CR0402-16W-1003FT
R4,R5,R6,R7,R8,R13	1k, 0603	Venkel	CR0603-16W-1001FT
R9,R10,R11,R12	120, 0603	Venkel	CR0603-16W-121JT
R14,R15,R20,R21,R22,R23	49.9, 0603	Venkel	CR0603-16W-49R9FT
R16,R17,R18,R19,R24,R25,	0, 0402	Venkel	CR0402-16W-000T
R26,R27,R29,R32			
R28	4.99k, 0603	Venkel	CR0603-16W-4991FT
SW1,SW2,SW3	101-0161	Mouser	101-0161
U1	Si5364_revB		
U4,U5	74LCX244	Fairchild	74LCX244MTC
U7,U6	74SZ14	Fairchild	NC7SZ14M5X

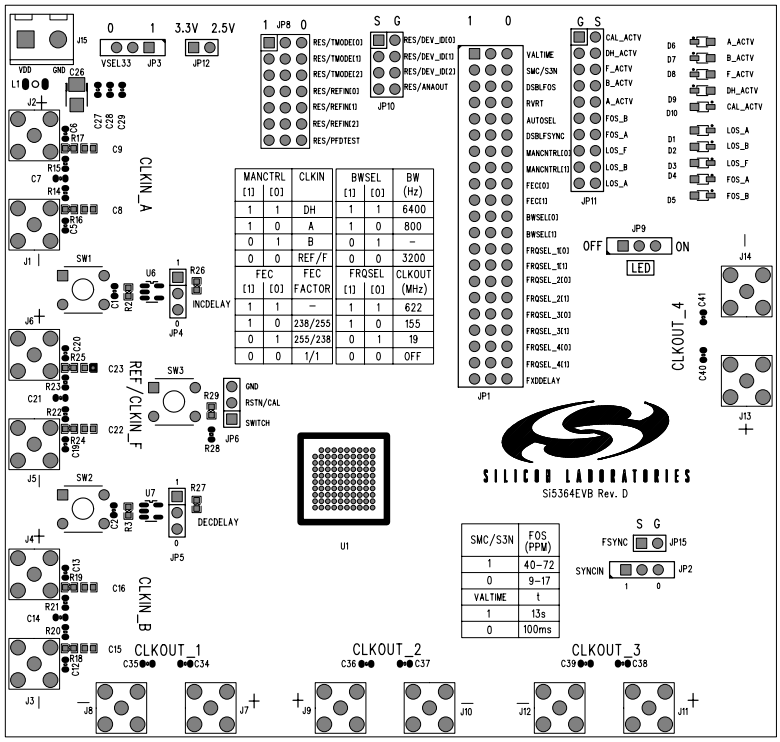


Figure 3. Si5364-EVB Top Silkscreen

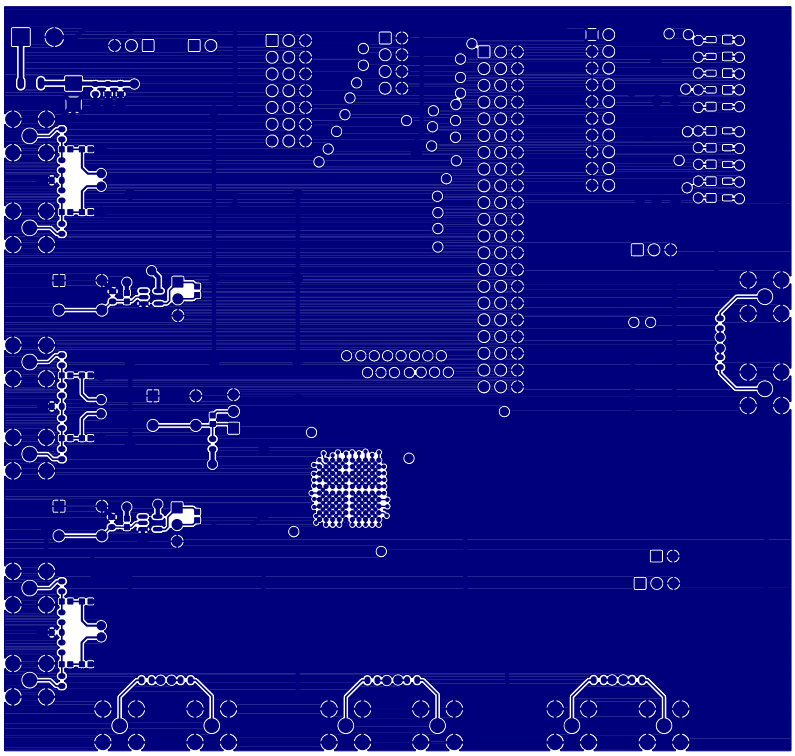


Figure 4. Si5364-EVB—Layer 1, Component Side

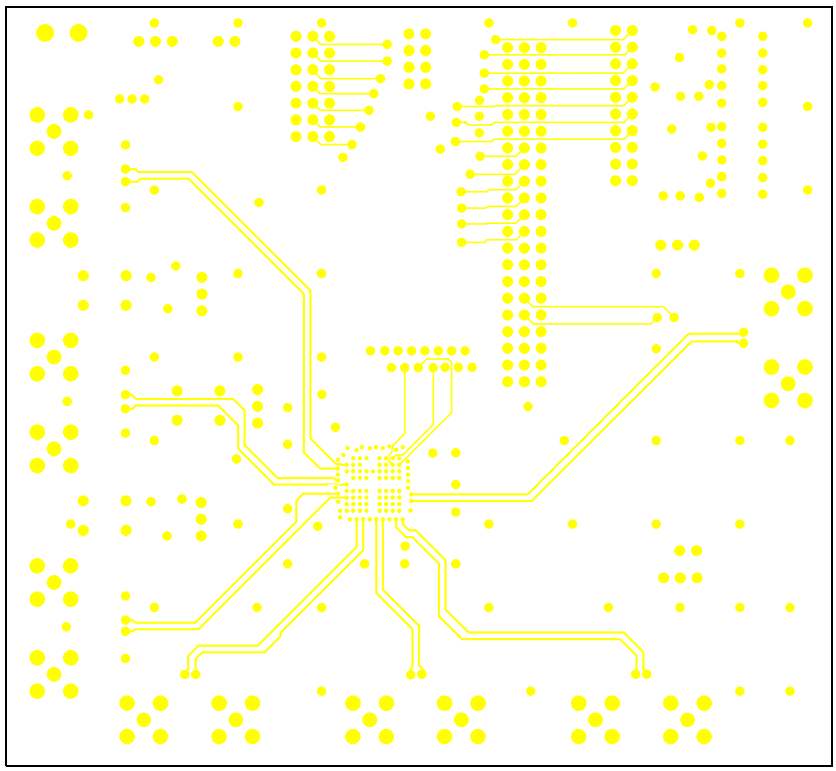


Figure 5. Si5364-EVB—Layer 2, High Speed Signals

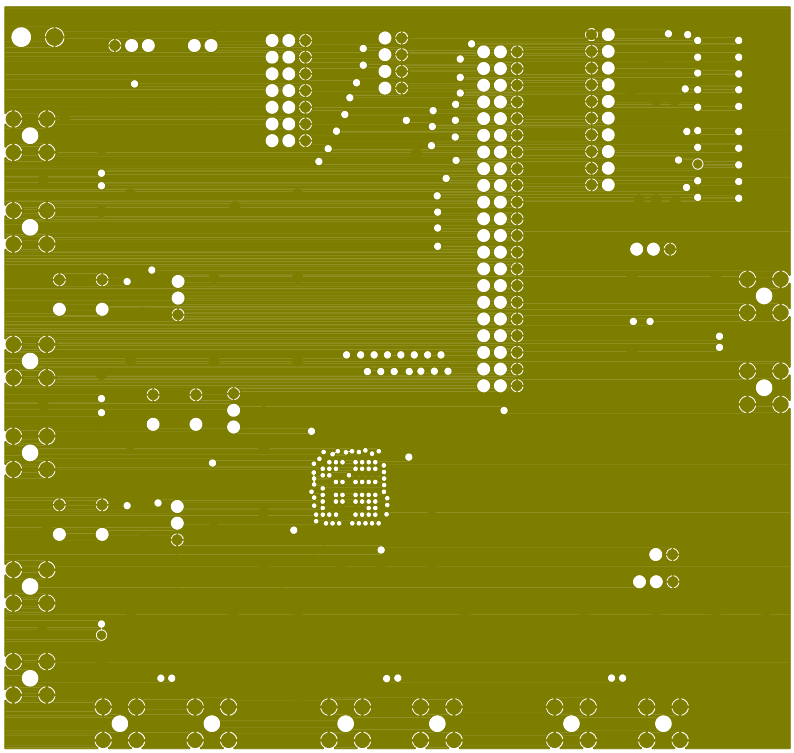


Figure 6. Si5364-EVB—Layer 3, GND

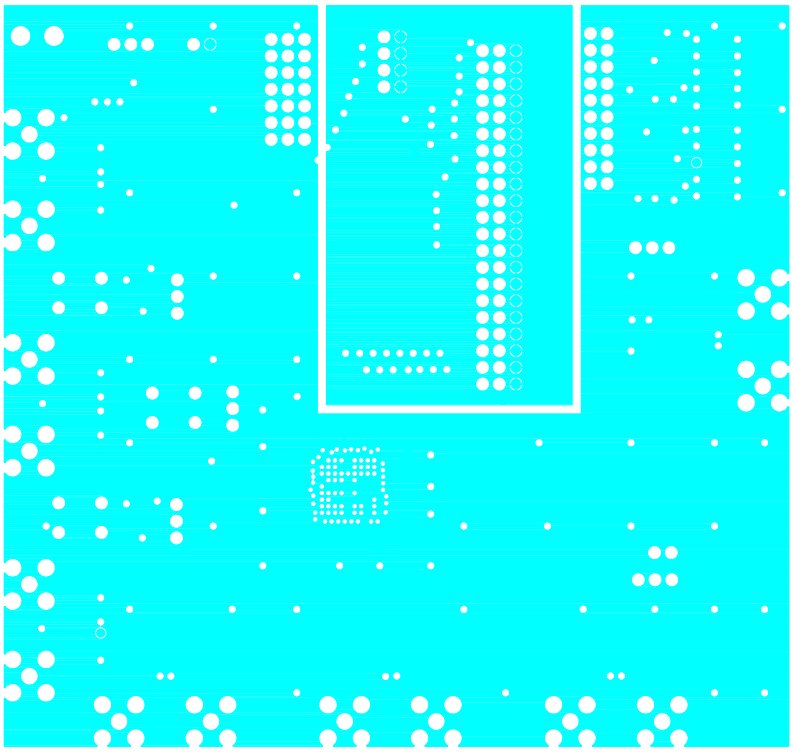


Figure 7. Si5364-EVB—Layer 4, VDD 2.5

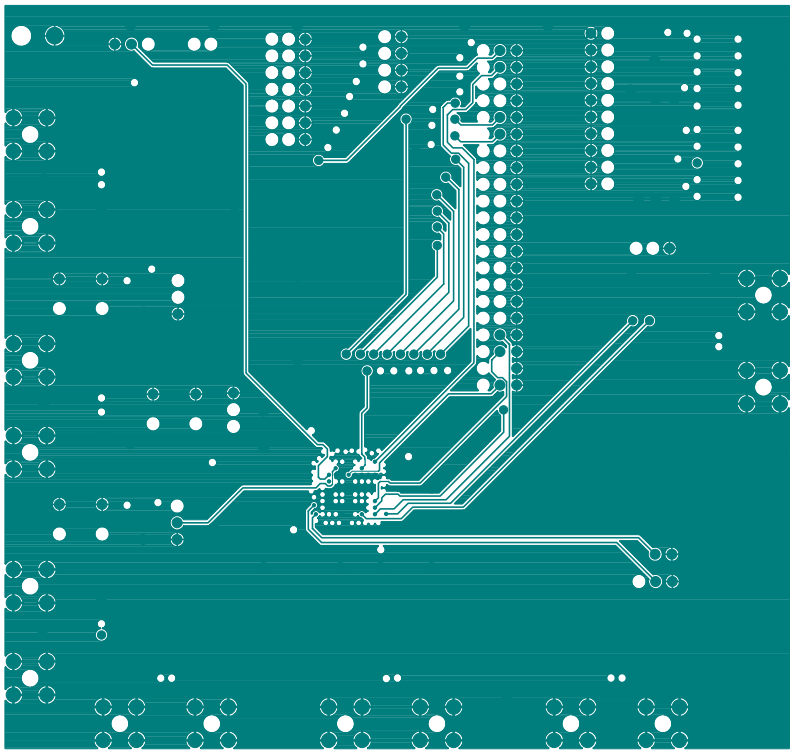


Figure 8. Si5364-EVB—Layer 5, GND

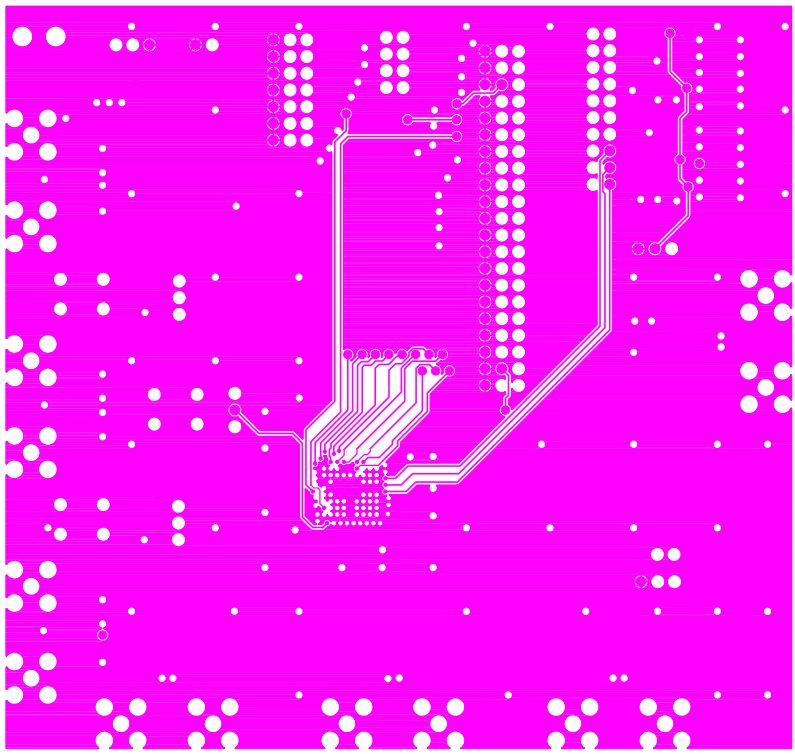


Figure 9. Si5364-EVB—Layer 6, VDD 3.3

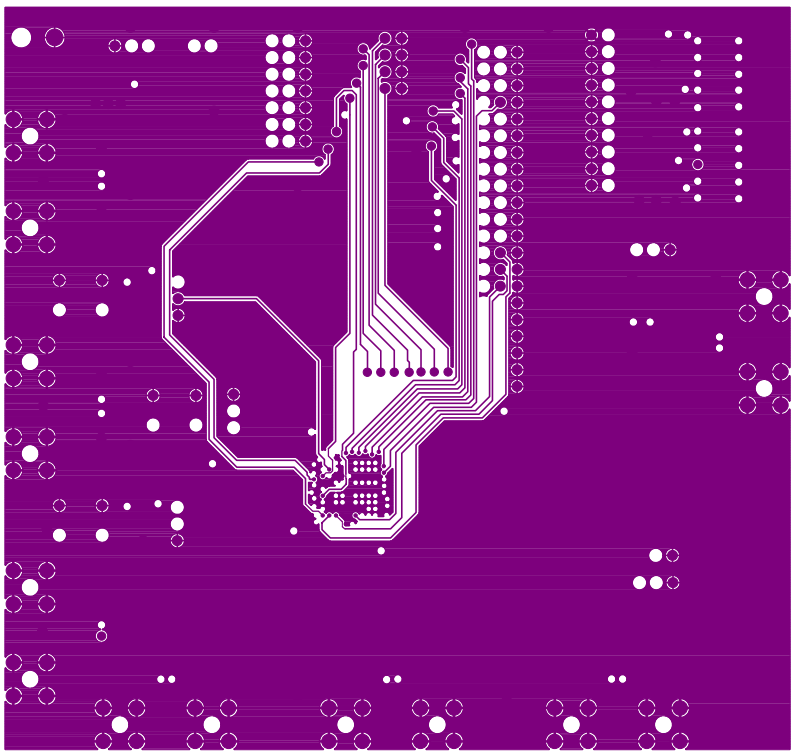


Figure 10. Si5364-EVB—Layer 7, GND

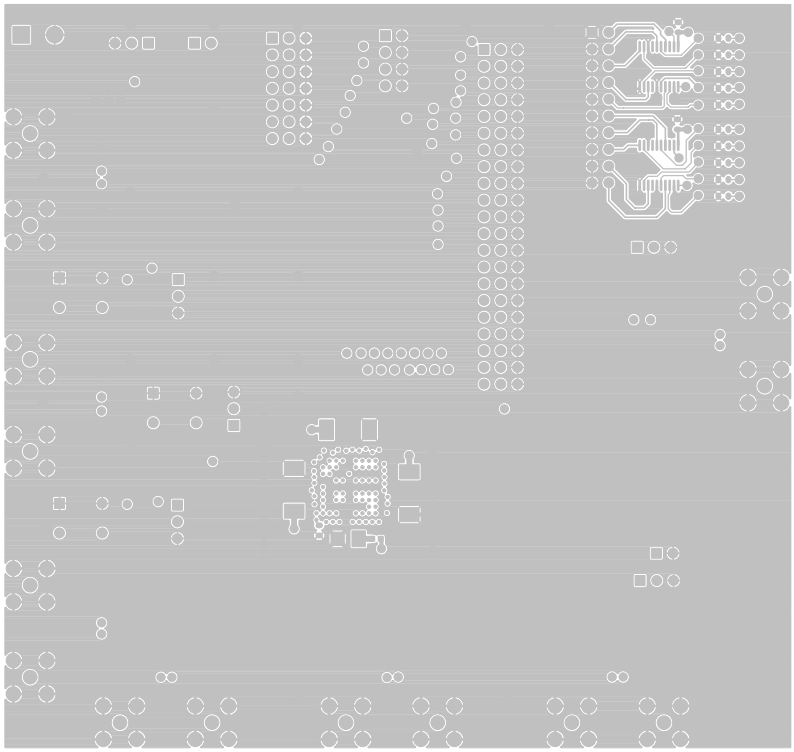


Figure 11. Si5364-EVB—Layer 8, Bottom

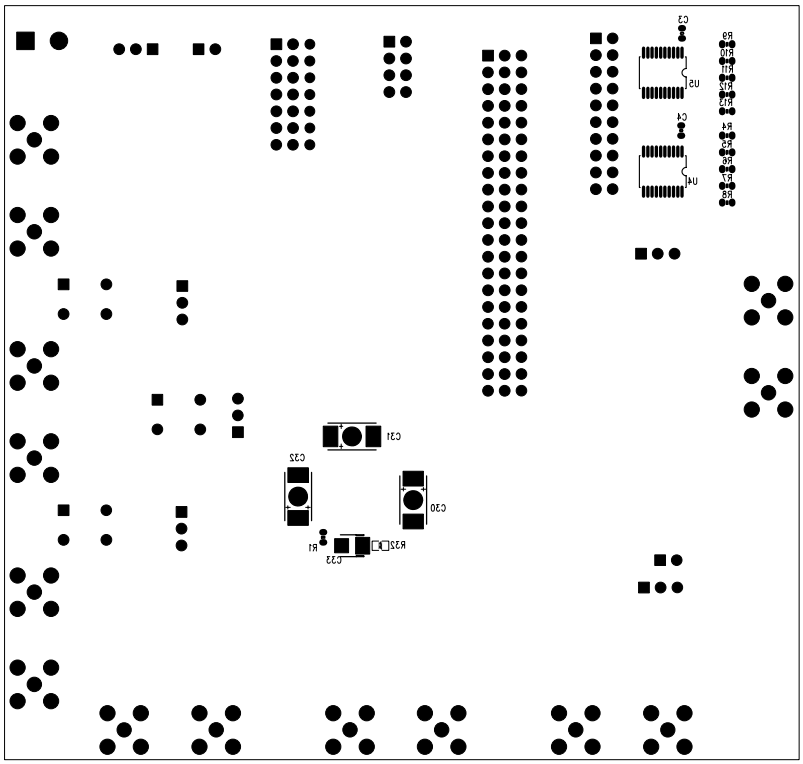


Figure 12. Si5364-EVB Bottom Silkscreen

Document Revision Change List

Revision 0.28 to Revision 0.33

Updated to reflect Rev. D printed circuit boards.

Evaluation Board Assembly Revision History

Assembly Level	PCB Rev.	Si5364 Rev.	Assembly Notes
C-01	Rev. D	Rev. C	Assemble per BOM rev C-01

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