

# HUF76107P3, HUF76107D3, HUF76107D3S

20A, 30V, 0.052 Ohm, N-Channel,  
Logic Level UltraFET Power MOSFETs

June 1998

## Features

- Logic Level Gate Drive
- 20A, 30V
- *Ultra Low On-Resistance*,  $r_{DS(ON)} = 0.052\Omega$
- *Temperature Compensating PSPICE Model*
- *Temperature Compensating SABER Model*
- *Thermal Impedance SPICE Model*
- *Thermal Impedance SABER Model*
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"



## Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

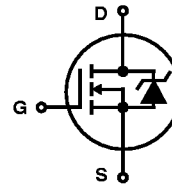
Formerly developmental type TA76107.

## Ordering Information

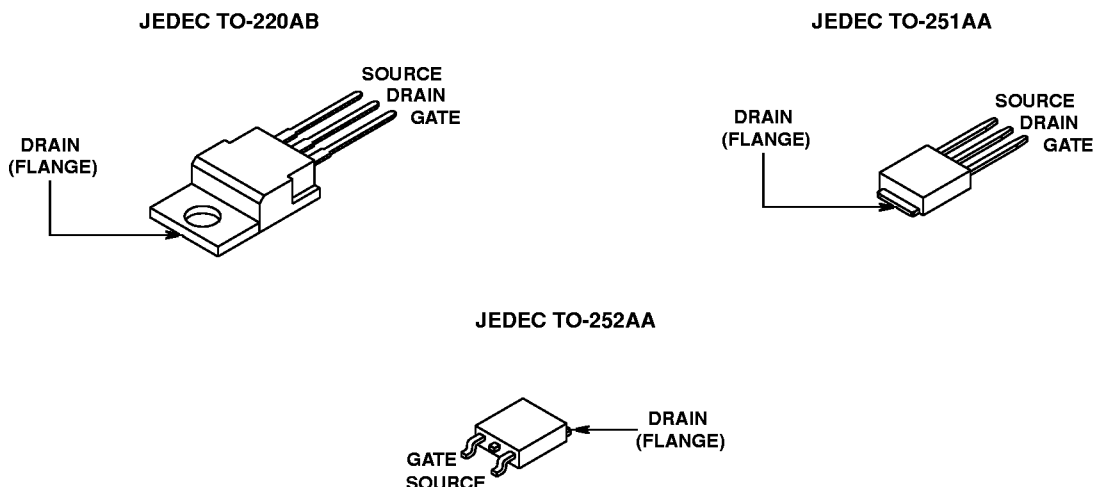
PART NUMBER	PACKAGE	BRAND
HUF76107P3	TO-220AB	76107P
HUF76107D3	TO-251AA	76107D
HUF76107D3S	TO-252AA	76107D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HUF76107D3ST.

## Symbol



## Packaging



## HUF76107P3, HUF76107D3, HUF76107D3S

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	$V_{DSS}$	30	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1)	$V_{DGR}$	30	V
Gate to Source Voltage	$V_{GS}$	$\pm 16$	V
Drain Current			
Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ ) (Figure 2)	$I_D$	20	A
Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 5\text{V}$ )	$I_D$	12	A
Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 4.5\text{V}$ ) (Figure 2)	$I_D$	12	A
Pulsed Drain Current	$I_{DM}$	Figure 4	
Pulsed Avalanche Rating	$E_{AS}$	Figures 6, 17, 18	
Power Dissipation	$P_D$	45	W
Derate Above $25^\circ\text{C}$		0.30	W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	$T_{pkg}$	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

### Off State Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{V}$	-	-	$\pm 100$	nA

### On State Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 20\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 9, 10)	-	0.042	0.052	$\Omega$
		$I_D = 12\text{A}$ , $V_{GS} = 5\text{V}$ (Figure 9)	-	0.058	0.080	$\Omega$
		$I_D = 12\text{A}$ , $V_{GS} = 4.5\text{V}$ (Figure 9,)	-	0.065	0.085	$\Omega$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 12\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 12\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	39	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 12\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	49	nC

### Thermal Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	3.3	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220	-	-	62	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251, TO-252	-	-	100	$^\circ\text{C}/\text{W}$

## HUF76107P3, HUF76107D3, HUF76107D3S

### Switching Specifications ( $V_{GS} = 4.5V$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	$t_{ON}$	$V_{DD} = 15V$ , $I_D \cong 12A$ , $R_L = 1.25\Omega$ , $V_{GS} = 4.5V$ , $R_{GS} = 33\Omega$ (Figures 15, 21, 22)	-	-	120	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	$t_r$		-	66	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	16	-	ns
Fall Time	$t_f$		-	22	-	ns
Turn-Off Time	$t_{OFF}$		-	-	57	ns

### Switching Specifications ( $V_{GS} = 10V$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	$t_{ON}$	$V_{DD} = 15V$ , $I_D \cong 20A$ , $R_L = 0.75\Omega$ , $V_{GS} = 10V$ , $R_{GS} = 33\Omega$ (Figures 16, 21, 22)	-	-	75	ns
Turn-On Delay Time	$t_{d(ON)}$		-	18	-	ns
Rise Time	$t_r$		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	62	-	ns
Fall Time	$t_f$		-	20	-	ns
Turn-Off Time	$t_{OFF}$		-	-	125	ns

### Gate Charge Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 15V$ , $I_D \cong 12A$ , $R_L = 1.25\Omega$ $I_g(REF) = 1.0mA$ (Figures 14, 19, 20)	-	8.6	10.3	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to $5V$		-	4.7	5.7	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $1V$		-	0.35	0.42	nC

### Capacitance Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	$C_{ISS}$	$V_{DS} = 25V$ , $V_{GS} = 0V$ , $f = 1MHz$ (Figure 13)	-	315	-	pF
Output Capacitance	$C_{OSS}$		-	170	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	30	-	pF

**Typical Performance Curves** Unless otherwise specified

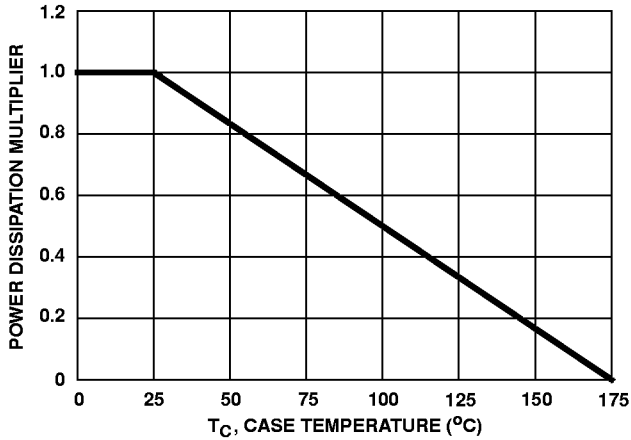


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

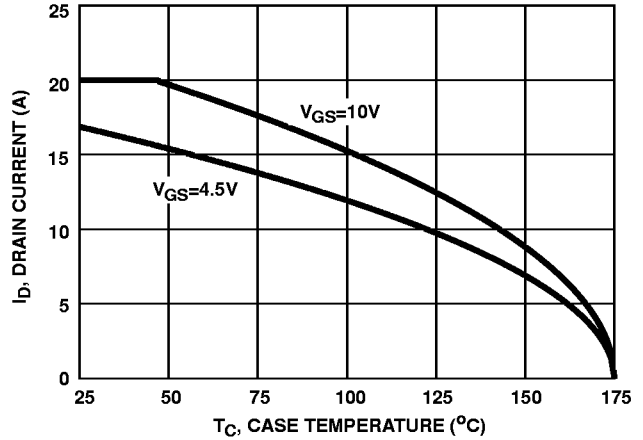


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

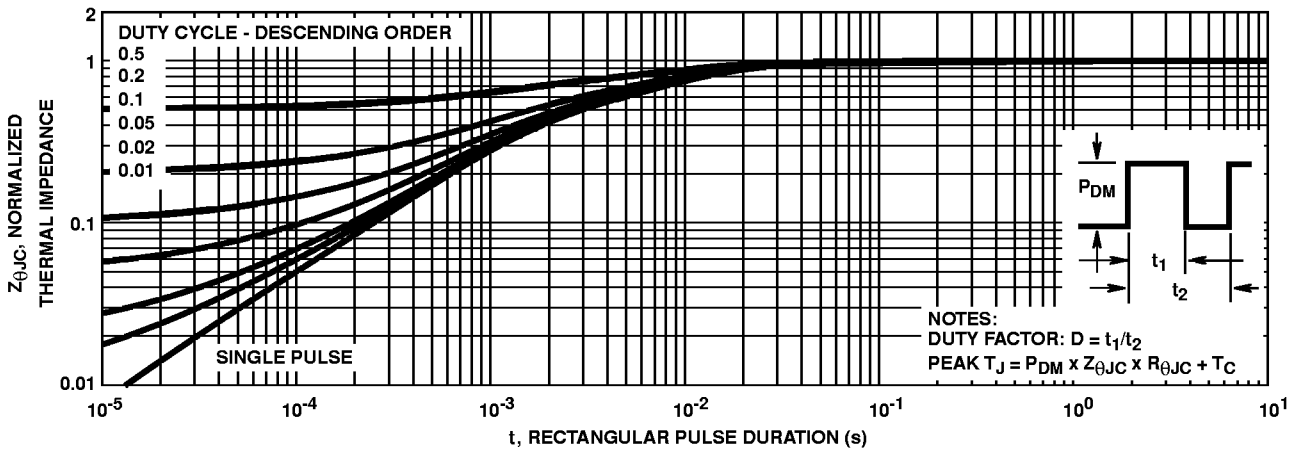


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

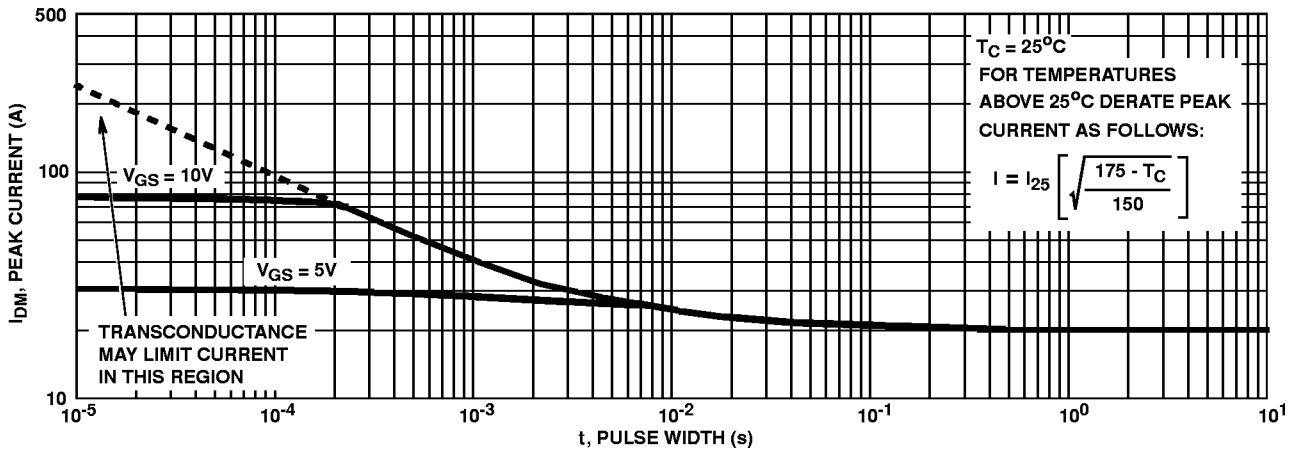


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless otherwise specified (Continued)

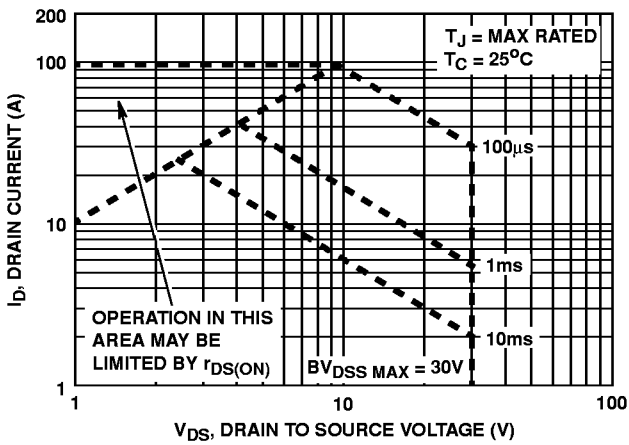
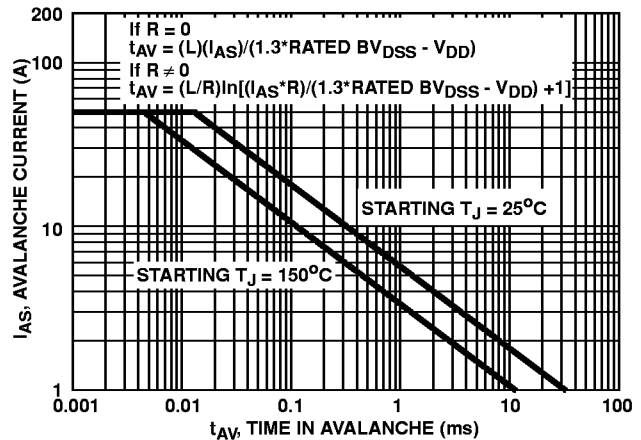


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

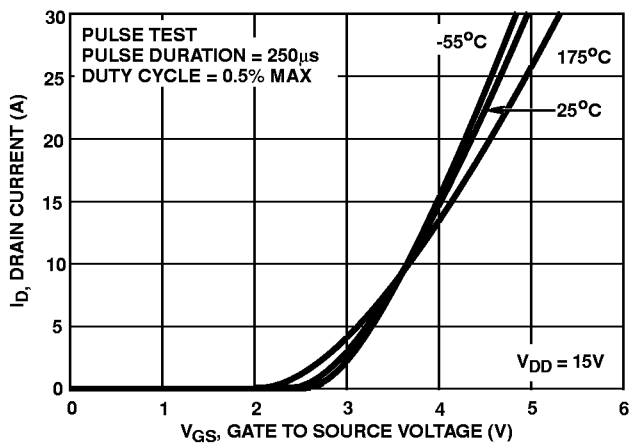


FIGURE 7. TRANSFER CHARACTERISTICS

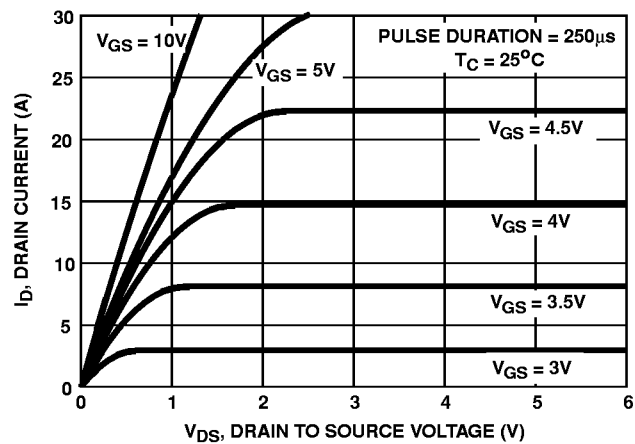


FIGURE 8. SATURATION CHARACTERISTICS

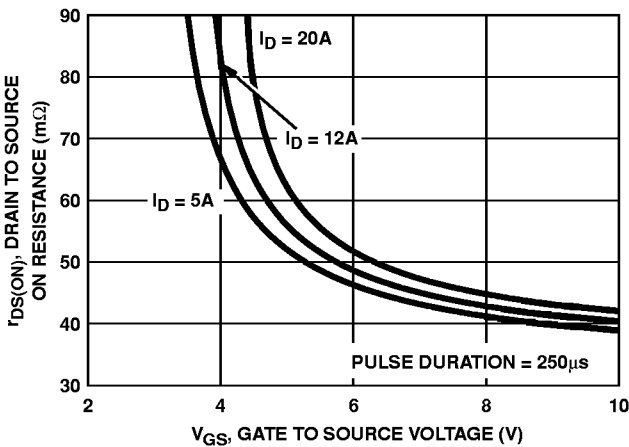


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

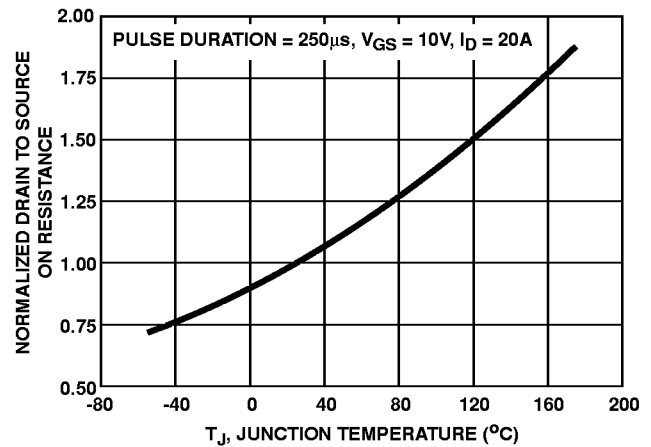


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

**Typical Performance Curves** Unless otherwise specified (Continued)

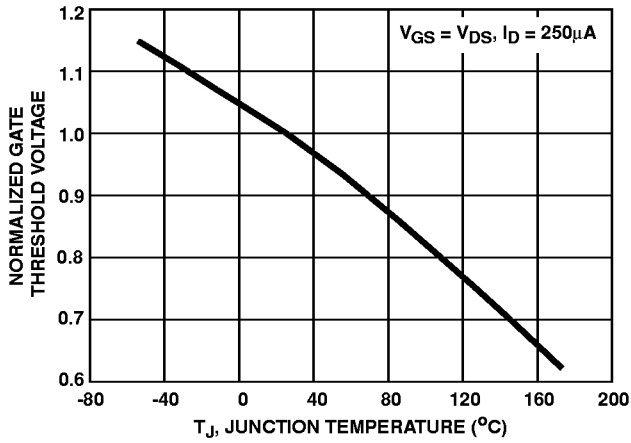


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

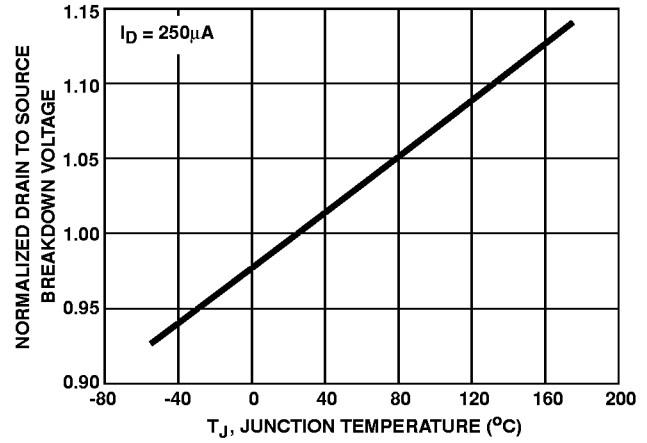


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

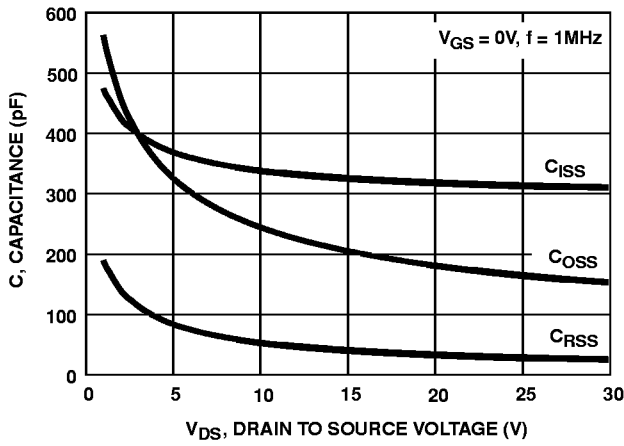
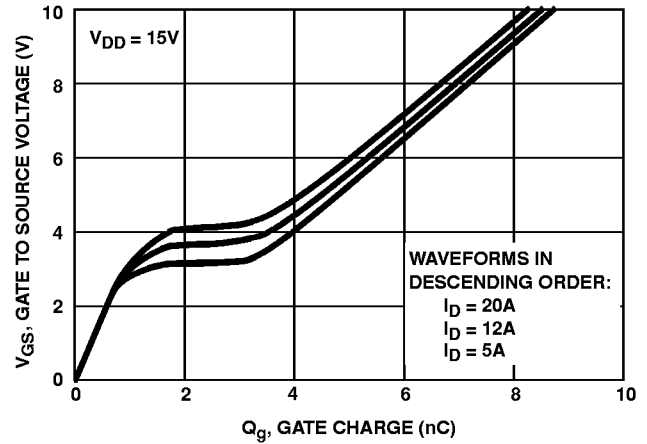


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

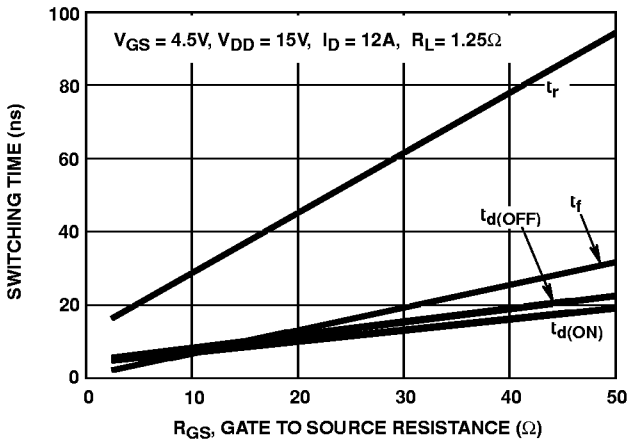


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

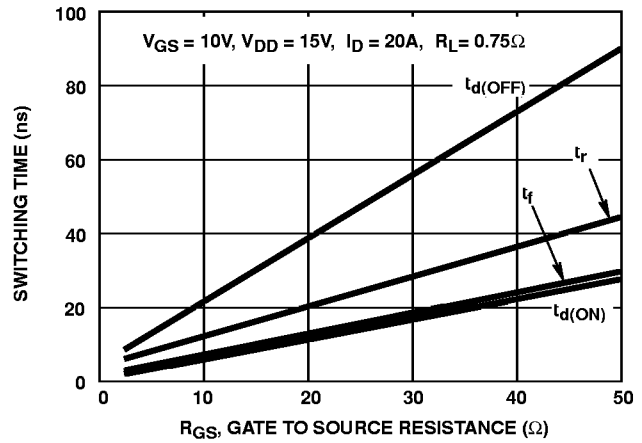


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

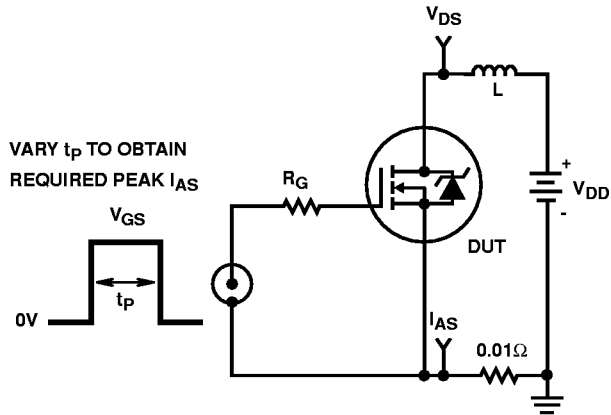


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

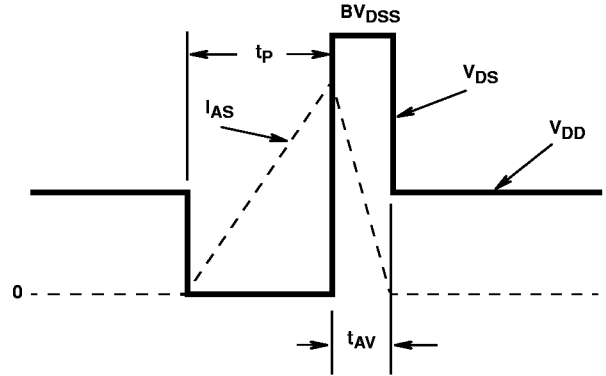


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

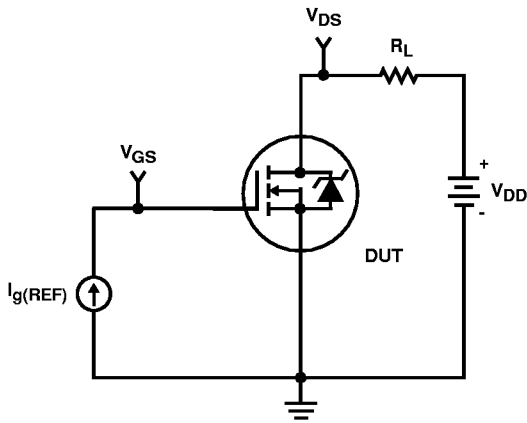


FIGURE 19. GATE CHARGE TEST CIRCUIT

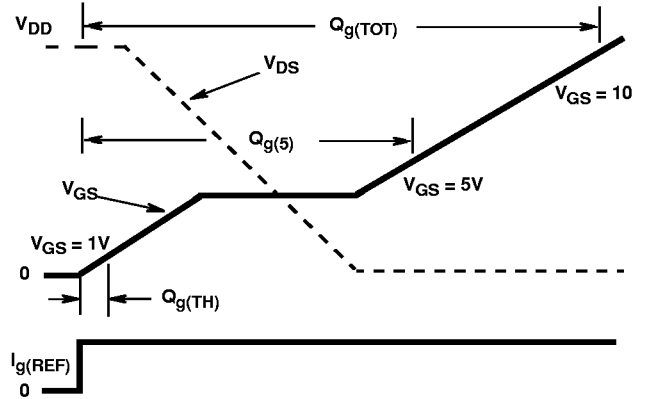


FIGURE 20. GATE CHARGE WAVEFORMS

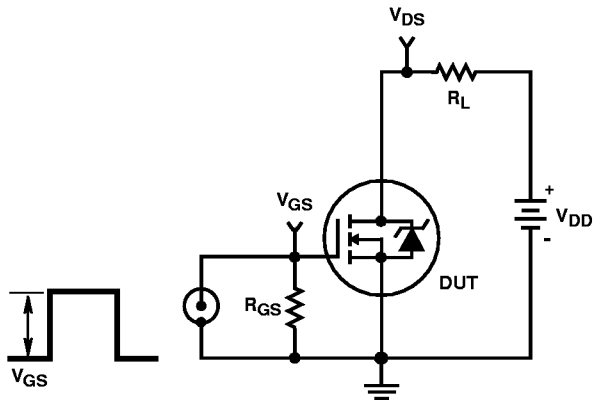


FIGURE 21. SWITCHING TIME TEST CIRCUIT

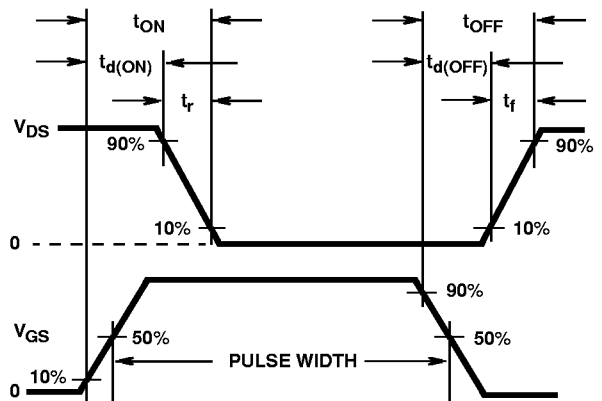


FIGURE 22. SWITCHING TIME WAVEFORM

# HUF76107P3, HUF76107D3, HUF76107D3S

## PSPICE Electrical Model

SUBCKT HUF76107 2 1 3 ; REV June 1998

CA 12 8 4.2e-10  
 CB 15 14 4.9e-10  
 CIN 6 8 2.85e-10

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.7  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 3.61e-9  
 LSOURCE 3 7 3.61e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 3.7e-3  
 RGATE 9 20 3.39  
 RLDRAIN 2 5 10  
 RLGATE 1 9 36.1  
 RLSOURCE 3 7 36.1  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 30e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

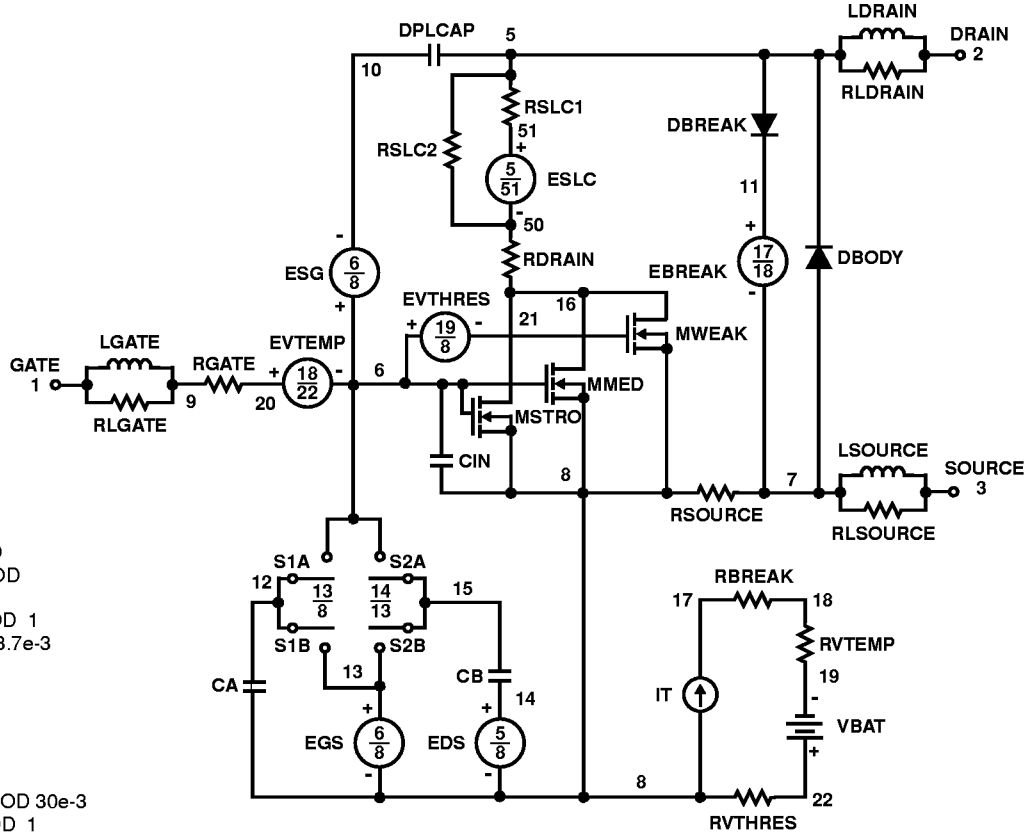
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*50),7))}

.MODEL DBODYMOD D (IS = 2.8e-13 IKF = 5 RS = 1.37e-2 TRS1 = 2e-4 TRS2 = 2e-6 CJO = 4.9e-10 TT = 2.88e-8 M = 3.9e-1 XTI = 4.75 )  
 .MODEL DBREAKMOD D (RS = 2.5e-1 TRS1 = 9.94e-4 TRS2 = 9.12e-7)  
 .MODEL DPLCAPMOD D (CJO = 3.2e-10 IS = 1e-30 N = 10 M = 7.4e-1)  
 .MODEL MMEDMOD NMOS (VTO = 2.07 KP = 1.25 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.39)  
 .MODEL MSTROMOD NMOS (VTO = 2.4 KP = 19.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 1.8 KP = 1e-1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33.9 RS = 1)  
 .MODEL RBREAKMOD RES (TC1 = 9.94e-4 TC2 = 9.84e-8)  
 .MODEL RDRAINMOD RES (TC1 = 3.9e-2 TC2 = 5.5e-5)  
 .MODEL RSLCMOD RES (TC1 = 1e-4 TC2 = 3.2e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 1e-12 TC2 = 6e-6)  
 .MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -5.96e-6)  
 .MODEL RVTEMPMOD RES (TC1 = -1.4e-3 TC2 = 1e-10)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.2 VOFF = -0.5)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = -4.2)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF = 0.0)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.0 VOFF = -0.8)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.







**SPICE Thermal Model**

REV June1998

HUF76107

CTHERM1 th 6 5.0e-5  
 CHERM2 6 5 9.0e-4  
 CHERM3 5 4 1.3e-3  
 CHERM4 4 3 1.3e-3  
 CHERM5 3 2 2.2e-2  
 CHERM6 2 tl 7.9e-3

RHERM1 th 6 2.0e-4  
 RHERM2 6 5 6.0e-3  
 RHERM3 5 4 3.5e-2  
 RHERM4 4 3 8.5e-1  
 RHERM5 3 2 5.1e-1  
 RHERM6 2 tl 1

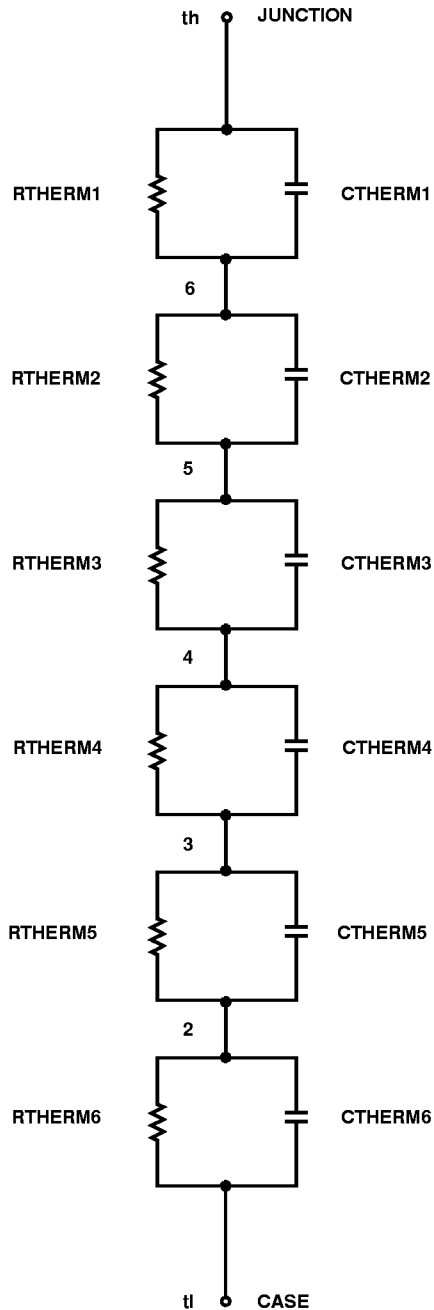
**SABER Thermal Model**

SABER thermal model HUF76107

template thermal\_model th tl  
 thermal\_c th, tl

```
{
    ctherm.ctherm1 th 6 = 5.0e-5
    ctherm.ctherm2 6 5 = 9.0e-4
    ctherm.ctherm3 5 4 = 1.3e-3
    ctherm.ctherm4 4 3 = 1.3e-3
    ctherm.ctherm5 3 2 = 2.2e-2
    ctherm.ctherm6 2 tl = 7.9e-3
```

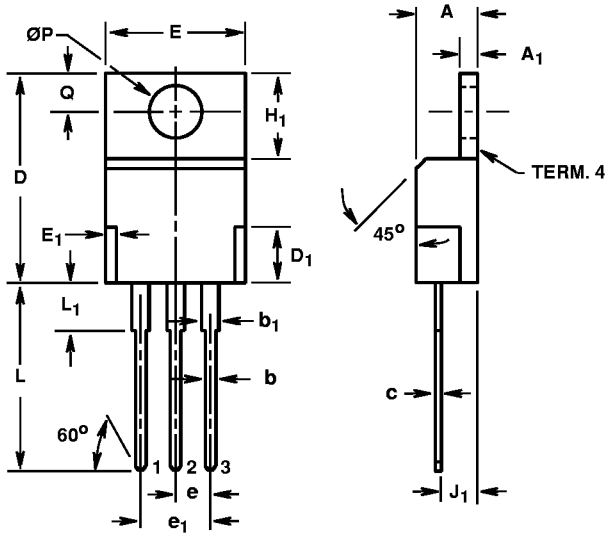
```
rtherm.rtherm1 th 6 = 2.0e-4
rtherm.rtherm2 6 5 = 6.0e-3
rtherm.rtherm3 5 4 = 3.5e-2
rtherm.rtherm4 4 3 = 8.5e-1
rtherm.rtherm5 3 2 = 5.1e-1
rtherm.rtherm6 2 tl = 1
}
```



HUF76107P3, HUF76107D3, HUF76107D3S

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D <sub>1</sub>	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E <sub>1</sub>	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.235	0.255	5.97	6.47	-
J <sub>1</sub>	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

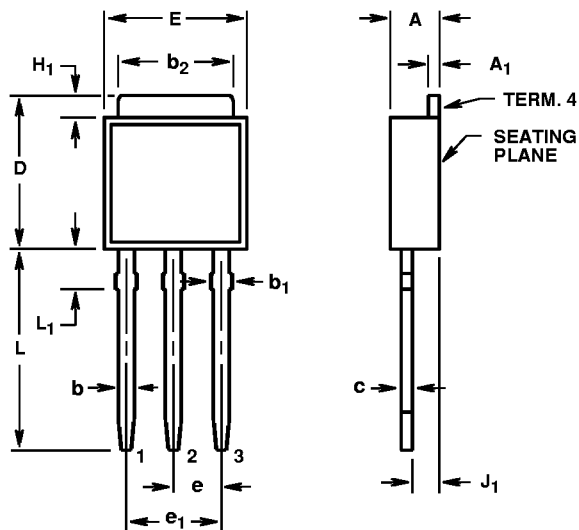
NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L<sub>1</sub>.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

# HUF76107P3, HUF76107D3, HUF76107D3S

## TO-251AA

### 3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



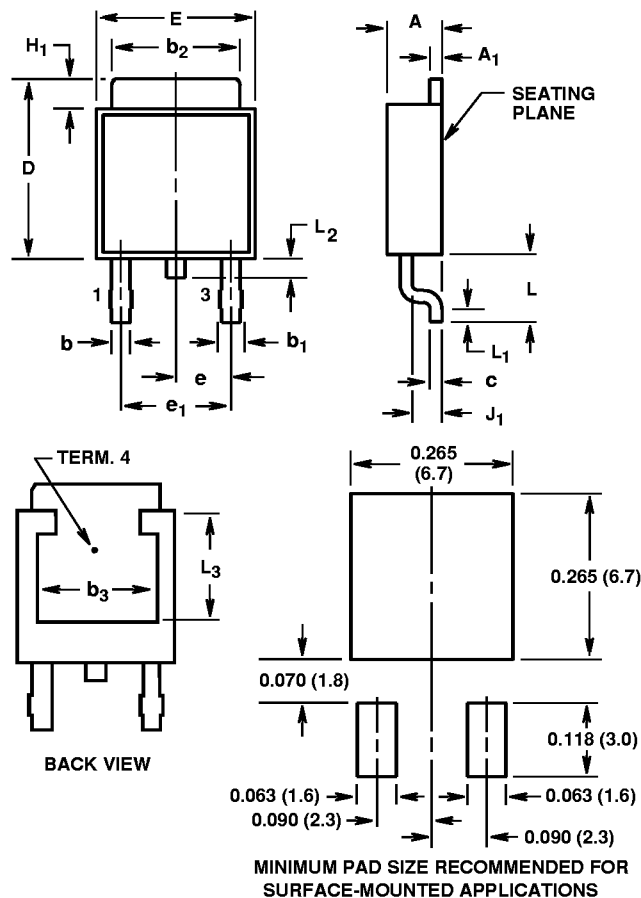
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b <sub>1</sub>	0.033	0.040	0.84	1.01	3
b <sub>2</sub>	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e <sub>1</sub>	0.180 BSC		4.57 BSC		5
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L <sub>1</sub>	0.075	0.090	1.91	2.28	2

#### NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

## TO-252AA

### SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b <sub>1</sub>	0.033	0.040	0.84	1.01	4
b <sub>2</sub>	0.205	0.215	5.21	5.46	4, 5
b <sub>3</sub>	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e <sub>1</sub>	0.180 BSC		4.57 BSC		7
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L <sub>1</sub>	0.020	-	0.51	-	4, 6
L <sub>2</sub>	0.025	0.040	0.64	1.01	3
L <sub>3</sub>	0.170	-	4.32	-	2

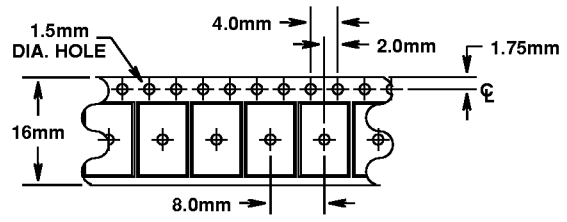
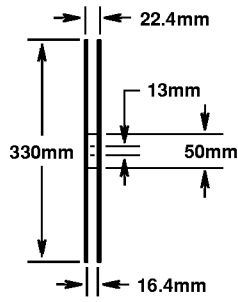
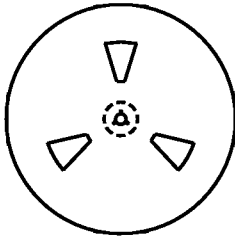
#### NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L<sub>3</sub> and b<sub>3</sub> dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L<sub>1</sub> is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 8 dated 1-98.

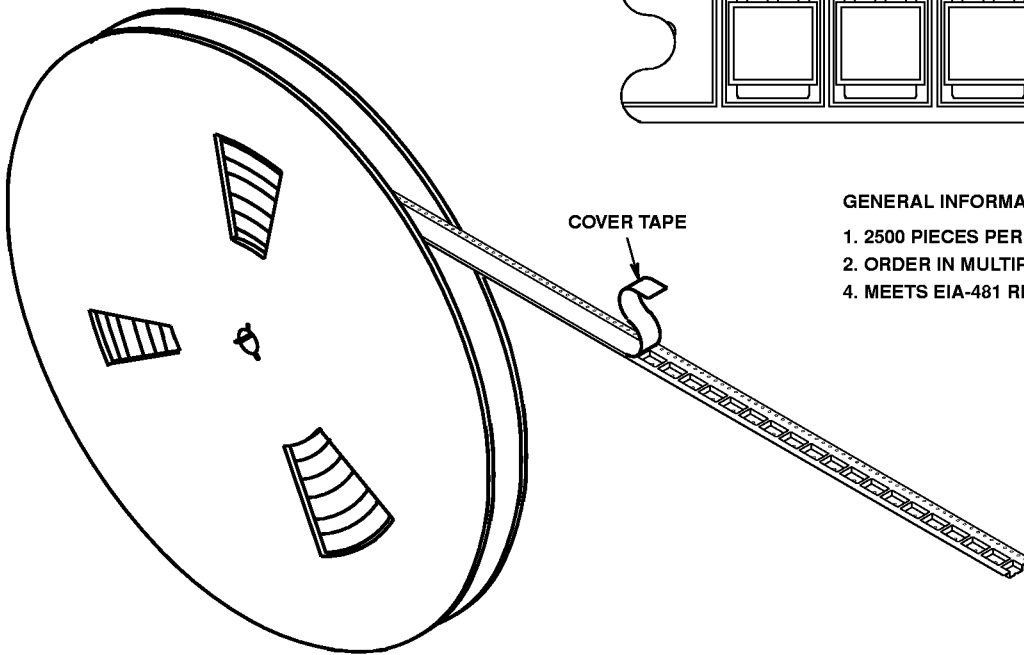
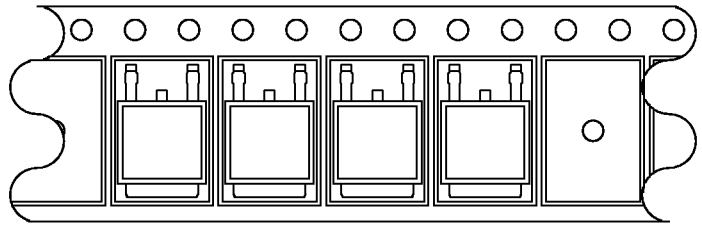
HUF76107P3, HUF76107D3, HUF76107D3S

**TO-252AA**

16mm TAPE AND REEL



USER DIRECTION OF FEED



**GENERAL INFORMATION**

- 1. 2500 PIECES PER REEL.
- 2. ORDER IN MULTIPLES OF FULL REELS ONLY.
- 4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 8 dated 1-98