Isolated Synchronous Flyback Controller with Integrated *i*Coupler

Data Sheet

ADP1071-1/ADP1071-2

FEATURES

- Current mode controller for flyback topology
- ADP1071-1: programmable LLM or CCM for high V_{IN} applications
- ADP1071-2: forced CCM operation
- Programmable slope compensation
- Integrated 5 kV isolation (wide body SOIC package) or 3.0 kV (LGA package) rated dielectric isolation voltage with Analog Devices, Inc., patented *i*Coupler technology
- Wide voltage supply range
  - Primary V_{DD}: up to 60 V (ADP1071-2 only)
  - Secondary V_{DD2}: up to 36 V
- Integrated 1 A primary side MOSFET driver
- Integrated 1 A secondary side MOSFET drivers for synchronous rectification
- Integrated error amplifier and <1% accurate reference voltage
- Programmable frequency range: 50 kHz to 600 kHz
- Duty cycle clamp limit 85%
- Programmable soft start and soft start from precharged load
- Protection features such as short circuit, output overvoltage, and overtemperature protection
- Power saving LLM using MODE pin (ADP1071-1only)
- Cycle by cycle input overcurrent protection
- Precision enable UVLO with hysteresis
- Frequency synchronization
- Safety and regulatory approvals (pending)
- UL recognition
  - 5000 V rms for 1 minute per UL 1577 (for wide body SOIC package)
  - 3000 V rms for 1 minute per UL 1577 (for LGA package)
- CSA Component Acceptance Notice 5A
- VDE certificate of conformity
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - V_{IORM} = 849 V peak (for wide body SOIC package)
  - V_{IORM} = 565 V peak (for LGA package)
- CQC certification per GB4943.1-2011
- Available in 16-lead SOIC_W package and 24 terminal LGA package

APPLICATIONS

- Isolated dc-to-dc or ac-to-dc power conversion
- Telecom, industrial
- Small cell
- PoE powered device
- Enterprise switches and routers

FUNCTIONAL BLOCK DIAGRAM

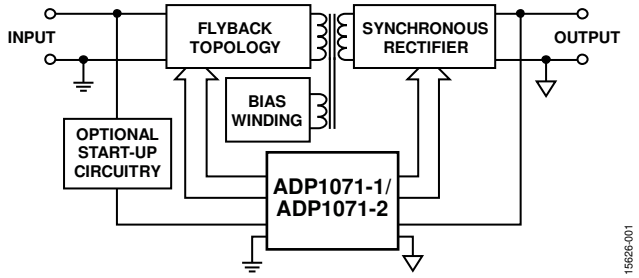

Figure 1.

GENERAL DESCRIPTION

The ADP1071-1/ADP1071-2 are pulse-width modulation (PWM) current mode fixed frequency synchronous flyback controllers designed for isolated dc-to-dc power supplies. Analog Devices proprietary *i*Couplers® are integrated in the ADP1071-1/ADP1071-2 to eliminate the bulky signal transformers and optocouplers that transmit signals over the isolation boundary. Integrating the *i*Couplers reduces system design complexity, cost, and component count and improves overall system reliability. With the integrated isolators and metal-oxide semiconductor field effect transistor (MOSFET) drivers on both the primary and the secondary side, the ADP1071-1/ADP1071-2 offer a compact system level design and yield a higher efficiency than a diode rectified flyback converter at heavy loads.

Output regulation is achieved by sensing the output voltage on the secondary side, where the feedback and the PWM signals are transmitted between the primary and secondary sides through the *i*Couplers.

The ADP1071-1/ADP1071-2 are offered in a 16-lead SOIC_W package with an isolation voltage rating of 5 kV rms. The ADP1071-2 is designed for isolated dc-to-dc applications typically with an input voltage less than 36 V, and the ADP1071-1 targets high input voltage applications, in which the dc input voltage can exceed 60 V.

The ADP1071-1/ADP1071-2 offer features such as input current protection, output overvoltage protection (OVP), undervoltage lockout (UVLO), precision enable with adjustable hysteresis, overtemperature protection (OTP), and power saving light load mode (LLM).

Rev. B

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9/2018—Revision 0: Initial Version

SPECIFICATIONS

ADP1071-1: VREG1 = 9 V, VDD2 = 12 V, T_A = −40°C to +125°C, unless otherwise noted. ADP1071-2: VIN = 24 V, VDD2 = 12 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ADP1071-1 SUPPLY (PRIMARY)						
Supply Voltage	V_{REG1}	1 µF capacitor from VREG1 to AGND1	4.7	8	12.5	V
Quiescent Supply Current	I_{VREG1}	VREG1 > VREG1 UVLO, GATE pin unloaded				
		At 100 kHz		3.8		mA
		At 300 kHz		4.6		mA
		At 600 kHz		6.8		mA
	I_{VREG1}	VREG1 > VREG1 UVLO, GATE pin loaded with 2.2 nF				
		At 100 kHz		5.5		mA
		At 300 kHz		10		mA
		At 600 kHz		16.6		mA
VREG1 Start-Up Current	$I_{VREG1\_STARTUP}$	V_{EN} < 1.2 V			160	µA
VREG1 UVLO		VREG1 rising			4.7	V
		VREG1 falling	4			V
UVLO Hysteresis				0.19		V
ADP1071-2 SUPPLY (PRIMARY)						
Supply Voltage	V_{IN}	4.7 µF capacitor from VIN to AGND1, 1 µF capacitor from VREG1 to AGND1	4.7	24	60	V
Quiescent Supply Current	I_{VIN}	VIN > VIN UVLO, GATE pin unloaded				
		At 100 kHz		3.8		mA
		At 300 kHz		4.4		mA
		At 600 kHz		6.8		mA
	I_{VIN}	VIN > VIN UVLO, GATE pin loaded with 2.2 nF				
		At 100 kHz		5.5		mA
		At 300 kHz		11		mA
		At 600 kHz		22		mA
VIN Shutdown Current		EN pin voltage (V_{EN}) < 1.2 V, VREG1 = 0 V, VIN = 60 V			55	µA
VIN and VREG1 Start-Up Current	$I_{VIN\_STARTUP}$	V_{EN} < 1.2 V, VREG1 = 12 V, VIN = 12 V			160	µA
VIN UVLO		VIN rising			4.7	V
		VIN falling	4			V
UVLO Hysteresis				0.19		V
SWITCHING TIME						
Time from EN High to GATE Output Switching		V_{EN} > 1.2 V, 1 µF capacitor on VREG1		1		ms
Time from EN Low to GATE Output Stops Switching		V_{EN} < 1.0 V, 1 µF capacitor on VREG1		1		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY (SECONDARY)						
Supply Voltage	V_{DD2}	4.7 µF capacitor from VDD2 to AGND2, 1 µF capacitor from VREG2 to AGND2	4.5	12	36	V
Quiescent Supply Current	I_{DD2}	SR unloaded				
		At 100 kHz		5.3		mA
		At 300 kHz		5.5		mA
		At 600 kHz		5.6		mA
	I_{DD2}	SR loaded with 2.2 nF				
		At 100 kHz		6.4		mA
		At 300 kHz		8.7		mA
		At 600 kHz		12.1		mA
VDD2 UVLO Threshold		VDD2 rising			3.55	V
		VDD2 falling	3			V
UVLO Hysteresis				145		mV
Secondary UVLO Hiccup Time				200		ms
OSCILLATOR						
Switching Frequency (f_S)		RT resistance (R_{RT}) = 480 kΩ (±1%)	50 − 10%	50	50 + 10%	kHz
		R_{RT} = 240 kΩ (±1%)	100 − 10%	100	100 + 10%	kHz
		R_{RT} = 120 kΩ (±1%)	200 − 10%	200	200 + 10%	kHz
		R_{RT} = 80 kΩ (±1%)	300 − 10%	300	300 + 10%	kHz
		R_{RT} = 60 kΩ (±1%)	400 − 10%	400	400 + 10%	kHz
		R_{RT} = 40 kΩ (±1%)	600 − 10%	600	600 + 10%	kHz
VREG1 PIN						
VREG1 Voltage Clamp		VREG1 current (I_{VREG1}) = 3 mA, V_{EN} < 1.2 V	13.5	14.3	15.2	V
VREG1 Clamp Series Resistance		VREG1 forced current of 5 mA and 10 mA		16		Ω
GATE DRIVERS (PRIMARY)						
GATE High Voltage		I_{VREG1} = 20 mA, VIN > 9 V (ADP1071-2 only)	7.8	8	8.2	V
Gate Short-Circuit Peak Current[1]		8 V on VREG1		1.0		A
GATE Rise Time		GATE loaded with 2.2 nF, 10% to 90%		17		ns
GATE Fall Time		GATE loaded with 2.2 nF, 90% to 10%		15		ns
GATE Source Resistance	R_{ON_SOURCE}	Source = 100 mA		4		Ω
GATE Sink Resistance	R_{ON_SINK}	Sink = 100 mA		2		Ω
GATE Maximum Duty Cycle				84		%
GATE Minimum On Time		At 300 kHz, includes blanking time		175		ns
SR DRIVER (SECONDARY)						
SR High Voltage		I_{VREG2} = 15 mA, VDD2 > 5.5 V	4.9	5	5.1	V
SR Short Circuit Peak Current[1]		5 V on VREG2		1.0		A
SR Rise Time		SR loaded with 2.2 nF, 10% to 90%		13		ns
SR Fall Time		SR loaded with 2.2 nF, 90% to 10%		10		ns
SR Minimum On Time		At 300 kHz		462		ns
SR Source Resistance	$R_{ON\_SR\_SOURCE}$	Source = 100 mA		3		Ω
SR Sink Resistance	$R_{ON\_SR\_SINK}$	Sink = 100 mA		1.5		Ω
DEAD TIME SETTING (GATE TO SR)		Dead time between SR falling and GATE rising		30		ns
		Dead time between GATE falling and SR rising		52		ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT-LIMIT SENSE (PRIMARY)						
CS Limit Threshold	V_{CS_LIM}	Overcurrent sense limit threshold		120		mV
CS Leading Edge Blanking Time				150		ns
Current Source di/dt for Slope Compensation		Switching period (t_S) = 1/f_S		20		µA per t_S
Overcurrent Protection (OCP) Comparator Delay				40		ns
Time in OCP Before Entering Hiccup Mode				1.5		ms
OCP Hiccup Time		See the Input/Output Current-Limit Protection section		40		ms
FB PIN AND ERROR AMPLIFIER						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C	−0.85%	+1.2	+0.85%	V
		T_J = −40°C to +125°C	−1.25%	+1.2	+1.25%	V
Temperature Coefficient					76	ppm/°C
FB Input Bias Current			−100	1	+100	nA
Transconductance	g_m		230	250	270	µS
Output Current Clamp						
Minimum				−57		µA
Maximum				43		µA
COMP Clamp Voltage						
Maximum				2.52		V
Minimum				0.7		V
Open-Loop Gain				80		dB
Output Shunt Resistance				5		GΩ
Gain Bandwidth Product				1		MHz
PRECISION ENABLE THRESHOLD						
EN Threshold	V_{EN}	EN rising	1.14	1.2	1.26	V
EN Hysteresis		V_{EN} < 1.2 V		4		µA
		V_{EN} > 1.2 V		1		µA
EN Hysteresis Current				3		µA
LIGHT LOAD MODE (ADP1071-1 ONLY)						
LLM Current Source		Resistor from MODE to AGND1	5.5	6.5	7.5	µA
TEMPERATURE						
Thermal Shutdown				155		°C
Hysteresis				−15		°C
SOFT START						
Open Loop Soft Start Time on Primary	t_{SS1}	GATE resistor = 10 kΩ		16 × 775		t_S
		GATE resistor = 22 kΩ		64 × 775		t_S
		GATE resistor = 47 kΩ		256 × 775		t_S
		GATE resistor = 100 kΩ		4 × 775		t_S
SS2 Current Source		During startup		20		µA
SS2 Discharging Current		During a fault condition or soft stop		30		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYNC PIN						
Synchronization Range			100		600	kHz
Input Pulse Width			100			ns
Number of Cycles Before Synchronization				7		Cycles
Input Voltage						
Low					0.4	V
High			3			V
Leakage Current					1	µA
*i*COUPLER DELAY						
COMP Signal Delay Through *i*Coupler				600		ns
OVP PIN THRESHOLDS						
OVP Pin OV Threshold		Overvoltage (OV) threshold for OVP pin	1.3	1.36	1.42	V
OVP Pin OV Hysteresis				36		mV
OVP Comparator Delay (Includes *i*Coupler Delay)				320		ns
OVP Pin Leakage Current					1	µA
OVP Hiccup		Time before entering OVP hiccup mode		200		ms
		Hiccup time trigged by OVP event		200		ms

[1] Short-circuit duration is less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
WIDE BODY SOIC *i*COUPLER						
Rated Dielectric Insulation Voltage		1 minute duration		5		kV
Minimum External Air Gap (Clearance)		Measured from input terminals to output terminals, shortest distance through air	7.6			mm
Minimum External Air Gap (Creepage)		Measured from input terminals to output terminals, shortest distance path along body	7.6			mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation		0.030		mm
Tracking Resistance (Comparative Tracking Index)	CTI			>400		V
Isolation Group		Material Group (DIN VDE 0110, 1/89, Table 1)		II		
LAND GRID ARRAY (LGA) *i*COUPLER						
Rated Dielectric Insulation Voltage		1 minute duration		2.5		kV
Minimum External Air Gap (Clearance)		Measured from input terminals to output terminals, shortest distance through air	4			mm
Minimum External Air Gap (Creepage)		Measured from input terminals to output terminals, shortest distance path along body	4			mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation		0.030		mm
Tracking Resistance (Comparative Tracking Index)	CTI			>400		V
Isolation Group		Material Group (DIN VDE 0110, 1/89, Table 1)		I		

REGULATORY INFORMATION

See Table 3, Table 4, and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 3. Regulatory Information for Wide Body SOIC Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011:
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (1 MOPP)), 490 V rms (686 V peak) Reinforced insulation (2 MOPP), 238 V rms (325 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 780 V secondary (1103 V peak)	Reinforced insulation, V_{IORM} = 849 peak, V_{IOTM} = 8000 V peak	Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 389 V rms (552 V peak), tropical climate, altitude ≤ 5000 meters
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each product is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

Table 4. Regulatory Information for LGA Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011:
Single Protection, 3000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (1 MOPP)), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 400 V secondary (565 V peak)	Reinforced insulation, V_{IORM} = 565 V peak, V_{IOTM} = 4242 V peak impulse voltage = 4242 V peak	Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak), tropical climate, altitude ≤ 5000 meters
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each product is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, EN	66 V
VDD2	42 V
VREG1	16 V
VREG2	6 V
GATE	−0.3 V to +16 V
RT, CS, SYNC, SS2, FB, COMP, OVP, MODE, SR	6.5 V
AGND1, AGND2	±0.3 V
Operating Temperature Range	−40°C to +125°C
Common-Mode Transients[1]	±50 kV/µs
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C
Electrostatic Discharge (ESD)	
Charged Device Model (CDM)	250 V
Human Body Model (HBM)	1 kV

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
RW-16 (Wide Body SOIC)	79.3	44.6	°C/W
CC-24-6 (LGA)	62.1	43	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

Table 7. Maximum Continuous Working Voltage Wide Body SOIC[1]

Parameter	Max	Unit	Constraint
Waveform			
AC Voltage			
Bipolar	565	V peak	50-year minimum lifetime
Unipolar	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 8. Maximum Continuous Working Voltage, LGA[1]

Parameter	Max	Unit	Constraint
Waveform			
AC Voltage			
Bipolar	565	V peak	50-year minimum lifetime
Unipolar	909	V peak	Limited by creepage
DC Voltage	565	V peak	Limited by creepage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

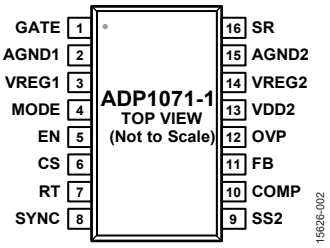

Figure 2. ADP1071-1 SOIC_W Pin Configuration

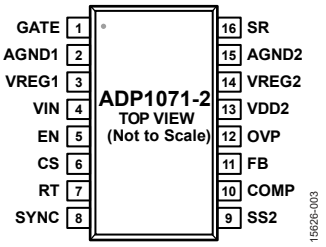

Figure 3. ADP1071-2 SOIC_W Pin Configuration

Table 9. Pin Function Descriptions, Wide-Body SOIC

Pin No.			
ADP1071-1	**ADP1071-2**	**Mnemonic**	**Description**
1	1	GATE	Driver Output for the Main Power MOSFET on the Primary Side. GATE is a multiple function pin. Connect a resistor from GATE to AGND1 to set up the open loop soft start time.
2	2	AGND1	Ground for the Primary Side.
3	3	VREG1	8 V Regulated Low Dropout (LDO) Output for the MOSFET Driver. Connect 1 µF or greater from VREG1 to AGND1.
4	Not applicable	MODE	Light Load Mode Pin. ADP1071-1 Only. This pin sets the light load mode threshold. Connect MODE to AGND1 to enable forced continuous conduction mode (CCM), or to a high logic (2.5 V or higher) to force an LLM operation, or to a resistor to set up an LLM threshold voltage.
Not applicable	4	VIN	Input Voltage (ADP1071-2 Only). See the Primary Side Supply, Input Voltage, and LDO section. Connect a 4.7 µF capacitor to this pin. The size of this capacitor can be reduced if the input voltage to this pin is guaranteed stable. Reference this pin to AGND1.
5	5	EN	Precision Enable Input. The controller is enabled when EN is above the EN threshold voltage. This pin also has a programmable EN hysteresis. This pin is referenced to AGND1.
6	6	CS	Input Current Sensing. This pin senses the input PWM current. Place a current sense resistor between the source terminal of the power MOSFET and AGND1. This current sense resistor sets up the input current limit. This pin is also used for the external slope compensator. Connect a resistor from CS to the current sense resistor to generate a voltage ramp for the slope compensation. Reference this pin to AGND1. Connect a 33 pF to 100 pF capacitor at this pin to act as a resistor capacitor (RC) filter along with the slope compensation resistor in noisy environments.
7	7	RT	Switching Period Resistor. Connect a resistor from RT to AGND1 to set the oscillator frequency.
8	8	SYNC	Frequency Synchronization. Connect an external clock to the SYNC pin to synchronize the internal oscillator to this external clock frequency. Connect SYNC to AGND1 if this feature is not used. It is recommended that the SYNC frequency be within 10% of the frequency set by the RT pin.
9	9	SS2	Soft Start on the Secondary Side. Connect a capacitor from SS2 to AGND2 to set up the soft start time on the secondary side.
10	10	COMP	Compensation Node on the Secondary Side. This pin is the output of the transconductance (g_m) amplifier. Reference this pin to AGND2.
11	11	FB	Feedback Node on the Secondary Side. Set up the resistive divider from the output voltage such that the nominal voltage, when the power supply is in regulation, is 1.2 V. Reference this pin to AGND2.
12	12	OVP	Output Overvoltage Protection. The OVP threshold is set at 1.36 V. Connect a resistive divider from OVP to the output and AGND2.
13	13	VDD2	Input Supply on the Secondary Side. Connect VDD2 to the output voltage of the power supply for a self driven configuration. Connect a 4.7 µF capacitor from VDD2 to AGND2. The size of this capacitor can be reduced if the input voltage to VDD2 is guaranteed to be stable.
14	14	VREG2	5 V Regulated LDO Output for Internal Bias and Powering of the Drivers of the Synchronous Rectifiers. Do not use VREG2 as a reference or load. Connect a 1 µF capacitor from VREG2 to AGND2.
15	15	AGND2	Analog Ground on Secondary Side.
16	16	SR	Driver Output for Synchronous Rectifier MOSFET.

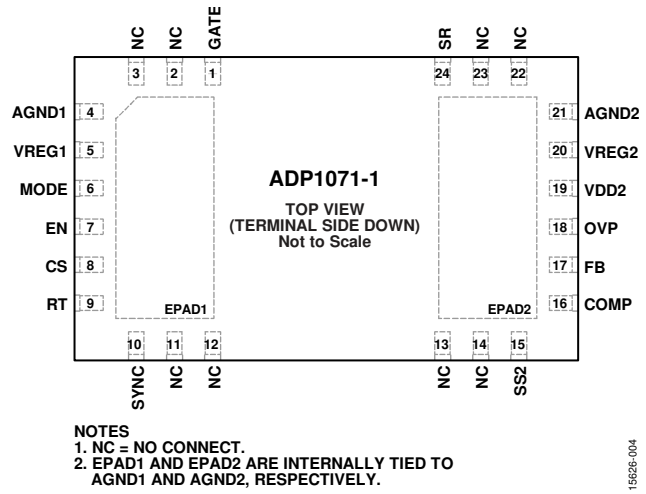

Figure 4. ADP1071-1 LGA Pin Configuration

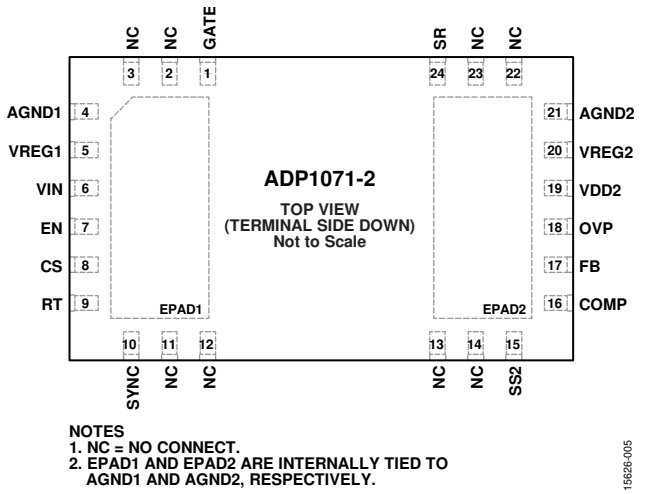

Figure 5. ADP1071-2 LGA Pin Configuration

Table 10. Pin Function Descriptions, LGA

Pin No.			
ADP1071-1	**ADP1071-2**	**Mnemonic**	**Description**
1	1	GATE	Driver Output for the Main Power MOSFET on the Primary Side. GATE is a multifunction pin. Connect a resistor from the GATE pin to AGND1 to set up the open loop soft start time.
2	2	NC	No Connect.
3	3	NC	No Connect.
4	4	AGND1	Ground for the Primary Side.
5	5	VREG1	8 V Regulated LDO Output for the MOSFET Driver. Connect 1 µF or greater from VREG1 to AGND1.
6	Not applicable	MODE	Light Load Mode Pin (ADP1071-1 Only). This pin sets the light load mode threshold. Connect the MODE pin to either AGND1 to enable forced continuous conduction mode (CCM), or to a high logic (2.5 V or higher) to force an LLM operation, or to a resistor to set up an LLM threshold voltage.
Not applicable	6	VIN	Input Voltage (ADP1071-2 Only). See the Primary Side Supply, Input Voltage, and LDO section. Connect a 4.7 µF capacitor to the VIN pin. The size of this capacitor can be reduced if the input voltage to the VIN pin is guaranteed stable. Reference the VIN pin to AGND1.
7	7	EN	Precision Enable Input. The controller is enabled when EN is above the EN threshold voltage. The EN pin also has a programmable EN hysteresis. The EN pin is referenced to AGND1.
8	8	CS	Input Current Sensing. The CS pin senses the input PWM current. Place a current sense resistor between the source terminal of the power MOSFET and AGND1.The current sense resistor sets up the input current limit. This pin is also used for the external slope compensator. Connect a resistor from the CS pin to the current sense resistor to generate a voltage ramp for the slope compensation. Reference the CS pin to AGND1. Connect a 33 pF to 100 pF capacitor at the CS pin to act as a resistor capacitor (RC) filter along with the slope compensation resistor in noisy environments.
9	9	RT	Switching Period Resistor. Connect a resistor from the RT pin to AGND1 to set the oscillator frequency.
10	10	SYNC	Frequency Synchronization. Connect an external clock to the SYNC pin to synchronize the internal oscillator to this external clock frequency. Connect the SYNC pin to AGND1 if this feature is not used. The SYNC frequency is recommended to be within 10% of the frequency set by the RT pin.
11	11	NC	No Connect.
12	12	NC	No Connect.
13	13	NC	No Connect.
14	14	NC	No Connect.
15	15	SS2	Soft Start on the Secondary Side. Connect a capacitor from SS2 to AGND2 to set up the soft start time on the secondary side.
16	16	COMP	Compensation Node on the Secondary Side. This pin is the output of the transconductance (g_m) amplifier. Reference the COMP pin to AGND2.
17	17	FB	Feedback Node on the Secondary Side. Set up the resistive divider from the output voltage such that the nominal voltage, when the power supply is in regulation, is 1.2 V. Reference the FB pin to AGND2.

18	18	OVP	Output Overvoltage Protection. The OVP threshold is set at 1.36 V. Connect a resistive divider from the OVP pin to the output and AGND2.
19	19	VDD2	Input Supply on the Secondary Side. Connect VDD2 to the output voltage of the power supply for a self driven configuration. Connect a 4.7 µF capacitor from VDD2 to AGND2. The size of this capacitor can be reduced if the input voltage to VDD2 is guaranteed to be stable.
20	20	VREG2	5 V Regulated LDO Output for Internal Bias and Powering of the Drivers of the Synchronous Rectifiers. Do not use VREG2 as a reference or load. Connect a 1 µF capacitor from VREG2 to AGND2.
21	21	AGND2	Analog Ground on Secondary Side.
22	22	NC	No Connect.
23	23	NC	No Connect.
24	24	SR	Driver Output for Synchronous Rectifier MOSFET.
		EPAD1	Exposed Pad 1. Exposed pad is internally tied to AGND1.
		EPAD2	Exposed Pad 2. Exposed pad is internally tied to AGND2.

TYPICAL PERFORMANCE CHARACTERISTICS

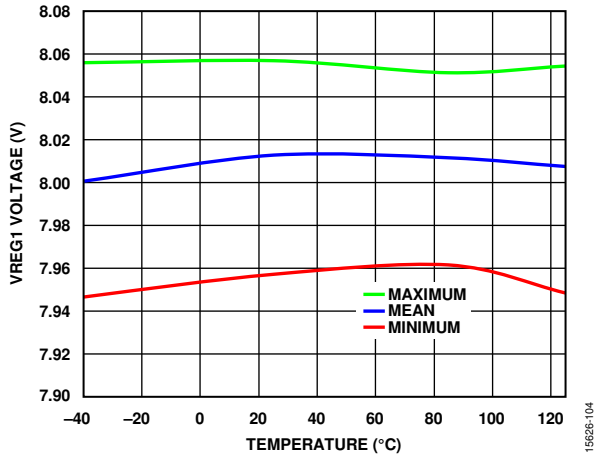

Figure 6. VREG1 Voltage vs. Temperature

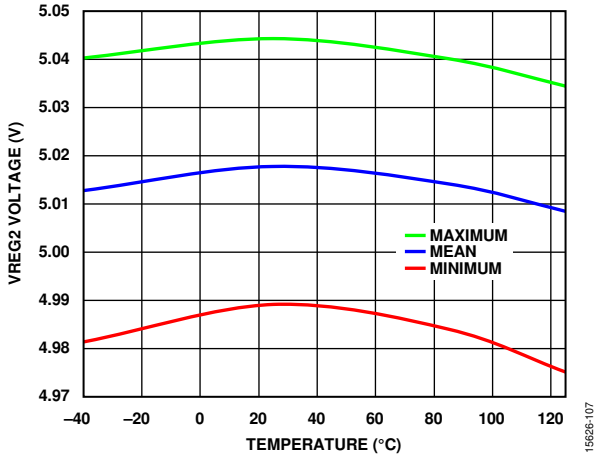

Figure 9. VREG2 Voltage vs. Temperature

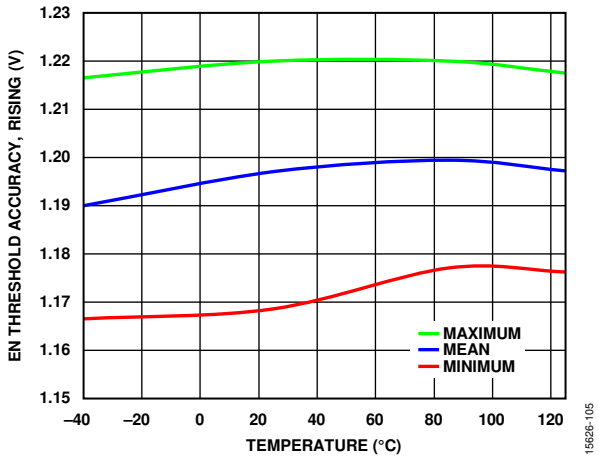

Figure 7. Rising EN Threshold Accuracy vs. Temperature

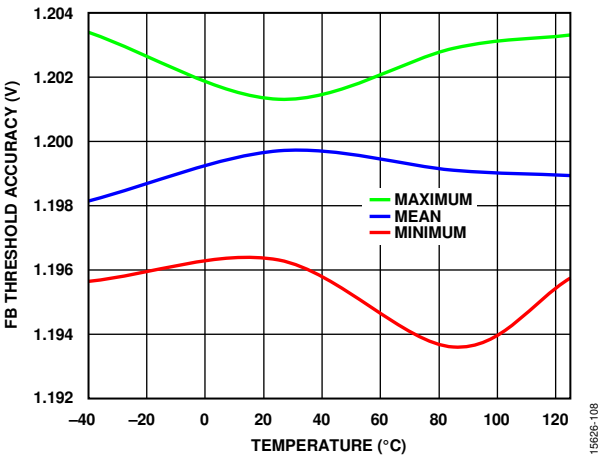

Figure 10. FB Threshold vs. Temperature

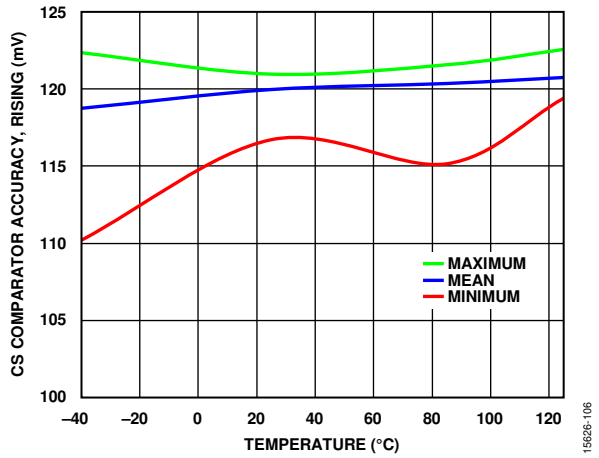

Figure 8. Rising CS Comparator Accuracy vs. Temperature

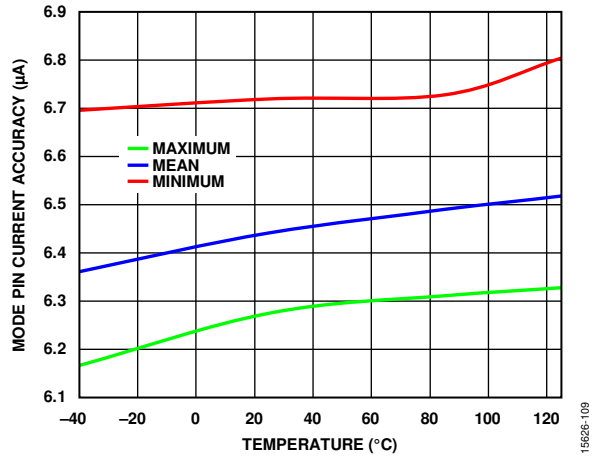

Figure 11. MODE Pin Current Source Accuracy vs. Temperature

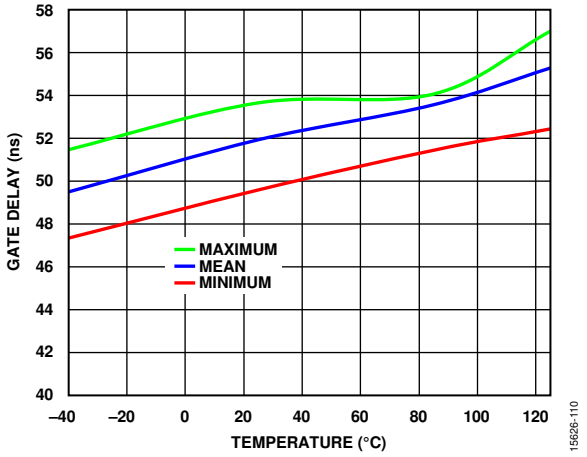

Figure 12. GATE Delay vs. Temperature (GATE Falling to SR Rising)

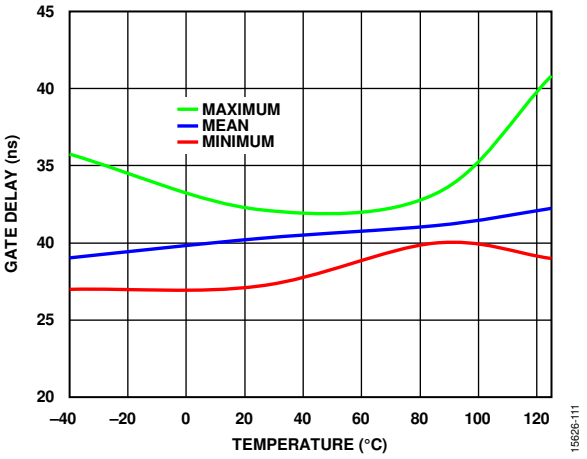

Figure 13. GATE Delay vs. Temperature (GATE Falling to SR Rising)

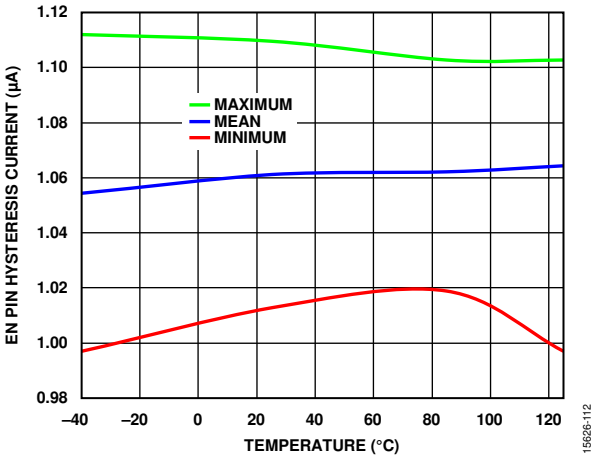

Figure 14. EN Pin Hysteresis Current vs. Temperature, EN > 1.2 V

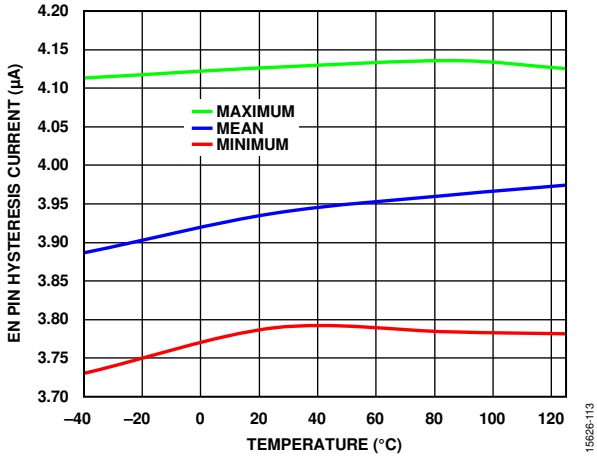

Figure 15. EN Pin Hysteresis Current vs. Temperature, EN < 1.2 V

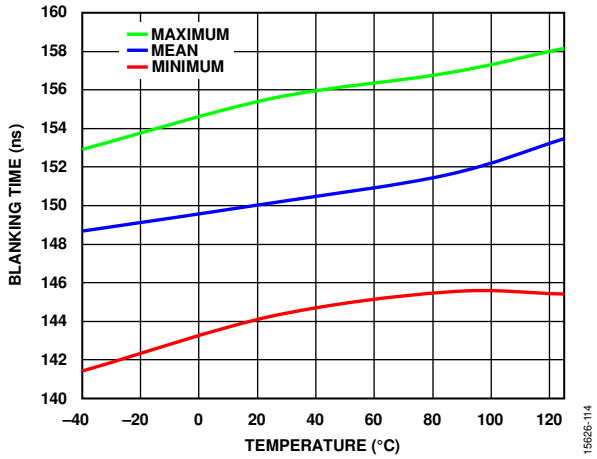

Figure 16. Blanking Time vs. Temperature

THEORY OF OPERATION

The ADP1071-1/ADP1071-2 are PWM, current mode, fixed frequency, synchronous flyback controllers designed for isolated dc-to-dc power supplies. Analog Devices *i*Couplers are integrated in the ADP1071-1/ADP1071-2 to eliminate the bulky signal transformers and optocouplers that transmit signals over the isolation boundary. Integrating the *i*Couplers reduces system design complexity, cost, and component count and improves overall system reliability. With the integrated isolators and MOSFET drivers on both the primary and the secondary side, the ADP1071-1/ADP1071-2 offer a compact system level design and yield a higher efficiency than a diode rectified flyback converter at heavy loads.

Traditionally in a forward or flyback converter, a discrete optocoupler is used in the feedback path to transmit the signal from the secondary to the primary side, and an external transformer is used for transmitting the PWM signal from the primary to the secondary side for synchronous rectification. However, the current transfer ratio (CTR) of the optocouplers degrades over time and over temperature and so the optocoupler must be replaced every 5 to 10 years, depending on the manufacturing quality and optocoupler grade that determines the initial CTR. The ADP1071-1/ADP1071-2 eliminate the use of an optocoupler and signal transformer, thus reducing system cost, PCB area, and complexity, while improving system reliability without the issue of CTR degradation of the optocouplers.

The ADP1071-1/ADP1071-2 controllers offer a complete solution for an isolated dc-to-dc power supply by integrating the 5 kV isolators and the primary and secondary control circuitries in one package.

The PWM controls are performed on the primary side by sensing the input peak current cycle by cycle with a sense resistor at the source of the main switching MOSFET. The output of the converter is sensed by the secondary circuitry, which sends the feedback and PWM signals to the primary side via the 5 kV integrated isolators for a complete control loop solution.

The primary circuitry in the ADP1071-1/ADP1071-2 includes an 8 V LDO, input current sensing, bias circuit, and MOSFET drivers including an active clamp reset driver, slope compensation, external frequency synchronization, PWM generator, and a programmable maximum duty cycle setting. The primary side also has pins for differential sensing of the current sense signal.

The secondary circuitry includes the feedback compensation, a 5 V LDO regulator, an internal reference, two MOSFET drivers for synchronous rectification, and a dedicated pin for overvoltage protection. Additionally, the secondary side features differential output voltage sensing and a programmable LLM setting.

The integrated *i*Couplers carry out the communications between the primary and secondary sides by transmitting the feedback signal and the PWMs over the isolation barrier.

The feedback signal and timing of synchronous rectifier PWMs are transmitted between the primary and the secondary sides, or between the secondary and primary sides, through the *i*Couplers using a proprietary transmission scheme.

The ADP1071-1/ADP1071-2 also offer features such as input current protection, OVP, UVLO, precision enable with adjustable hysteresis, OTP, LLM, and tracking.

DETAILED BLOCK DIAGRAM

Figure 17 shows a detailed block diagram of the ADP1071-1/ADP1071-2.

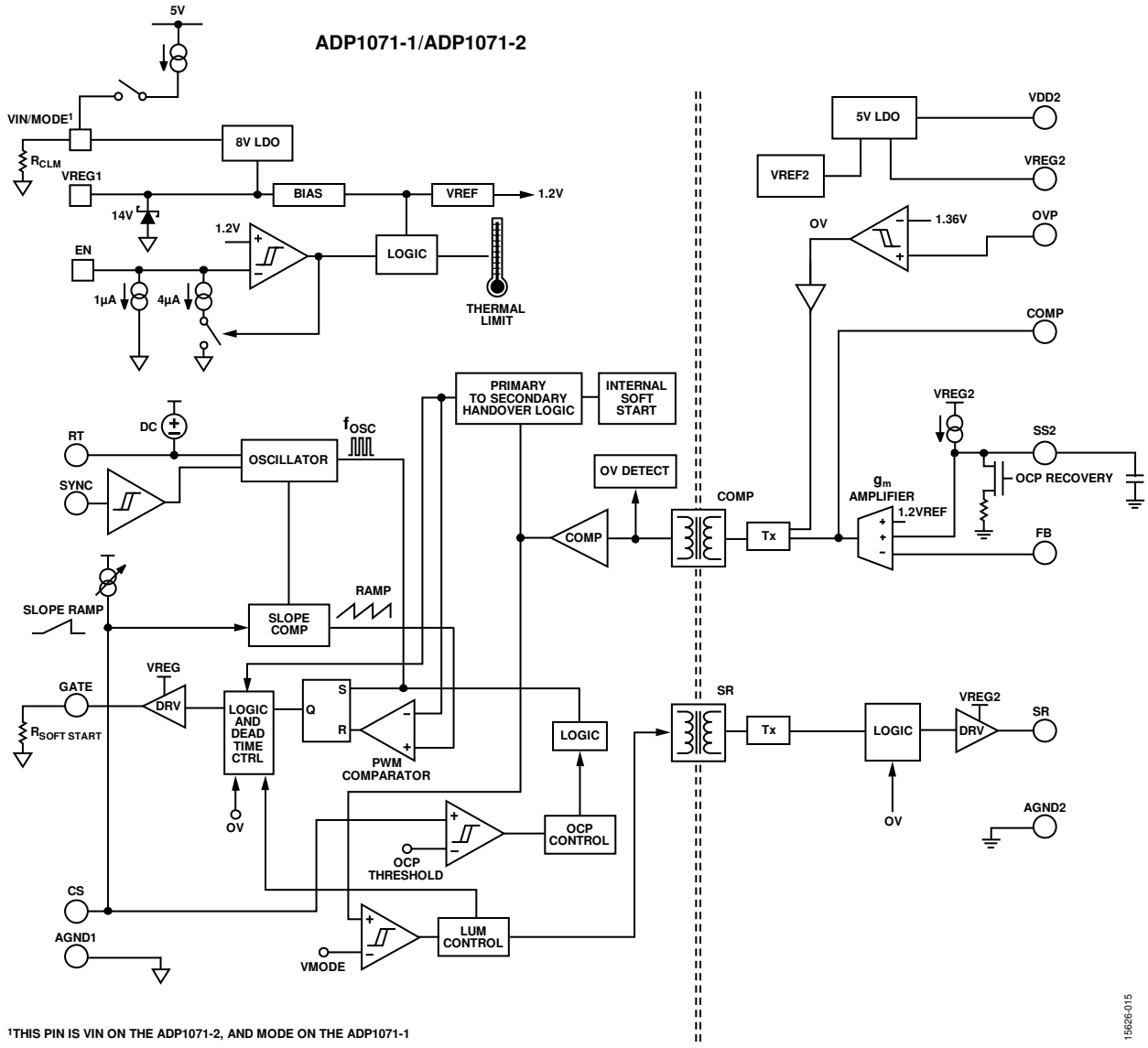

Figure 17. Detailed Block Diagram

PRIMARY SIDE SUPPLY, INPUT VOLTAGE, AND LDO

The voltage at the VREG1 pin powers the internal circuitry, primary side *i*Couplers, housekeeping circuits, and the primary MOSFET driver at the GATE pin.

In the ADP1071-1, power must be supplied to the VREG1 using an external start-up circuit.

In the ADP1071-2, a high voltage LDO regulator is connected to the VIN pin and has a regulated output of 8 V at VREG1.

In the ADP1071-2, to reduce power consumption in the LDO for input voltages higher than approximately 30 V, an auxiliary winding on the transformer of the active clamp forward topology can be used to power VREG1. This auxiliary supply voltage must be higher than the regulated output at VREG1 so that the LDO shuts off during normal operation.

In both the ADP1071-1 and ADP1071-2, the recommended auxiliary voltage is from 8.5 V to 12.5 V because an internal 14 V Zener diode is connected at VREG1.

SECONDARY SIDE SUPPLY AND LDO

Two pins on the secondary side are supply pins: VDD2 and VREG2.

The secondary side is typically powered by the output rail of the converter by connecting it to the VDD2 pin. The UVLO for the secondary side is typically 3.55 V, at which the secondary side starts up. For output voltages less than the secondary UVLO voltage, a third winding is required to generate an auxiliary voltage to power the secondary circuitry. The internal 5 V LDO regulator at the VREG2 pin powers the MOSFET drivers, secondary side *i*Couplers, and housekeeping circuits. When VDD2 is less than 5 V, the LDO regulator operates in dropout mode.

For output voltages higher than 24 V, connecting the output voltage directly to VDD2 can result in significant power dissipation in the LDO. For instance, at 24 V and with the total driver current at 10 mA, the power dissipated in the LDO is 0.19 W (10 mA × 19 V). It is recommended to power VDD2 with an auxiliary voltage in the 8 V to 12 V range.

PRECISION ENABLE

The enable threshold at the EN pin is precision voltage referenced at 1.2 V.

In the ADP1071-1, the soft start procedure commences immediately when VIN is above the UVLO voltage (typically 4.5 V) and the voltage at the EN pin rises above 1.2 V.

In the ADP1071-2, the soft start procedure commences after a small delay when VIN is above the UVLO voltage (typically 4.5 V) and the voltage at the EN pin rises above 1.2 V. This delay comprises the time taken to charge the capacitor at the VREG1 pin through the internal 8 V LDO. After the internal biasing is finished, the soft start procedure initiates.

Connect a resistive divider between EN and VIN to set up the input start-up voltage (see Figure 18). An internal current source at EN allows the user to program the UVLO start-up voltage with a desirable hysteresis. To calculate the start-up voltage with hysteresis, use the superposition theorem or nodal analysis to obtain the EN pin voltage, as follows:

$$V_{EN} = V_{IN} \times \frac{R_2}{R_1 + R_2} - I_{EN} \times (R_1 \,||\, R_2 + R_H)$$

where:
V_{EN} is the EN pin voltage.
I_{EN} is the current source at the EN pin (1 µA for turn on and 4 µA for turn off).

The user can adjust the R_1, R_2, and R_H resistors such that $V_{EN} \geq 1.2$ V and obtain the desired hysteresis.

An internal 1 µA pull-down current is always on, and the 3 µA current is active only when the V_{EN} is below the EN threshold and becomes inactive when V_{EN} is above the EN threshold.

In general, a higher input voltage requires a larger hysteresis. It is recommended to keep a capacitor on the EN pin to AGND1 to provide a low impedance path that prevents any noise, which toggles the EN pin when the input voltage hovers at the threshold.

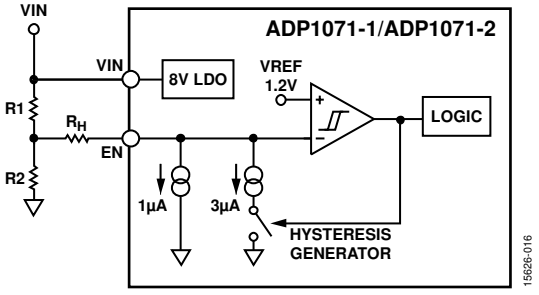

Figure 18. Precision EN with Adjustable Hysteresis

When the EN pin is less than the threshold, the system enables the soft stop procedure. SR takes up to a maximum of two switching periods to terminate. See the Soft Start Procedure section for more details.

SOFT START PROCEDURE

The following procedure assumes that the VDD2 pin is powered directly from the output voltage of the power supply.

To ensure a smooth output voltage ramp during startup, the soft start sequence is controlled by two soft start control circuits, one in the primary (for open-loop soft start using the GATE pin) and the other in the secondary (for closed-loop soft start, using the SS2 pin). Proper handshaking between the primary side and the secondary side is needed prior to the secondary side taking control.

The open-loop soft start time is determined by the resistor on the GATE pin prior to startup. The primary peak current is increased gradually every switching period. The slew rate of the increase in peak current is determined by selecting the GATE resistor prior to startup. The current increases from a minimum of 0 A to a maximum of 120 mV/R_{SENSE}. This rate is the open-loop soft start. Four speeds are available: 4 × 775, 16 × 775, 64 × 775, and 256 × 775 switching periods for resistors 100 kΩ, 10 kΩ, 22 kΩ, and 47 kΩ, respectively.

During this time, the ADP1071-1/ADP1071-2 start firing the PWM pulses and the output voltage continues to build up slowly if the average current on the secondary side exceeds the load current. Because the ADP1071-1/ADP1071-2 are current mode controllers, the output capacitor starts charging only when the primary current limit exceeds the load current requirement.

The handshaking process is as follows.

When VDD2 reaches the UVLO of approximately 3.5 V, the internal circuitry on the secondary side is activated and the ADP1071-1/ADP1071-2 initiate the following two processes:

1. The ADP1071-1/ADP1071-2 make the voltage on the SS2 pin equal to the value on the FB pin, with an SS2 pin current, at 10 times the nominal current source of 20 μA on the SS2 pin.
2. Simultaneously, the current limit on the primary side is transferred over to the secondary side and the voltage on the COMP pin is made equal to the instantaneous current limit of ±100 mV. There is a timeout for this process, which is 1.5 ms after the VDD2 UVLO threshold is crossed.

When this process is satisfied, the transmission of the COMP signal occurs from the secondary to the primary side. The ADP1071-1/ADP1071-2 transmit the COMP signal by continuously sampling the analog signal at the COMP pin. The sampled value is then transmitted using a proprietary scheme to the primary side where the instantaneous value of the CS pin is compared to the COMP level to determine the falling edge of the GATE pulse. The COMP signal is, therefore, a representation of the primary current limit.

After COMP transmission begins, the primary side receives the signal and control is completely handed over to the secondary side when either the received level of COMP on the primary side is within ±100 mV or up to 128 switching periods (typically 8) have passed, starting from the first pulse being transmitted to the primary side.

Then, after the control is handed over to the secondary side, the closed-loop soft start begins, where the SS2 capacitor is charged at a nominal rate of 20 μA. The output voltage then rises to the regulation voltage based on the SS2 pin voltage. The voltage on the SS2 pin continues to rise to 1.2 V, that is, the steady state voltage on the FB pin. At this stage, the power supply is in regulation, and the output voltage is at its target value.

At the end of the soft start process, the voltage on the SS2 pin continues to rise to approximately 1.4 V. In steady state, the FB pin (that is, the reference voltage) is 1.2 V.

The SR1 and SR2 synchronous drivers begin to pulse after VDD2 crosses the UVLO threshold.

If the voltage at the VDD2 pin is greater than the UVLO voltage, such as a soft start from the precharged output, or if the VDD2 pin is powered by an external supply, the secondary side assumes control from the moment the EN pin is enabled, and only SS2 is used for the soft start procedure.

When initiating a soft start from the precharged output, the SS2 pin tracks the FB pin and then initiates a soft start. This process eliminates any glitches in the output voltage.

When soft starting into a precharged output, the SR gate is prevented from turning on until the SS2 voltage reaches the precharged voltage at the FB pin. This soft start scheme prevents the output from being discharged, and it prevents reverse current.

Under abnormal situations, such as a shorted load or a transient condition on the load during the soft start process, FB may not be able to track SS2 accurately. If this condition occurs before the VDD2 UVLO threshold is crossed, the open loop soft start is in effect. If it occurs after the VDD2 UVLO threshold is crossed, SS2 tracks the FB pin and then continues with the soft start process until the regulation voltage is reached. In all conditions, control is handed over to the secondary side if FB ≥ 1.2 V.

When the secondary VDD2 is directly powered by the output of the converter, the minimum output voltage required is higher than the secondary UVLO voltage. For output voltages less than the secondary UVLO voltage, a third winding is needed to generate an auxiliary voltage to power the secondary side circuitry. Alternately, in most cases, a diode resistor capacitor combination from the switch node can provide the voltage to VDD2.

OUTPUT VOLTAGE SENSING AND FEEDBACK

The output voltage of the converter is set by a resistive divider to the FB pin. The resistive divider must be set in a manner such that the voltage at the FB pin is 1.2 V in steady state. The output voltage must be differentially sensed using the FB pin and the AGND2 pin.

LOOP COMPENSATION AND STEADY STATE OPERATION

The FB pin feeds into the negative terminal of a transconductance amplifier (or g_m amplifier) with a gain of approximately 250 µA/V. The positive input terminal of the g_m amplifier is connected to SS2, which provides the reference setpoint voltage. The output of the g_m amplifier is connected to the COMP pin. The voltage on the COMP pin is representative of the current peak limit required to sustain regulation. This pin is continuously sampled, and the signal is transmitted to the primary side, where it is compared to the sensed primary current using a comparator. When the comparator trips, it causes GATE to terminate.

Typically, an RC network in series is connected between the COMP pin and AGND2 for compensation. A high frequency pole in the form of a capacitor can also be added in parallel to the RC network.

The output of the g_m amplifier is clamped to a minimum and maximum current of approximately +40 µA and −65 µA, respectively.

The COMP node is clamped to a lower and higher level of approximately 0.7 V and 2.52 V, respectively. This is representative of the CS range from 0 mV to 120 mV.

SLOPE COMPENSATION

For a peak current mode controller with a duty cycle higher than 50%, slope compensation is necessary for a stable operation. To set up an external compensation in the ADP1071-1/ADP1071-2, connect the external R_{RAMP} resistor (see Figure 30) between CS and the current sense resistor, R_{SENSE}, to set up the slope voltage ramp for the control signal. It is important to sense the signal differentially. See the Layout Guidelines section for more details.

An internal ramp current starts from 0 µA at the minimum duty cycle (that is, the beginning of the switching period) and increases linearly toward a maximum of 20 µA at the end of the switching period. The slope of the voltage ramp is the ramp current times R_{RAMP}. R_{RAMP} is sized using the following equation:

$$R_{RAMP} \geq k \frac{V_{OUT}}{L} \times \frac{N_2}{N_1} \times \frac{R_{SENSE}}{20\,\mu A} \times t_S$$

where:
k = 0.5 for nominal cases and k = 1 for deadbeat control.
V_{OUT} is the desired output voltage.
L is the output inductor.
$N1$ and $N2$ are the primary and secondary turns of the transformer.
t_S is the switching period.

INPUT/OUTPUT CURRENT-LIMIT PROTECTION

There is no direct current-limit sensing circuit in the secondary side, but the output current limit is indirectly set by sensing the input primary peak current cycle by cycle. A leading edge blanking time is added after the rising edge of the GATE signal to avoid picking up any unwanted noise or ringing at the CS pin at the start of the switching period.

The input peak current limit is set by connecting a sense resistor, R_{SENSE}, from the source of the main MOSFET to AGND1, and the sensed voltage appears at the CS pin. To generate the slope-comp ramp, insert the slope compensation resistor, R_{RAMP}, between CS and R_{SENSE}.

The CS current limit, V_{CSLIM}, is internally set to 120 mV. Calculate the R_{SENSE} value by

$$R_{SENSE} = \frac{V_{CS\_LIM} - R_{RAMP} \times 20\ \mu A}{I_{PKPRI}}$$

where:
V_{CS_LIM} is the CS current limit.
I_{PKPRI} is the primary peak current.

When the sensed input peak current is above the CS limit threshold, the controller operates in the cycle by cycle constant current limit mode for 1.5 ms. Then, the controller immediately shuts down the primary and secondary drivers. The controller then enters hiccup mode for the next 40 ms and restarts the soft start sequence after this timeout period.

The slope ramp can affect the accuracy of the current-limit threshold because the voltage drop across R_{RAMP} contributes to the inaccuracy of the peak current limit. For instance, if the added slope ramp voltage is 20% of the current-limit threshold, the actual input peak current limit can be off by as much as 20% depending on where the peak current-limit threshold is tripped during the on cycle. In the event of an output short circuit, the controller treats this condition as an overcurrent event and enters the 40 ms hiccup mode.

Under certain situations, the ADP1071-1/ADP1071-2 exit OCP hiccup mode. In this condition, even though the COMP pin is at the maximum clamp level, the device does not enter hiccup mode. It is guaranteed that the PWMs are terminated whenever the CS maximum threshold is reached. The conditions under which this can occur are as follows.

Under certain conditions, the ADP1071-1/ADP1071-2 exit OCP hiccup mode. In these conditions, the COMP pin is at the maximum clamp level, but the device does not enter hiccup mode. However, it is guaranteed that the PWMs are terminated whenever the CS maximum threshold is reached. The condition under which the ADP1071-1/ADP1071-2 skip entering hiccup mode is when VDD2 is powered through an auxiliary winding, and an output short circuit occurs that results in the FB pin having a voltage that is less than 300 mV. This event is more prominent at high temperatures (>85°C) and can be exacerbated at higher temperatures.

The root cause of the device exiting hiccup mode is due to the effect that the OCP hiccup mode feature has on the SS2 pin. During OCP recovery, the SS2 pin tracks the FB pin and attempts a soft start from the precharge sequence. During this time that SS2 tracks FB, the SS2 pin voltage can be less than the FB pin voltage for a short interval, which causes the COMP pin (output of the g_m amplifier) to momentarily fall below the maximum COMP pin clamp level. This event means that the current limit required for the next few switching periods is less than the maximum threshold and puts the device out of hiccup mode because the ADP1071-1/ADP1071-2 fail to register 1.25 ms worth of consecutive overcurrent cycles and fails to enter OCP hiccup mode.

The following scenarios guarantee OCP hiccup mode based on the configuration of the VDD2 power supply:

- When VDD2 is powered directly from the output voltage, if a short circuit on the output terminals of the load occurs after steady state regulation is achieved, the VDD2 pin voltage is less than the UVLO threshold, and the device enters hiccup mode for 200 ms, similar to the hiccup time described in the Remote System Reset section.
- When VDD2 is powered through auxiliary winding or another configuration, when a short circuit occurs on the output terminals, the auxiliary winding is not shorted and maintains a positive voltage above the VDD2 UVLO threshold. To enter hiccup mode, the following circuit is recommended, as shown in Figure 19. The circuit operates as follows: when the output voltage goes low due to a short circuit, the D1 diode turns on, which pulls the base of the bipolar junction transistor (BJT) low, shutting off VDD2. The system then enters hiccup mode, as described in the Remote System Reset section.

R3 is sized to bias the Zener diode and R4 is sized such that $(V_{ZENER} - 1)/R4 > I_{ZENER}$, where V_{ZENER} is the voltage of the diode and I_{ZENER} is the biasing current of the diode. This sizing ensures that the impedance of the resistor is less than the impedance of the diode, which causes the voltage of the diode to drop, and allows VDD2 to enter UVLO.

If the output voltage is <5 V, the same procedure can be used to size the R4 resistor. If a discrete LDO is not used, a simple resistor and diode connector to the output voltage is sufficient. In this case, the R4 resistor is sized to limit the current through the D1 diode when the output voltage is 0 V during a short circuit event. Because the bandwidth of the system is high, the ADP1071-1/ADP1071-2 are able to maintain voltage regulation at the proper voltage level, even if the auxiliary winding voltage is higher than the output voltage. The soft start and soft start from precharge conditions is met with the addition of this circuit due to the bandwidth of the overall system.

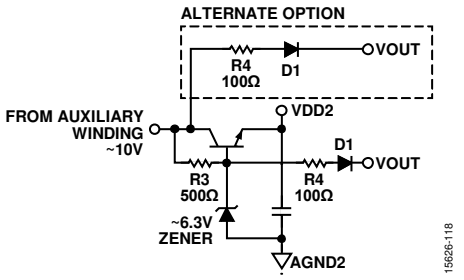

Figure 19. Recommended Circuit to Guarantee Hiccup Mode

TEMPERATURE SENSING

The ADP1071-1/ADP1071-2 have an internal temperature sensor that shuts down the controller when the internal temperature exceeds the OTP limit. At this time, the primary and secondary MOSFET drivers (GATE and SR) are held low. When the temperature drops below the OTP hysteresis level, the ADP1071-1/ADP1071-2 restart with a soft start sequence.

FREQUENCY SETTING (RT PIN)

The switching frequency can be programmed in a range of 50 kHz to 600 kHz by connecting a resistor from RT to AGND1. A small current flows out of the RT pin and the voltage across it sets up the internal oscillator frequency. The value of this pin is approximately 1.224 V in steady state. Use the following equation to determine the resistor (in Ω) for a particular switching frequency (in kHz):

$$f_S(\text{kHz}) = \frac{1}{41.67 \times 10^{-12} \times R} \times \frac{1}{1000}$$

where:
f_S is the switching frequency.
R is the resistor on the RT pin.

MAXIMUM DUTY CYCLE

To prevent the transformer core from saturating in the event of high current or extreme load transient, a maximum duty cycle clamp is internally set to 85%.

As an added protection feature to prevent open-loop conditions, the maximum duty cycle is also applicable during soft start. If the controller reaches the maximum duty cycle during soft start for three consecutive switching periods, the 40 ms hiccup timer is initiated.

FREQUENCY SYNCHRONIZATION

The switching frequency of the ADP1071-1/ADP1071-2 can be synchronized to an external clock at the SYNC pin. When an external clock rising edge is first detected, it takes approximately seven to ten periods for the internal clock to lock in the SYNC clock frequency. In between the time that the SYNC clock is detected and the time that it is locked in, the controller continues to operate with the internal oscillator frequency.

The SYNC frequency must be within ±10% of the internal oscillator frequency set by the RT pin. Otherwise, synchronization does not take place.

A clock signal can be applied to SYNC on the fly or prior to the soft start sequence. A dithered clock can also be applied to SYNC to reduce the peak electromagnetic interference (EMI) noise in the converter output and switch node. The internal clock is able to lock onto the dithered clock cycle by cycle.

It is recommended to connect the SYNC pin to AGND1 if this feature is not used.

SYNCHRONOUS RECTIFIER (SR) DRIVER

There is a synchronous rectifier driver on the secondary side for driving the synchronous switch. VDD2 is the front end of the LDO at VREG2. The 5 V internal LDO at VREG2 powers the SR drivers and all internal circuits on the secondary side. The recommended power supply range at VDD2 is from 6 V to 36 V. However, at 36 V input to VDD2, the power dissipation in the LDO can be significant. If VDD2 is less than 5 V, the LDO operates in the dropout region, where VREG2 and the driver output are less than 5 V. In this case, it is recommended to supply VDD2 with an auxiliary power supply greater than 5 V.

VDD2 can be directly connected to the converter output or an auxiliary power supply, by using a third winding of the main transformer. For additional drive strength, SR can be fed into an external MOSFET driver such as the ADP3624 or the ADP3654.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

When the output voltage exceeds the OVP threshold of 1.36 V, the controller immediately shuts off the drivers (GATE and SR) on both the primary and secondary side. When the voltage at the OVP drops below the OV hysteresis level, the controller resumes switching in the next switching period with the primary drivers, followed by the phasing in of SR. The OVP feature causes the system to enter hiccup for 200 ms if the voltage on the OVP pin exceeds 1.36 V for a sustained period of 200 µs.

SR DEAD TIME

To maximize efficiency and avoid cross conduction between the primary and secondary sides, a fixed dead time between GATE and SR is provided, as shown in Figure 20.

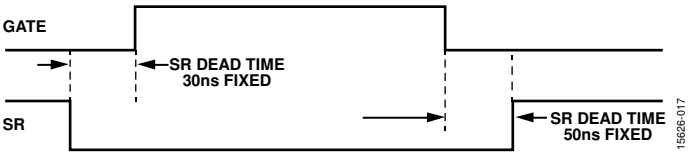

Figure 20. Gate to SR Dead Time

LIGHT LOAD MODE (LLM) AND CONTINUOUS CONDUCTION MODE (CCM)

The ADP1071-1 has a power saving mode feature in which the LLM threshold is programmable by connecting a resistor from the MODE pin to AGND1. A current source flowing through this resistor directly sets up the LLM threshold, which is compared to the COMP voltage on the primary side. The SR driver is turned off when the COMP voltage on the primary is below the LLM threshold, and conduction current continues to flow through the body diode of the SR MOSFET. However, the primary gate driver continues to operate in full PWM mode. When the COMP voltage moves above the LLM threshold, the controller operates in forced CCM.

When the COMP voltage rises above the LLM threshold (that is, the MODE pin voltage), the SR PWMs gradually increase (or phase in) from the duty cycle at light load to the steady state duty cycle at the SR phase in rate. The SR phase in rate moves the SR edges every 1.5 ns per µs. Without the phase in sequence, a dip in the output voltage can occur if the SR PWMs transition from zero to full duty cycle instantaneously.

In a load dump situation, for example, when the load is stepped from full load to light load, that is, from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) operation, the duty cycles of the SR PWMs gradually phase out at the SR phase out rate, which has the same numerical value of the SR phase in rate. The phase out sequence of the SR PWMs prevents reverse current in the secondary side, and at the same time, optimizes the dynamic performance of the output response. Note that the level of COMP is still above the minimum COMP clamp level at this point, and the ADP1071-1 outputs duty cycles with minimum on time.

If the load is further reduced and the COMP pin voltage becomes equal to the minimum COMP clamp level, the ADP1071-1 enters pulse skip mode.

Note that when the system enters light load mode, the synchronous rectifiers terminate at the falling edge of GATE, which prevents termination at a negative current.

Use the following formula to set up the LLM threshold:

$$R_{MODE} = \frac{I_{PEAK\_LLM} \times CS_{GAIN} + 0.8}{I_{MODE}}$$

where:

I_{PEAK_LLM} is the peak primary current at the particular no load condition.

CS_{GAIN} = 12.5.

I_{MODE} is the current flowing out of the MODE pin.

For full time CCM operation, connect MODE to AGND1.

The ADP1071-2 does not have an LLM and always operates in forced CCM. Pulse skipping is not available in the ADP1071-2.

SOFT STOP

The ADP1071-2 employs a soft stop feature that brings the output voltage gradually down to zero by using the SS2 pin as a reference. During the soft stop procedure, the SS2 pin is discharged to zero by a current sink of approximately 1.5 times the value during closed-loop soft start.

When the voltage at EN drops below the EN threshold, the SR secondary driver shuts off immediately, and the primary GATE pulse width gradually decreases the duty cycle from the last known condition to the minimum pulse width and down to zero, causing the output voltage to decrease. The soft stop feature prevents any reverse current when the controller is shut down.

When the output voltage decreases below the VDD2 UVLO threshold, there is no transmission of the COMP signal to the primary side. Therefore, the output voltage continues to decrease at the rate at which the load current discharges the output capacitor.

When the load is at a minimum or at no load, the output voltage does not discharge because any reduction in duty cycle or current limit does not discharge the output voltage linearly.

OCP/FEEDBACK RECOVERY

During steady state, the FB pin is at 1.2 V. At this time, the SS2 pin voltage is 1.4 V. Under abnormal situations, such as an overload condition, the output voltage can dip severely. In such an event, the current limit is at the maximum level, and the COMP pin voltage is at its clamp level. If the two conditions of the COMP pin voltage being clamped and V_{FB} < (1.2 V − 100 mV) are satisfied, the controller discharges the SS2 pin using a fast current sink (200 µA) to make the SS2 pin equal to the FB pin. The controller then attempts to perform a soft start from this precharged condition, that is, from the last known value of the output voltage. This process is how the OCP/feedback recovery feature operates.

However, if at any time the voltage on the COMP pin is above the maximum clamp voltage for a period greater than 1.5 ms, the system enters hiccup mode.

During the soft start from precharge, the output voltage rises at the same rate as determined by the capacitor on the SS2 pin. The SS2 pin voltage determines the current limit during this period. If, however, there is a detrimental fault in the power stage that prevents the rise of the output voltage, V_{FB} does not track SS2 and when SS2 > (V_{FB} + 100 mV), the COMP pin voltage increases to the clamp level and the system again enters the OCP/feedback recovery mode.

OUTPUT VOLTAGE TRACKING

The ADP1071-1/ADP1071-2 offer a tracking feature. During steady state, the FB pin is at 1.2 V. At this time, the SS2 pin voltage is at 1.4 V. Using an external digital-to-analog converter (DAC), the voltage on the SS2 pin can modulate the output voltage. It is recommended that the SS2 pin voltage be changed only after the VDD2 UVLO point is crossed, and control is handed over to the secondary side, or else the handover process does not occur smoothly, resulting in glitches in the output voltage.

The SS2 voltage must be brought down from 1.4 V to 1.2 V, and it must be brought down even further to effect any change in the output voltage. The rate at which the output tracks the SS2 pin is dependent upon the overall system bandwidth.

REMOTE SYSTEM RESET

For a remote (secondary side) system shutdown, an open-drain general-purpose input/output (GPIO) of an external microcontroller can be used to force the SS2 pin to 0 V.

This pull-down causes the ADP1071-1/ADP1071-2 to regulate to 0 V, and the ADP1071-1/ADP1071-2 enter pulse skip mode or output a minimum duty cycle because the SS2 pin offsets because of the finite resistance of the GPIO.

When the VDD2 is charged from the output bus, this setup is equivalent to a system shutdown because when VDD2 < VDD2 UVLO, the ADP1071-1/ADP1071-2 enter a special hiccup mode of 200 ms, (instead of the standard 40 ms hiccup).

When VDD2 is powered using auxiliary winding, the system regulates to the voltage proportional to the voltage on the SS2 pin and eventually enters the special hiccup mode previously mentioned, after the auxiliary rail decays below the VDD2 UVLO threshold.

Therefore, the SS2 pin can achieve output tracking as well as a secondary side shutdown, also known as remote system reset, as shown in Figure 21.

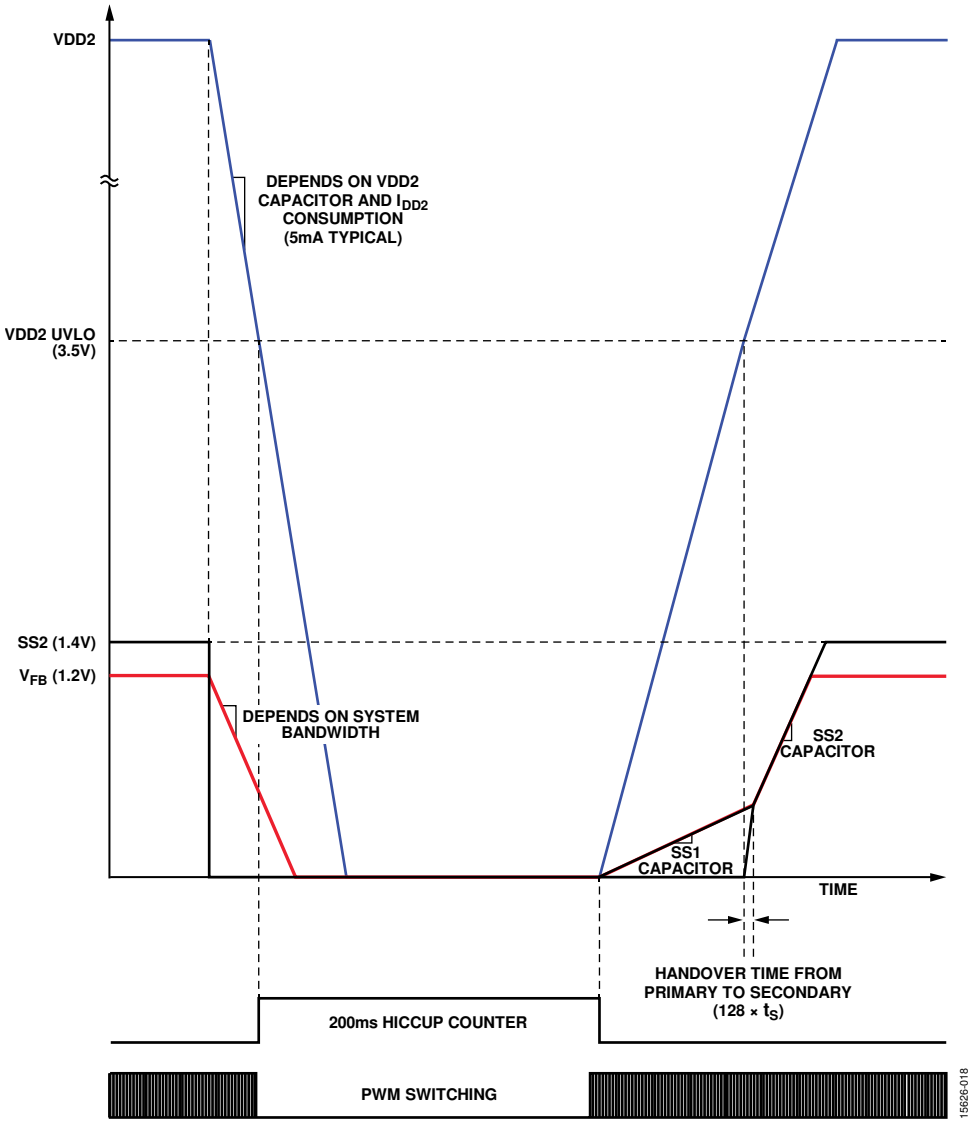

Figure 21. Remote Software Reset with 200 ms Hiccup

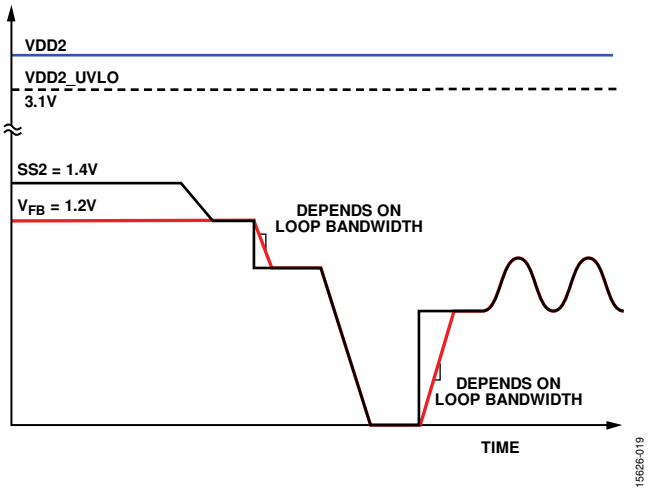

Figure 22. Tracking with SS2 Pin

OCP COUNTER

During overload conditions when the peak sensed currents exceed the OCP threshold voltage of 120 mV on the CS pin, the ADP1071-1/ADP1071-2 immediately terminate the remainder of the PWM pulse. If the peak sense current continues to exceed the threshold every switching period for 1.5 ms, the system enters hiccup mode, by which it shuts down for approximately 40 ms and then soft starts. During an exceeded overcurrent situation, such as a dead short, it is likely that the programmed slope compensation is not enough, and therefore, the system enters subharmonic oscillation. If this is the case, the system cannot enter hiccup mode because the OCP threshold is crossed every alternate switching period, and the 1.5 ms hiccup counter resets.

To prevent this scenario, the ADP1071-1/ADP1071-2 latch the last known state, whereby if an OCP condition registered as a 1 in one switching period and as a 0 in the next switching period, it is still counted as a 1. In this manner, the system can enter

hiccup mode even in subharmonic oscillation. Missing two OCP thresholds consecutively resets the hiccup counter.

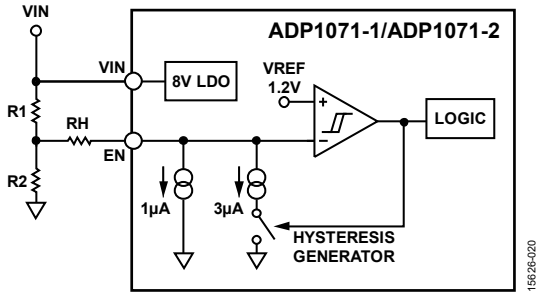

Figure 23. Precision EN with Adjustable Hysteresis

EXTERNAL START-UP CIRCUIT

For input voltages higher than 36 V, in which the power dissipation in the internal 8 V LDO can be significant, the use of an external start-up circuit is recommended. (See Figure 24 for an example.) In this case, the VIN and VREG1 pins are shorted together and connect to the output of the start-up circuit. Because the input pre-enable bias current, the VIN and VREG1 start-up current, is approximately 160 µA, the output of the start-up circuit must be able to provide this level of current in order to soft start. The auxiliary winding then provides the bias voltage, shutting off the start-up circuit after soft start completes.

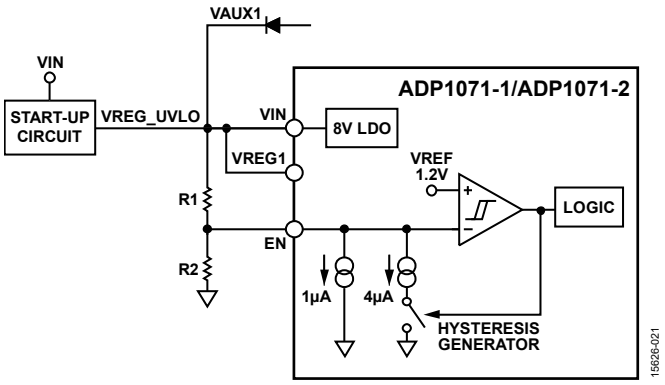

Figure 24. Precision EN Circuit Connection with an External Start-Up Circuit

A fast start-up circuit is shown in Figure 25. This circuit requires two components: a Zener diode, which sets up the start-up voltage at the VIN and VREG1 pin, and a negative positive negative (NPN) transistor, which sets up a fast current path for charging up the start-up capacitor, C1. The start-up current through R1 must be more than 160 µA, which is the minimum specified start-up current, and the start-up voltage at VREG1 and VIN must be approximately 8 V to 13 V. The auxiliary winding then provides the bias voltage, shutting off the NPN transistor after the soft start completes.

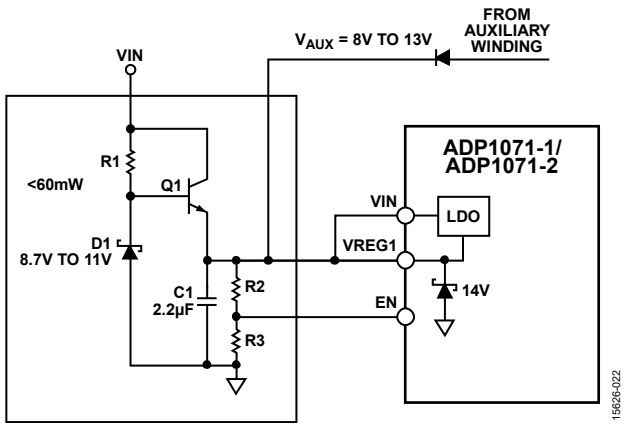

Figure 25. Fast Start-Up Circuit

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent upon the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADP1071-1/ ADP1071-2.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 7 and Table 8 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The ADP1071-1/ADP1071-2 insulation lifetime depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 26, Figure 27, and Figure 28 show these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products yet meets the 50-year operating lifetime recommended by Analog Devices for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. The low stress allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross insulation voltage waveform that does not conform to Figure 27 or Figure 28 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 7 and Table 8.

Note that the voltage presented in Figure 27 is shown as sinusoidal for illustration purposes only. It is meant to represent

any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

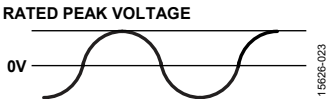

Figure 26. Bipolar AC Waveform

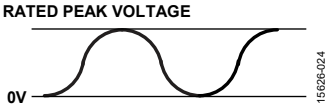

Figure 27. Unipolar AC Waveform

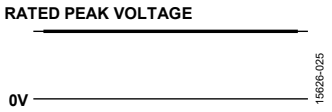

Figure 28. DC Waveform

LAYOUT GUIDELINES

The layout guidelines for the primary side are as follows:

1. Ground all the capacitors to their respective grounds. For example, ground the VREG1 capacitor to AGND1.
2. Use the CS pin and the AGND1 pin to differentially sense the primary current measurement through the sense resistor. Do not cross the CS and AGND1 traces for current sensing across any switch nodes.
3. Place a capacitor (33 pF to 470 pF typical) close to the CS pin, connected to AGND1.
4. Place resistors (1 Ω to 5 Ω typical) in series with GATE and the main power MOSFET. These resistors aid in eliminating any ringing on the drive voltages. Use a 100 nF capacitor on the MODE pin if LLM is used in noisy environments.
5. Ensure that RT pin resistor is Kelvin connected to AGND1 and not to a ground plane to avoid noise pickup.

The layout guidelines for the secondary side are as follows:

1. Ground all the capacitors to their respective grounds. For example, ground the SS2 capacitor to AGND2.
2. Place resistors (1 Ω to 5 Ω) in series with SRx and the synchronous MOSFET. These resistors aid in eliminating any ringing on the drive voltages.
3. The ground plane on the secondary side must be connected to AGND2. The negative terminal of the output voltage must be Kelvin connected to the AGND2 pin.
4. Use the FB pin and the AGND2 pin to remotely differentially sense the output voltage by connecting AGND2 to the negative terminal of the output voltage using a 0 Ω resistor.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUITS

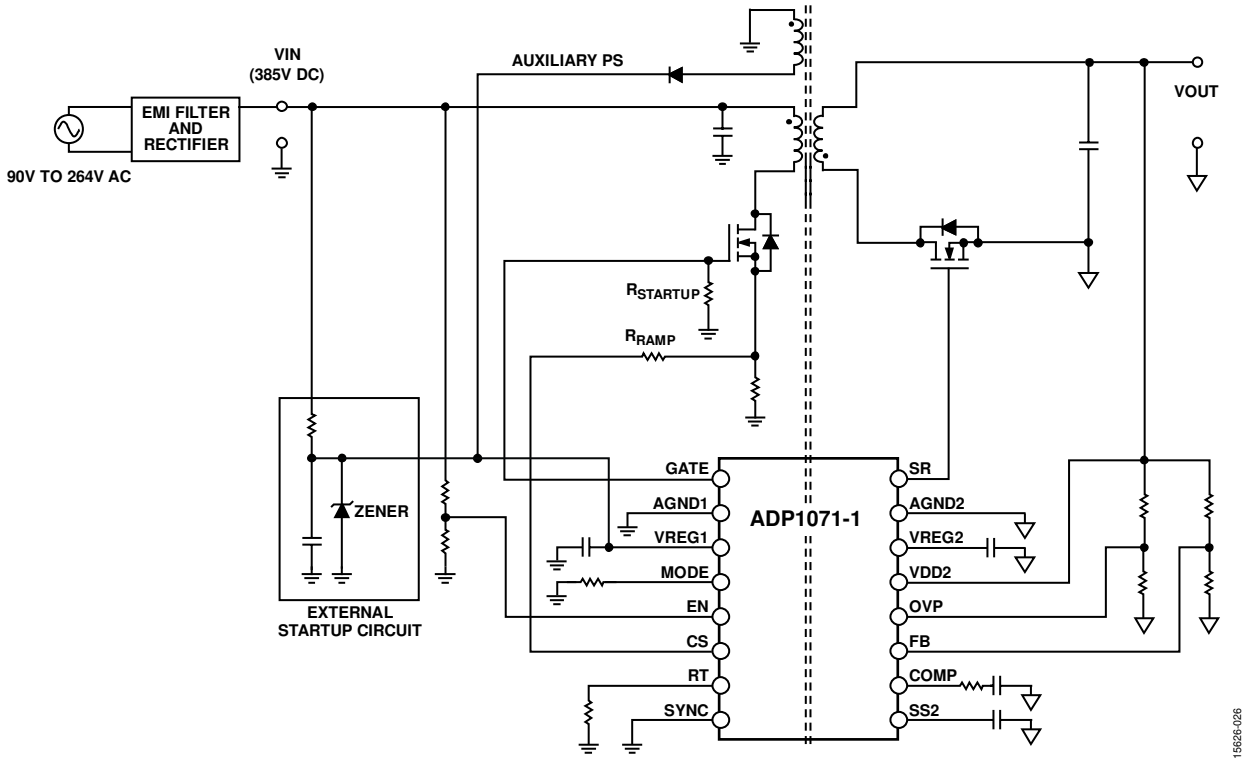

Figure 29. ADP1071-1 Typical Application with External Start-Up Circuit and Auxiliary Power

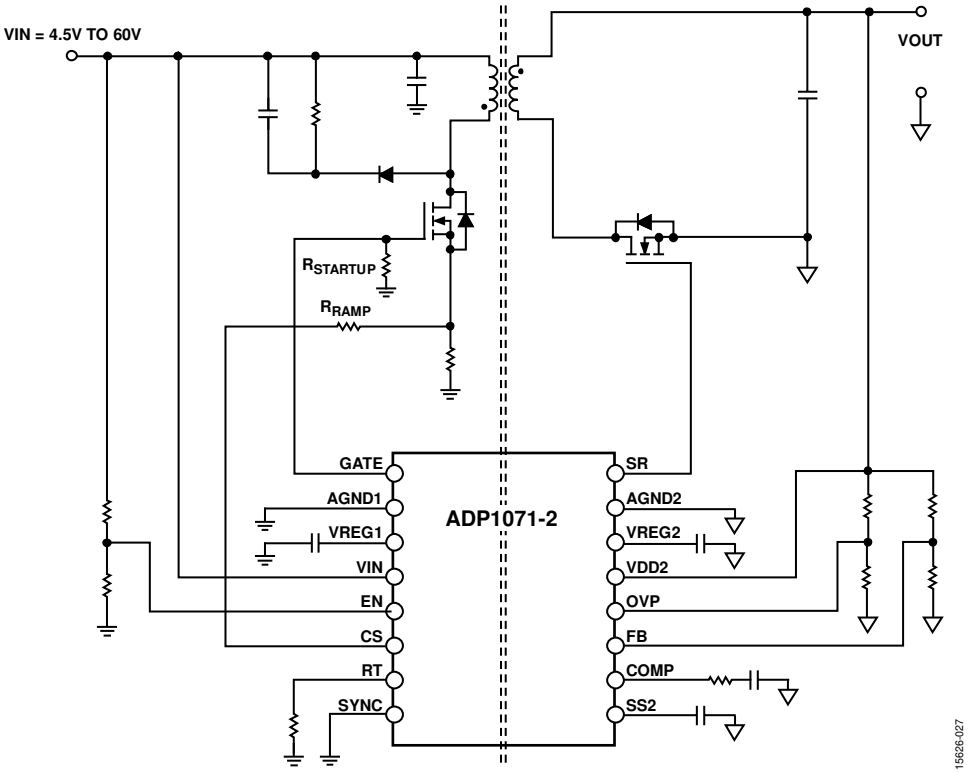

Figure 30. ADP1071-2 Low Input Voltage Flyback Application Circuit

OUTLINE DIMENSIONS

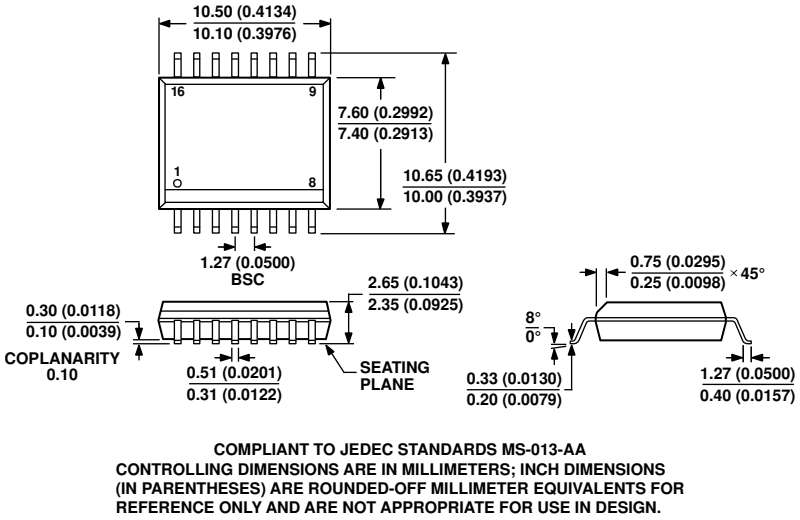

Figure 31. 16-Lead Standard Small Outline Package [SOIC_W]
Wide-Body
(RW-16)
Dimensions shown in millimeters and (inches)

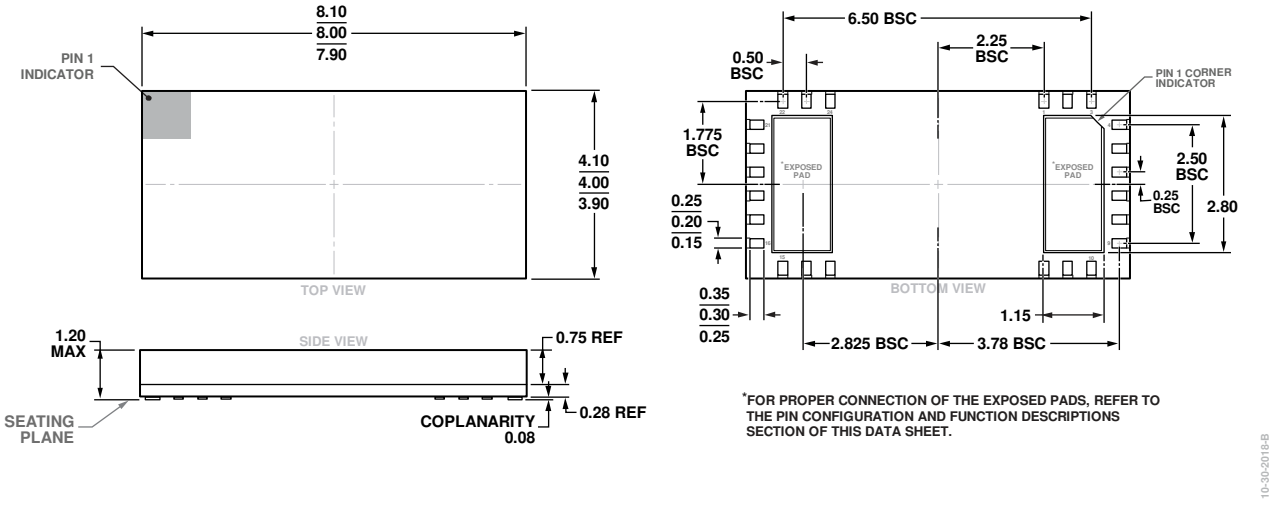

Figure 32. 24-Terminal Land Grid Array [LGA]
(CC-24-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1071-1ARWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-1ARWZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-1ARWZ-R7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-1ACCZ	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-1ACCZ-RL	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-1ACCZ-R7	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-2ARWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-2ARWZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-2ARWZ-R7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADP1071-2ACCZ	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-2ACCZ-RL	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-2ACCZ-R7	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1071-1EVALZ		ADP1071-1 Evaluation Board with Wide-Body IC	
ADP1071-2EBZ12.1V		ADP1071-2 Evaluation Board with Wide-Body IC	

[1] Z = RoHS Compliant Part.