MPQ3362

Single-String, 3V V_{IN-MIN}, 36V V_{OUT} Boost LED Driver, AEC1-Q100

DESCRIPTION

The MPQ3362 is a fixed-frequency driver, which makes it well-suited for low-current and high-current boost applications. The low 0.2V feedback voltage offers higher efficiency in white LED driver applications.

The device regulates the output voltage up to 36V with efficiency as high as 95%. Current mode regulation and external compensation components allow the MPQ3362 control loop to be optimized across a wide variety of input voltages.

The MPQ3362 supports analog dimming and PWM dimming on the same pin. A <2kHz input dimming frequency activates PWM dimming, while a >5kHz input dimming frequency activates analog dimming.

Soft start, cycle-by-cycle current limiting, and input under-voltage lockout (UVLO) protections prevent sensitive external circuitry from being damaged or overstressed during start-up or potential overload current conditions.

The MPQ3362 is available in a TSOT23-8 package.

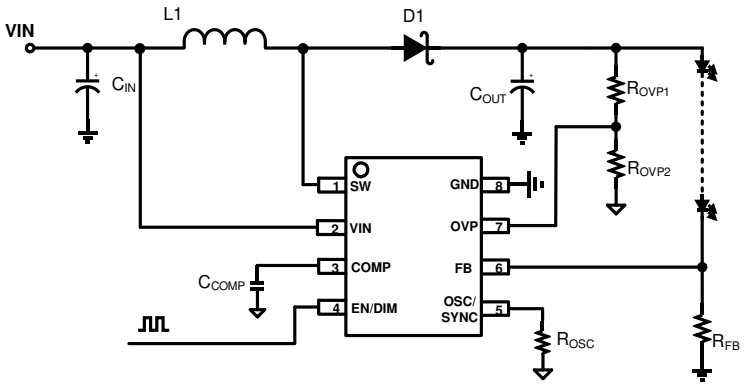
FEATURES

- 3V to 36V Input Voltage Range
- 4A Peak Current Limit
- 0.3μA Shutdown Current
- Low 200mV Feedback Voltage
- Configurable 200kHz to 2.2MHz f_{SW}
- Internal 80mΩ, 40V Power Switch
- High Efficiency
- Analog and PWM Dimming
- Under-Voltage Lockout (UVLO) Protection
- Open/Short LED Protection
- Short FB Protection
- Soft-Start Operation
- Thermal Shutdown
- Available in a TSOT23-8 Package
- AEC1-Q100

APPLICATIONS

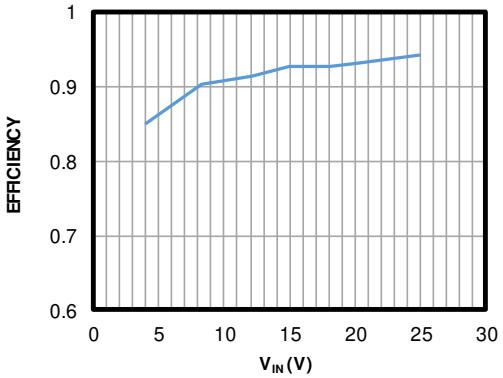
- Automotive Backlighting Displays
- Middle-Size Backlighting LCDs
- General Lighting

TYPICAL APPLICATION



Efficiency

f_{SW} = 1MHz, 10LEDs, I_{LED} = 200mA, inductor: 4.7μH/9.5mΩ



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ3362GJ-AEC1*	TSOT23-8	*See Below*	1

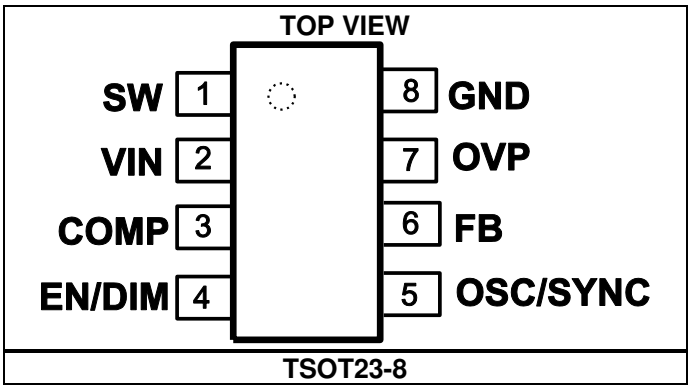
* For Tape & Reel, add suffix –Z (e.g. MPQ3362GJ-AEC1–Z).

TOP MARKING

BJFY

BJF: Product code of MPQ3362GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Output switch node.** SW is the drain of the internal N-Channel MOSFET. Connect the inductor and rectifier to the SW pin to complete the boost converter.
2	VIN	**Input supply pin.** This pin can be connected to the regulator's input supply or to the output for boot-strapped operation.
3	COMP	**Error amplifier output compensation.** The COMP pin is the error amplifier output. Connect COMP to a series RC network to compensate the regulator control loop.
4	EN/DIM	E**nable** and **dimming pin**. The EN/DIM pin is used to enable or disable the device, PWM dimming, and analog dimming. If this pin is pulled low for 20ms, the IC is disabled. If a PWM signal frequency below 2kHz is applied to this pin, the IC works in PWM dimming mode. If a PWM signal frequency exceeding 5kHz is applied to this pin, the IC works in analog dimming mode.
5	OSC/SYNC	**Switching frequency setting and synchronization pin.** Connect a resistor to the OSC/SYNC pin to configure the switching frequency (f_{SW}) between 200kHz and 2.2MHz. Apply a pulse signal between 200kHz to 2.2MHz to synchronize the switching frequency.
6	FB	**Regulation feedback input.** The regulation threshold is 0.2V.
7	OVP	**Open LED protection pin.** The OVP pin senses the output voltage to protect the IC during open LED operation.
8	GND	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{SW} .....-0.3V to +40V
All other pins .....-0.3V to +5.3V
Continuous power dissipation (T_A = 25°C) (2)
TSOT23-8 ..... 1.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±1000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 36V
Maximum LED load voltage (V_{LED})..... 36V
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4)	***θ_{JA}***	***θ_{JC}***
TSOT23-8	100	55 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may produce an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = -40 to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN shutdown supply current		V_{EN} ≤ 0V		0.3	1.5	μA
IN operating supply current	I_{Q1}	V_{EN} > 2V, V_{FB} = 0.5V		1	1.25	mA
	I_{Q2}	With switching, 400kHz			2.5	mA
IN under-voltage lockout threshold	V_{UVLO}	V_{IN} rising	2.35	2.5	2.65	V
IN under-voltage lockout hysteresis	V_{UVLO_HYS}			100		mV
EN/DIM input low voltage	V_{EN_L}				0.4	V
EN/DIM input high voltage	V_{EN_H}		1.3			V
EN/DIM input bias current	I_{EN}	V_{EN} = 5V			7	μA
EN power off time	t_{EN}	EN/DIM pulls low to disable the IC	16	20	24	ms
SW switching frequency	f_{SW}	R_{OSC} = 100kΩ	360	400	440	kHz
		R_{OSC} = 20kΩ	1650	1850	2050	
SW maximum duty cycle		V_{FB} = 0.15V, f_{SW} = 400kHz	90	93		%
Error amplifier transconductance	G_{EA}			250		μA/V
COMP maximum output current	I_{EA}	Source and sink		30		μA
FB regulation threshold	V_{FB}	100% analog dimming (25°C)	196	200	204	mV
		100% analog dimming (-40°C to +125°C)	195	200	205	mV
FB input biased current	I_{FB}	V_{FB} = 0.5V			2.5	μA
SW on resistance	R_{ON}	V_{IN} = 4V		80		mΩ
SW current limit	I_{LIM}	Duty = 80%	3.4	4	4.6	A
SW leakage current	I_{SW}	V_{SW} = 36V			1.5	μA
OVP threshold	V_{OVP}		1.1	1.18	1.26	V
OVP hysteresis	V_{OVP_HYS}			100		mV
OVP under-voltage threshold	V_{OVP_UV}			50	100	mV
Short load protection	V_{SP}	V_{FB} > V_{SP}, short load protection is triggered	540	600	660	mV
Latch-off current limit	I_{CL}			6.5		A
Thermal shutdown (5)	T_{SD}			170		°C
Thermal shutdown hysteresis	T_{SD_HYS}			20		°C

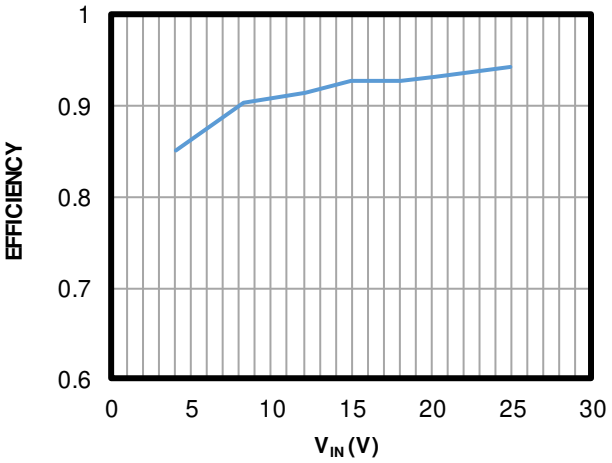
Note:

5) Not tested in production. Guaranteed by characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency

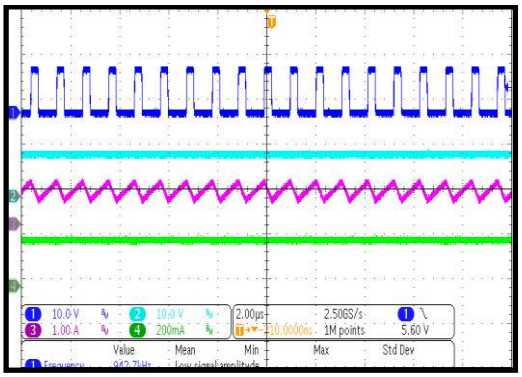
f_{SW} = 1MHz, 10LEDs, I_{LED} = 200mA,
inductor: 4.7µH/9.5mΩ



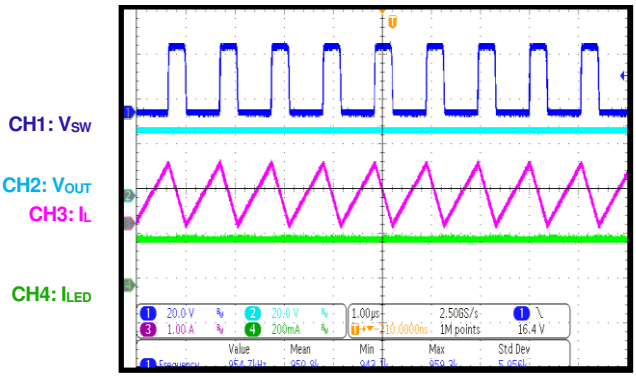
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 10V, 10LEDs, I_{LED} = 200mA, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

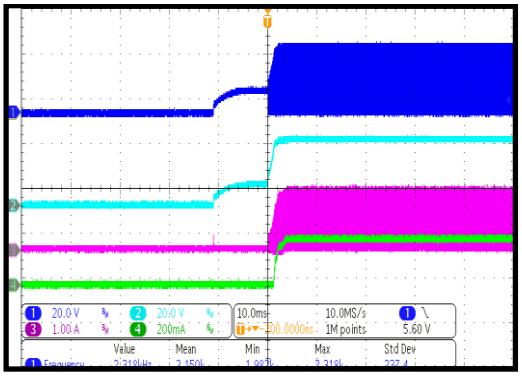
Steady State
V_{IN} = 3V, load = 3LEDs



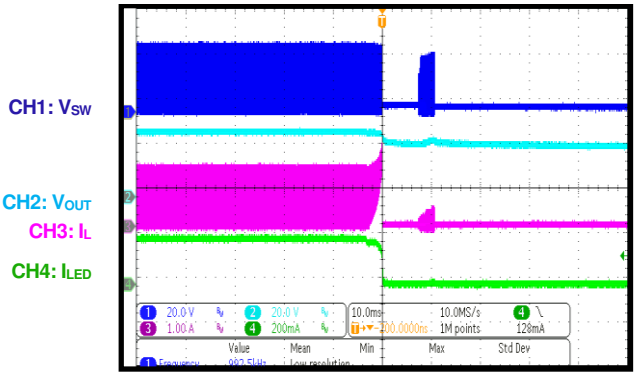
Steady State
V_{IN} = 10V, load = 10LEDs



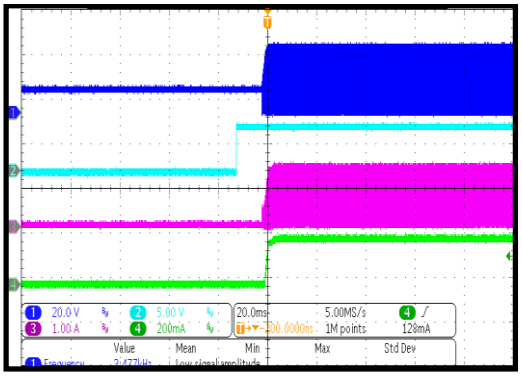
Start-Up through VIN



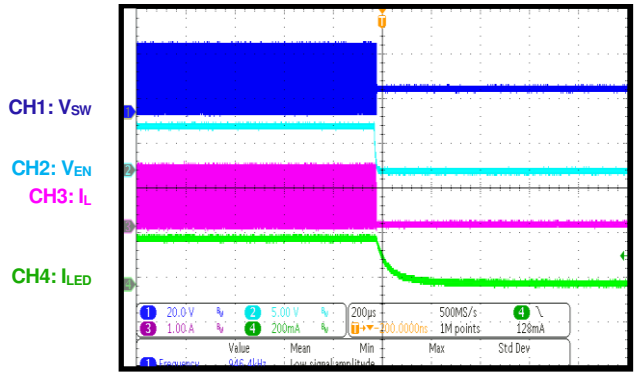
Shutdown through VIN



Start-Up through EN/DIM



Shutdown through EN/DIM

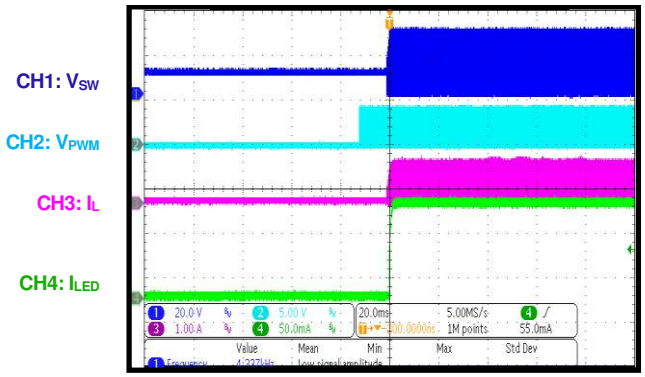


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 10V, 10LEDs, I_{LED} = 200mA, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

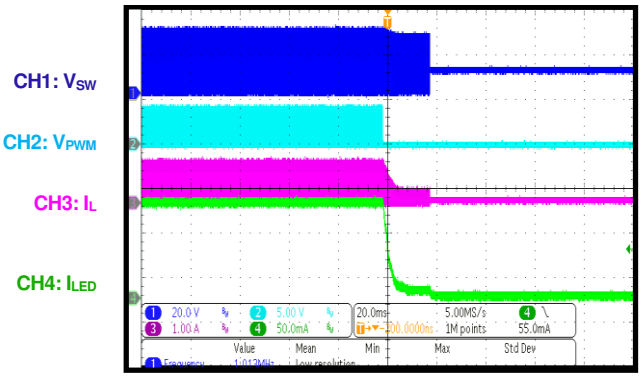
PWM On through the EN/DIM Pin

f_{PWM} = 10kHz (D = 0.5)



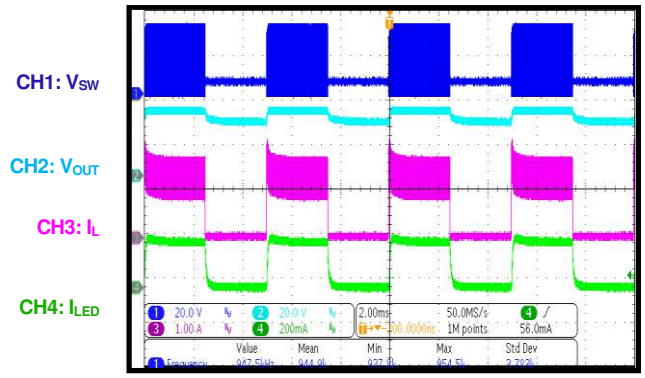
PWM Off through the EN/DIM Pin

f_{PWM} = 10kHz (D = 0.5)



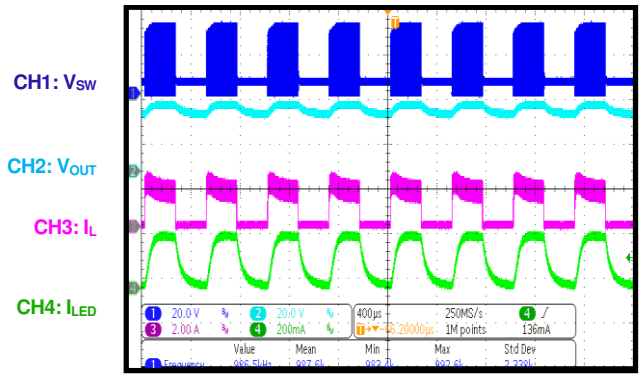
PWM Dimming

f_{PWM} = 200Hz (D = 0.5)



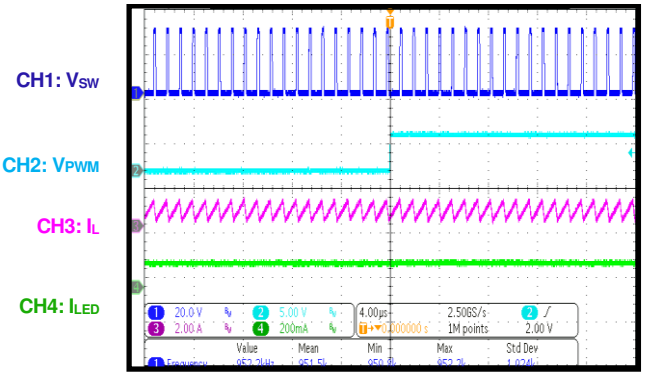
PWM Dimming

f_{PWM} = 2kHz (D = 0.5)

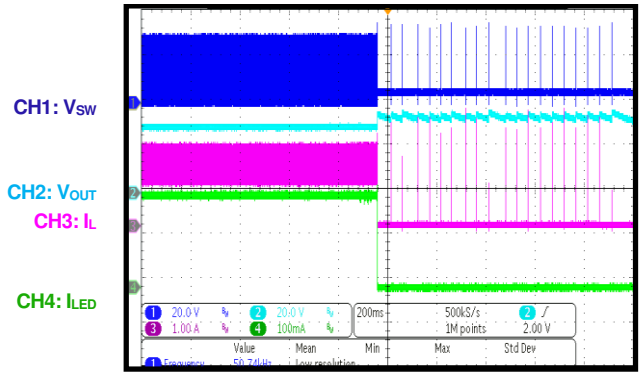


Analog Dimming

f_{PWM} = 5kHz (D = 0.5)



OVP during Normal Operation



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 10V, 10LEDs, I_{LED} = 200mA, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

Inductor Short during Normal Operation then Recovery

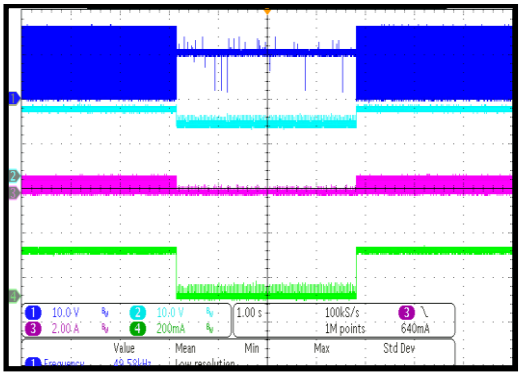
Load = 5LEDs

CH1: V_{SW}

CH2: V_{OUT}

CH3: I_L

CH4: I_{LED}



FUNCTIONAL BLOCK DIAGRAM

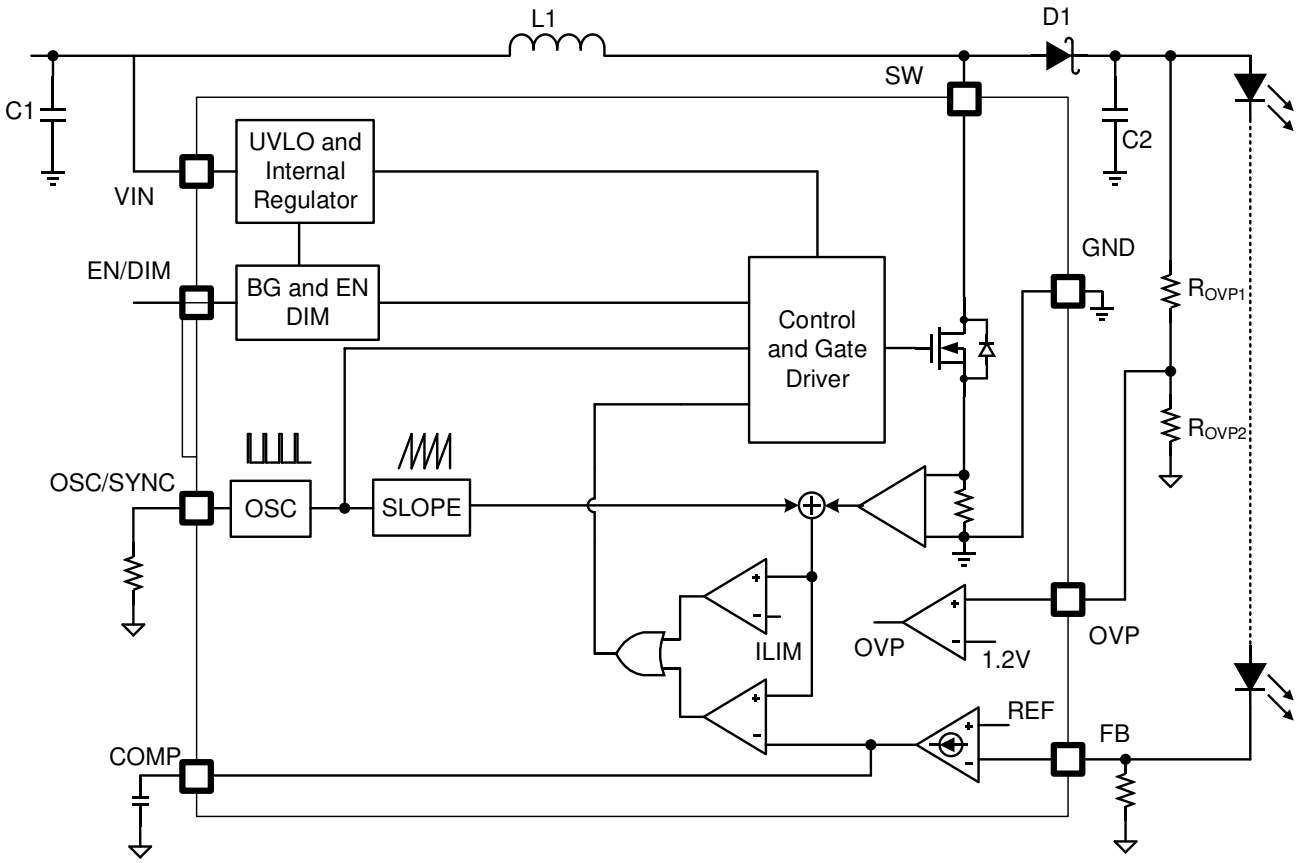


Figure1: Functional Block Diagram

OPERATION

The MPQ3362 drives an internal MOSFET with current mode architecture to regulate the LED current, which is measured through an external current-sense resistor.

The device employs a special circuit to regulate the internal power supply across a wide input voltage range. The switching frequency can be configured. The device integrates under-voltage lockout (UVLO), over-voltage protection (OVP), over-current protection (OCP), short LED protection, short FB to GND protection, short inductor and diode protection, and thermal protection.

Step-Up Converter

The MPQ3362 uses peak current mode control to regulate the output power. At the beginning of each switching cycle, the internal clock turns on the internal N-channel MOSFET. During normal operation, the minimum turn-on time is about 50ns. A stabilizing ramp is added to the output of the current-sense amplifier to prevent sub-harmonic oscillations for duty cycles exceeding 50%. This result is fed into the PWM comparator. If the summed voltage reaches the output voltage of the error amplifier, the internal MOSFET turns off. For improved stability, the turn-off time should exceed 100ns.

The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the FB voltage.

If the feedback voltage drops below the reference, the output of the error amplifier increases. This results in more current flowing through the MOSFET, which increases the power delivered to the output. This forms a closed loop that regulates the output voltage.

If V_{OUT} is almost equal to V_{IN} under light-load conditions, the converter runs in pulse-skip mode. The MOSFET turns on for a minimum on time, and then the converter discharges the power to the output for the remaining period. The internal MOSFET remains off until the output voltage requires another boost.

Soft Start

The MPQ3362 implements soft start by limiting the current capability of the internal error amplifier during start-up. The COMP voltage jumps to its clamped voltage at the beginning of start-up. The source/sink current of the internal error amplifier is limited to about 10μA until the FB voltage reaches 80% of the internal reference voltage during start-up. The maximum soft-start time is limited to 10ms. This prevents the IC from always being in soft start during deep analog dimming.

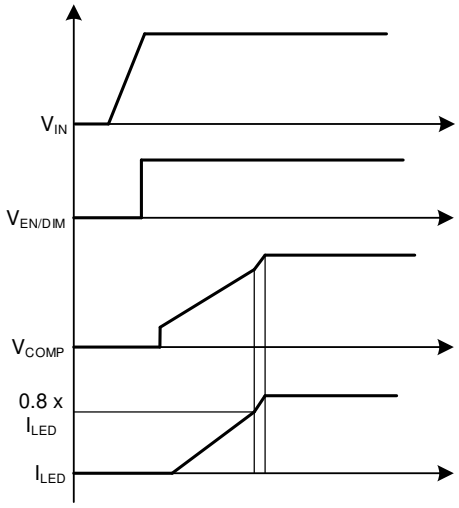


Figure 2: Soft-Start Process

Enable (EN) and Dimming (DIM)

The EN/DIM pin can be used for different functions when different signals are applied to the pin. These functions are described in greater detail below:

1. Enable/disable: If the EN/DIM is pulled high, the IC is enabled. If EN/DIM is pulled low for 20ms, the IC is disabled.
2. PWM dimming (f_{PWM} < 2kHz): If the PWM signal has a frequency below 2kHz, the IC operates in PWM dimming mode. If the PWM signal is low in PWM dimming mode, the IC stops switching, then the output voltage and output current drop. If the PWM signal is high, the IC starts switching, then the output voltage and output current rise. There is no soft start under this condition.
3. Analog dimming (f_{PWM} > 5kHz): If the PWM signal has a frequency exceeding 5kHz, the IC operates in analog dimming mode. If the input PWM signal duty changes, so do the PWM duty and LED current amplitude.

The LED current can be calculated with Equation (1):

$$I_{LED} = \frac{V_{FB}}{R_{FB}} \times Duty \quad (1)$$

Where V_{FB} is FB voltage (typically 200mV), R_{FB} is the feedback resistor, and Duty is PWM signal duty.

Protections

The MPQ3362's protections include under-voltage lockout (UVLO), over-voltage protection (OVP), short load protection, short inductor and diode over-current protection (OCP), short FB to GND protection, and thermal protection.

Under-Voltage Lockout (UVLO) Protection

The MPQ3362 integrates V_{IN} under-voltage lockout (UVLO) protection. The internal circuit does not work until V_{IN} reaches the UVLO rising threshold.

Over-Voltage Protection (OVP)

Over-voltage (OV) conditions are detected by the voltage on the OVP pin. When the OVP pin's voltage rises to its high threshold, over-voltage protection is triggered, and the IC stops switching. The IC tries to recover when the OVP voltage drops to its low threshold.

Short Load Protection

If a short load condition occurs, a large short current is detected by the FB-sense resistor. If the sensed voltage exceeds 600mV for 20 switching cycles, short load protection is triggered, and the IC stops switching. The IC resumes normal operation when the short condition disappears.

High voltage appears on the FB pin under short load conditions. Additional protection components are required to protect FB from damage (see Figure 3).

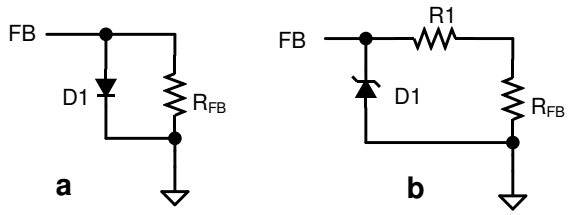


Figure 3: Short Load Protection on the FB Pin

Note that there is a short loop from the input to GND under short load conditions. A fuse or other external circuit should be used to cut off the short loop.

OVP Pin Under Voltage Protection (UVP)

If the OVP pin's voltage drops below 60mV for 10µs during normal operation, the IC stops switching, and under-voltage protection (UVP) is triggered. This protection is blanked during soft start.

Over-Current Protection (Short Inductor/ Diode Protection)

The MPQ3362 implements cycle-by-cycle current limiting for protection. If an inductor or diode short occurs, and the MOSFET's current exceeds the latch-off current limit value (typically 6.5A) for 7 consecutive cycles, over-current protection (OCP) is triggered. The IC stops switching, then resumes normal operation when the short is removed.

Short FB to GND Protection

If the FB voltage drops below 50mV, and COMP saturation lasts for 20ms, the IC stops switching. The IC resumes normal operation when the short is removed.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds the upper threshold (about 170°C), the COMP is pulled to low. It resumes normal operation when the die temperature drops below the lower threshold. (the hysteresis is about 20°C).

APPLICATION INFORMATION

LED Current Setting

The LED current is set by the LED current feedback resistor (R_{FB}). R_{FB} can be estimated with Equation (2):

$$R_{FB} = \frac{200mV}{I_{LED}} \quad (2)$$

Switching Frequency Setting

The switching frequency (f_{SW}) is set by an external resistor (R_{OSC}) at the OSC/SYNC pin. f_{SW} can be calculated with Equation (3):

$$f_{SW}(kHz) = \frac{40000}{R_{OSC}(k\Omega)} \quad (3)$$

Applying a PWM signal between 200kHz and 2.2MHz on the OSC/SYNC pin can also synchronize f_{SW}.

Selecting the Inductor

Select the inductor to make the circuit work in continuous conduction mode (CCM). The inductance can be calculated with Equation (4):

$$L = \frac{V_{IN} \times (V_O - V_{IN})}{V_O \times \Delta I_L \times f_{sw}} \quad (4)$$

Where ΔI_L is the peak-to-peak current of the inductor. Design ΔI_L to be approximately 30% to 60% of the inductor's average current. The average current can be estimated with Equation (5):

$$I_{L\_AVG} = \frac{V_O \times I_{LED}}{V_{IN}} \quad (5)$$

Ensure that the inductor's saturated current exceeds the inductor's peak current. The peak current can be estimated with Equation (6):

$$I_{L\_PK} = I_{L\_AVG} + \frac{1}{2}\Delta I_L \quad (6)$$

Over-Voltage Protection (OVP) Setting

Generally, set the over-voltage protection (OVP) threshold to be 10% to 20% higher than the output voltage. To set the OVP threshold, see Figure 5 on page 14. The OVP threshold can be calculated with Equation (7):

$$V_{OVP}(V) = \frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \times 1.2(V) \quad (7)$$

Selecting the Diode

Choose the diode with a voltage rating that exceeds the OVP point. Generally, leave about 20% for the margin. The current rating is about 2 to 3 times greater than the LED current.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply, as well as switching noise from the device. Use a low-ESR ceramic capacitor with X7R dielectrics and small temperature coefficients.

Select an input capacitor (C_{IN}) that limits the input voltage ripple (ΔV_{IN}) to less than 5% to 10% of its DC value. C_{IN} can be calculated with Equation (8):

$$C_{IN} \geq \frac{\Delta I_L}{8 \times \Delta V_{IN} \times f_{SW}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) should limit the output voltage ripple (ΔV_O) to be below 1% to 5% of its DC value while ensuring feedback loop stability. C_{OUT} can be estimated with Equation (9):

$$C_{OUT} \geq \frac{I_{LED} \times (V_O - V_{IN})}{\Delta V_O \times f_{sw} \times V_O} \quad (9)$$

Compensation Network Setting

The MPQ3362 implements peak current mode control to regulate the LED current through a compensation network on the COMP pin. An RCC network is used for most applications (see Figure 4)

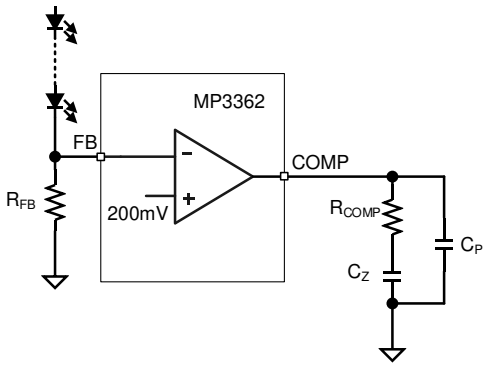


Figure 4: Compensation Network

Assuming C_Z exceeds C_P, the error amplifier (EA) can be calculated with Equation (10):

$$EA(s) \approx \frac{G_{EA} \times R_{FB}}{R_{FB}+R_{LED\_AC}} \times \frac{1}{s \times C_Z} \times \frac{1+s \times C_Z \times R_{COMP}}{1+s \times C_P \times R_{COMP}} \quad (10)$$

Where G_{EA} is the transconductance of the internal error amplifier (about 350μA/V), and R_{LED_AC} is the dynamic resistor of LED load, which can be estimated with Equation (11):

$$R_{LED\_AC}=\frac{\Delta V_{LED}}{\Delta I_{LED}} \quad (11)$$

The zero of this compensation network can be calculated with Equation (12):

$$f_{Z\_EA}=\frac{1}{2\pi \times C_Z \times R_{COMP}} \quad (12)$$

The pole of this compensation network can be estimated with Equation (13):

$$f_{P\_EA}=\frac{1}{2\pi \times C_P \times R_{COMP}} \quad (13)$$

The power stage of the boost converter can be calculated with Equation (14):

$$f_{P\_PS}=\frac{1}{2\pi \times (\frac{V_O}{I_{LED}} // (R_{LED\_AC}+R_{FB})) \times C_{OUT}} \quad (14)$$

Where V_O is the output voltage, I_{LED} is the LED current, and C_{OUT} is the output capacitance.

The right-half plane (RHP) zero of the boost converter stage can be estimated with Equation (15):

$$f_{RHP\_Z}=\frac{(1-D)^2 \times \frac{V_O}{I_{LED}}}{2\pi \times L} \quad (15)$$

Choose the cross frequency (f_C) to be below 33% of f_{RHP_Z}. Then R_{COMP} can be calculated with Equation (16):

$$R_{COMP}=\frac{R_{LED\_AC}+R_{FB}}{R_{FB}} \frac{f_c \times C_{OUT} \times 2\pi}{G_{EA} \times (1-D) \times G_{CS}} \quad (16)$$

Where G_{CS} is conductance of the internal current-sense circuit.

The zero of the compensation network (C_Z) compensates for the power stage pole. C_Z can be estimated with Equation (17):

$$C_Z=\frac{1}{2\pi \times f_{PS\_P} \times R_{COMP}} \quad (17)$$

The pole of the compensation network (C_P) compensates for the RHP zero. C_P can be calculated with Equation (18):

$$C_P=\frac{1}{2\pi \times f_{RHP\_Z} \times R_{COMP}} \quad (18)$$

TYPICAL APPLICATION CIRCUIT

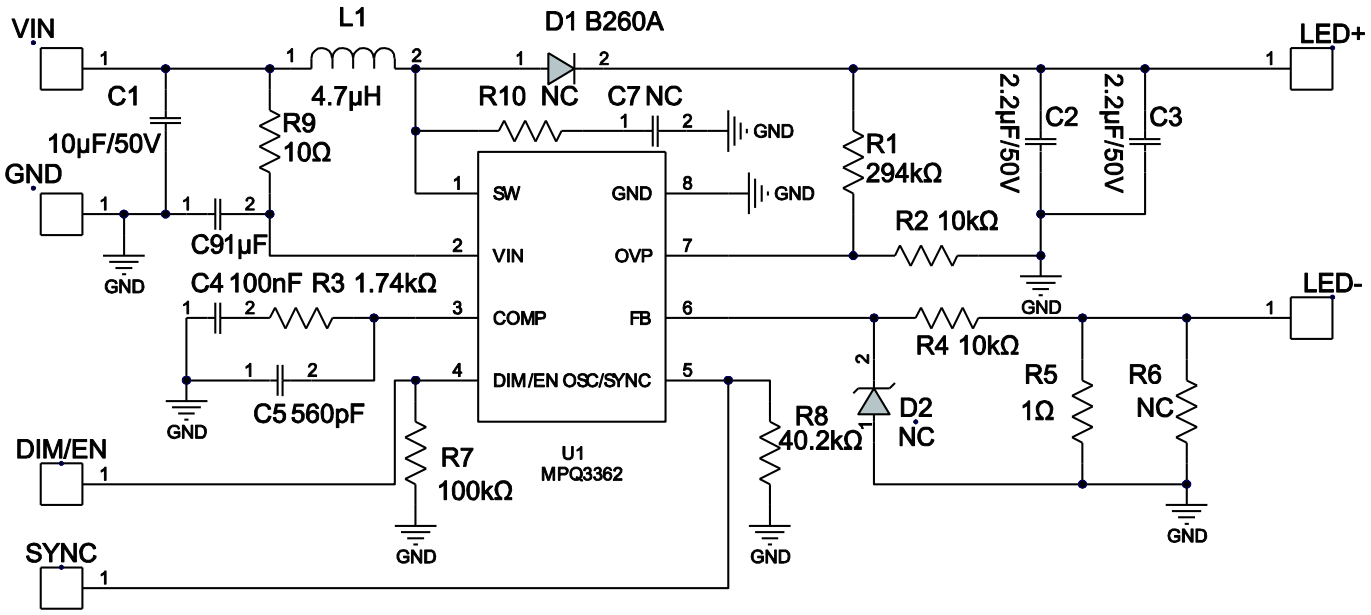
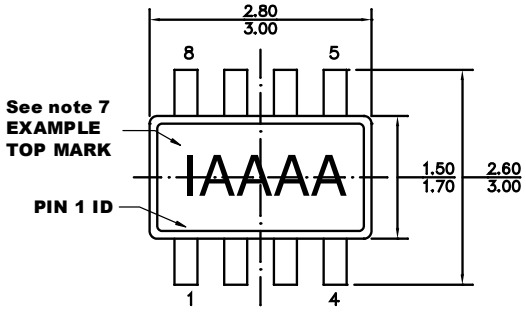


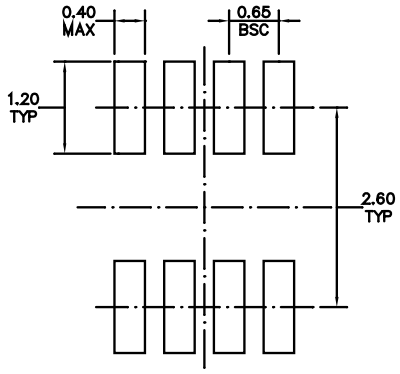
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

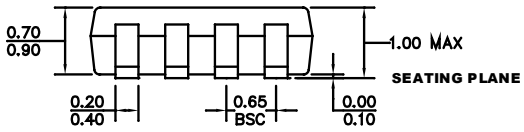
TSOT23-8



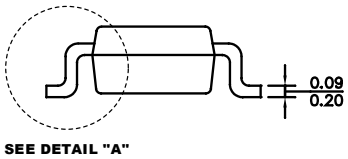
TOP VIEW



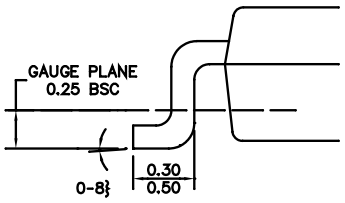
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

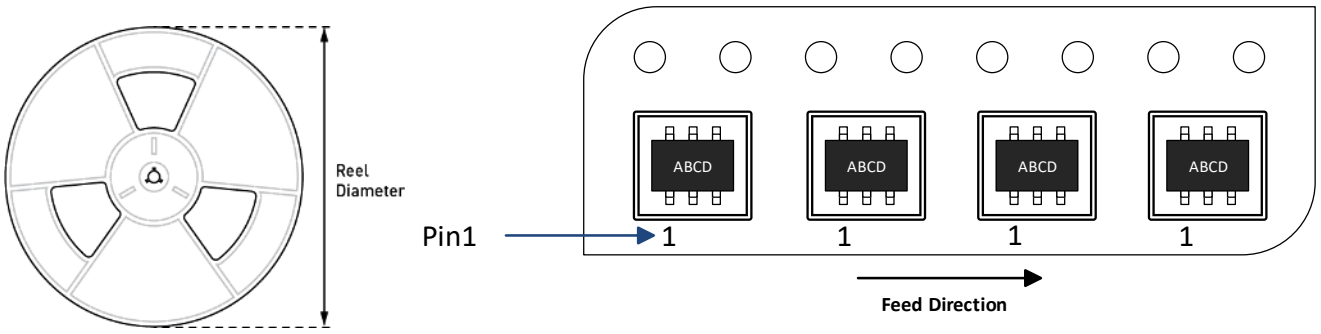


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3362GJ-AEC1-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/21/2020	Initial Release	-