

# μPA2821T1L

R07DS0753EJ0100

Rev.1.00

## MOS FIELD EFFECT TRANSISTOR

May 25, 2012

### Description

The μPA2821T1L is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer and Lithium-Ion battery protection circuit.

### Features

- $V_{DSS} = 30\text{ V}$  ( $T_A = 25^\circ\text{C}$ )
- Low on-state resistance  
—  $R_{DS(on)} = 3.8\text{ m}\Omega$  MAX. ( $V_{GS} = 10\text{ V}$ ,  $I_D = 26\text{ A}$ )
- 4.5 V Gate-drive available
- Small surface mount package (8-pin HVSON (3333))
- Pb-free, Halogen Free

### Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2821T1L-E1-AT *1	Pure Sn (Tin)	Tape 3000 p/reel	8-pin HVSON (3333) typ. 0.028 g
μPA2821T1L-E2-AT *1			

Note: \*1. Pb-free (This product does not contain Pb in external electrode and other parts.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0\text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0\text{ V}$ )	$V_{GSS}$	±20	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	±26	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±104	A
Total Power Dissipation *2	$P_{T1}$	1.5	W
Total Power Dissipation (PW = 10 sec) *2	$P_{T2}$	3.8	W
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T3}$	52	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current *3	$I_{AS}$	18	A
Signal Avalanche Energy *3	$E_{AS}$	32.4	mJ

### Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	2.4	°C/W

Notes: \*1.  $PW \leq 10\ \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

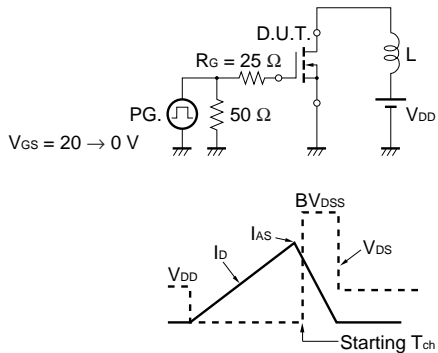
\*3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{ V}$ ,  $R_G = 25\ \Omega$ ,  $V_{GS} = 20 \rightarrow 0\text{ V}$ ,  $L = 100\ \mu\text{H}$

**Electrical Characteristics (T<sub>A</sub> = 25°C)**

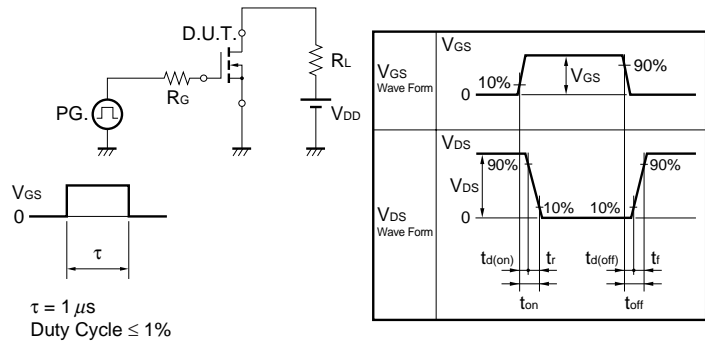
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V
Gate Cut-off Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance *1	y <sub>fs</sub>	14			S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 6.5 A
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>		3.0	3.8	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 26 A
	R <sub>DS(on)2</sub>		4.9	10.5	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.5 A
Input Capacitance	C <sub>iss</sub>		2490		pF	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		820		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		740		pF	
Turn-on Delay Time	t <sub>d(on)</sub>		29		ns	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 13 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 10 Ω
Rise Time	t <sub>r</sub>		69		ns	
Turn-off Delay Time	t <sub>d(off)</sub>		98		ns	
Fall Time	t <sub>f</sub>		54		ns	
Total Gate Charge	Q <sub>G</sub>		51		nC	V <sub>GS</sub> = 10 V,
			32		nC	V <sub>GS</sub> = 5 V
Gate to Source Charge	Q <sub>GS</sub>		4		nC	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 26 A
Gate to Drain Charge	Q <sub>GD</sub>		22		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9		V	I <sub>F</sub> = 26 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		49		ns	I <sub>F</sub> = 26 A, V <sub>GS</sub> = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		41		nC	

Note: \*1. Pulsed

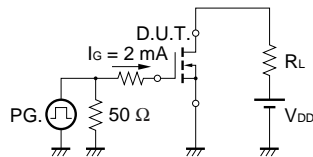
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

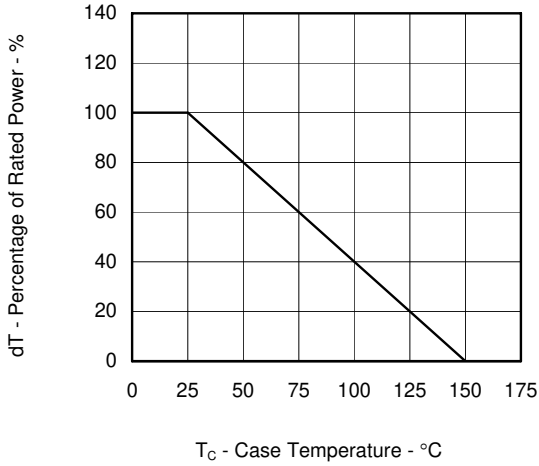


**TEST CIRCUIT 3 GATE CHARGE**

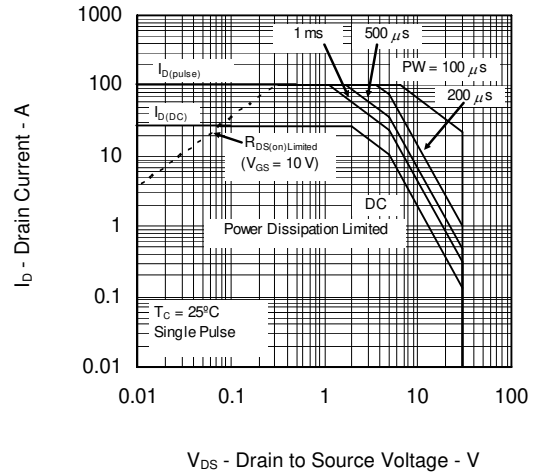


Typical Characteristics (T<sub>A</sub> = 25°C)

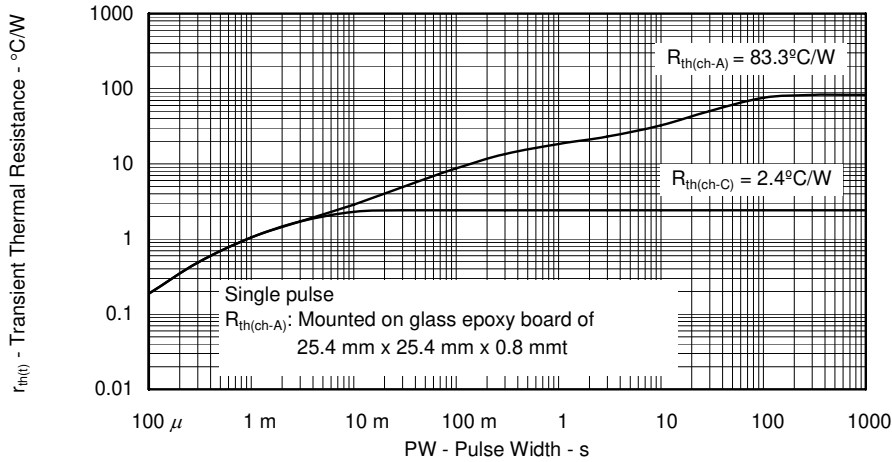
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



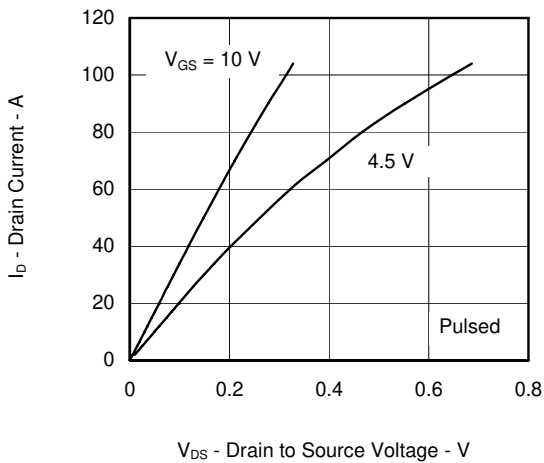
FORWARD BIAS SAFE OPERATING AREA



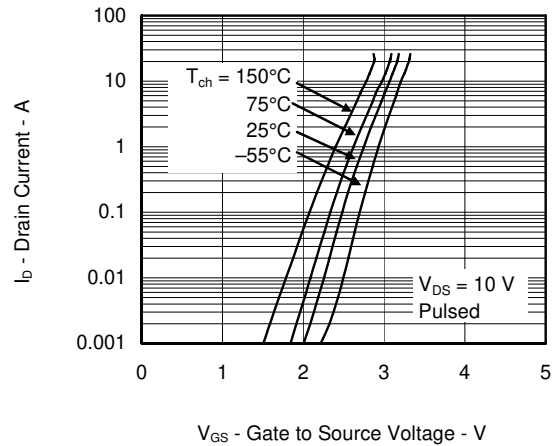
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



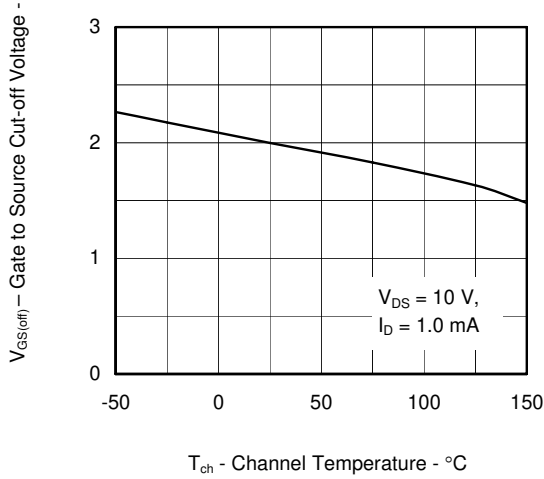
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



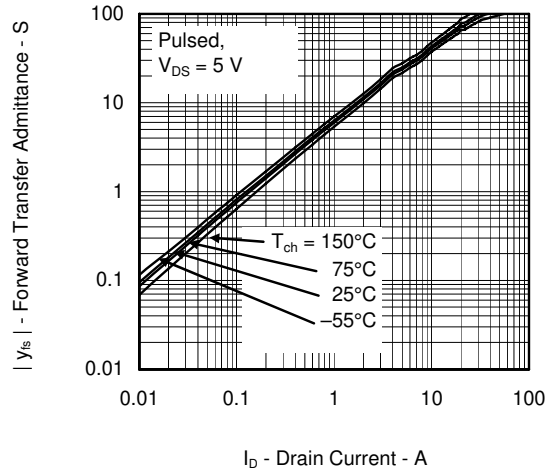
FORWARD TRANSFER CHARACTERISTICS



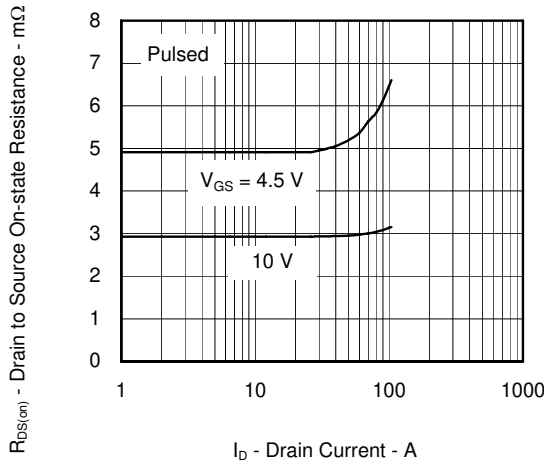
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



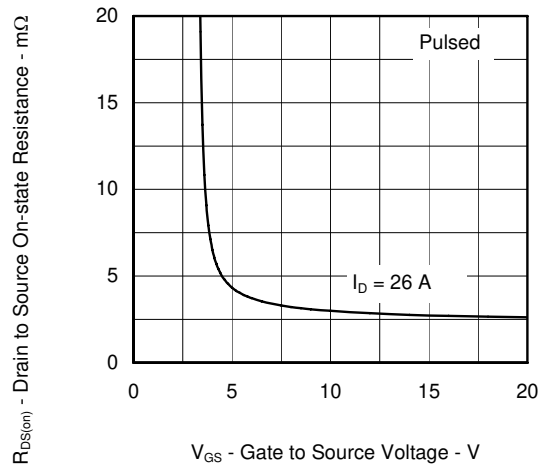
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



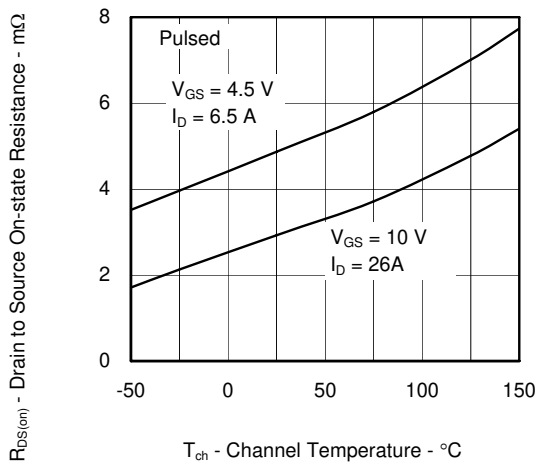
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



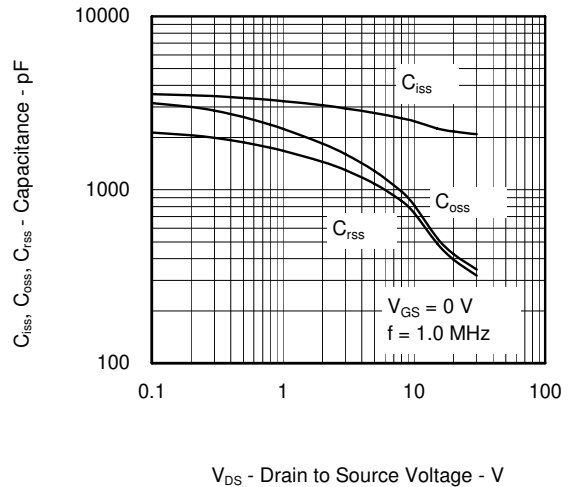
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



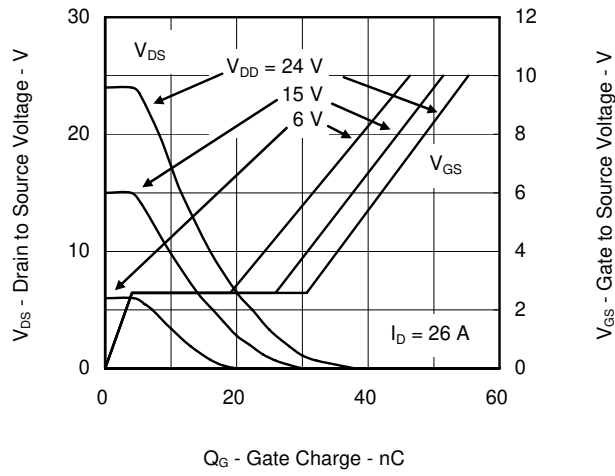
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



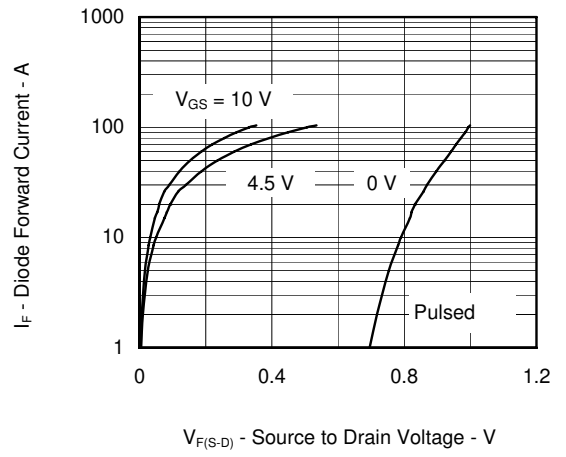
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

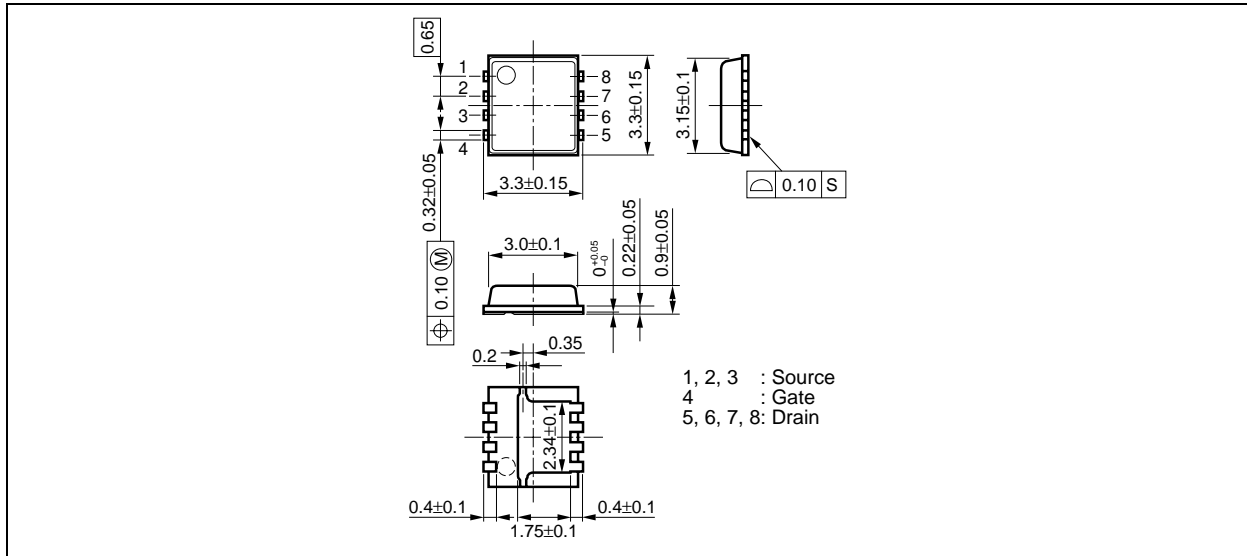


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

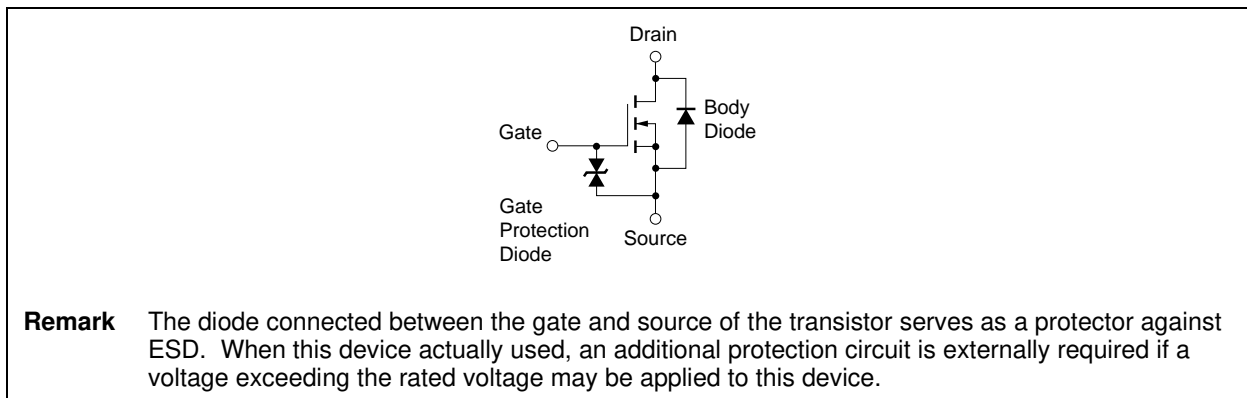


## Package Drawings (Unit: mm)

### 8-pin HVSON (3333)



## Equivalent Circuit



<b>Revision History</b>	<b>μPA2821T1L Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	-	First Edition Issued

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