CGD15HB62LP

Dual Channel Differential Isolated Gate Driver

Cree CAS325M12HM2 C2M SiC Half Bridge Module Optimized

V_{Drive}	+18/-5 V
I_G	±14 A
R_G	5 Ω

Features

- Optimized for Cree's High Performance CAS325M12HM2 Half Bridge Power Modules
- High-Frequency, Ultra-Fast Switching Operation
- On Board 3 W or 6 W Isolated Power Supplies
- Configurable UVLO with Hysteresis
- Direct Mount Low Inductance Design
- On-Board Overcurrent, Overlap, and Reverse Polarity Protection
- Differential Inputs for Increased Noise Immunity
- Differential to Single-Ended Daughter Board Available Upon Request

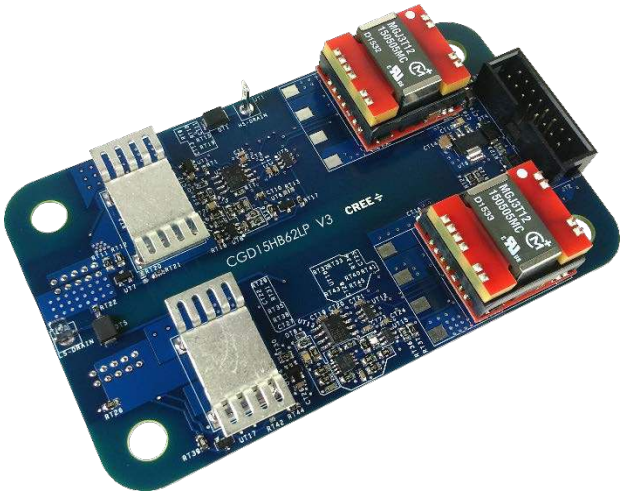
For Use with Cree Module

- CAS325M12HM2, 1200 V, 325 A Module Half Bridge CPM2 Variants for Module Junction Temperatures up to 175 °C

Applications

- DC Bus Voltages up to 1000 V

Package



Part Number	Package	Marking
CGD15HB62LP	PCBA	CGD15HB62LP V3

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions
V_{DC}	Supply Voltage	-0.5 to 18	V	
V_I	Logic Level Inputs	-0.5 to 5.5		
I_O	Output Peak Current	±14	A	T_A = 25 °C
$I_{O(avg)}$	Output Average Current	±4		
F_{max}	Maximum Switching Frequency	115	kHz	3 W Power Supply + CAS325M12HM2
T_{op}	Ambient Operating Temperature	-50 to 95	°C	
T_{stg}	Storage Temperature	-50 to 125		

Gate Driver Electrical Characterization

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{DC}	Supply Voltage	9	12	18	V	
V_{UVLO}	Secondary UVLO Inactive Level	+13.5	+14	+14.5		
	Secondary UVLO Active Level	+11.2	+12	+12.7		
	Secondary UVLO Hysteresis		2			
V_{IH}	High Level Logic Input Voltage	3.5		5.5		Single-Ended Inputs
V_{IL}	Low Level Logic Input Voltage	0		1.5		
V_{IDCM}	Differential Input Common Mode Range	-7	-	+12		Differential Inputs
V_{IDTH}	Differential Input Threshold Voltage	-200	-125	-50	mV	$V_{ID} = V_{Pos\text{-}Line} - V_{Neg\text{-}Line}$
V_{ODH}	Differential Output High Level	2.2	3.4		V	I_{OD} = -20 mA
V_{ODL}	Differential Output Low Level		0.2	0.4		I_{OD} = 20 mA
V_{OD}	Differential Output Magnitude	2	3.1			R_L=100 Ω
$V_{GATE,HIGH}$	High Level Output Voltage		+18			
$V_{GATE,LOW}$	Low Level Output Voltage		-5			
V_{IOWM}	Working Isolation Voltage		1500			V_{RMS}
C_{ISO}	Isolation Capacitance		17		pF	Per Channel
CMTI	Common Mode Transient Immunity	100			kV/µs	
$R_{GIC\text{-}ON}$	Output Resistance[1]		0.4	1.5	Ω	Gate Drive IC
$R_{GIC\text{-}OFF}$	Output Resistance[1]		0.3	1.2		
$R_{GEXT\text{-}ON}$	External Output Resistance[2]		4.99			External SMD Resistor
$R_{GEXT\text{-}OFF}$	External Output Resistance[2]		4.99			
$D_{VF\text{-}OFF}$	Turn-off Diode Forward Voltage	0.62	0.67	0.82	V	
t_{ON}	Output Rise Time		250		ns	C_{Load} = 19 nF From 10% to 90%
t_{OFF}	Output Fall Time		140			
$t_{PHL/PLH}$	Propagation Delay		75			
t_{PD}	Over-current Propagation Delay to FAULT Signal Low		40			Does Not Include Blanking
R_{SS}	Soft-Shutdown Resistance[3]		30.1		Ω	
$t_{OFF\text{-}SS}$	Output Fall Time Soft-Shutdown		1.5		µs	Output pulled low through R_{SS}

[1] Output resistance of totem pole IC

[2] Additional output resistance is added with SMD resistors. A diode is provided to allow control of turn-off separately. The diode makes the effective turn-off resistance be the parallel combination of the $R_{GEXT\text{-}ON}$ and $R_{GEXT\text{-}OFF}$ while the turn-on effective resistance is $R_{GEXT\text{-}ON}$. Standard value is 4.99 Ω for both turn-on and turn-off. See Figure 1 for configuration.

[3] Soft-Shutdown Resistor will safely turn off the Gate in the event an over-current is detected by the Desaturation Protection circuit.

Input Connector Information

Pin Number	Name	Description
1	VDC	Power Supply Input Pin
2	Common	Common
3	HS-P (*)	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω.
4	HS-N (*)	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω.
5	LS-P (*)	Positive Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω.
6	LS-N (*)	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω.
7	$\overline{\text{FAULT}}$ - P (*)	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
8	$\overline{\text{FAULT}}$ - N (*)	Negative Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
9	RTD-P (*)	Positive Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
10	RTD-N (*)	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.
11	$\overline{\text{PS-Dis}}$	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
12	Common	Common
13	PWM-EN	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
14	Common	Common
15	OC-EN	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
16	Common	Common

(*) Inputs 3 – 10 are differential pairs.

Block Diagram

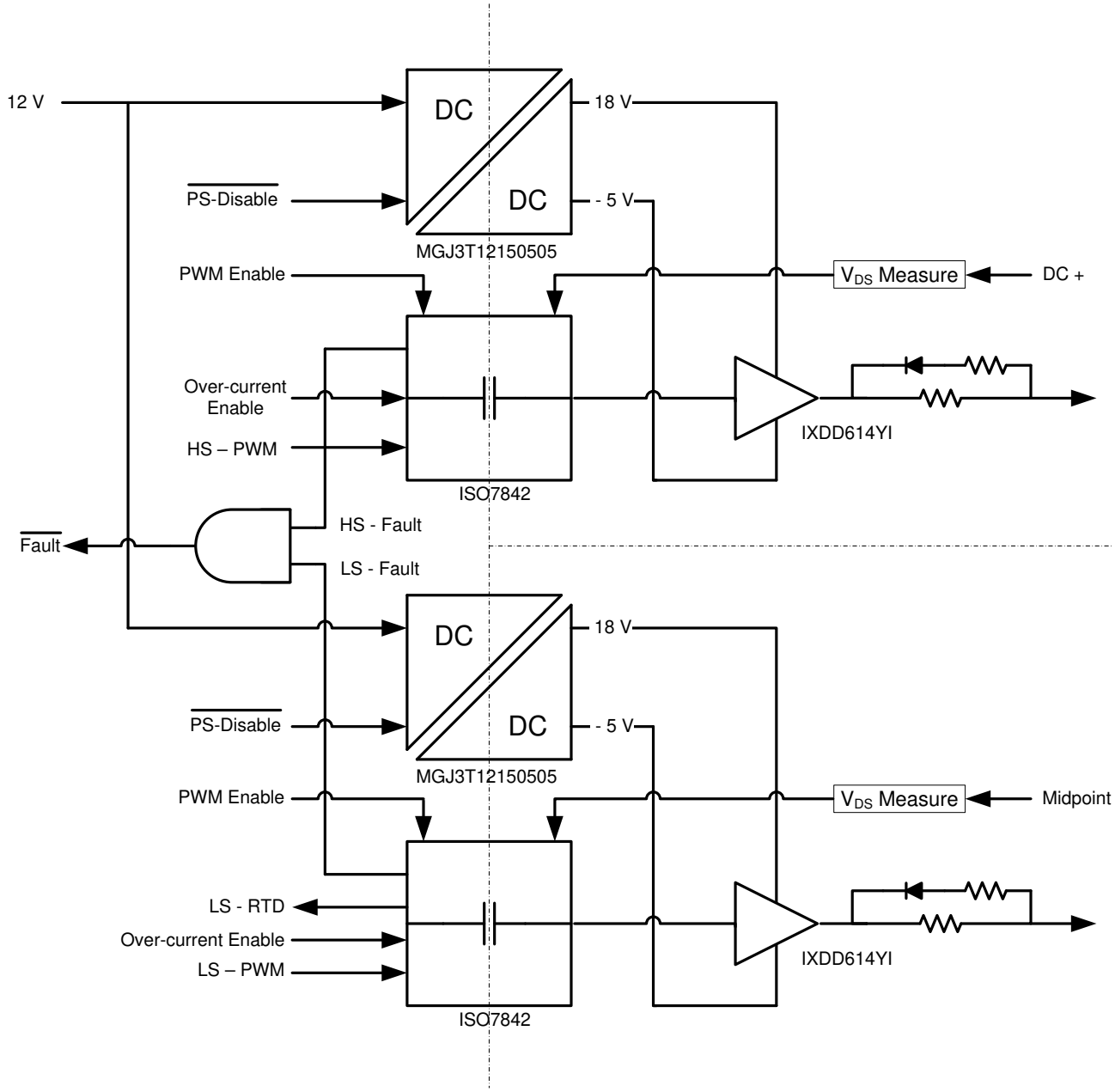


Fig 1. Block Diagram

Driver Interface

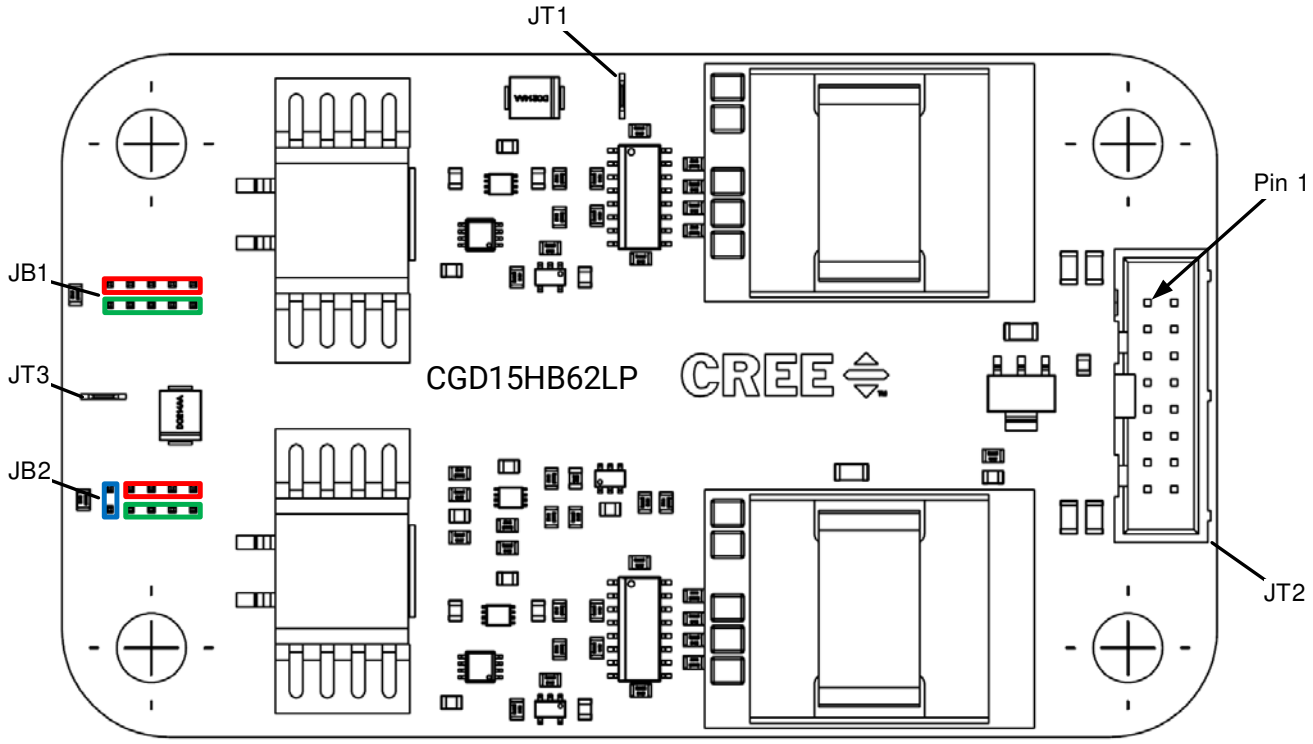


Fig 2. Top View

Connector	Name	Description
JT2	Signal Input	Description in Input Connection Information
JT1	HS-Drain	High Side Over-current protection connector Connect to DC +
JT3	LS-Drain	Low Side Over-current protection connector Connect to the Midpoint or populate RT19 with a 0 Ω resistor
JB1	HS-GS	Red – Gate Green – Source
JB2	LS-GS	Red – Gate Green – Source Blue – RTD

Signal Description

- **PWM Signals**: High side and low side PWM must be differential signals[4]. The termination impedance of the differential receiver is 250 Ω. A reference single-ended to differential converter is available as an optimized companion product. Overlap protection is provided to prevent both the high side and low side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.
- **FAULT Signal**: The fault signal is a differential output[4] with a maximum drive strength of 20mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if a UVLO or over-current fault is detected on either channel. See below for further description for what the individual faults indicate.
- **UVLO Fault**: The UVLO circuit detects when the output rails of the isolated DC/DC converter falls below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through R_G for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions, and the inactive and active regions can be configured through on-board resistors. The UVLO faults for both channels are combined along with the over-current fault in the FAULT output signal.
- **Over-Current Fault**: An over-current fault is an indication of an over-current event in the SiC power module. The over-current protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. A drain sense connection is provided by quick-connect spade connectors for both high side and low side. The low side drain connection can optionally be connected on-board to the high side source through jumper RT19. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistor, R_{SS}[3]. The drain-source limit can be configured through on-board resistors. The over-current protection is enabled by default, but it can be disabled by pulling the OC-EN pin low. The gate driver will operate correctly with this protection disabled. The over-current fault is latched upon detection and must be cleared by the user with a low pulse of at least 2.5 ns on the OC-EN signal.
- **RTD Signal**: RTD output is a differential signal[4] that measures the resistance of the RTD integrated into XAS325M12HM2 modules. The signal is a 50 kHz PWM that encodes the resistance of the RTD. The minimum and maximum duty cycles are 5% and 95% respectively to guarantee a signal is always present. The approximate temperature of the module can be determined from this resistance[5]. The module temperature can be calculated using the formula, $T_{RTD} = 5.42 * (DutyCycle) - 244\ °C$.
- **PS-Dis Signal:** PS-DIS signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. This can be used for startup sequencing.

[4] A single-ended to differential converter for both input and output is available as an optimized companion product.

[5] See *CAS325M12HM2 with Optional RTD Application Note* for further description of the RTD measurements.

- **PWM-EN Signal**: This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled and the gates will both be pulled low through R_G. All protection circuitry and power supplies will continue to operate including FAULT and RTD outputs.
- **Over-Voltage and Reverse Polarity Protection:** Power input on pin 1 of connector JT2 features a Zener diode to protect the gate driver from damage by connecting a power source that exceeds the voltage rating of the gate driver. If over-voltage protection has occurred power should be removed to allow the PTC fuse to reset. There is also a diode in-line with the power input to protect against connecting a power source with positive and negative polarity reversed.

Input Connector

- SBH11-PBPC-D08-ST-BK
- Drain connector for Overcurrent Protection: TE Connectivity 735187-2

Suggested Mating Parts

- SFH210-PPPC-D08-ID-BK
- SFH11-PBPC-D08-ST-BK
- SFH11-PBPC-D08-RA-BK
- Drain connector for Overcurrent: TE Connectivity 2-520272-2

Power Estimates

The gate driver power required is calculated using the formula below. The gate charge is dependent on the datasheets of the module being driven. The gate driver voltage (V_{GD}) is 23V for this gate driver. Once the required gate driver power is calculated the required input power can be calculated from the MGJ3T12150505MC and MGJ6T12150505MC efficiency curves on the power supplies datasheet. This calculation is for one channel of the gate driver.

$$P_{sw} = Q_G * F_{SW} * \Delta V_{GD}$$

P_{sw} : gate driver power
Q_G : total gate charge
F_{SW} : switching frequency
ΔV_{GD} : total gate drive voltage ($V_{GATE,HIGH}$ - $V_{GATE,LOW}$)

Dimensions [in(mm)]

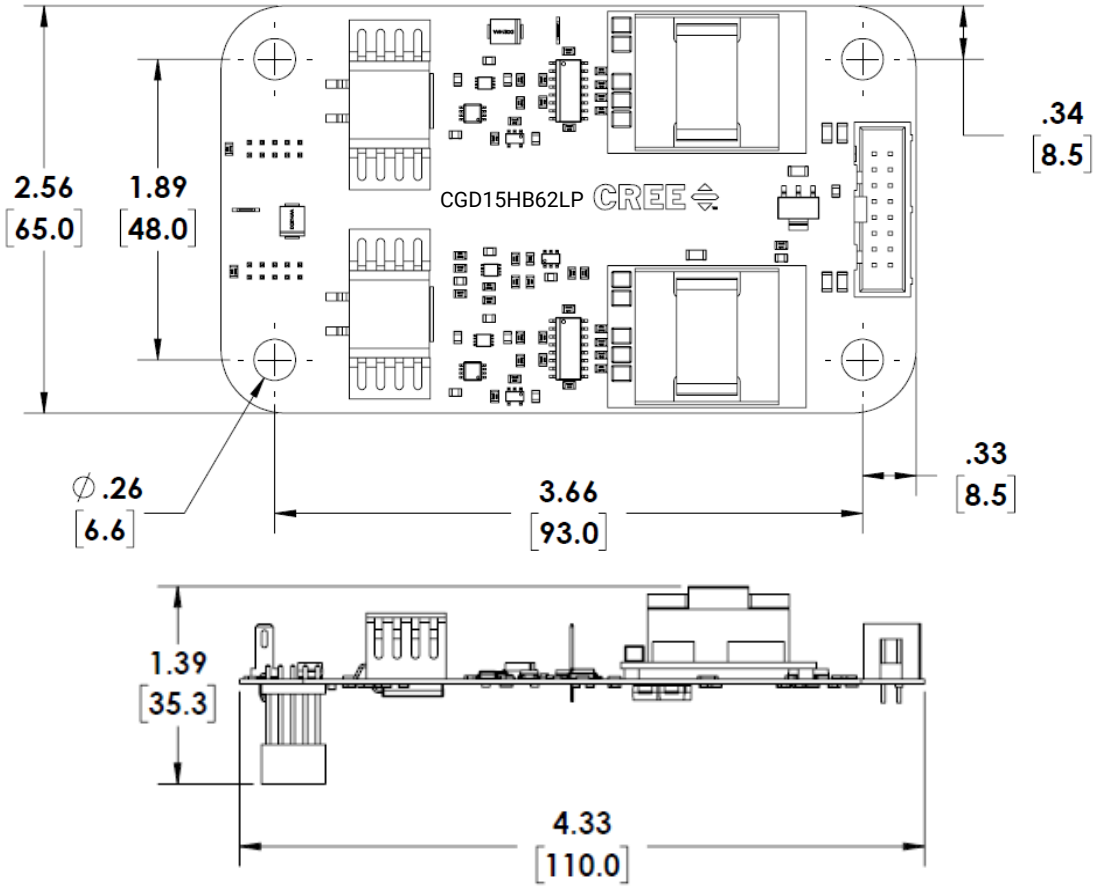


Fig 3. Dimensions

Important Notes

Suitability of this product for any application may depend on product parameters not specified in this document. Accordingly, buyers are cautioned to evaluate actual products against their needs and not to rely solely on the data and information presented in this document.

The product described has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body or in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, vehicle navigation, communication or control systems, or air traffic control systems.

The product described is not eligible for Distributor Stock Rotation or Inventory Price Protection.

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