

TPS53515 Step-Down Converter Evaluation Module User's Guide



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1 Introduction

The TPS53515EVM-PWR587 evaluation module (EVM) uses the TPS53515 device. The TPS53515 device is a D-CAP3™ mode, 12-A synchronous buck-converter with integrated MOSFETs. The device provides a fixed 1.2-V output at up to 12 A from a 12-V input bus.

2 Description

The TPS53515EVM-PWR587 is designed for a regulated 12-V bus to produce a regulated 1.2-V output at up to 12 A of load current. The TPS53515EVM-PWR587 is designed to demonstrate the TPS53515 device in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS53515 device.

2.1 Typical Applications

- Servers and storage
- Workstations and desktops
- Telecommunication infrastructure

2.2 Features

The TPS53515EVM-PWR587 features include the following:

- 12-A DC steady-state output current
- Support for a prebias-output voltage at startup
- Jumper, J2, for enable function
- Jumper, J5, for auto-skip and forced-continuous-conduction-mode (FCCM) selection
- Jumper, J7, for extra 5-V input for further power saving purpose
- Convenient test points for probing critical waveforms

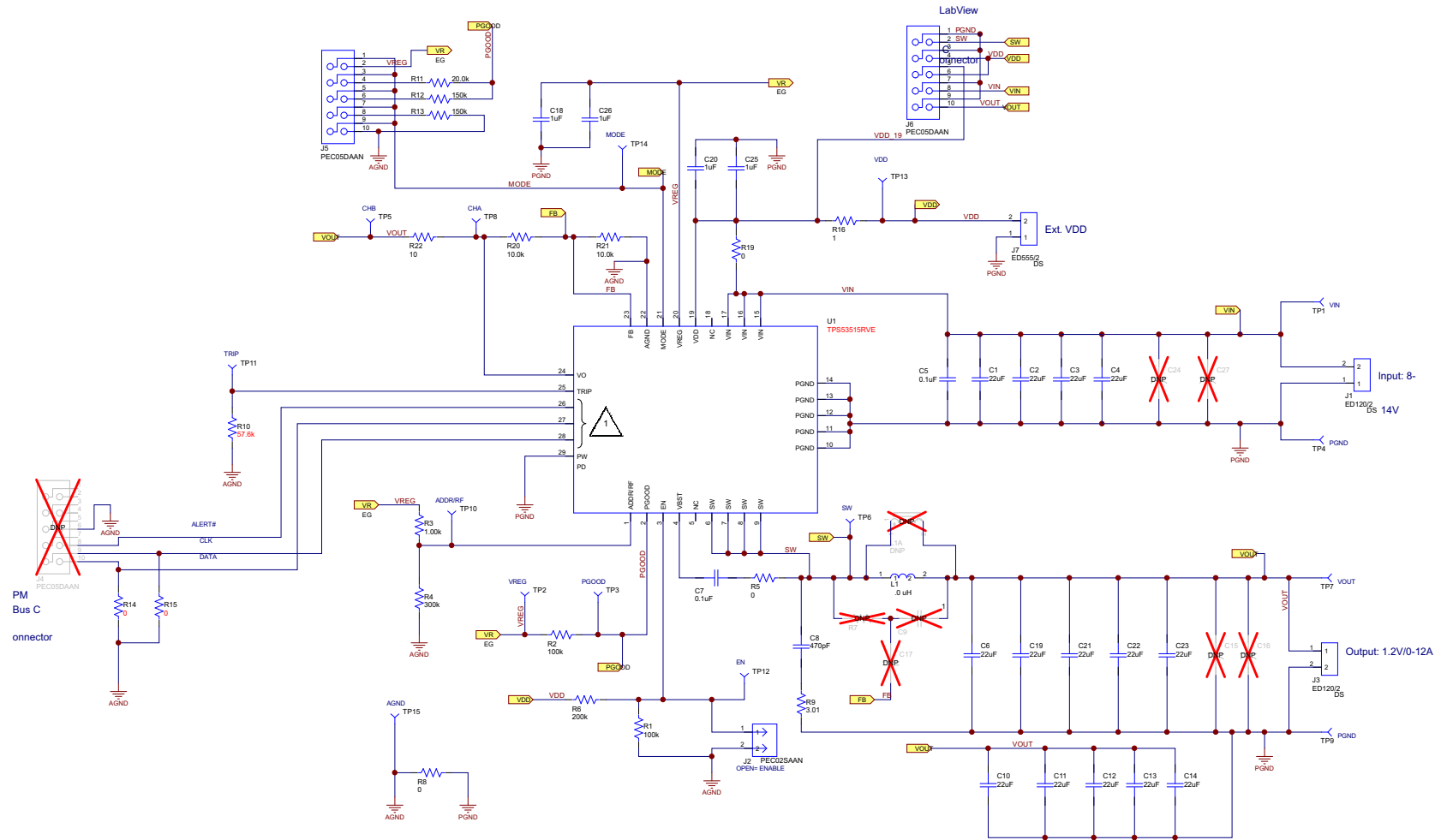
3 Electrical Performance Specifications

Table 3-1. TPS53515EVM-PWR587 Electrical Performance Specifications⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range	V_{IN}	5	12	18	V
Maximum input current	$V_{IN} = 5\text{ V}$, $I_O = 8\text{ A}$		2.5		A
No load input current	$V_{IN} = 12\text{ V}$, $I_O = 0\text{ A}$ with auto-skip mode		1		mA
Output Characteristics					
Output voltage V_{OUT}			1.2		V
Output voltage regulation	Line regulation ($V_{IN} = 5\text{ V} - 14\text{ V}$) with FCCM		0.2		%
	Load regulation ($V_{IN} = 12\text{ V}$, $I_O = 0\text{ A} - 8\text{ A}$) with FCCM		0.5		
Output voltage ripple	$V_{IN} = 12\text{ V}$, $I_O = 8\text{ A}$ with FCCM		10		mVpp
Output load current		0		12	A
Output over current			15		A
Soft-start			1		ms
Systems Characteristics					
Switching frequency	$V_{IN} = 12\text{ V}$, 1.2 V / 4 A		1000		kHz
Peak efficiency	$V_{IN} = 12\text{ V}$, 1.2 V / 8 A		88.5		%
Full load efficiency			86.9		%
Operating temperature			25		°C

(1) Jumpers set to default locations, See [Section 6](#).

4 Schematic



NOTES:



VARIANT PINOUT FOR U1

TABLE 1			
IC	TPS53915	TPS53513	TPS53515
PIN 26	ALERT#	NC	NC
PIN 27	SDA	GND1	GND1
PIN 28	SCL	GND2	GND2

Figure 4-1. TPS53515EVM-PWR587 Schematic

5 Test Setup

5.1 Test Equipment

- Oscilloscope** A digital or analog oscilloscope measures the output ripple. The oscilloscope must be set for the following: 1-M Ω impedance, 20-MHz bandwidth, AC coupling, 1- μ s / division horizontal resolution, 20-mV / division vertical resolution. Test points TP7 and TP9 measure the output ripple voltage by placing the oscilloscope probe tip through TP7 and holding the ground barrel on TP9 as shown in Figure 5-1. Using a leaded ground connection can induce additional noise due to the large ground loop.
- Voltage Source** The input voltage source V_{IN} must be a 0 to 14-V variable-DC source capable of supplying 10 ADC. Connect V_{IN} to J1 as shown in Figure 5-2.
- Multimeters** V1: V_{IN} at TP1 (V_{IN}) and TP4 (GND).
V2: V_{OUT} at TP7 (V_{OUT}) and TP9 (GND).
- Output Load** The output load must be an electronic constant-resistance-mode load capable of 0 to 15 ADC at 1.2 V.

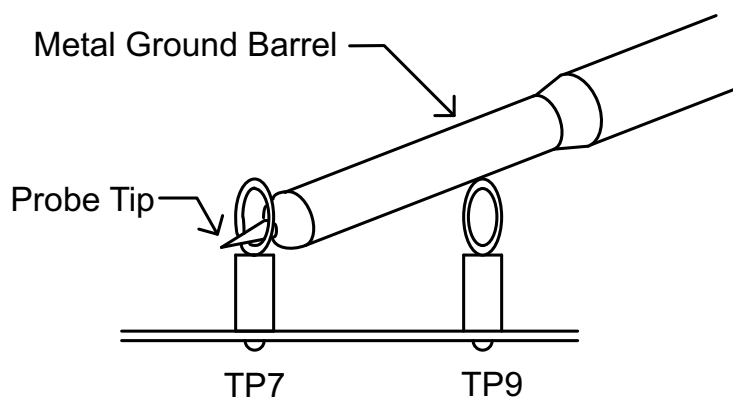


Figure 5-1. Tip and Barrel Measurement for V_{OUT} Ripple

Recommended Wire Gauge:

1. V_{IN} to J1 (12-V input)
 - The recommended wire size is 1 \times AWG number 14 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
2. J3 to LOAD
 - The minimum recommended wire size is 2 \times AWG number 14, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

5.2 Recommended Test Setup

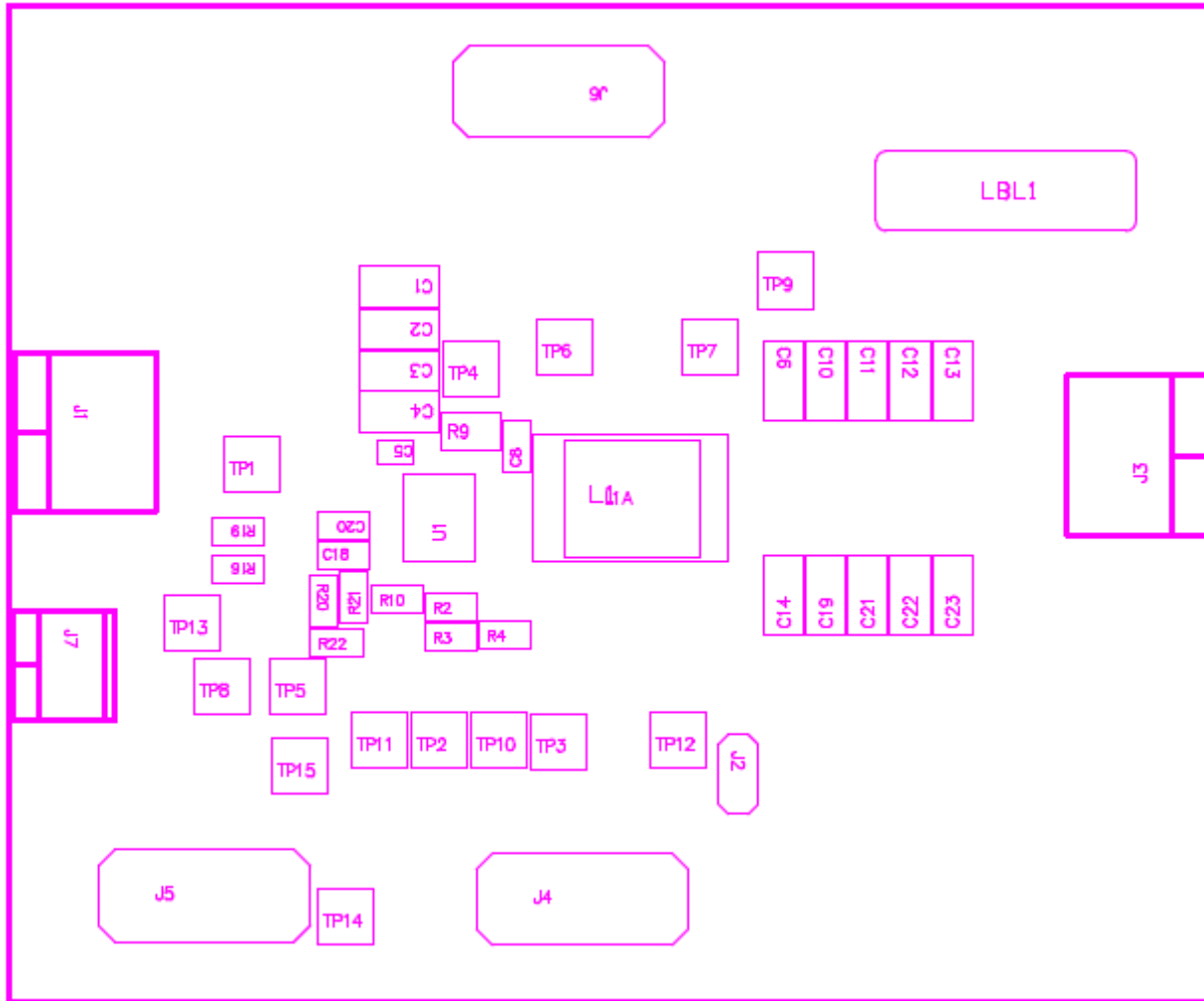


Figure 5-2. TPS53515EVM-587 Top Layer for Test Setup

Input Connections:

1. Prior to connecting the DC input-source, VIN, TI recommends to limit the source current from VIN to 10 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in [Figure 5-2](#).
2. Connect the voltmeter V1 at TP1 (VIN) and TP4 (GND) to measure the input voltage.

Output Connections:

1. Connect the load to J3 and set the load to constant-resistance-mode to sink 0 ADC before VIN is applied.
2. Connect the voltmeter V2 at TP7 (VOUT) and TP9 (GND) to measure the output voltage.

6 Configurations

All Jumper selections must be made prior to applying power to the EVM. Configure this EVM using the following configuration selections.

6.1 Switching Frequency Selection

Switching frequency can be changed as shown in [Table 6-1](#).

Table 6-1. Switching Frequency Selection

SWITCHING FREQUENCY ⁽¹⁾ (f_{sw}) (kHz)	RESISTOR DIVIDER RATIO (R_{DR})	EXAMPLE RF FREQUENCY COMBINATIONS	
		R_{RF_H} (k Ω)	R_{RF_L} (k Ω)
1000	> 0.557	1	300
850	0.461	180	154
750	0.375	200	120
600	0.297	249	105
500	0.229	240	71.5
400	0.16	249	47.5
300	0.096	255	27
200	< 0.041	270	11.5

(1) Default Setting: 1 MHz.

For different switching frequency setting, please change R3 and R4 as shown in [Table 6-1](#).

6.2 Mode Selection

The MODE can be set by J5.

Table 6-2. Mode Selection

JUMPER SET TO:	MODE SELECTION
1 to 2 pin shorted	FCCM with 2x RC time constant
3 to 4 pin shorted ⁽¹⁾	FCCM ⁽²⁾ with 1x RC time constant ⁽¹⁾
5 to 6 pin shorted	FCCM ⁽²⁾ with 2x RC time constant
7 to 8 pin shorted	Auto-skip mode with 2 \times RC time constant
9 to 10 pin shorted	Auto-skip mode with 1 \times RC time constant

(1) Default setting.

(2) The device enters FCCM after PGOOD goes high.

6.3 VDD Pin Supply Selection

The controller can be enabled and disabled by J7.

Table 6-3. Enable Selection

SET ON CONNECTION	ENABLE SELECTION
R19 = 0 Ω ⁽¹⁾	VDD pin connected to VIN pins ⁽¹⁾
R19 = Open	VDD pin disconnected to VIN pins

(1) Default setting: the VDD pin connected to the VIN pins through R19.

For power-up, input J7 with proper voltage. The VDD pin input voltage range is from 4.5 V to 25 V.

7 Test Procedure

7.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in [Section 5](#) and [Figure 5-2](#).
2. Ensure the load is set to constant-resistance mode and to sink at 0 ADC.
3. Ensure all jumper settings are configured as shown in [Section 6](#).
4. Ensure the jumper provided in the EVM shorts on J2 before VIN is applied.
5. Increase VIN from 0 to 12 V. Use V1 to measure input voltage.
6. Remove the jumper on J2 to enable the controller.
7. Use V2 to measure the VOUT voltage.
8. Vary the load from 0 to 10 ADC, VOUT must remain in load regulation.
9. Vary VIN from 8 to 14 V, VOUT must remain in line regulation.
10. To disable the converter, place the jumper on J2.
11. Decrease the load to 0 A.
12. Decrease VIN to 0 V.

7.2 Control-Loop Gain and Phase-Measurement Procedure

The TPS53515EVM-PWR587 contains a 10- Ω series resistor in the feedback loop for loop response analysis.

1. Set up the EVM as described in [Section 5](#) and [Figure 5-2](#).
2. Connect the isolation transformer to the test points marked TP5 and TP8.
3. Connect the input-signal amplitude-measurement probe (channel A) to TP10. Connect the output-signal amplitude-measurement probe (channel B) to TP11.
4. Connect the ground lead of channel A and channel B to TP15.
5. Inject around 20 mV or less signal through the isolation transformer.
6. To measure control-loop gain and phase margin, change the frequency from 100 Hz to 1 MHz using a 10-Hz or less post filter.
7. Disconnect the isolation transformer from the bode-plot test points before making other measurements.
 - Signal injection into feedback can interfere with the accuracy of other measurements.

7.3 List of Test Points

Table 7-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	VIN	Converter input supply voltage
TP2	VREG	LDO voltage
TP3	PGOOD	Power good output
TP4	PGND	Power ground
TP5	CHB	Input B for loop injection
TP6	SW	Switch Node
TP7	VOUT	VOUT terminal +
TP8	CHA	Input A for loop injection
TP9	PGND	Power ground
TP10	RF	RF pin
TP11	TRIP	TRIP pin
TP12	EN	Enable pin
TP13	VDD	VDD pin
TP14	MODE	MODE pin
TP15	AGND	Analog ground

7.4 Equipment Shutdown

Follow these steps when shutting down the equipment.

1. Shut down load
2. Shut down VIN

8 EVM Assembly Drawing and PCB Layout

The following figures show the design of the TPS53515EVM-PWR587 printed circuit board (see [Figure 8-1](#), [Figure 8-2](#), [Figure 8-3](#), [Figure 8-4](#), [Figure 8-5](#), [Figure 8-6](#), [Figure 8-7](#), and [Figure 8-8](#)). The EVM has been designed using a six-layer, 2-oz copper-circuit board.

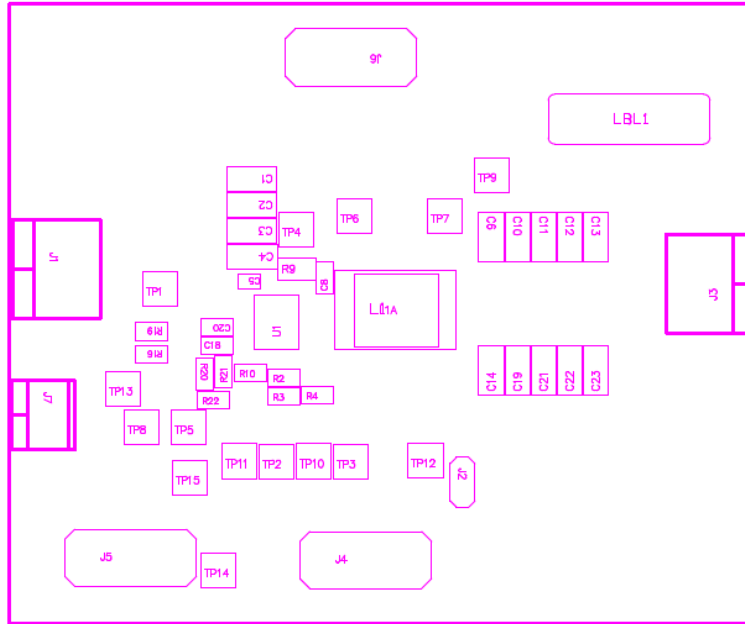


Figure 8-1. TPS53515EVM-587 Top-Layer Assembly Drawing

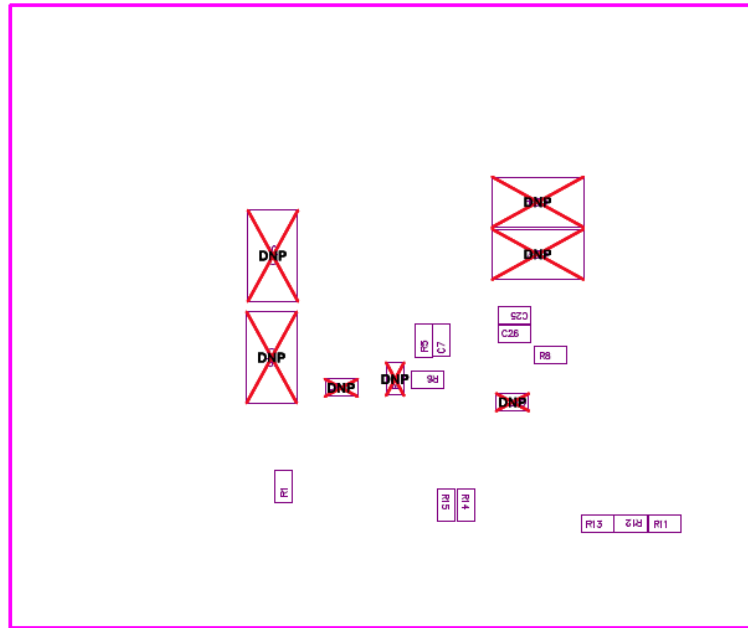


Figure 8-2. TPS53515EVM-587 Bottom-Layer Assembly Drawing

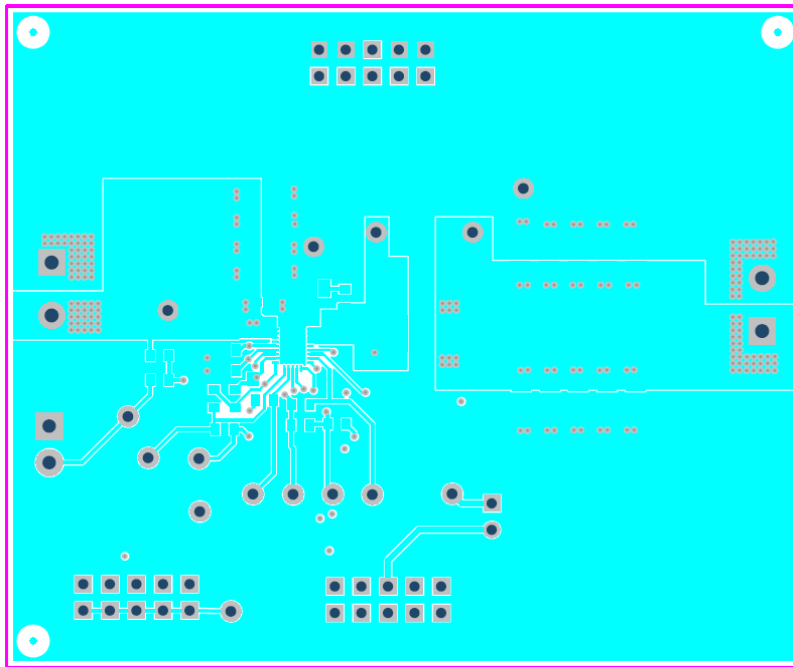


Figure 8-3. TPS53515EVM-587 Top Layer, Copper

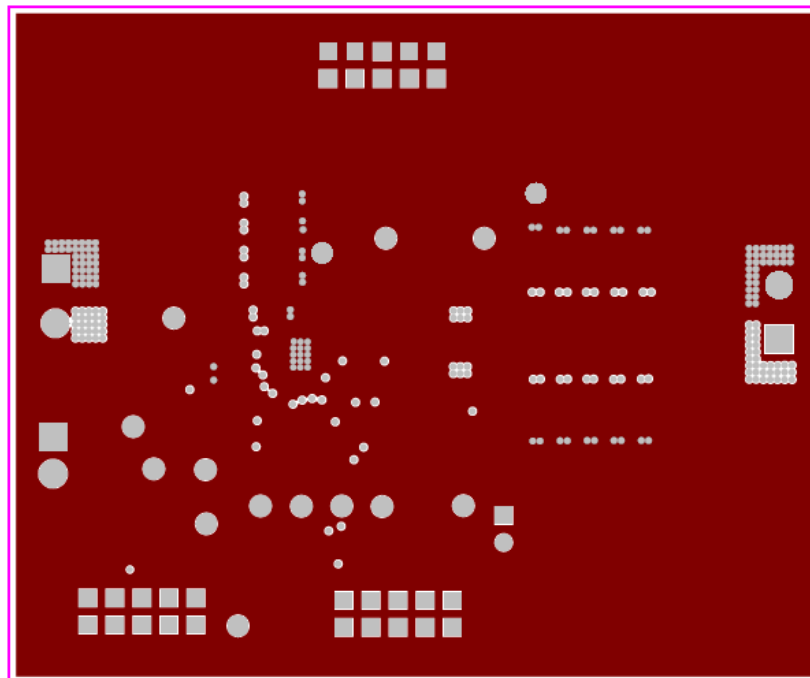


Figure 8-4. TPS53515EVM-587 Layer Two, Copper

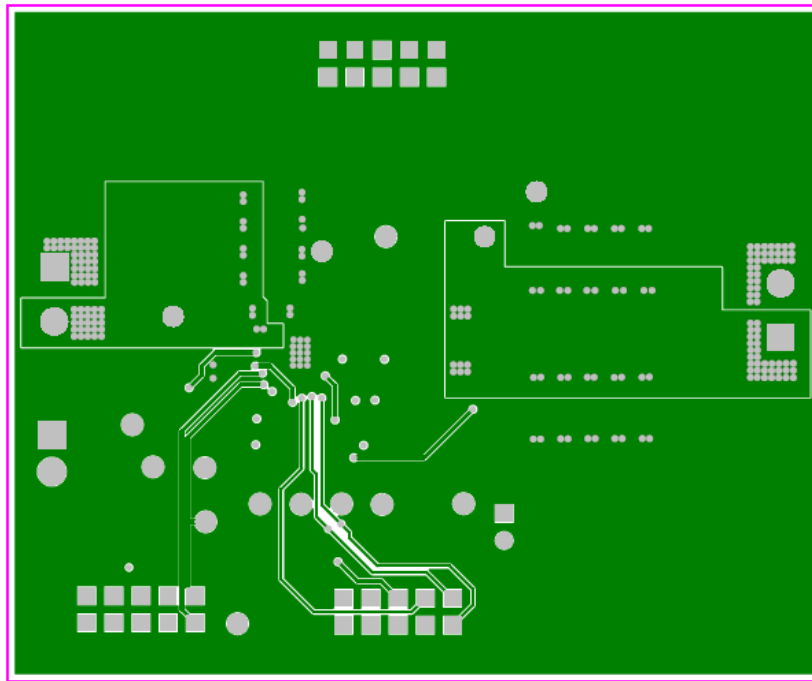


Figure 8-5. TPS53515EVM-587 Layer Three, Copper

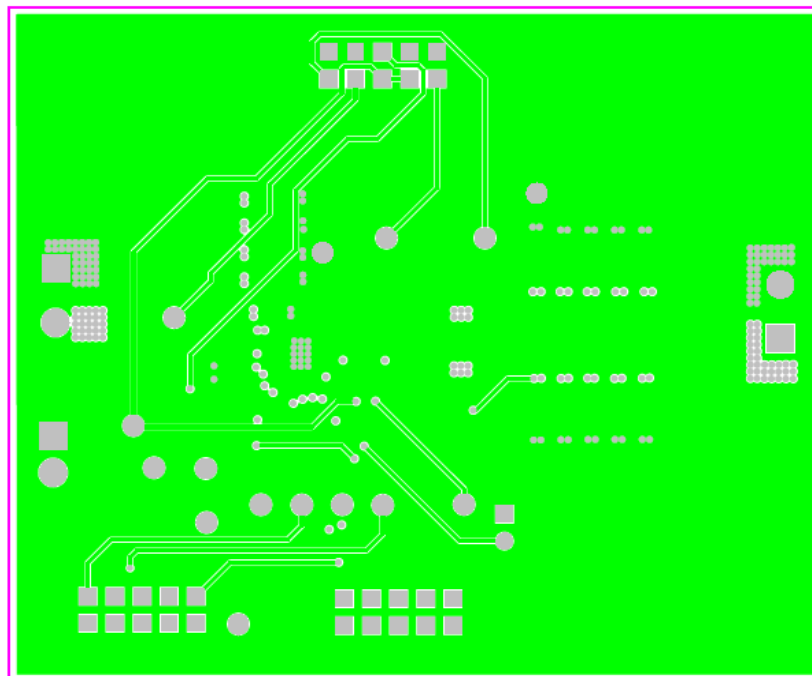


Figure 8-6. TPS53515EVM-587 Layer Four, Copper

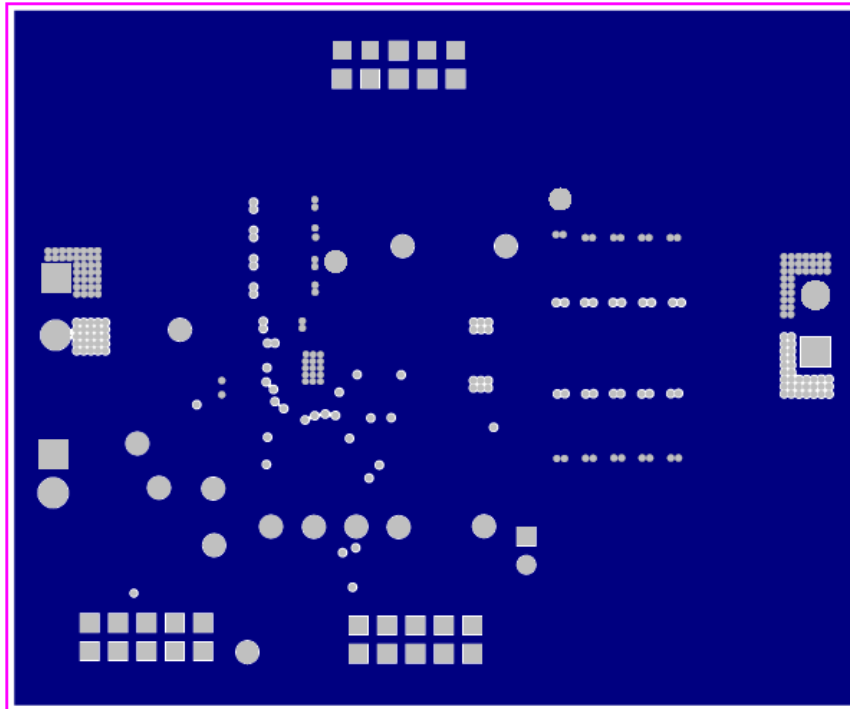


Figure 8-7. TPS53515EVM-587 Layer Five, Copper

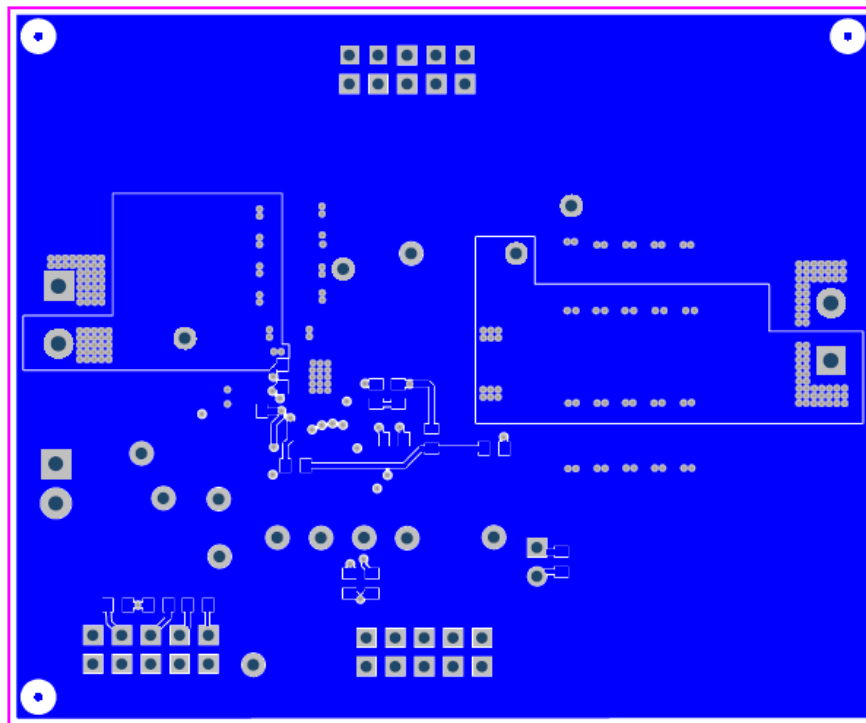


Figure 8-8. TPS53515EVM-587 Bottom Layer, Copper

9 Bill of Materials

Table 9-1. EVM Components List (Based on the Schematic, See Figure 4-1)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2, C3, C4	4	22 μ F	Capacitor, Ceramic, 25 V, X5R, 10%	1206	GRM31CR61E226KE15L	Murata
C5	1	0.1 μ F	CAP CER 0.1 μ F 25 V 10% X5R 0402	0402	GRM155R61E104KA87D	Murata
C6, C10, C11, C12, C13, C14, C19, C21, C22, C23	10	22 μ F	Capacitor, Ceramic, 6.3 V, X5R, 20%	1206	GRM31CR60J226KE19L	Murata
C7	1	0.1 μ F	CAP CER 0.1 μ F 50 V 10% X7R 0603	0603	GRM188R71H104KA93D	Murata
C8	1	470 pF	CAP CER 470 pF 50 V 10% X7R 0603	0603	GRM188R71H471KA01D	Murata
C9, C17	0	Open	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Standard	Standard
C15, C16, C24, C27	0	Open	Capacitor, POSCAP, SMT, 2.5 V, 330 μ F, 8 m Ω	7343(D)	2R5TPE330M9 or 6TPE330MIL	Sanyo
C18, C20, C25, C26	4	1 μ F	CAP CER 1 μ F 16 V 10% X7R 0603	0603	GRM188R71C105KA12J	Murata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J1, J3	2	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1 mm	0.4 \times 0.35 inch	ED120/2DS	OST
J2	1	PEC02SAAN	Header, Male 2-pin, 100-mil spacing,	0.1 \times 2 inch	PEC02SAAN	Sullins
J4, J5, J6	3	PEC05DAAN	Header, Male 2 \times 5-pin, 100-mil spacing	0.1 \times 2 \times 5 inch	PEC05DAAN	Sullins
J7	1	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5 mm	0.27 \times 0.25 inch	ED555/2DS	OST
L1	1	1 μ H	Inductor, Power Chokes SMD	6.6 \times 7.1 mm	PIMB065T-1R0MS	Cyntec
L1A	0	DNP	Inductor, High Fq Power, \pm 15%	0.283 \times 0.433 inch	69P987xN	Vitec
LBL1	1		Thermal Transfer Printable Labels, 0.650 (W) \times 0.2 inch (H) — 10,000 per roll	PCB Label 0.65 (H) \times 0.2 inch (W)	THT-14-423-10	Brady
R1, R2, R14, R15	4	100k	RES, 100 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R3	1	1k	RES, 1 k Ω , 1%, 0.1 W, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R4	1	300k	RES, 300 k Ω , 1%, 0.1 W, 0603	0603	RC0603FR-07300KL	Yageo America
R5, R8, R19	3	0	RES, 0 Ω , 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R6	1	200k	RES, 200 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603200KFKEA	Vishay-Dale
R7	0	Open	Resistor, Chip, 1/16 W, 1%	0603	Standard	Standard
R9	1	3.01	RES, 3.01 Ω , 1%, 0.125 W, 0805	0805	CRCW08053R01FKEA	Vishay-Dale
R10	1	57.6k	RES, 57.6 k Ω , 1%, 0.1 W, 0603	0603	RC0603FR-0757K6L	Yageo America
R11	1	20k	RES, 20.0 k Ω , 1%, 0.1 W, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R12, R13	2	150k	RES, 150 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603150KFKEA	Vishay-Dale
R16	1	1	RES, 1 Ω , 1%, 0.1 W, 0603	0603	CRCW06031R00FKEA	Vishay-Dale
R20, R21	2	10k	RES, 10 k Ω , 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R22	1	10	RES, 10 Ω , 1%, 0.1 W, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
TP1, TP2, TP3, TP5, TP6, TP7, TP8, TP10, TP11, TP12, TP13, TP14, TP15	13	5000	Test Point, Red, Thru Hole Color Keyed	0.1 \times 0.1 inch	5000	Keystone
TP4, TP9	2	5001	Test Point, Black, Thru Hole Color Keyed	0.1 \times 0.1 inch	5001	Keystone
U1	1	TPS53515RVE	IC, High Performance, 12-A Single Sync. Step-Down Converter with PMBus.		TPS53515RVE	TI

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2014) to Revision C (May 2021) Page

- Changed user's guide title..... 2
- Updated the numbering format for tables, figures, and cross-references throughout the document. 2

Changes from Revision A (December 2013) to Revision B (February 2014) Page

- Changed the test points in the *Tip and Barrel Measurement for VOUT Ripple* image from TPS5 and TPS7 to TPS7 and TPS9 (respectively from left to right)..... 4
-

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