1.6 MHz, 3-V TO 6-V INPUT, 3-A SYNCHRONOUS STEP-DOWN SWIFT™ CONVERTER

Check for Samples: TPS54317

FEATURES

- **60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Current**
- **Adjustable Output Voltage Down to 0.9 V With 1% Accuracy**
- **Switching Frequency: Adjustable From 280 kHz to 1600 kHz**
- **Externally Compensated for Design Flexibility**
- **Fast Transient Response**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**
- **Spacing Saving 4mm x 5mm QFN Packaging**
- **For SWIFT Documentation, Application Notes, and Design Software, see the TI website at www.ti.com/swift**

APPLICATIONS

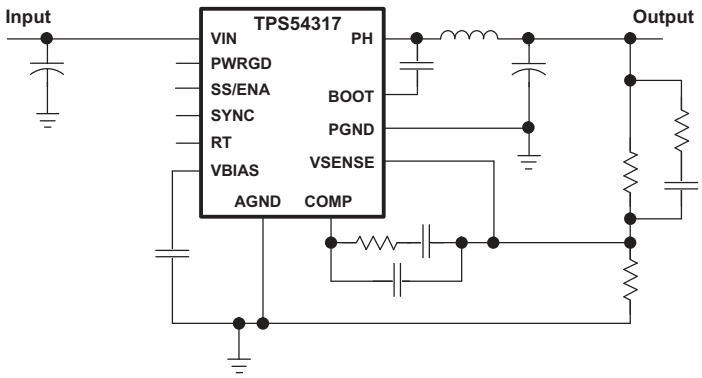
- **Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**

DESCRIPTION

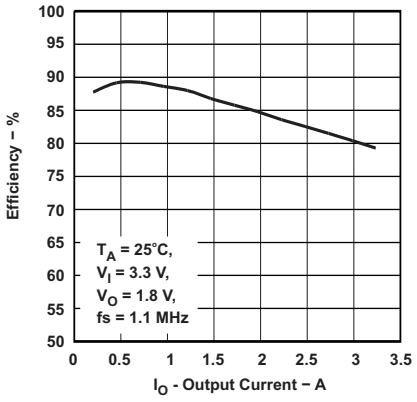
As members of the SWIFT™ family of dc/dc regulators, the TPS54317 low-input-voltage high-output-current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54317 device is available in a thermally enhanced 24-pin QFN (RHF) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT designer software tool to aid in achieving high-performance power supply designs to meet aggressive equipment development cycles.

Simplified Schematic



EFFICIENCY vs LOAD CURRENT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_J	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 125°C	Adjustable Down to 0.9 V	QFN (RHF)(1) (2)	TPS54317RHF

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RHF package is available in two different tape and reel quantities. Add an R suffix to the device type (i.e. TPS54317RHFR) for a 3000 piece reel and add a T suffix (TPS54317RHFT) for a 250 piece reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_I	Input voltage range	VIN, SS/ENA, SYNC	–0.3 to 7	V
		RT	–0.3 to 6	V
		VSENSE	–0.3 to 4	V
		BOOT	–0.3 to 17	V
V_O	Output voltage range	VBIAS, PWRGD, COMP	–0.3 to 7	V
		PH (steady state)	–0.6 to 10	V
		PH (transient < 20 ns)	–2 to 10	V
I_O	Output current range	PH	Internally Limited	
		COMP, VBIAS	6	mA
	Sink current	PH	6	A
		COMP	6	mA
		SS/ENA, PWRGD	10	mA
	Voltage differential	AGND to PGND	±0.3	V
	Continuous power dissipation		See Power Dissipation Rating Table	
T_J	Operating virtual junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3		6	V
T_J	Operating junction temperature	–40		125	°C

PACKAGE DISSIPATION RATINGS(1) (2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	THERMAL IMPEDANCE JUNCTION-TO-CASE
24-Pin RHF with solder	19.7°C/W	1.7°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.
(2) Test board conditions:
(a) 3 inch x 3 inch, 4 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground plane on the bottom of the PCB
(d) 2 oz. copper ground planes on the 2 internal layers
(e) 6 thermal vias (see the Recommended land pattern, Figure 12)

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
V_I	Input voltage range, VIN		3		6	V
	Quiescent current	f_s = 350 kHz, SYNC = 0.8 V, RT open		6.2	9.6	mA
		f_s = 550 kHz, SYNC ≥ 2.5 V, RT open, phase pin open		8.4	12.8	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDERVOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3	V
	Stop threshold voltage, UVLO		2.7	2.8		
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE						
V_O	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.7	2.8	2.9	V
	Output current, VBIAS (2)				100	µA
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation(1) (3)	I_L = 1.5 A, f_s = 1.1 MHz, T_J = 25°C		0.04		%/V
	Load regulation(1) (3)	I_L = 0 A to 3 A, f_s = 1.1 MHz, T_J = 25°C		0.09		%/A
OSCILLATOR						
	Internally set free-running frequency range	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set free-running frequency range	RT = 100 kΩ (1% resistor to AGND)	460	500	540	kHz
		RT = 43 kΩ (1% resistor to AGND)	995	1075	1155	
	High-level threshold voltage, SYNC		2.5			V
	Low-level threshold voltage, SYNC				0.8	V
	Pulse duration, SYNC(1)		50			ns
	Frequency range, SYNC		330		1600	kHz
	Ramp valley(1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time				150	ns
	Maximum duty cycle		90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10 .

ELECTRICAL CHARACTERISTICS (continued)

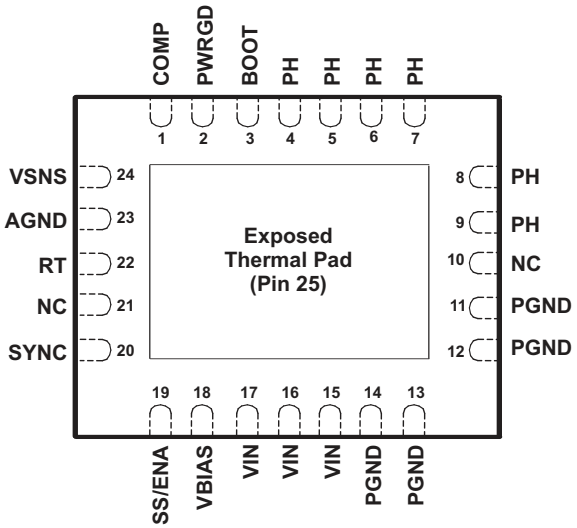
T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(4)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(4)	3	5		MHz
	Error amplifier common-mode input voltage range	Powered by internal LDO(4)	0		VBIAS	V
I_{IB}	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
V_O	Output voltage slew rate (symmetric), COMP		1	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)	10 mV overdrive(4)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
	Voltage to regulate using the internal V_{ref}, SS/ENA			1.95	2.2	V
	Enable hysteresis voltage, SS/ENA (4)			0.03		V
	Falling edge deglitch, SS/ENA (4)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, V_I = 2.7 V	1.5	2.3	4	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		90		%V_{ref}
	Power good hysteresis voltage (4)			3		%V_{ref}
	Power good falling edge deglitch (4)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	V_I = 5.5 V			1	µA
CURRENT LIMIT						
	Current limit trip point	V_I = 3 V, output shorted (4)	4	6.5		A
		V_I = 6 V, output shorted (4)	4.5	7.5		
	Current limit leading edge blanking time(4)			100		ns
	Current limit total response time (4)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point (4)		135	150	165	°C
	Thermal shutdown hysteresis (4)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	V_I = 6 V		59	88	mΩ
		V_I = 3 V		85	136	

(4) Specified by design

PIN ASSIGNMENTS

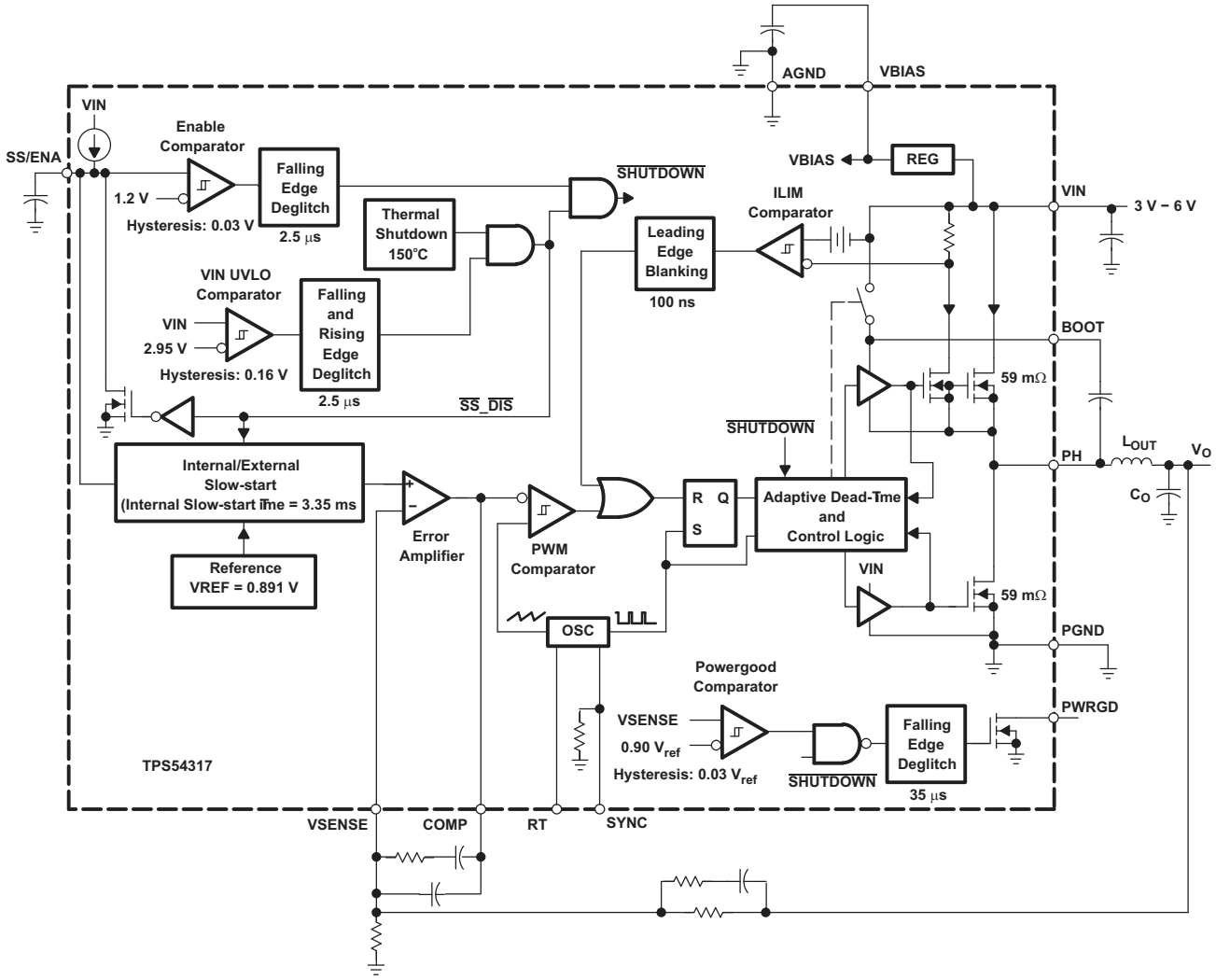
RHF PACKAGE
(BOTTOM VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
COMP	1	Error amplifier output. Connect compensation network from COMP to VSENSE.
PWRGD	2	Power good open drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
BOOT	3	Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
PH	4-9	Phase input/output. Junction of the internal high and low-side power MOSFETs, and output inductor.
PGND	11-14	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
VIN	15-17	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1-µF to 10-µF ceramic capacitor.
VBIAS	18	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1-µF to 1.0-µF ceramic capacitor.
SS/ENA	19	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	20	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
RT	22	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
AGND	23, 25	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Make PowerPAD connection to AGND.
VSNS	24	Error amplifier inverting input.
NC	10, 21	Not connected internally.

FUNCTIONAL BLOCK DIAGRAM



ADDITIONAL 3-A SWIFT DEVICES

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS54310	Adjustable	TPS54372	DDR/Adjustable
TPS54380	Sequencing/Adjustable	TPS54373	Prebias/Adjustable

RELATED DC/DC PRODUCTS

- TPS40007 – dc/dc controller
- PTH0407W – 3-A plug-in module
- UC282-ADJ – 3-A low dropout regulator

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

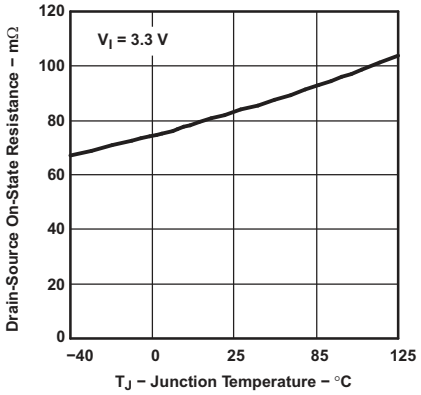


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

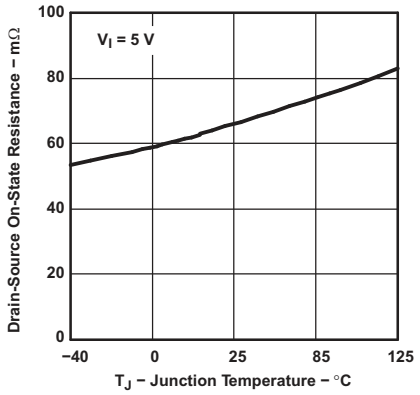


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

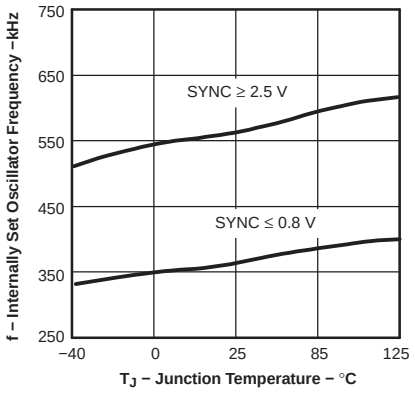


Figure 3.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

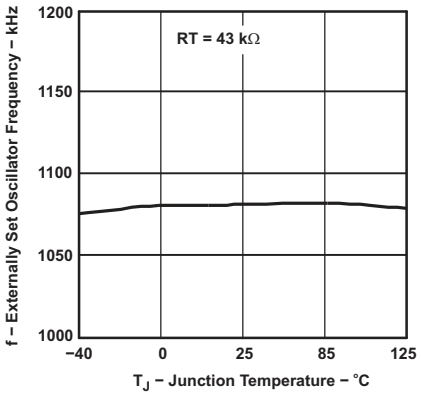


Figure 4.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

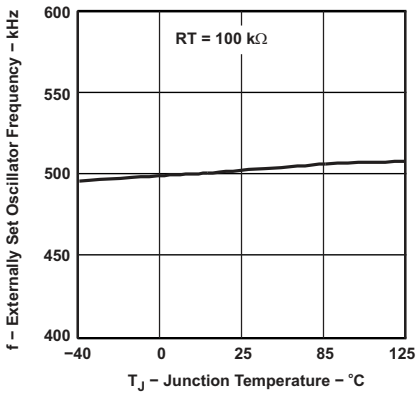


Figure 5.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

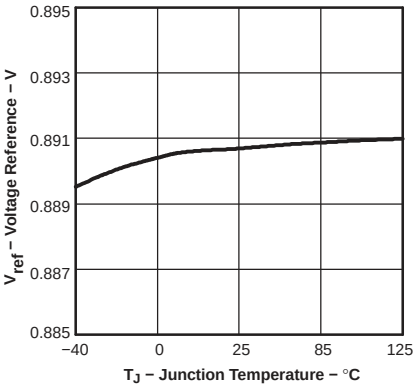


Figure 6.

ERROR AMPLIFIER OPEN LOOP RESPONSE

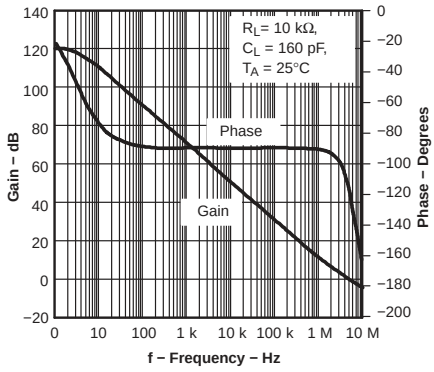


Figure 7.

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

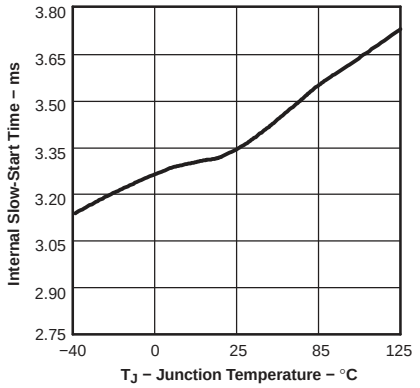


Figure 8.

DEVICE POWER LOSSES vs LOAD CURRENT

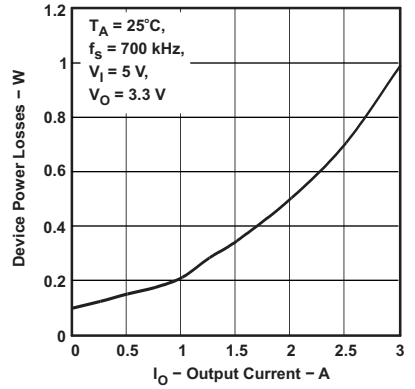


Figure 9.

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54317 application. The TPS54317 (U1) provides up to 3 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the power pad underneath the TPS54317 integrated circuit needs to be soldered well to the printed circuit board.

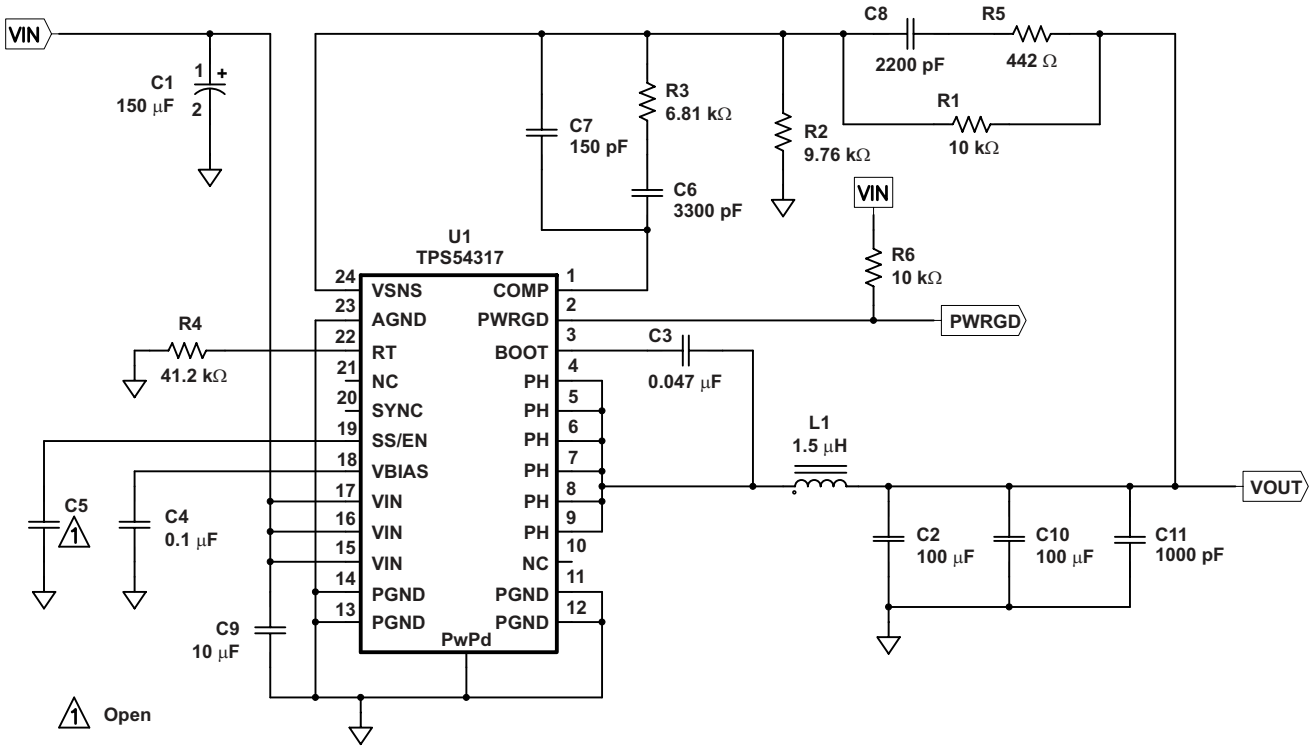


Figure 10. TPS54317 Schematic

INPUT VOLTAGE

The input to the circuit is a nominal 3.3 VDC, applied at J1. The optional input filter (C1) is a 150-µF capacitor, with a maximum allowable ripple current of 3 A. C9 is the decoupling capacitor for the TPS54317 and must be located as close to the device as possible.

FEEDBACK CIRCUIT

The resistor divider network of R1 and R2 sets the output voltage for the circuit at 1.8 V. R1, along with R5, R3, C5, C7, and C8 forms the loop compensation network for the circuit. For this design, a Type 3 topology is used.

OPERATING FREQUENCY

In the application circuit, the 1.1-MHz operation is selected. Connecting a 41.2-kΩ between RT (pin 22) and analog ground can be used to set the switching frequency from 280 kHz to 1.6 MHz. To calculate the RT resistor, use the Equation 1:

$$R(\Omega) = \frac{51\text{ k}}{f\text{ (MHz)}} - 4.7\text{ k} \quad (1)$$

OUTPUT FILTER

The output filter is composed of a 1.5-µH inductor and two capacitors. The inductor is a low dc resistance (0.017 Ω) type, Coilcraft DO1813P-122HC. The feedback loop is compensated so that the unity gain frequency is approximately 75 kHz.

PCB LAYOUT

Figure 11 shows a generalized PCB layout guide for the TPS54317.

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54317 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.

The TPS54317 has two internal grounds (analog and power). Inside the TPS54317, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54317, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54317. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the voltage set point divider, timing resistor RT, slow start capacitor and bias capacitor grounds. Connect this trace directly to AGND (pin 1).

The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, L_O, C_O and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they must be routed close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. The bias capacitor should be as close as possible to the VBIAS pin and analog ground . If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

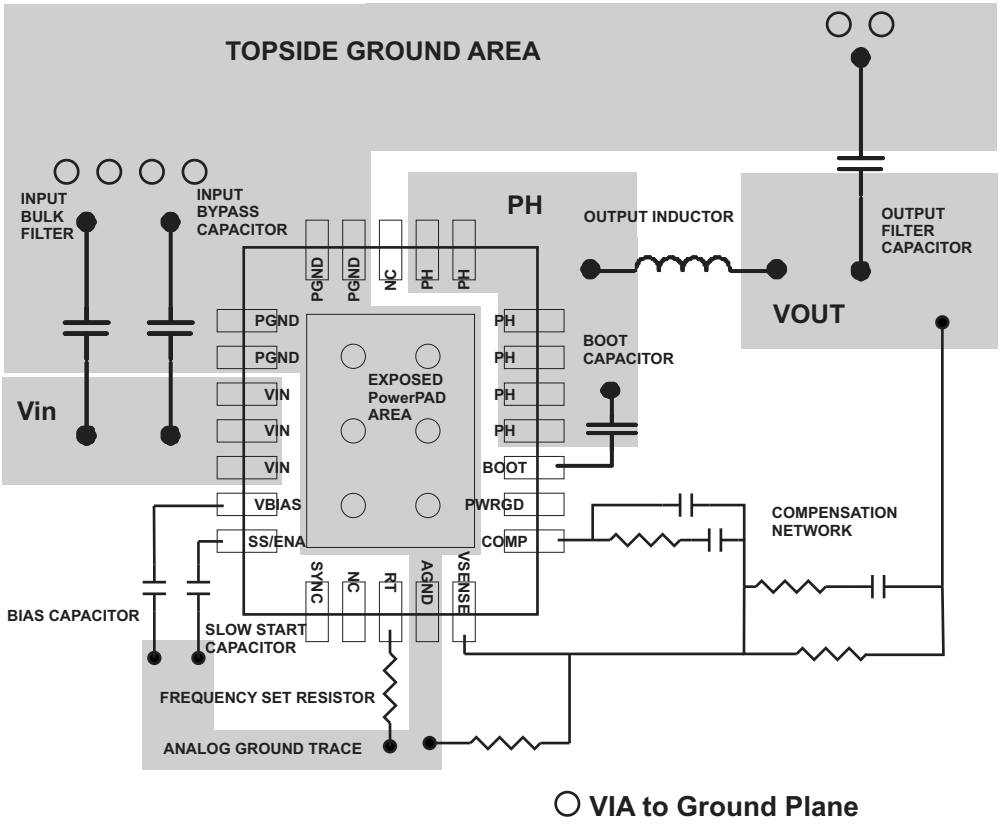


Figure 11. TPS54317 PCB Layout

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area additional vias located under the device package may be added to enhance thermal performance. The vias under the package, but not in the exposed thermal pad area, can be increased in size to 0.018.

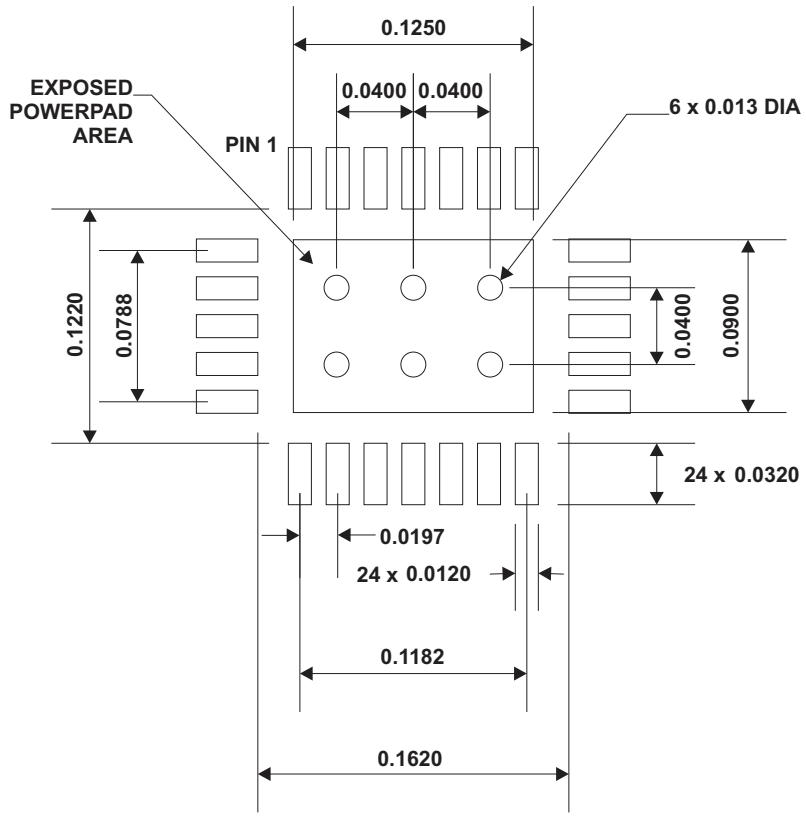


Figure 12. Recommended Land Pattern for 24-Pin QFN PowerPAD

PERFORMANCE GRAPHS

T_A = 25°C, f_s = 1.1 MHz, V_I = 3.3 V, V_O = 1.8 V (unless otherwise specified)

EFFICIENCY vs OUTPUT CURRENT

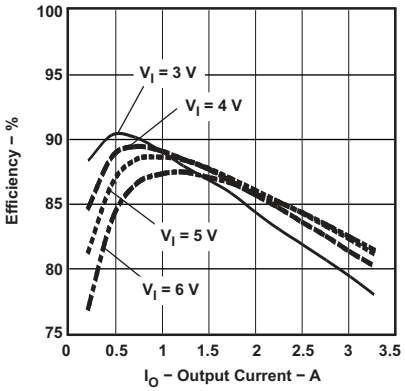


Figure 13.

OUTPUT VOLTAGE vs OUTPUT CURRENT

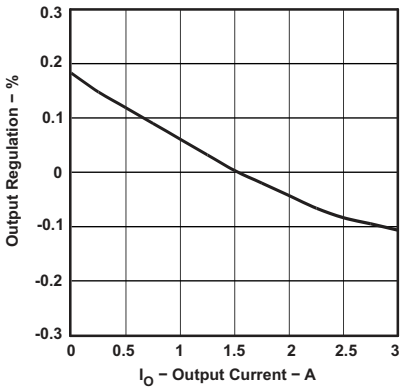


Figure 14.

LOOP RESPONSE

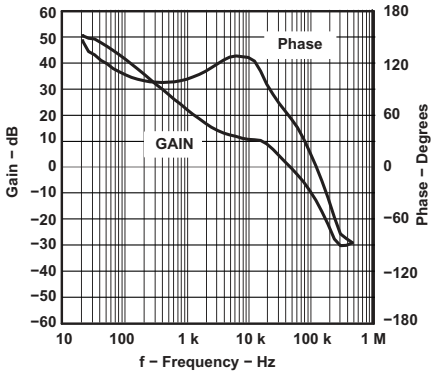


Figure 15.

OUTPUT RIPPLE VOLTAGE

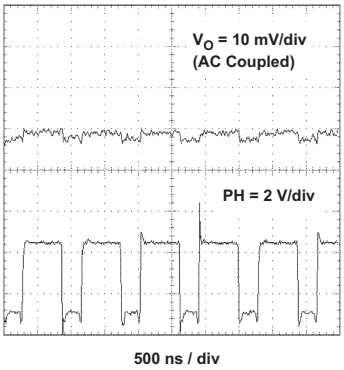


Figure 16.

LOAD TRANSIENT RESPONSE

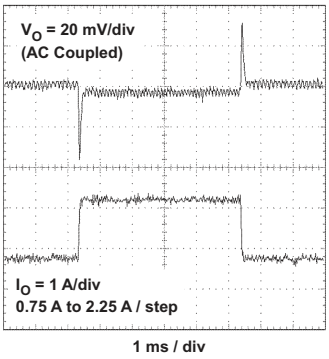


Figure 17.

SLOW-START TIMING

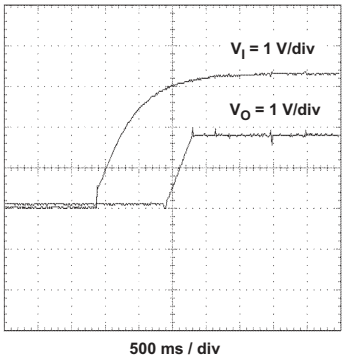
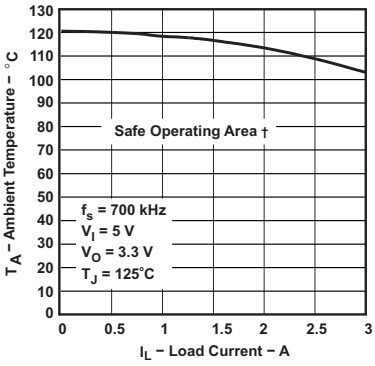


Figure 18.

AMBIENT TEMPERATURE vs LOAD CURRENT



† Safe operating area is applicable to the test board conditions listed in the dissipation rating table section of this data sheet.

Figure 19.

INPUT RIPPLE VOLTAGE

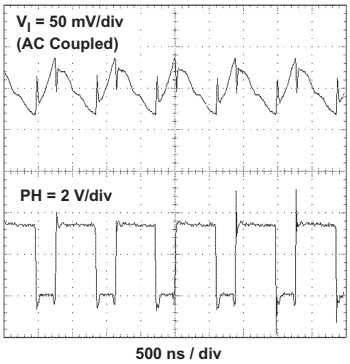


Figure 20.

LINE REGULATION vs INPUT VOLTAGE

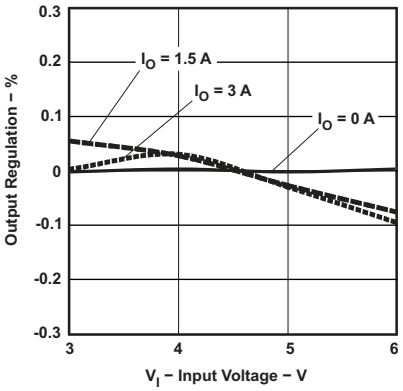


Figure 21.

DETAILED DESCRIPTION

Undervoltage Lock Out (UVLO)

The TPS54317 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions; first, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. To make sure the part is regulating using the internal V_{ref}, the SS/ENA pin must be pulled above 1.95 V typically, 2.2 V max. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (3)$$

The actual slow-start is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

Voltage Reference

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54317, since it cancels offset errors in the scale and error amplifier circuits.

Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 1600 kHz by connecting a resistor to the RT pin to ground and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY (MHz)} = \frac{51\ k}{R(\Omega) + 4.7\ k} \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 1600 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose an RT resistor that sets the free-running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations.

Table 1. Summary of the Frequency Selection Configurations

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 1600 kHz	Float	R = 27.4 k to 180 k
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

Error Amplifier

The high performance, wide bandwidth, voltage error amplifier sets the TPS54317 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse duration. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn off the high-side FET and turns on the low-side FET. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as V_{ref}. If the error amplifier output is low, the pwm latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54317 is capable of sinking current continuously until the C_O reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor, and consequently, the output current. This process is repeated each cycle in which the current limit comparator is tripped.

Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFETs is below 2 V. The high-side and low-side drivers are designed with a 300-mA source and sink capability to drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

Overcurrent Protection

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and differential amplifier, and comparing it to the preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown point.

Power Good (PWRGD)

The power good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

OUTPUT VOLTAGE LIMITATIONS

Due to the internal design of the TPS54317, there are both upper and lower output voltage limits for any given input voltage. Additionally, the lower boundary of the output voltage set point range is also dependent on operating frequency. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 90% and is given by Equation 5:

$$V_O max = 0.9 \times V_I min - I_O max \left[(-0.016 \times V_I min + 0.184) + RL \right] \quad (5)$$

Where:

$V_I$min = minimum input voltage

$I_O$max = maximum load current

RL = series resistance of the output inductor

Equation 5 assumes maximum on resistance for the internal high-side and low-side FETs.

The lower limit is constrained by the minimum controllable on time which may be as high as 150 ns. The approximate minimum output voltage for a given input voltage, operating frequency, and minimum load current is given in Equation 6:

$$V_O min = (150E\text{-}9 \times V_I max \times Fs \times 1.08) - I_o min \times \left[\left(\frac{-0.026}{3} \times V_i max + 0.111 \right) + RL \right] \quad (6)$$

Where:

V_I = maximum input voltage

Fs = programmed operating frequency

I_O = minimum load current

RL = series resistance of the output inductor

Equation 6 assumes nominal on resistance for the high-side and low-side FETs, and has an eight percent factor for variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked for proper functionality.

REVISION HISTORY

Changes from Original (November 2005) to Revision A **Page**

- Changed Abs Max Table - From: V_O - PH (transient) value -1.5 to 10 V To: PH (transient < 20 ns) value -2 to 10 V 2
- Added MAX value = 3V to the Electrical Characteristics - Start threshold voltage, UVLO 3
- Changed the Functional Block Diagram component value near pin BOOT From: 30 mΩ To: 59 mΩ 6
- Changed Figure 1 label From: Drain-Source On-State Resistabce - Ω To: Drain-Source On-State Resistabce - mΩ 7
- Changed Figure 2 label From: Drain-Source On-State Resistabce - Ω To: Drain-Source On-State Resistabce - mΩ 7

Changes from Revision A (February 2006) to Revision B **Page**

- Added Voltage to regulate using the internal V_{ref}, SS/ENA 4
- Added text to the first paragraph of the Slow-Start/Enable (SS/ENA) section - To make sure the part is regulating using the internal Vref, the SS/ENA pin must be pulled above 1.95 V typically, 2.2 V max. 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54317RHFR	NRND	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54317	
TPS54317RHFT	NRND	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54317	
TPS54317RHFTG4	NRND	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54317	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

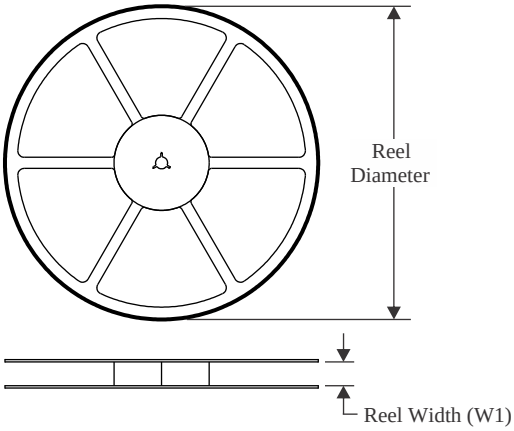
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

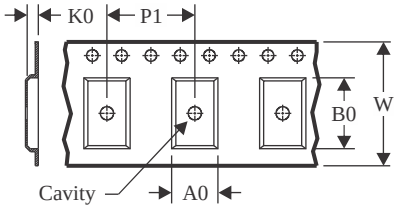
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

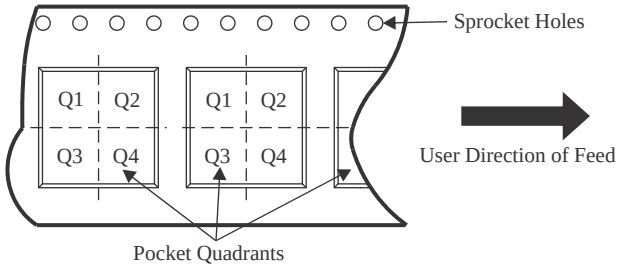


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

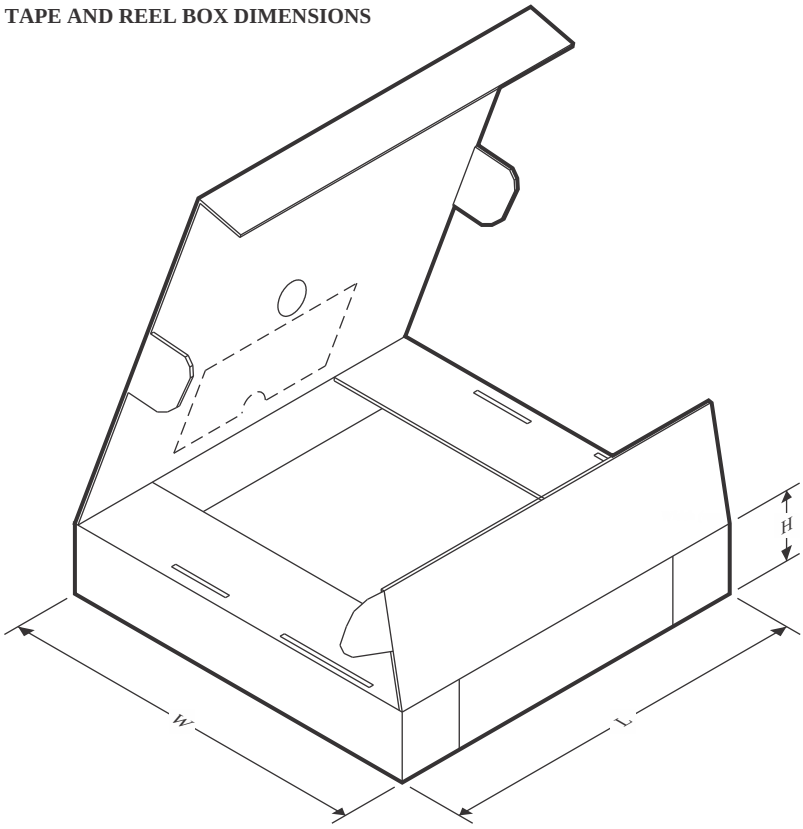
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54317RHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS54317RHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

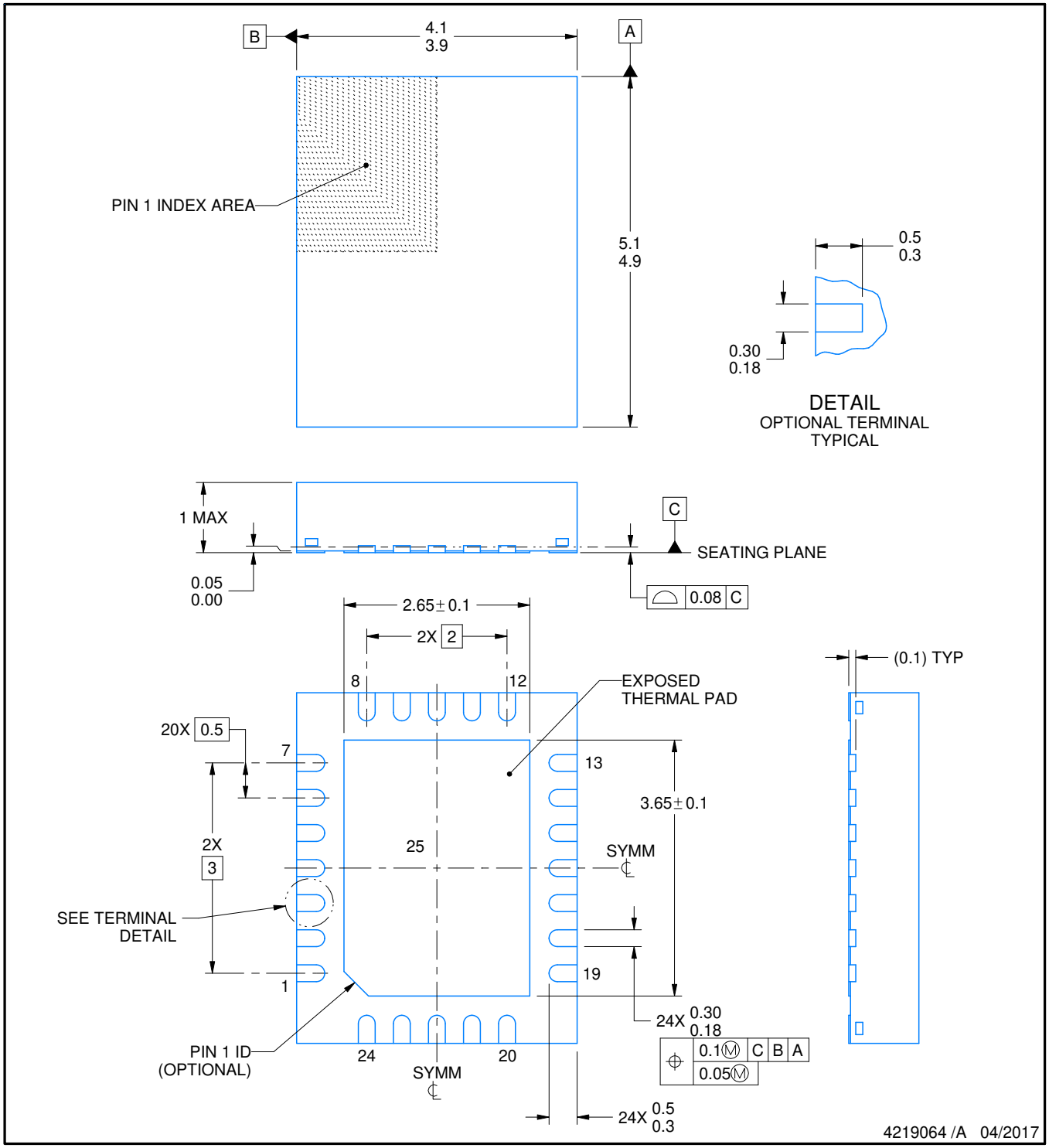
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54317RHFR	VQFN	RHF	24	3000	356.0	356.0	35.0
TPS54317RHFT	VQFN	RHF	24	250	210.0	185.0	35.0

RHF0024A

PACKAGE OUTLINE

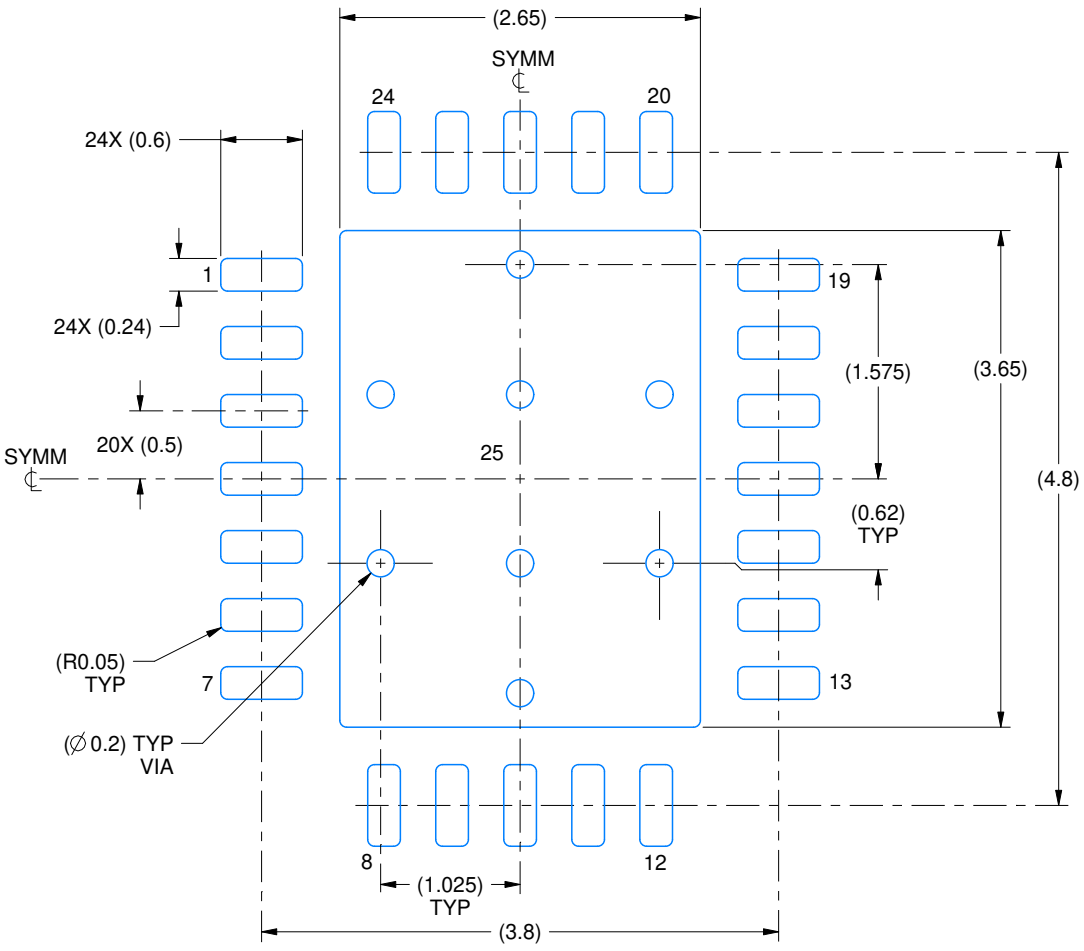
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

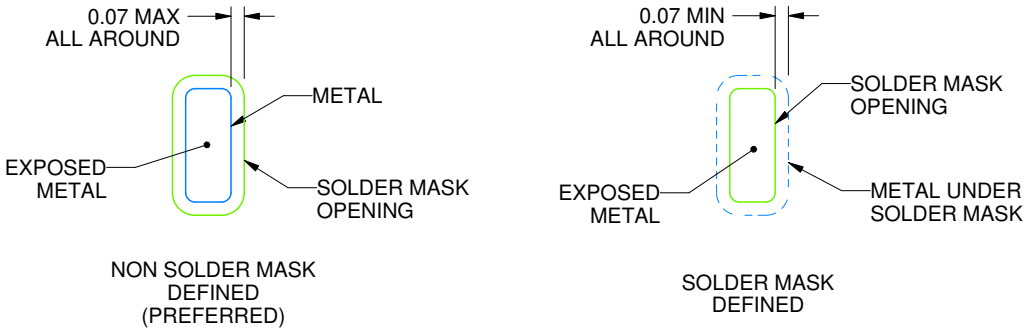


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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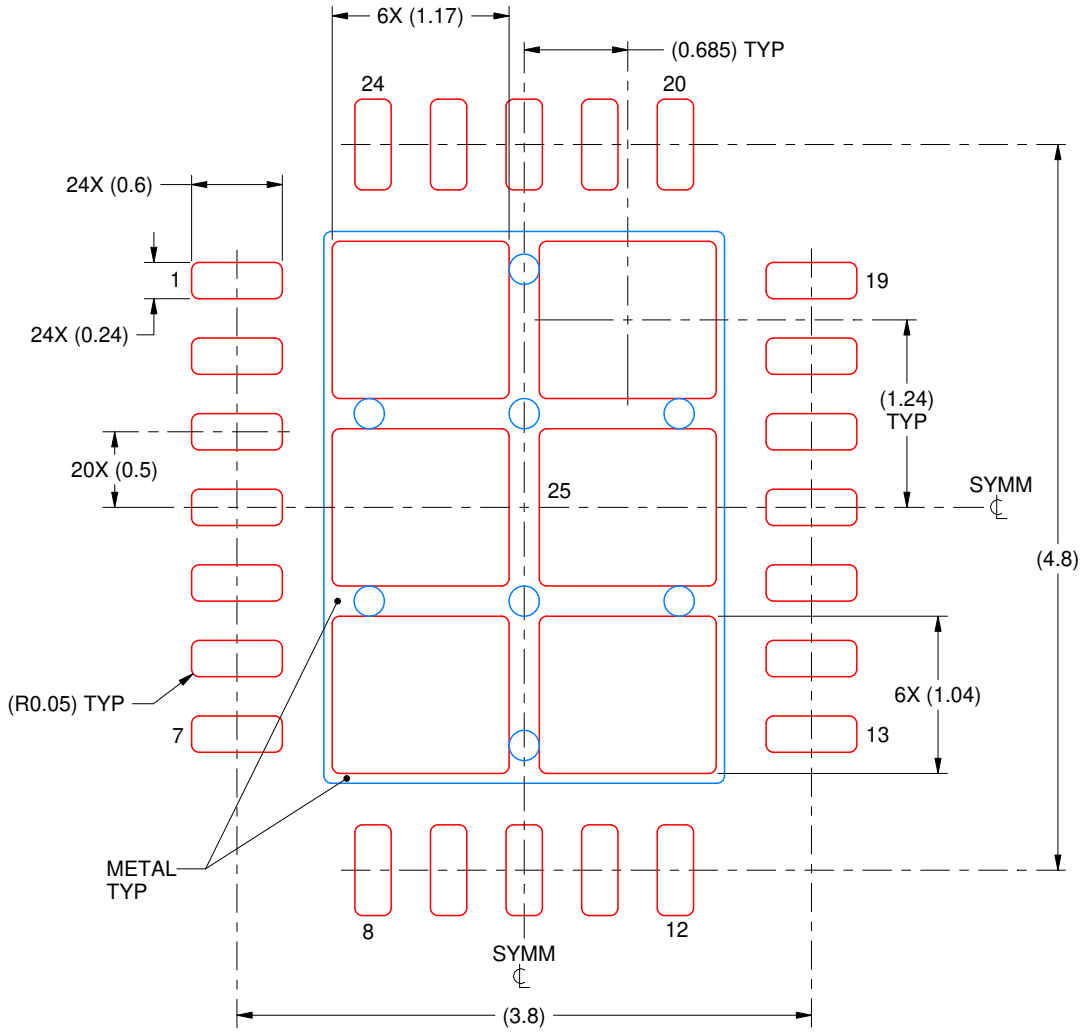
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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