SN65LVDS822RGZEVM Evaluation Module

User's Guide

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Introduction

The TI SN65LVDS822RGZEVM is a functional board design of a single device that implements an LVDS-to-CMOS deserializer. The EVM supports both 4:27 and 2:27 deserialization modes and output voltages from 1.8 to 3.3 V. This EVM acts as a hardware reference design for any implementation of the SN65LVDS822. Figure 1-1 shows the SN65LVDS822RGZEVM top layer layout.

Upon request, layout files for the EVM can be provided to illustrate techniques used to route the differential pairs, split power planes, place filters, and show methods to achieve length matching of critical signals.

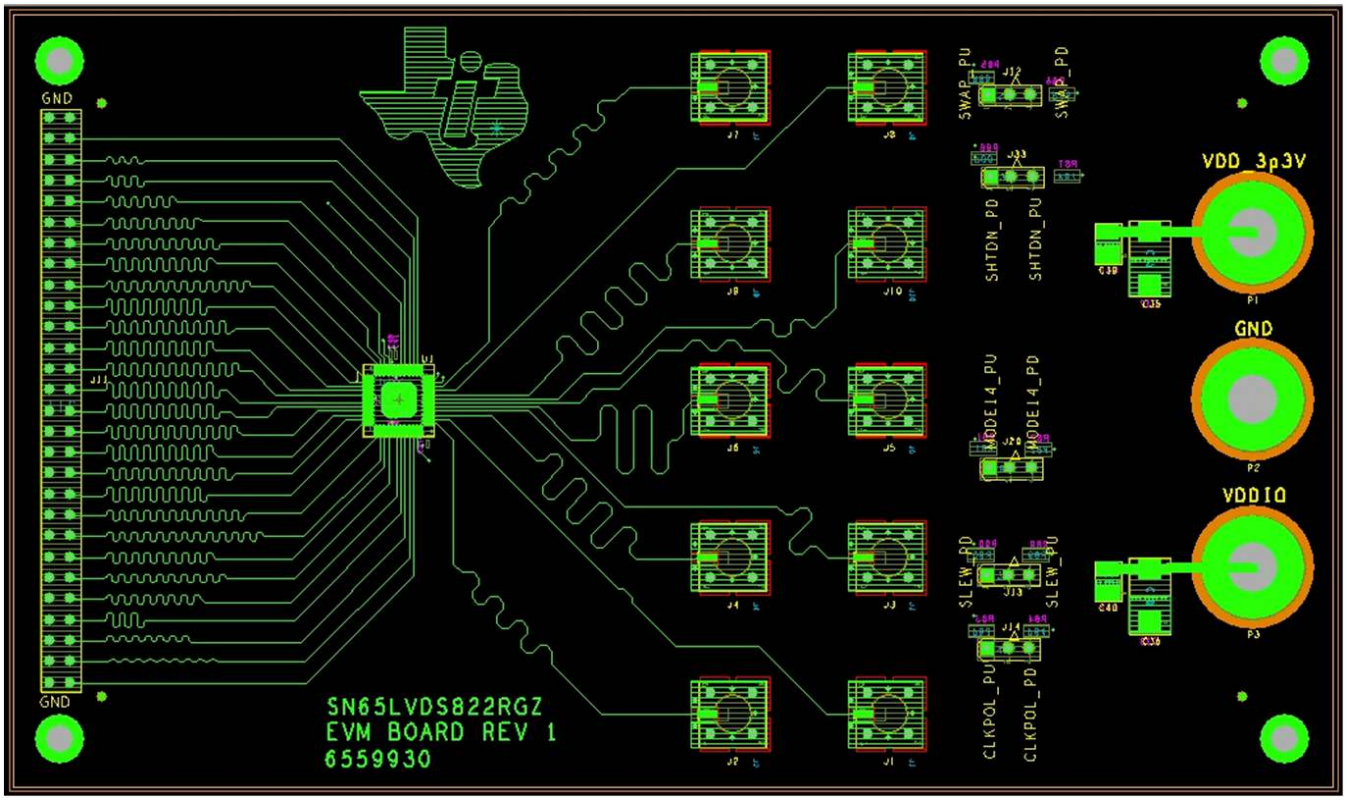

Figure 1-1. SN65LVDS822RGZEVM Top Layer Layout

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Hardware Overview

The four functional areas of the SN65LVDS822RGZEVM (EVM) board are explained in Section 2.1 through Section 2.4.

2.1 SN65LVDS822

The SN65LVDS822 on the EVM (U1 on the schematic) operates as an LVDS-to-CMOS deserializer. It has several unique features including three selectable CMOS output slew rates, CMOS output voltage support of 1.8 V to 3.3 V, a pinout swap option, integrated differential termination (configurable), and automatic low-power mode. The SN65LVDS822RGZEVM implements five low-voltage differential signal (LVDS) line receivers: four data lanes and one clock lane. The clock is internally multiplied by 7 or 14 (depending on pin MODE14), and used for sampling LVDS data. Each input lane contains a shift register that converts serial data to parallel. 27 total bits-per-clock period are deserialized and presented on the CMOS output bus.

A clock frequency range of 4 MHz to 54 MHz is supported in the standard 7× mode, which is used with LVDS data rates of 28 to 378 Mbps. The 14× mode supports 4 to 27 MHz, for LVDS data rates of 56 to 378 Mbps. The LVDS clock frequency always matches the CMOS output clock frequency. The device is designed to support resolutions as low as one-sixteenth VGA (160x120), and as high as 1024x600, with 60 frames per second and 24-bit color.

2.2 LVDS Connectors

The EVM is equipped with 10 SMA connectors, J1-J10, for the five LVDS line receivers. The LVDS lines are compatible with TI FlatLink™ transmitters such as the SN75LVDS83B, SN65LVDS93A, and the standard industry LVDS transmitters that comply with TIA/EIA-644-A.

2.3 Power Supply

The EVM operates from the power provided by two banana jack connectors (P1 and P3) common ground. The VDD terminal (P1) is connected to the main power supply to the SN65LVDS822 device and must be 3.3 V (±10%). The VDDIO terminal (P3) is connected to the power supply of the SN65LVDS822 CMOS outputs and must be in the range of 1.8 to 3.3 V.

2.4 CMOS Output Bus Connector

The EVM is equipped with a 56-pin header (J11) for the CMOS output bus. The even pins in the J11 connector are tied to GND and the odd pins are connected to the CMOS outputs lines. Table 2-1 shows the CMOS output and bit mapping and terminal assignments. Because some LCD panels require a reversed order, the SN65LVDS822 device is capable of reversing the output bus and simplifying PCB routing. When the pin is tied to high, the CMOS outputs are in normal order, otherwise the CMOS outputs are in reverse order.

Table 2-1. Bit Mapping and Terminal Assignments

Output signal	Signal	J11
D0	R0	1
D1	R1	3
D2	R2	5
D3	R3	7
D4	R4	9
D5	R5	11
D21	R6	13
D22	R7	15
D6	G0	17
D7	G1	19
D8	G2	21
D9	G3	23
D10	G4	25
D11	G5	27
D23	G6	29
D24	G7	31
D12	B0	33
D13	B1	35
D14	B2	37
D15	B3	39
D16	B4	41
D17	B5	43
D25	B6	45
D26	B7	47
D18	HS	49
D19	VS	51
D20	DE	53
CLK	CLK	55

Hardware Set Up

This chapter describes the jumper connections on the EVM.

3.1 Configuration Jumpers

Configuration inputs are read while the EVM is powered-on and are always in effect. Please refer to Appendix A for additional information about the EVM schematics. The switch definitions described in Section 3.1.1 to Section 3.1.5.

3.1.1 CLKPOL (J14)

The SN65LVDS822RGZEVM has the CLKPOL terminal to determine the clock polarity. If the CLKPOL jumper is set on the power-down position, a pull-down resistor is connected to the terminal to indicate that D[26:0] is valid during the CLKOUT falling edge. If the CLKPOL jumper is set on the power-up position, a pull-up resistor is connected to the terminal to indicate that D[26:0] is valid during the CLKOUT rising edge. TI does not recommend leaving this jumper floating.

3.1.2 SLEW (J13)

The SN65LVDS822RGZEVM has a SLEW terminal to set the CMOS output slew rate. If the SLEW jumper is set on the power-down position, a pull-down resistor is connected to the terminal to set the CMOS outputs to the slowest rise and fall time. If the SLEW jumper is left floating, the terminal will be floating too, setting the CMOS outputs to the medium rise and fall time. Finally, if the SLEW jumper is set on power-up position, a pull-up resistor is connected to the terminal to set the CMOS outputs to the fastest rise and fall time.

3.1.3 MODE14 (J20)

The SN65LVDS822RGZEVM has a MODE14 terminal to set the number of LVDS serial bits per lane per clock period. If the MODE14 jumper is set in power-down position, a pull-down resistor is connected to the terminal to indicate that all the data lanes (A0 – A3) are used (7 bits per lane per clock period). If the MODE14 jumper is set in power-up position, a pull-up resistor is connected to the terminal to indicate that only lanes A0 and A2 are used (14 bits per-lane per-clock period).

3.1.4 SHTDN (J33)

The SN65LVDS822RGZEVM enters in shutdown mode with a low voltage applied to the terminal SHTDN. In this mode, all CMOS outputs are driven low. If the SHTDN jumper is set in power-down mode, a pull-down resistor is connected to the terminal and the device enters in shutdown mode, otherwise the device works normally.

3.1.5 SWAP (J12)

The SN65LVDS822RGZEVM has a SWAP terminal that selects the CMOS output pinout and also controls differential input termination. If the SWAP jumper is set on power-down position, a pull-down resistor is connected to the terminal to set the CMOS outputs to the default pinout and to set the differential input termination connected. If the SWAP jumper is left floating, the CMOS outputs are set to the default pinout and the differential inputs termination are disconnected (requires external termination). If the SWAP jumper is set on power-up position, a pull-up resistor is connected to the terminal to set an output swapped pinout and to set the differential input termination connected.

EVM Installation

Install the EVM by following steps 1 – 7:

1. Configure the jumpers in the SN65LVDS822RGZEVM as follows:

CLKPOL	pull-up
SLEW	pull-up
MODE14	pull-down
SHTDN	pull-up
SWAP	pull-down

2. Connect the serial outputs of the LVDS transmitter (for example, the SN65LVDS83B) to the serial inputs of the SN65LVDS822RGZEVM as shown in Table 4-1.

Table 4-1. LVDS Inputs

LVDS Transmitter	SN65LVDS822RGZEVM
A0P	J1
A0N	J2
A1P	J3
A1N	J4
A2P	J5
A2N	J6
A3P	J7
A3N	J8
CLKp	J9
CLKn	J10

3. Configure the power supply to 3.3 V. Turn off the power supply.
4. Connect all the ground jacks of both the LVDS transmitter and the SN65LVDS822RGZEVM and tie them to the ground terminal at the power supply.
5. Connect all the VCC jacks of both the LVDS transmitter and SN65LVDS822RGZEVM and tie them to the V+ terminal at the power supply.
6. Connect the oscilloscope's probes to both pin 1 and pin 55 in the EVM J11 connector. The ground of the probes can be connected to every even pin in the EVM J11 connector.
7. Turn on the power supply.

SN65LVDS822RGZEVM Schematics

Figure A-1 through Figure A-3 contain the schematics for this EVM.

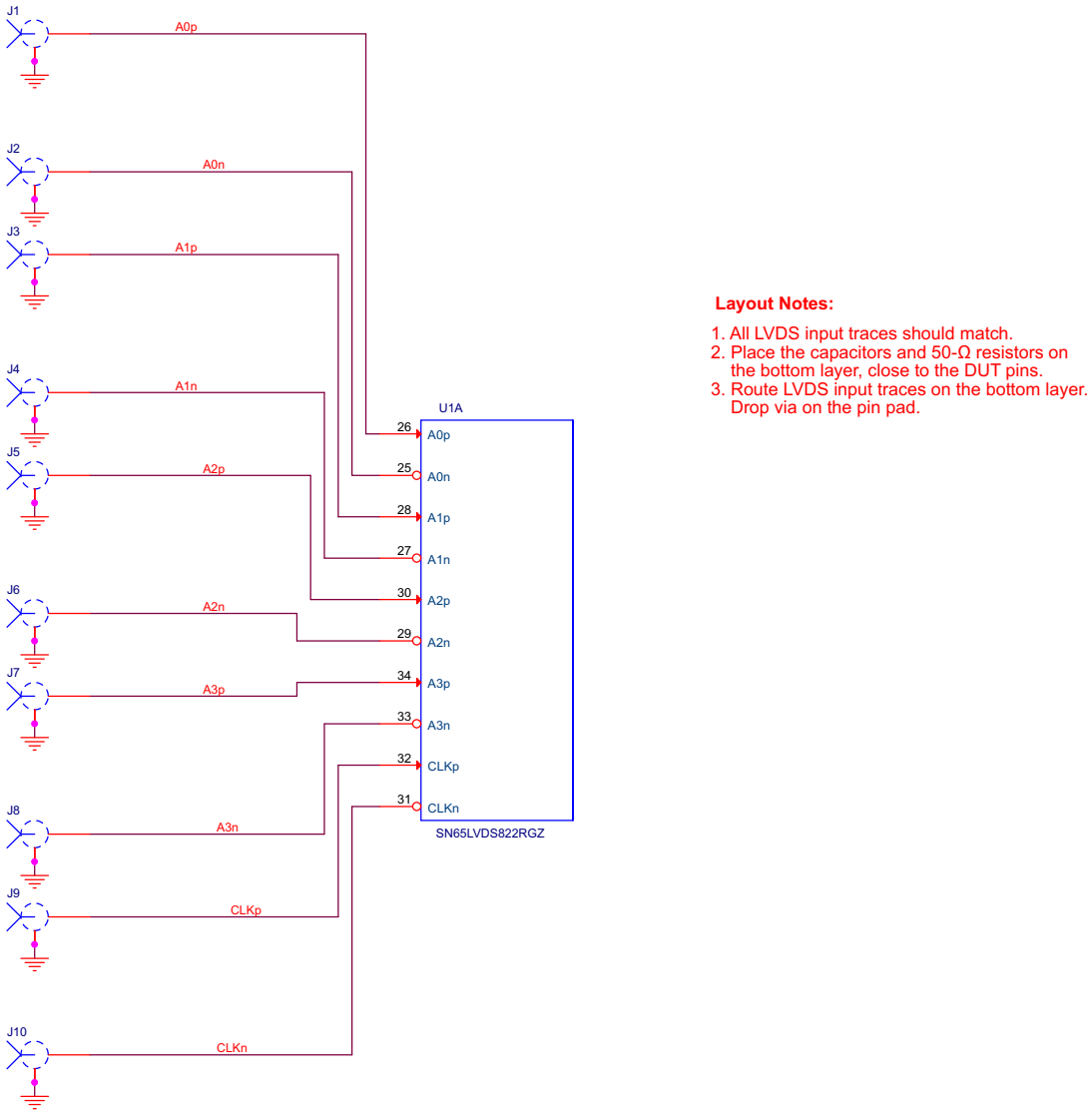


Figure A-1. LVDS Inputs

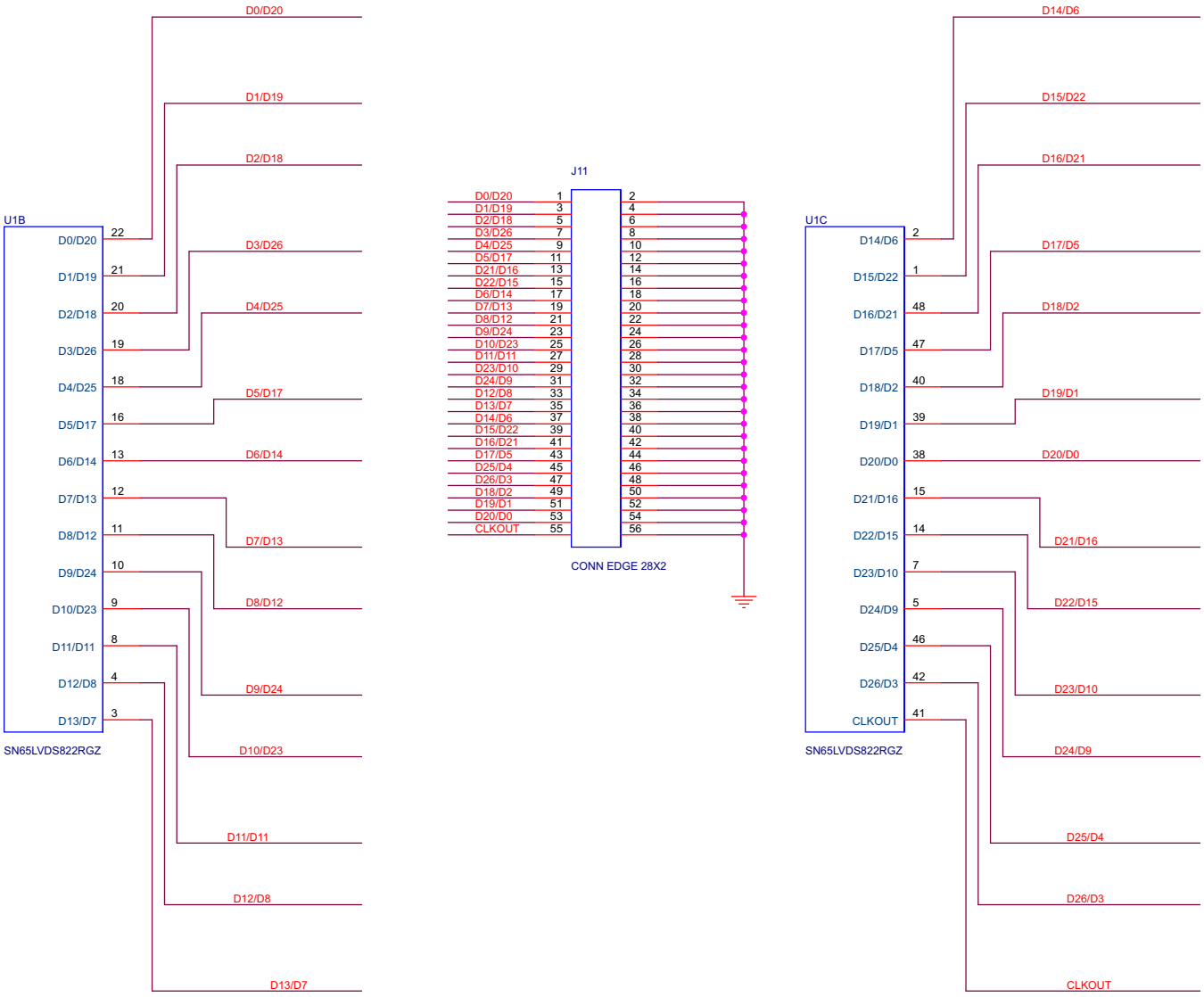


Figure A-2. CMOS Output Bus

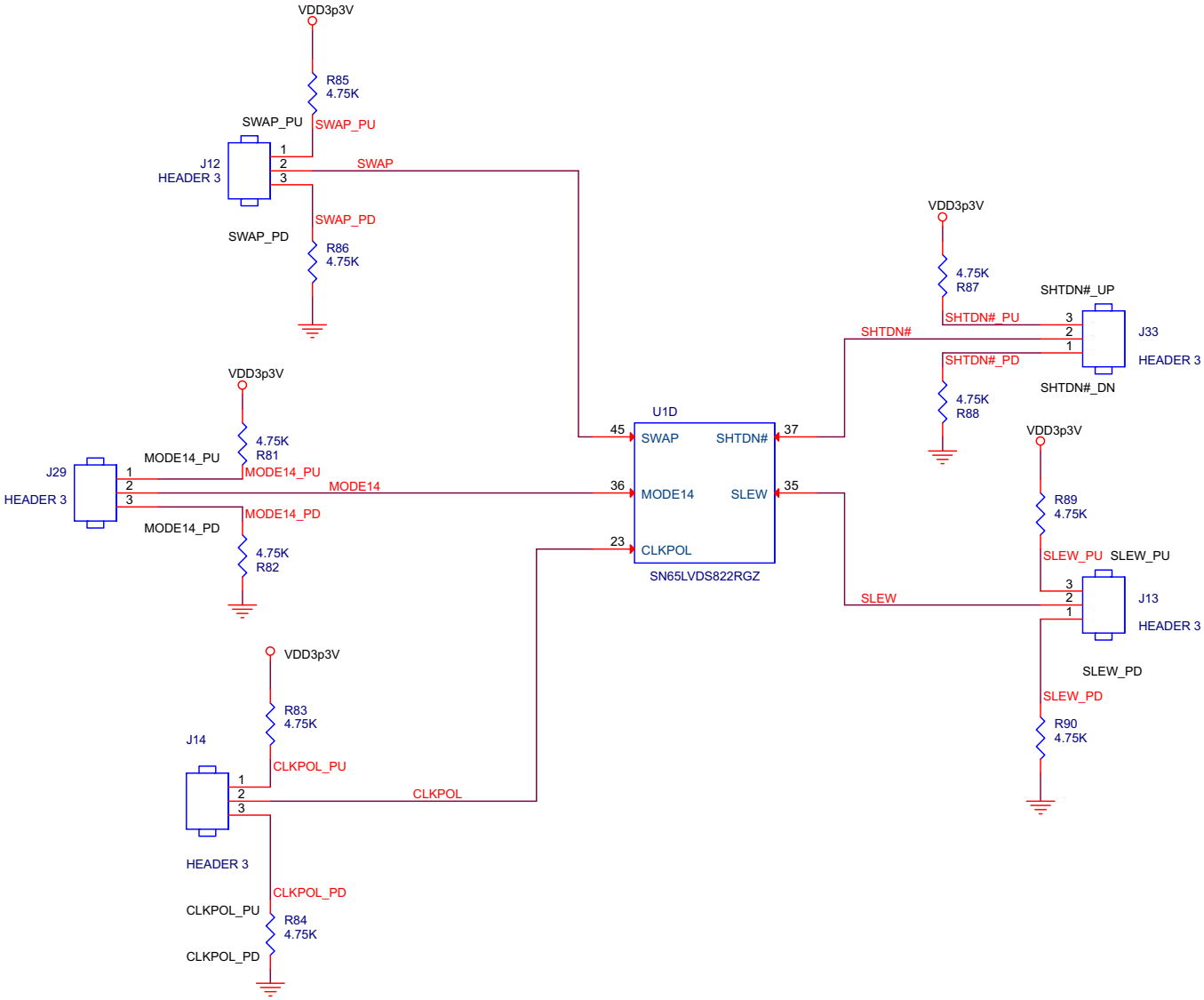
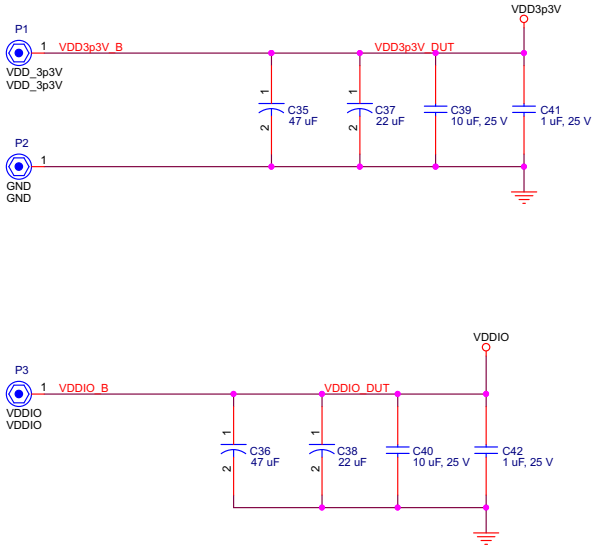


Figure A-3. Configuration Jumpers



Layout Notes:

1. Place banana jacks in two rows, P1 and P3 in the first row and P2 and P4 in the second row, 750 mils apart (center-to-center).
2. Place TI logo on top side metal.
3. Add mounting holes.

Layout Notes:

1. Place these caps near DUT on the bottom side of the board.
2. Each group should share one via to the power pin, but should not share via to GND.
3. Minimize the trace length between the power pin and caps.
4. Connect capacitors to GND through thermal pad.

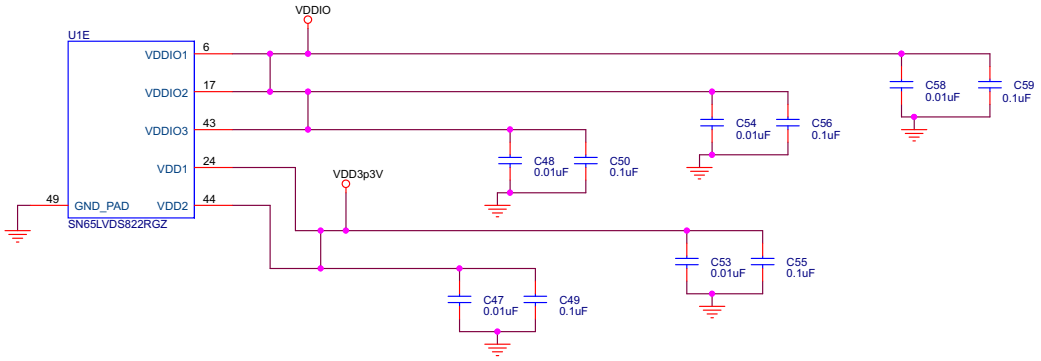


Figure A-4. Power

SN65LVDS822RGZEVM Bill of Materials

Table B-1 contains the BOM for the EVM.

Table B-1. SN65LVDS822RGZEVM BOM

Item	Qty	Reference	Part	Manufacturer	Part Number	Digikey Part Number	Pkg
1	2	C35,C36	47 uF	Vishay	293D476X9016D2TE3	718-1090-2-ND	7343
2	2	C37,C38	22 uF	Vishay	293D226X9025D2TE3	718-1070-2-ND	7343
3	2	C39,C40	10 uF, 25 V	AVX	TAJB106K025RNJ	478-5257-2-ND	1210
4	2	C41,C42	1 uF, 25 V	Kemet	C1210C105K3NACTU	399-5737-2-ND	1210
5	5	C47,C48,C53,C54,C58	0.01uF	TDK	C0603X5R0J103M	445-4704-1-ND	201
6	5	C49,C50,C55,C56,C59	0.1uF	TDK	C0603X5R0J104M	445-4711-1-ND	201
7	10	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10	32K141-40ML5	Rosenberger	32K141-40ML5		T/H_SMT SMA
8	1	J11	2 x 28	Samtec	HTSW-150-07-G-S	HTSW-150-07-G-S-ND	0.1x0.1"
9	5	J12,J13,J14,J29,J33	1 x 3	Samtec	HTSW-150-07-G-S	HTSW-150-07-G-S-ND	0.1x0.1"
10	3	P1,P2,P3	Banana Jack-Metal	Emerson Network	108-0740-001	J147-ND	4mm
11	10	R81,R82,R83,R84,R85,R86,R87,R88,R89,R90	4.75K	Vishay	CRCW06034K75FKEA	541-4.75KHCT-ND	603
12	1	U1	SN65LVDS822RGZR	Texas Instruments	SN65LVDS822RGZR		48-QFN

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