

CBTL02GP023

5 Gbps rail-to-rail low insertion loss switch

Rev. 2 — 14 August 2017

Product data sheet

1. General description

The CBTL02GP023 is a one port high performance 5 Gbps rail-to-rail low insertion loss 4x SPST switch chip optimized to interface USB3.0 signals with high voltage (e.g. USB2 signals) off isolation. It supports 5 Gbps USB3.0 signals and large swing USB2 or UART signals in dongle or plug applications. It also can be used as a general purpose 5 Gbps rail-to-rail low insertion loss switch chip in other applications.

The common mode voltage of all the input or output pins have wide common mode range from 0 V to VDD.

CBTL02GP023 is available in 1.5 mm × 2.1 mm × 0.32 mm DHX2QFN14 package with 0.4 mm pitch.

2. Features and benefits

- One port (two differential channels) 5 Gbps rail-to-rail low insertion loss switch
- Differential channels:
 - ◆ Low insertion loss: -1.5 dB at 2.5 GHz; -1 dB at 100 MHz
 - ◆ Low return loss: < -15 dB at 2.5 GHz
 - ◆ Low ON-state resistance: 11 Ω (typ)
 - ◆ Bandwidth: 7 GHz (typ)
 - ◆ Low off-state isolation: -16 dB at 2.5 GHz; -40 dB at 100 MHz
 - ◆ Low DDNEXT crosstalk: < -35 dB at 2.5 GHz and 500 MHz
 - ◆ VIC common mode input voltage: 0 to VDD
 - ◆ Differential input voltage VID: 1.2 V (Max)
 - ◆ Intra-pair skew: 6 ps (typ)
- VDD Power Supply voltage range in the dongle or plug:
 - ◆ 2.7 V (min) to 3.5 V (max)
- Low active current consumption: 500 μ A (max)
 - ◆ Minimum disable current (ENH = LOW): 12 μ A (max)
- Back current protection on all I/O pins
- Patent pending high performance analog pass-gate technology
- All channels support rail-to-rail input voltage
- Small DHX2QFN14 1.5mm × 2.1 mm × 0.32 mm package with 0.4 mm pitch
- ESD protection exceeds 2000V HBM per JDS-001-2012 and 750 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: -20 °C to +85 °C



3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTL02GP023	23	DHX2QFN14	Plastic, super thin quad flat package; no leads; 14 terminals; body 1.5 mm x 2.1 mm x 0.32 mm; 0.4 mm pitch	SOT1458-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTL02GP023	CBTL02GP023HOZ	DHX2QFN14	REEL 13" Q1/T1 *STANDARD MARK SBB	20000	T _{amb} = -20 °C to +85 °C

4. Block diagram

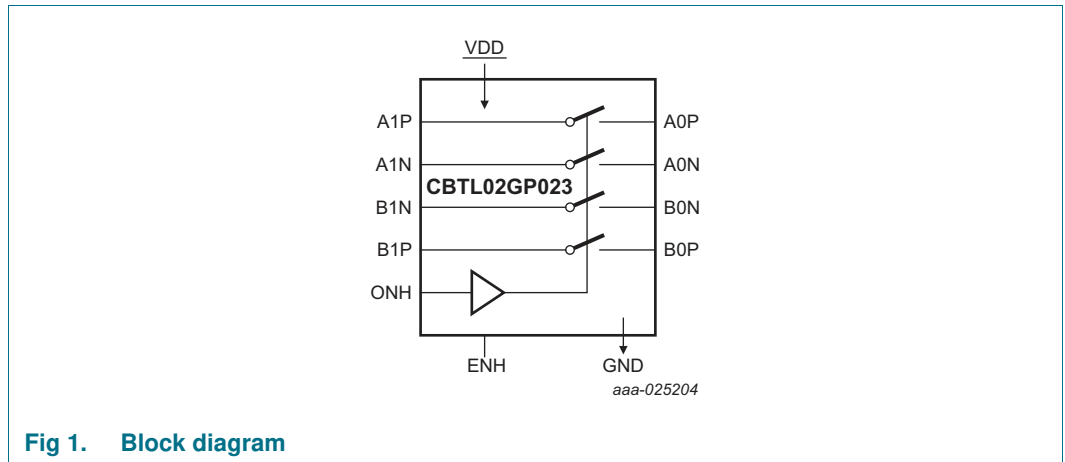


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

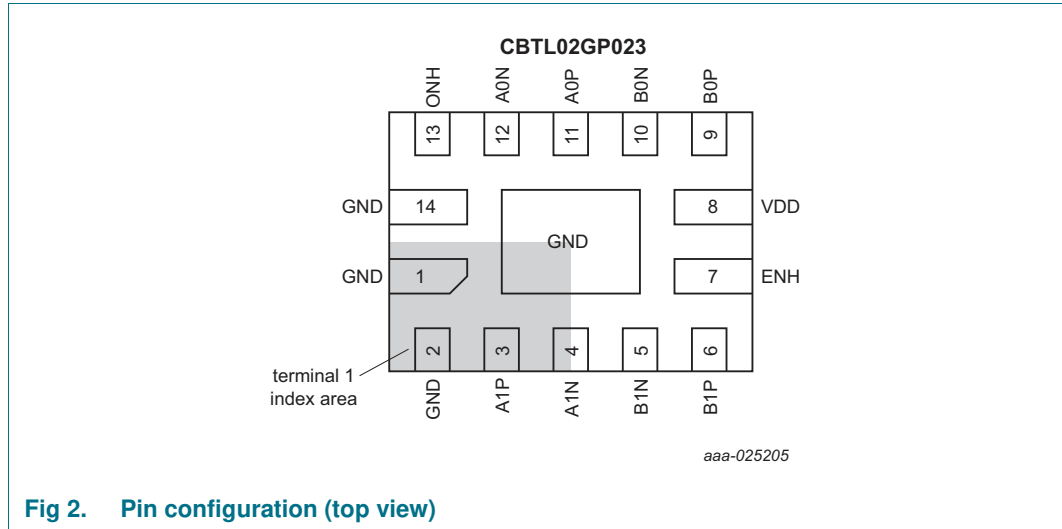


Fig 2. Pin configuration (top view)

Refer to [Section 10 “Package outline”](#) for package related information.

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Data path signals			
A1P	3	differential I/O	USB3.0 differential signals for A port
A1N	4	differential I/O	
A0N	12	differential I/O	USB3.0 differential signals for A port (P and N is crossed for A port)
A0P	11	differential I/O	
B1N	5	differential I/O	USB3.0 differential signals for B port
B1P	6	differential I/O	
B0N	10	differential I/O	USB3.0 differential signals for B port (P and N is a flow through differential path for B port)
B0P	9	differential I/O	
Control signal			
ENH	7	control input	When HIGH, enables switches. When LOW, whole chip is powered down
ONH	13	control input	When HIGH, all switches are turned on. When LOW, all switches are OFF, but the control circuit is still working to improve isolation performance
Power supply			
VDD	8	power	Power supply range between 2.7 V and 3.5 V
Ground connection			
GND	1, 2, 14, center pad	ground	0 V

6. Functional description

Refer to [Figure 1 “Block diagram”](#) of CBTL02GP023.

ENH pin is used to power down the switches. When ENH is low, the switches are in high impedance sleep mode. ONH can also be used to control the switch with better OFF isolation performance.

Table 4. Enable control table

ENH	Switch state	Max current consumption
0	OFF	12 μ A
1	ON	500 μ A

Table 5. ONH and ENH control table

ONH	ENH	Switch state	Max current	OFF isolation at 2.5 GHz
0	0	OFF	12 μ A	-11 dB
0	1	OFF	500 μ A	-16 dB
1	0	OFF	12 μ A	-11 dB
1	1	ON	500 μ A	NA

7. Limiting values

Table 6. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage	[2]	-0.3	+4.6	V
V _I	input voltage of control pins	[2]	-0.3	+5.5	V
V _{IO}	voltage of I/O pins of switches	[2]	-0.3	+4.6	V
T _{stg}	storage temperature		-65	+150	°C
V _{ESD}	electrostatic discharge voltage	HBM [3]	-	2000	V
		CDM [4]	-	750	V

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, except differential voltages, are with respect to network ground terminal.

[3] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[4] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

8. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage	3.3 V supply option	2.7	-	3.5	V
V _I	input voltage	CMOS inputs	-0.3	-	+5.5	V
		MUX I/O pins	-0.3	-	+3.5	V
T _{amb}	ambient operating temperature	operating in free air	-20	-	+85	°C

9. Characteristics

9.1 Device general characteristics

Table 8. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD}	supply current	VDD = 3.5 V	-	-	0.5	mA
P _{cons}	power consumption	VDD = 3.5 V	-	-	1.75	mW
P _{sleep}	sleep mode power consumption	ENH = 0	-	-	42	μW
T _{Startup}	start-up time	supply voltage valid and ENH goes HIGH to channel specified operating characteristics	-	220	500	μs
T _{switch}	5 Gbps rail-to-rail low insertion loss switching time	ONH goes from LOW to HIGH	-	2	10	μs
		ONH goes from HIGH to LOW	-	200	1000	μs

9.2 Switch channel characteristics

Table 9. Dynamic and static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDIL	differential insertion loss	Channel is off with ENH = HIGH and ONH = LOW				
		f = 2.5 GHz	-	-16	-	dB
		f = 100 MHz	-	-40	-	dB
		Channel is off with whole chip disabled ENH = LOW and ONH = X (don't care)				
		f = 2.5 GHz	-	-11	-	dB
		f = 100 MHz	-	-30	-	dB
		Channel is on with ONH = HIGH and ENH = HIGH				
		f = 2.5 GHz	-	-1.5	-	dB
		f = 100 MHz	-	-1	-	dB
DDRL	Differential Return Loss	f = 2.5 GHz	-	-15	-	dB

Table 9. Dynamic and static characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDNEXT	High Speed Tx to Rx. Differential near-end crosstalk	A1P/N to B1P/N or A0P/N to B0P/N				
		f=-2.5GHz	-	-20	-	dB
DDFEXT	High Speed Tx to Rx. Differential far-end crosstalk	A1P/N to B0P/N or A0P/N to B1P/N				
			-	-20	-	dB
R _{on}	ON-state resistance	V _{DD} = 2.7 V; V _I = 2.2 V; I _I = 10 mA	-	11	15	Ω
C _{in}	Input capacitance	V _{DD} = 2.8 V; V _I = 1.4 V; at 10 MHz	-	3	-	pF
B _{-3dB}	Bandwidth	V _{IC} = 0 V	-	7	-	GHz
T _{pd}	Propagation delay	From input to output pairs	-	70	-	ps
T _{sk(diff)}	Differential skew time	Intra-pair	-	6	-	ps
V _I	Input voltage	for all switch ports	0	-	3.5	V
V _{IC}	Common-mode input voltage	for all switch ports	0	-	VDD	V
I _{LIH}	High level input leakage current	V _{DD} =MAX; V _I =V _{DD}	-	-	±1	μA
I _{LIL}	Low level input leakage current	V _{DD} =MAX; V _I =GND	-	-	±1	μA

9.3 Control signals characteristics

Table 10. ENH input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	HIGH-level input voltage	CMOS inputs	0.7* VDD	-	-	V
V _{IL}	LOW-level input voltage	CMOS inputs	-	-	0.3* VDD	V
I _{LI}	Input leakage current	Measured with input at V _I =VDD and V _I =0V			1	μA

Table 11. ONH input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS input	2.15	-	-	V
V_{IL}	LOW-level input voltage	after glitch filter to debounce noise	-	-	0.5	V
I_{LI}	Input leakage current	Measured with input at $V_{IH} = V_{DD}$ and $V_{IL} = 0$ V	-	-	0.1	μ A
t_{degl}	deglitch time	time from ONH signal going LOW and staying LOW below V_{IL} level	-	200	1000	μ s

[1] The I_{LI} value is guaranteed by design and bench test

10. Package outline

DHX2QFN14: plastic dual in-line compatible thermal exchanged super thin quad flat package; no leads; 14 terminals; body 1.5 x 2.1 x 0.32 mm

SOT1458-1

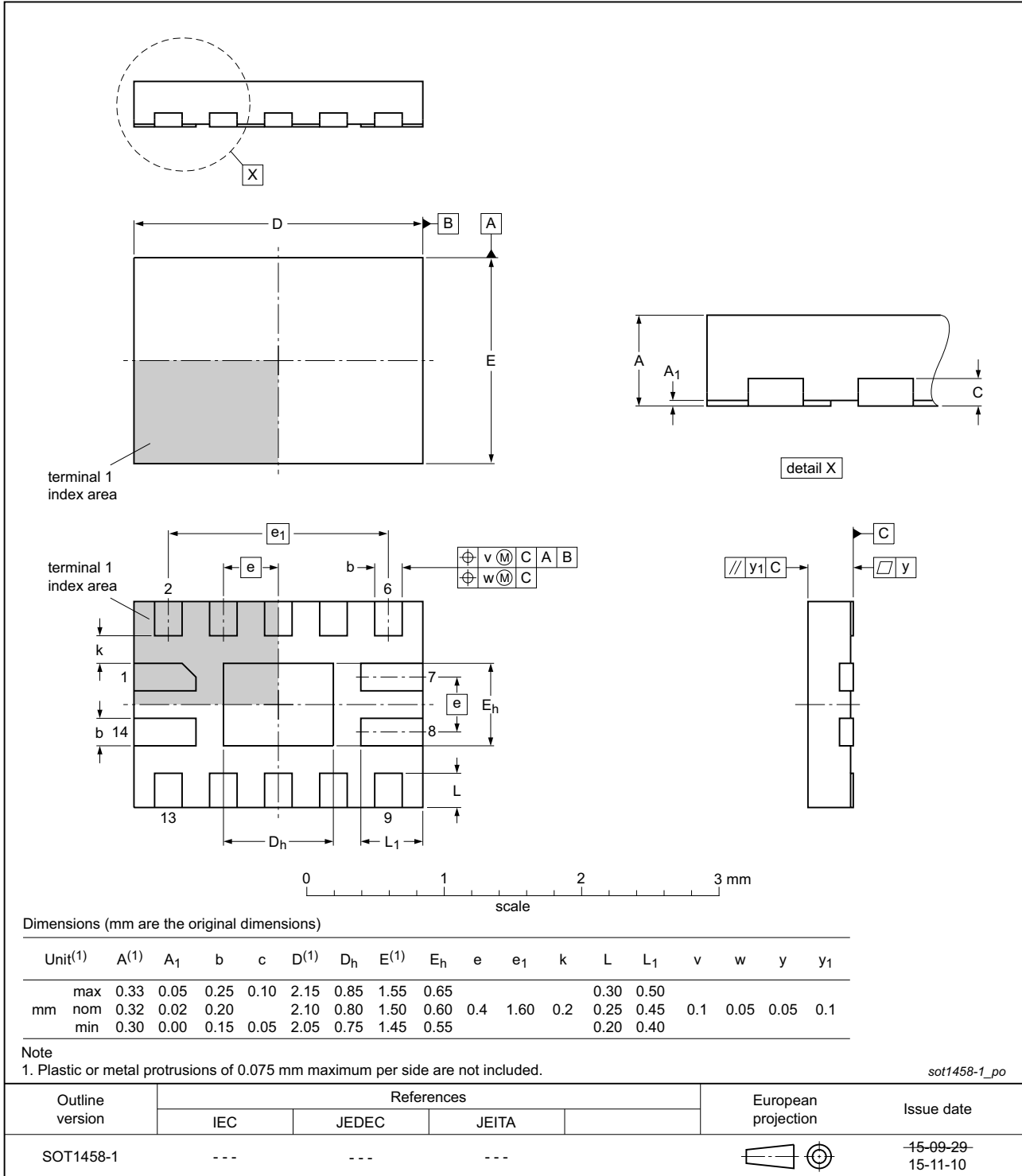


Fig 3. Package outline SOT1458-1 (DHX2QFN14)

11. Packing information

11.1 DHX2QFN14; Reel pack, SMD, 13"; Q1/T1 standard product orientation; Orderable part number ending ,431 or Z; Ordering code (12NC) ending 431

11.1.1 Packing method

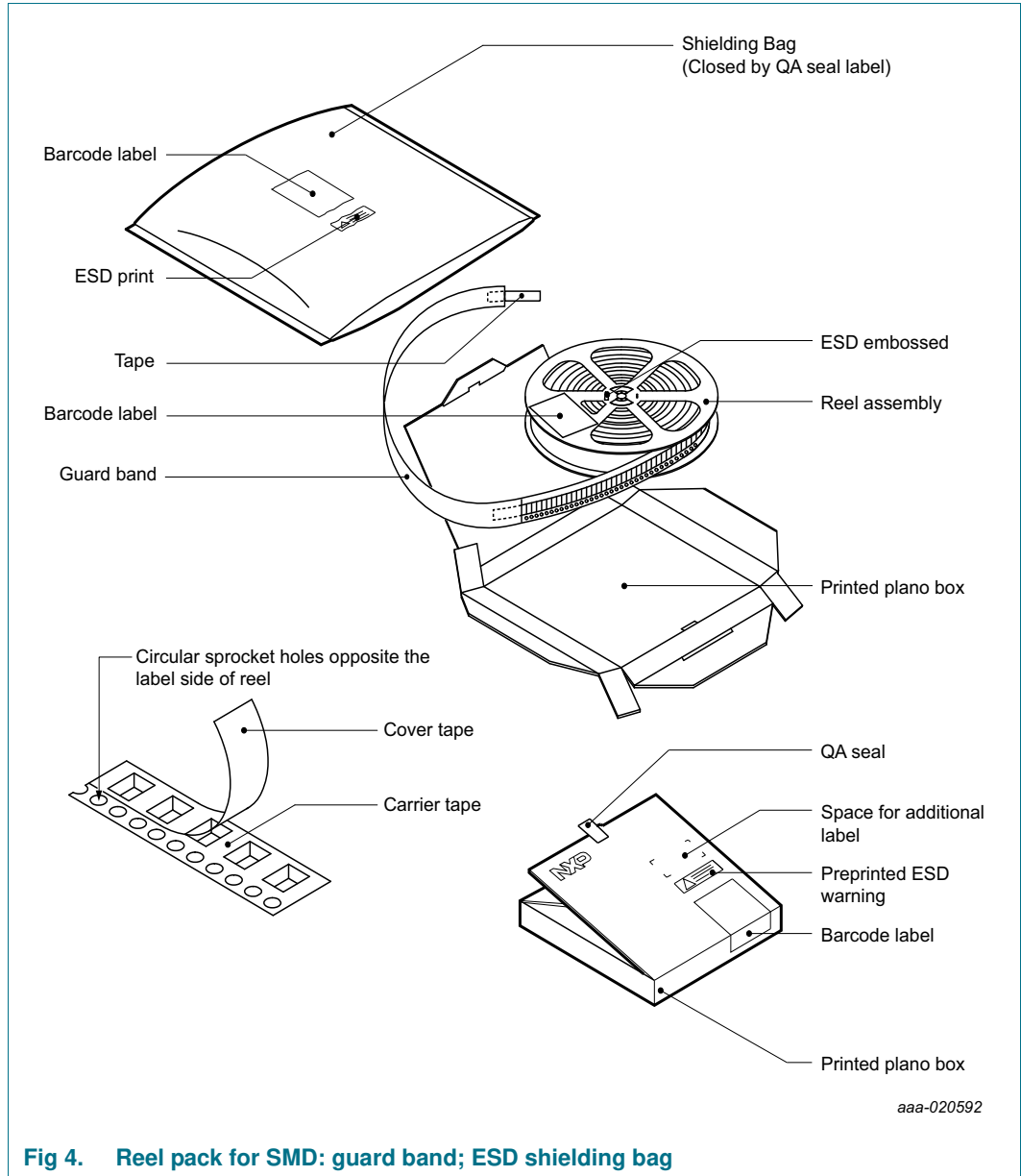


Table 12. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
330 × 8	20000	1	342 × 338 × 25

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.

View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

11.1.2 Product orientation



Fig 5. Product orientation in carrier tape

11.1.3 Carrier tape dimensions

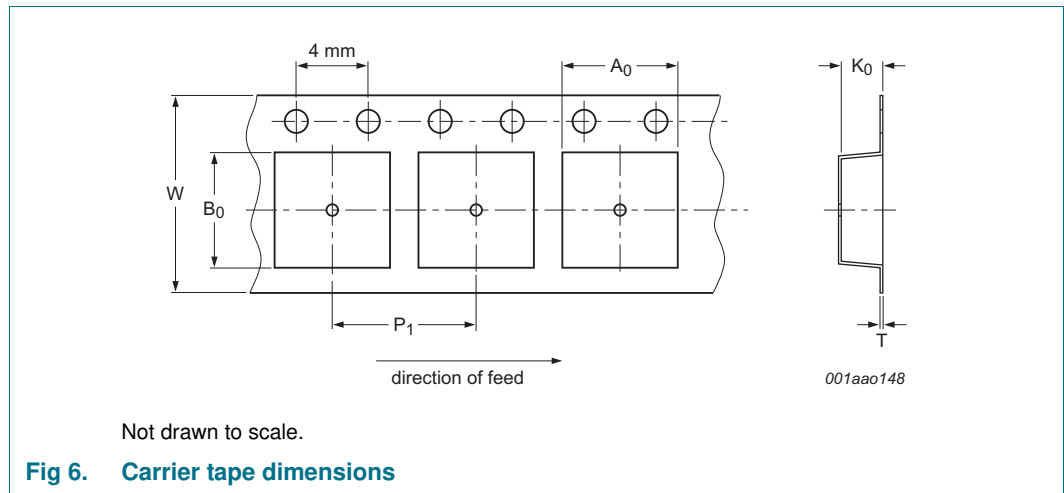


Fig 6. Carrier tape dimensions

Table 13. Carrier tape dimensions

In accordance with IEC 60286-3.

A ₀ (mm)	B ₀ (mm)	K ₀ (mm)	T (mm)	P ₁ (mm)	W (mm)
1.80 ± 0.05	2.40 ± 0.05	0.45 ± 0.05	0.25 ± 0.03	4.0 ± 0.10	8.0 ± 0.1

11.1.4 Reel dimensions

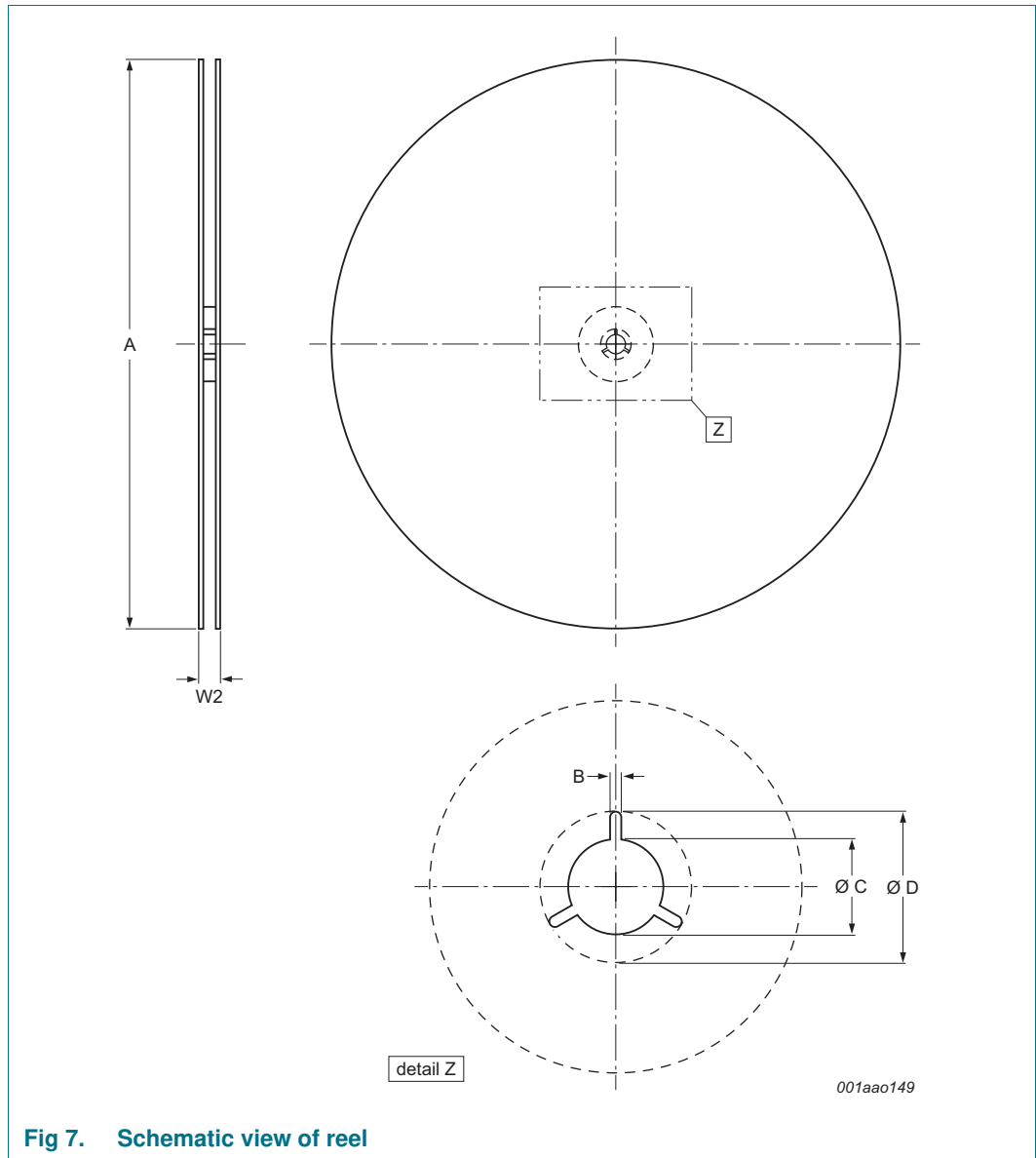


Fig 7. Schematic view of reel

Table 14. Reel dimensions
In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
330	14.4	1.5	12.8	20.2

11.1.5 Barcode label

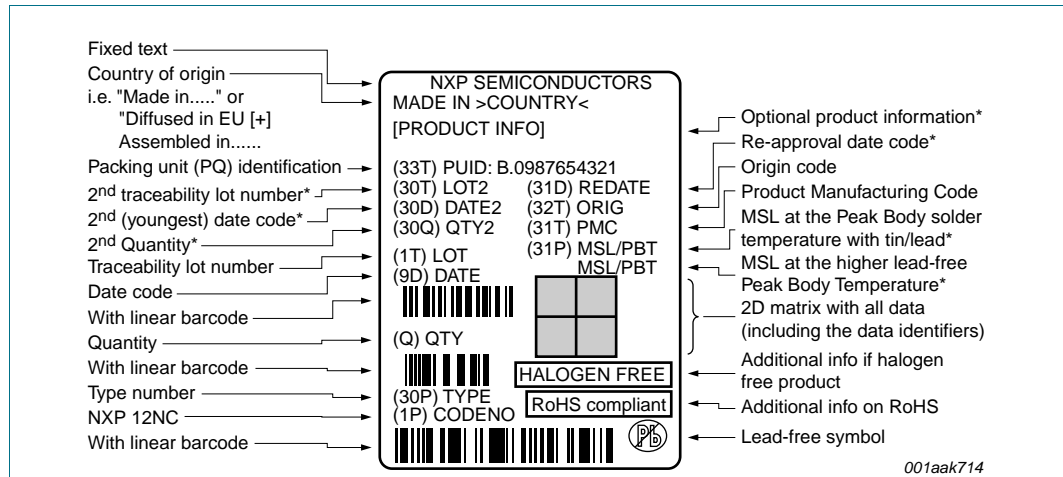


Fig 8. Example of typical box and reel information barcode label

Table 15. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#) and [17](#)

Table 16. SnPb eutectic process (from J-STD-020D)

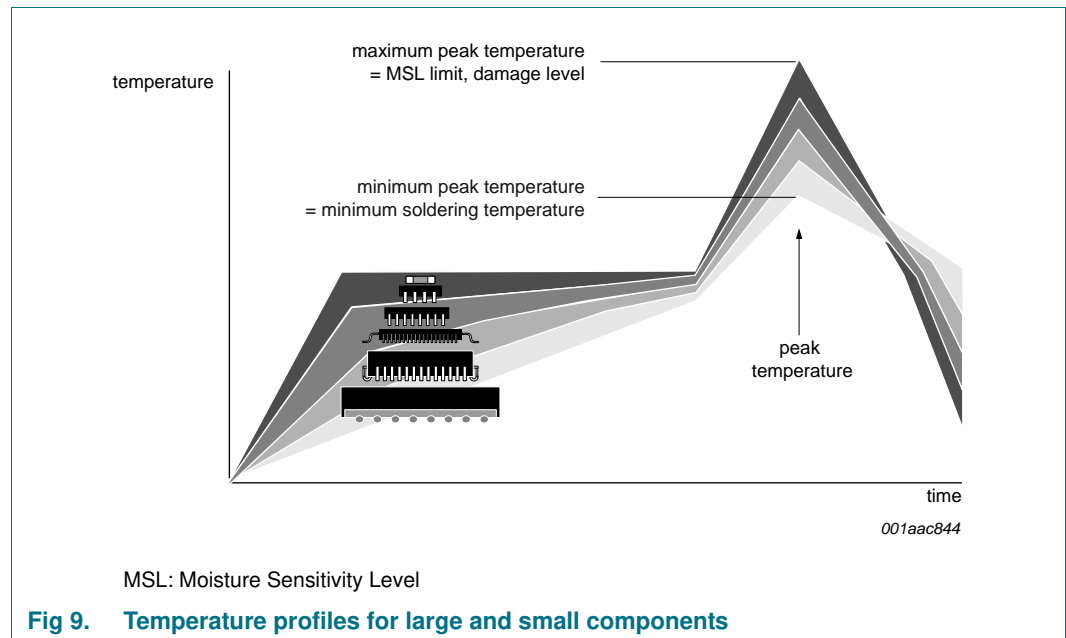
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

13. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
Gbps	Gigabits per second
HBM	Human Body Model

14. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL02GP023 v.2	20170814	Product data sheet	-	CBTL02GP023 v.1
Modifications:	Changed description of switch from "ON/OFF switch" to "5 Gbps rail-to-rail low insertion loss switch" throughout			
CBTL02GP023 v.1	20170601	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b)

whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
3.1	Ordering options	2
4	Block diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	5
8	Recommended operating conditions	5
9	Characteristics	6
9.1	Device general characteristics	6
9.2	Switch channel characteristics	6
9.3	Control signals characteristics	7
10	Package outline	9
11	Packing information	10
11.1	DHX2QFN14; Reel pack, SMD, 13"; Q1/T1 standard product orientation; Orderable part number ending ,431 or Z; Ordering code (12NC) ending 431	10
11.1.1	Packing method	10
11.1.2	Product orientation	11
11.1.3	Carrier tape dimensions	11
11.1.4	Reel dimensions	12
11.1.5	Barcode label	13
12	Soldering of SMD packages	13
12.1	Introduction to soldering	13
12.2	Wave and reflow soldering	13
12.3	Wave soldering	14
12.4	Reflow soldering	14
13	Abbreviations	15
14	Revision history	16
15	Legal information	17
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	18
16	Contact information	18
17	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 August 2017

Document identifier: CBTL02GP023