

WT21 EVALUATION KIT

DATA SHEET

Friday, 05 February 2010

Version 1.3

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VERSION HISTORY

Version	Comment
0.1	First draft
1.0	First release
1.1	Added images
1.2	Bootstrap added
1.3	Pin out numbers fixed

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1 Introduction

FEATURES

- Evaluation kit for WT32 *Bluetooth* audio module containing
 - RS-232 serial interface (230400bps)
 - USB interface for power supply
 - SPI for upgrading the firmware and parameters
 - Reset button
 - PCM codec (OKI MSM7702-01)
 - 2 x 3,5mm audio jacks for line in and line out
 - 24 pin I/O interface (PIO1 – PIO9, UART, SDIO, PCM, GND, 3V3, ENA)
 - DIP switches for host interface configuration
 - Current measurement point

- Host controller interface

TARGET APPLICATIONS

WT21 Evaluation Kit is meant for evaluation and development of WT21 *Bluetooth* module or prototyping and piloting *Bluetooth* systems utilizing WT21 module.

ELECTRICAL FUNCTIONALITY

Please, refer to the latest WT21 data sheet for information about WT21 *Bluetooth* module. The physical outlook, schematics, assembly and the PIN configurations of the interfaces of WT21 evaluation Kit are described in this document.

SOFTWARE FUNCTIONALITY

WT32 evaluation kit is delivered with Host Controller Interface (HCI) firmware, so WT21 only implements the lowest levels of Bluetooth stack. WT21 always requires a host system that implements the upper layers of Bluetooth stack and at least one Bluetooth profile.

2 Physical outlook



Figure 1: WT21 front view

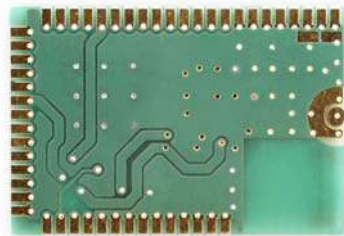


Figure 2: WT21 back view

3 Schematics

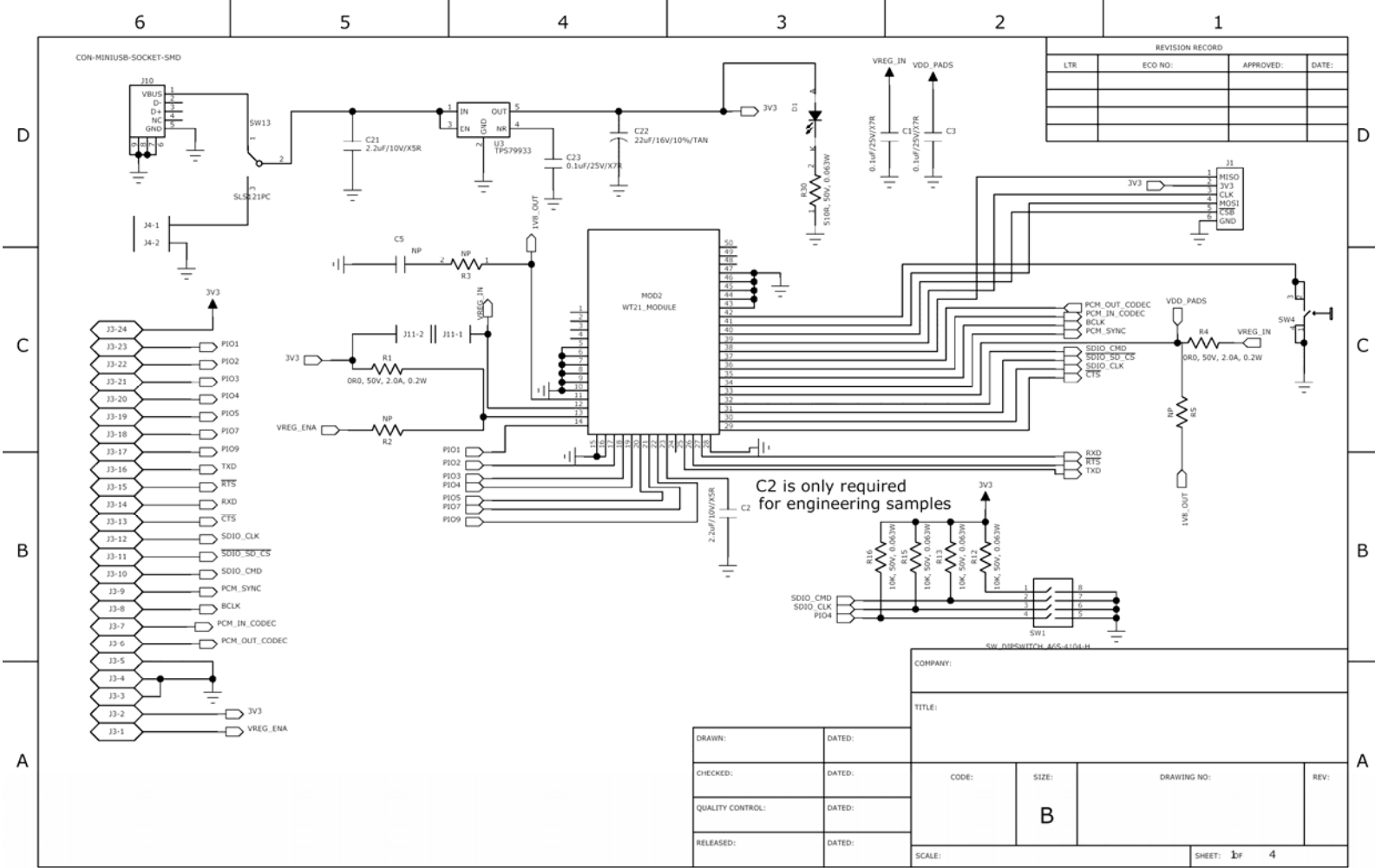


Figure 3: EKWT21 Schematic (1/3)

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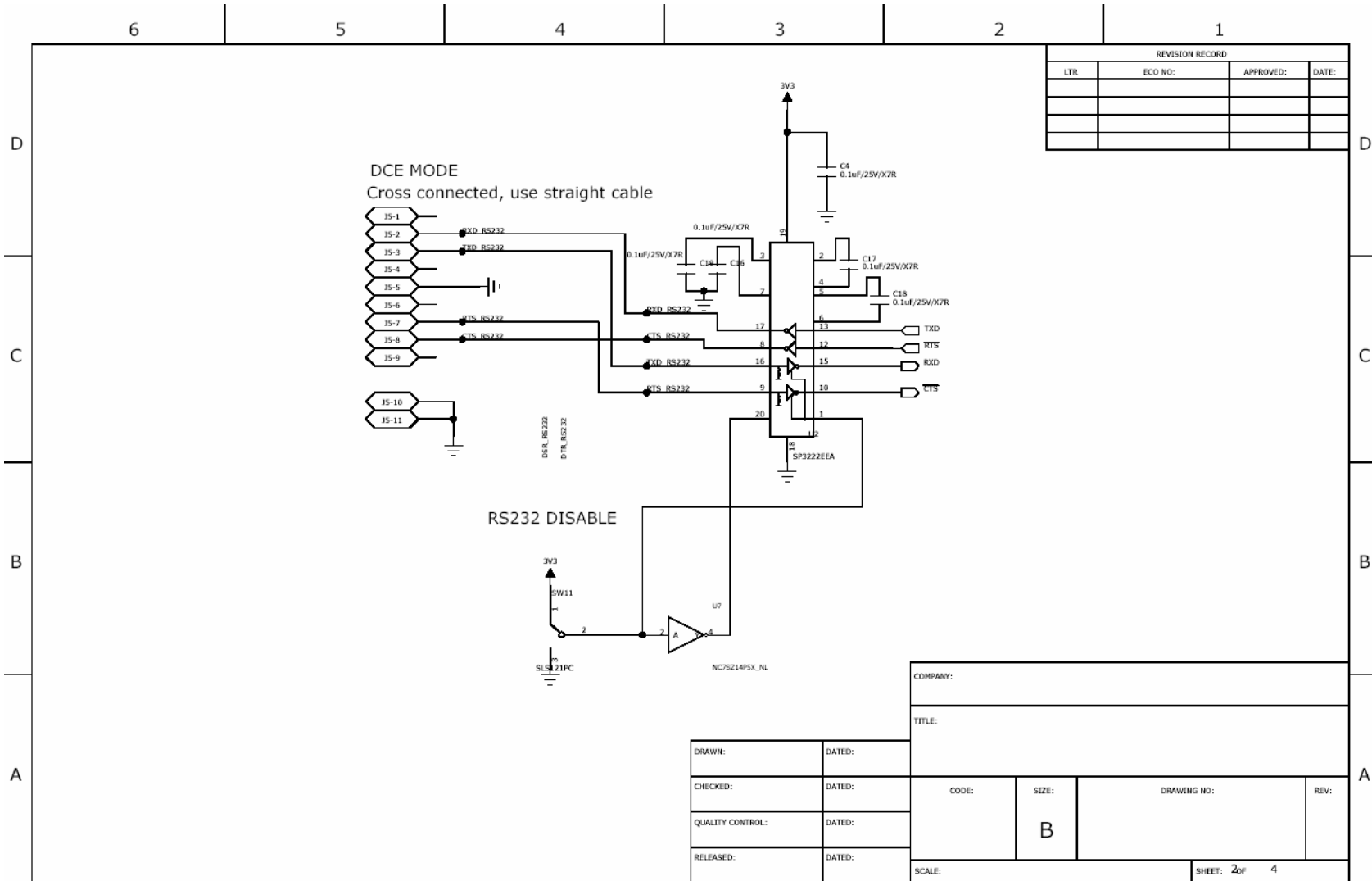


Figure 4: EKWT21 Schematic (2/3)

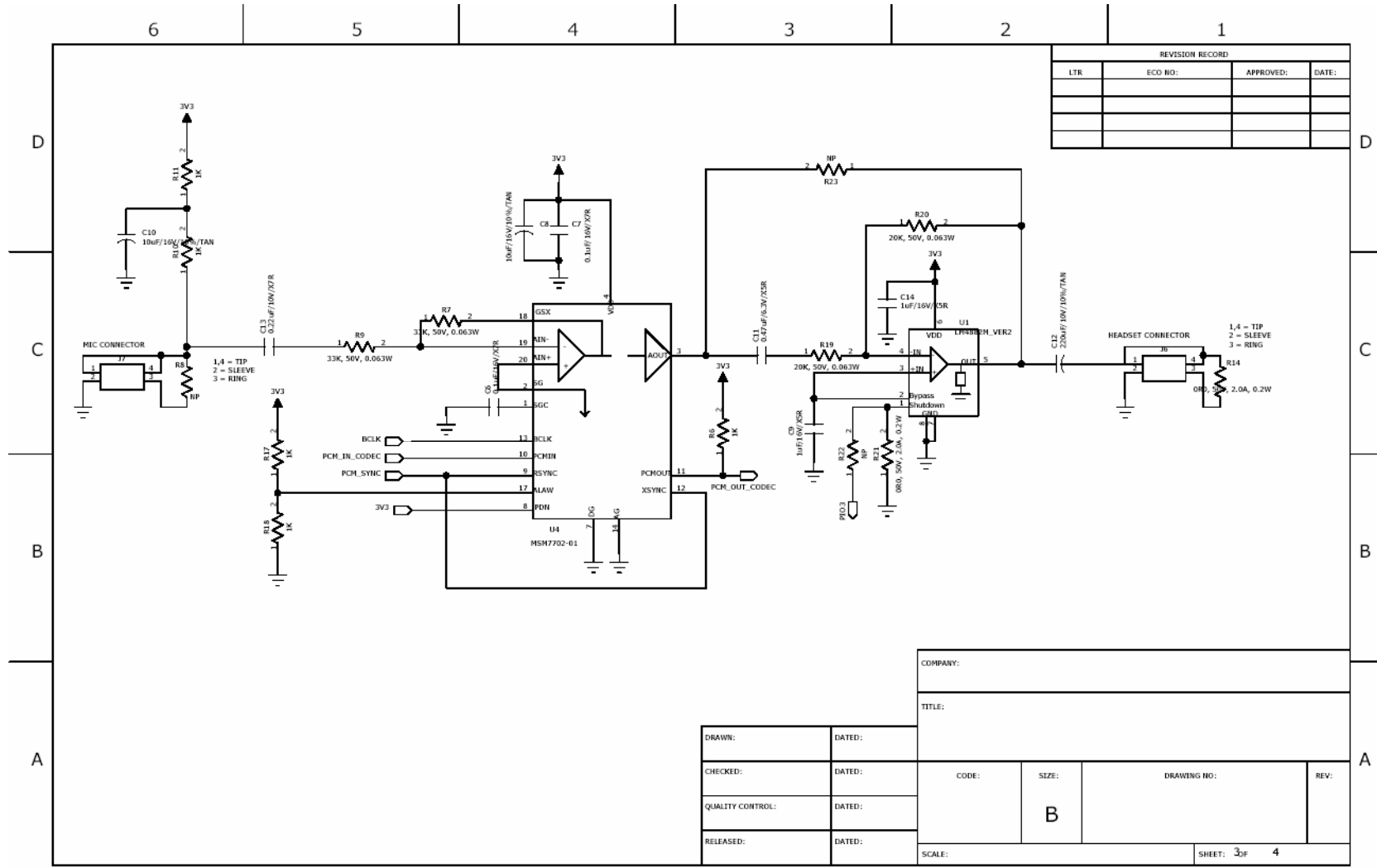


Figure 5: EKWT21 Schematic (3/3)

DRAWN:		DATED:		COMPANY:	
CHECKED:		DATED:		TITLE:	
QUALITY CONTROL:		DATED:		CODE:	SIZE:
RELEASED:		DATED:		DRAWING NO:	
SCALE:				SHEET: 3 of 4	REV:

4 Assembly

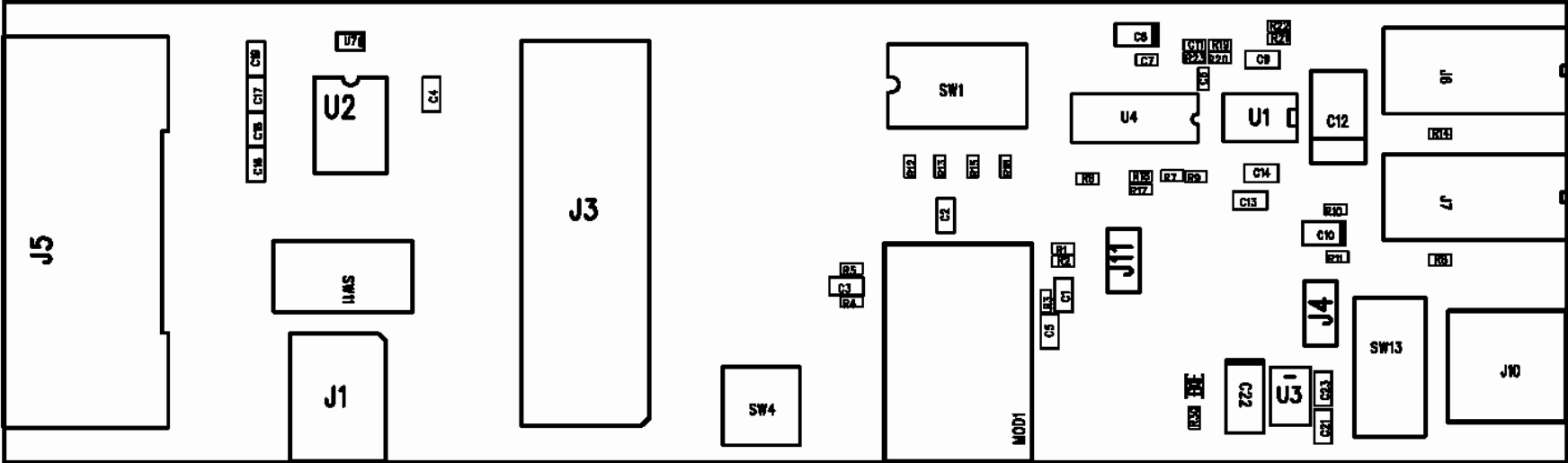


Figure 6: Assembly Drawing of EKWT21

5 Layout

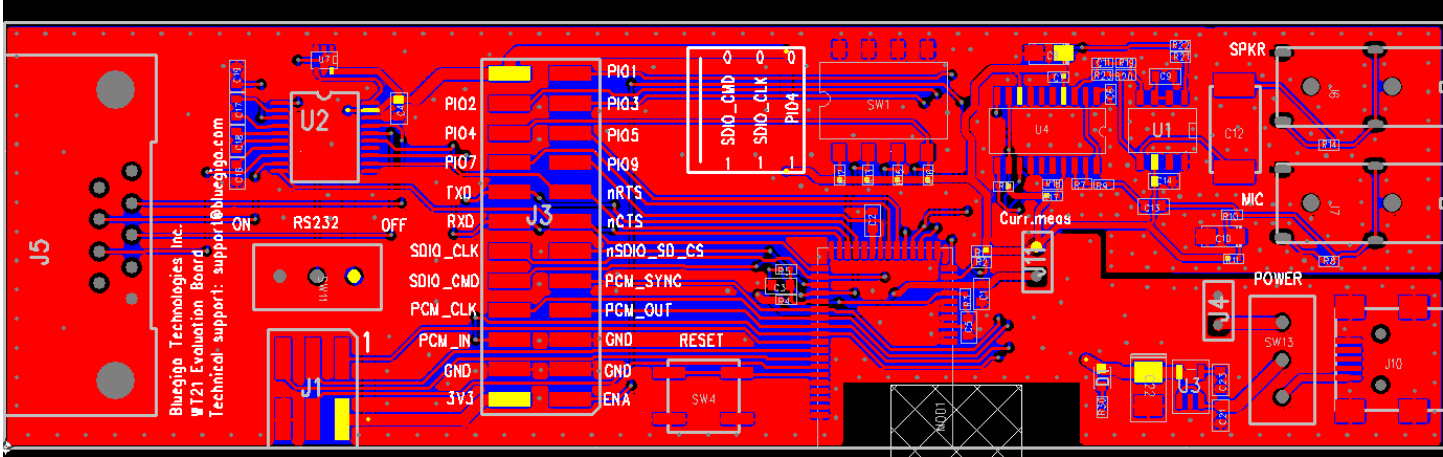


Figure 7: Top Layer Layout

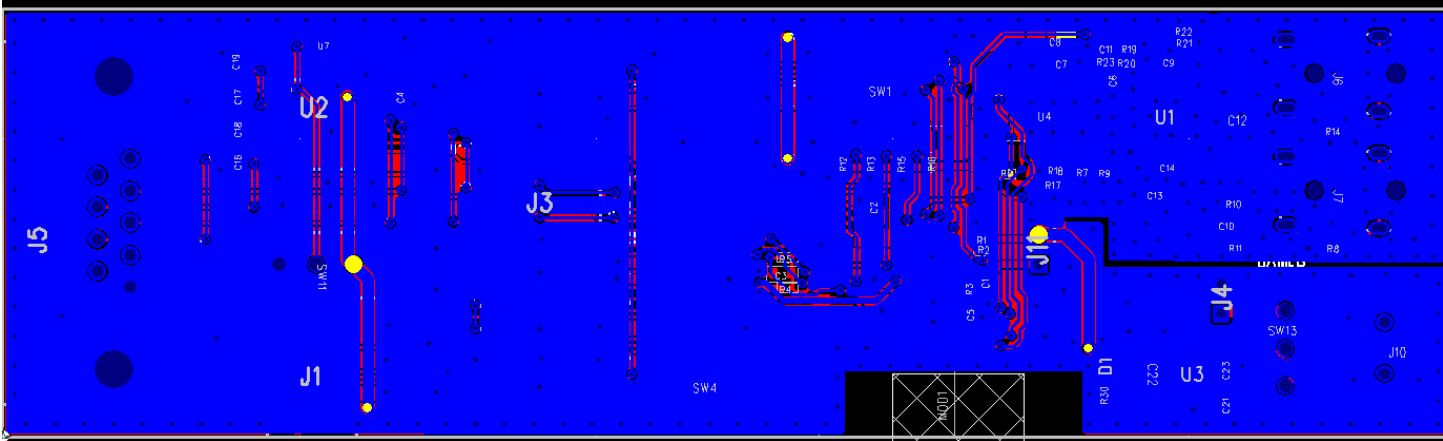


Figure 8: Bottom Layer Layout

6 Interfaces

6.1 Powering the evaluation board

The board can be powered either through a USB connector J10 or using a laboratory power supply through pin header J4. LDO TPS79933DDCT is used to regulate 3.3V supply voltage for the module (VREG_IN and VDD_PADS). Maximum input voltage for the regulator is 6.5V. Enable pins of the internal regulators of the module (VREG_ENA) are tight to 3.3V supply through zero ohm resistor R1.

6.2 UART

UART interface of the module is available in the pin header J3. When UART is being used through the pin header the RS232 transceiver U2 should be switched to high impedance using SW11. When using RS232 through J5 the transceiver should be enabled with SW11. The maximum baud rate of the transceiver in the evaluation board is 235kbps.

6.3 Host selection DIP switch

DIP switch SW1 is used for the host selection as described below.

The MCU of WT21 selects the UART/SDIO interfaces by reading PIO[4] at boot-time. When PIO[4] is high, the SDIO interface is enabled; when PIO[4] is low, the UART is enabled.

If in UART mode, the MCU selects the UART transfer protocol automatically using the unused SDIO pins shown in Table 1.

SDIO_CLK	SDIO_CMD	Protocol
0	0	bcsp
0	1	h4
1	0	h4ds
1	1	h5

Table 1: SDIO_CLK and SDIO_CMD transfer Protocols

6.3.1 UART protocol selection

At bootup the module looks at PIO4 to determine whether it should use UART or SDIO/CSPI. If PIO4 is pulled low then UART will be used. It then checks SDIO_CLK and SDIO_CMD pins to determine which mode it should use for receiving initial pskeys over UART.

Note:

When the switch on the eval board is conducting (marked by "on") then the pin is pulled low which is marked by 0.

To use the H4 UART protocol for configuring the WT21 the PIO4 should be pulled low, the SDIO_CLK should be pulled low and SDIO_CMD must be pulled high. Note that by default there is a weak pull-up for these pins so if nothing is connected to them, they will be pulled high.

6.3.2 UART baudrate negotiation

When PIO4, CLK and CMD are all pulled low, BCSP over UART is selected. The speed for this initial communication should be between 57600bps and 115200bps and must use even parity.

Since the WT21 doesn't know its internal clock frequency nor the baud rate it should communicate at, a form of baud rate auto-negotiation is implemented on the module. The host needs to send some data packets so that the WT21 can assess the baud rate the host uses.

Any seemingly non-uniform data can be used but for BCSP sending Link Establishment packets is the natural choice. Once the WT21 has received enough samples it will start communicating back to the host by replying to the Link Establishment messages.

Since the H4 doesn't have any link protocol, repeated queries for some known value can be used. Once the host has started receiving replies for the queries, it can be assumed that the baud rate has been established.

Note:

The number of packets the WT21 will need for assessing the baud rate is dependent on the host's UART hardware. With poor quality UARTs the auto-negotiation may fail, which means the WT21 will use an incorrect baud rate to communicate back. The host will see this as packets of garbage, i.e. full of crc errors and checksum errors when using BCSP. To restart the negotiation the host will need to reset the WT21. The host should have some way to power cycle the WT21 to restart the baud rate negotiation, either by controlling the reset pin or directly the module's VCC.

6.3.3 Loading the PS keys

Once a communications link has been established, BCCMD packets are used to load PS Keys. At least the following PS Keys need to be set:

Key address	Value	Description
&0001	00dd eeff 00cc aabb	Bluetooth address (aa:bb:cc:dd:ee:ff)
&01be	01d8	UART baud rate (01d8 = 115200)
&01fe	6590	Chrystal frequency. Do not modify.
&025d	0001	VM disable. Do not modify.
&01f9	0001	Host interface, (0001 = BCSP)

For the host interface the following protocols are supported:

- BCSP 0001
- H4 0003
- H5 0006
- H4DS 0007

To activate the changes the command for warm reset is sent to the WT21.

After this the module will immediately reboot using the configured settings and thus switch to the specified baud rate.

6.4 SPI interface

SPI is available in the pin header J1. Following table shows the connections in the pin header. 3.3V is an output from the evaluation board and it is used to power the on board installation kit delivered with the kit.

PIN name	No.	I/O	Description
MISO	1	O	MISO
3.3 V	2	POWER	3.3 V power supply input
CLK	3	I	CLK
MOSI	4	I	MOSI
CSB	5	I	CSB
GND	6	GND	GND

Table 2: SPI interface pin description

6.5 SDIO and PIO interface

All SDIO and PIO connections are available in the pin header J3.

6.6 PCM Codec and Audio Interface

The evaluation board uses MSM7702 PCM codec by OKI Semiconductor. PS settings for the codec are as follows:

- PCM_DATAFORMAT 0200
- PCM_CONFIG32 180000C0
- HOST_IO_MAP_SCO_PCM true

Headset can be connected to 3.5mm jack connectors J6 and J7.

7 WEEE Compliance



The crossed-out wheeled bin means that within the European Union the product must be taken to separate collection at the product end-of-life. Do not dispose of these products as unsorted municipal waste.

8 Contact Information

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