GENLINX™II GS9035A
Serial Digital Reclocker

DATA SHEET

FEATURES

- **adjustment-free operation**
- **auto-rate selection for 5 SMPTE data rates: 143, 177, 270, 360, 540Mb/s**
- **data rate indication output**
- **serial data output mute when PLL is not locked**
- **immune to harmonic locking**
- **operation independent of SAV/EAV sync signals**
- **low jitter, low power**
- **single external VCO resistor for operation with five input data rates**
- **large input jitter tolerance: typically 0.45 UI beyond loop bandwidth**
- **power savings mode (output serial clock disable)**
- **system friendly: serial clock remains active when data outputs muted**
- **robust lock detect**
- **Pb-free and Green**

APPLICATIONS

The GS9035A is used for Clock and Data recovery, and Jitter elimination for all high speed serial digital interface applications involving SMPTE 259M and other data standards.

DESCRIPTION

The GS9035A is a high performance clock and data recovery IC designed for serial digital data. The GS9035A receives either single-ended or differential PECL data and outputs differential PECL clock and retimed data signals.

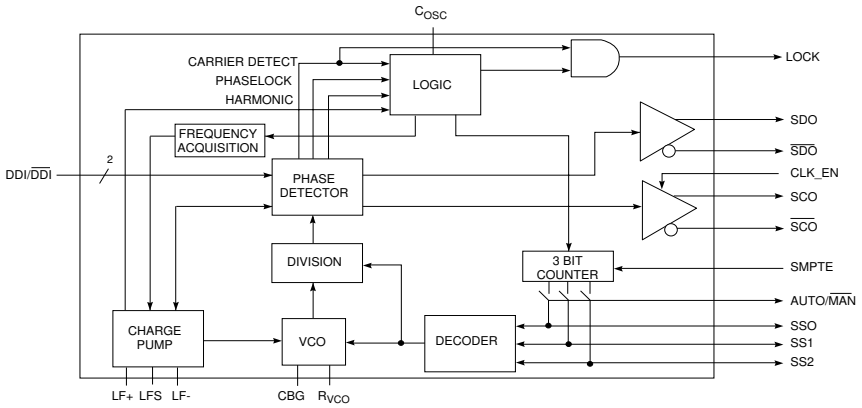
The GS9035A can operate in either auto or manual rate selection mode. In auto mode the GS9035A is ideal for multi-rate serial data protocols such as SMPTE 259M. In this mode the GS9035A automatically detects and locks onto the incoming data signal. For single rate data systems, the GS9035A can be configured to operate in manual mode. In both modes, the GS9035A requires only one external resistor to set the VCO centre frequency and provides adjustment-free operation.

The GS9035A has dedicated pins to indicate LOCK and data rate. In addition, an internal muting function forces the serial data outputs to a static state when input data is not present or when the PLL is not locked. The serial clock outputs can also be disabled resulting in a 10% power savings.

The GS9035A is packaged in a 28 pin PLCC and operates from a single +5 or -5 volt power supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS9035ACPJ	28 pin PLCC	0°C to 70°C	No
GS9035ACTJ	28 pin PLCC Tape	0°C to 70°C	No
GS9035ACPJE3	28 pin PLCC	0°C to 70°C	Yes
GS9035ACTJE3	28 pin PLCC Tape	0°C to 70°C	Yes



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	V_{CC} + 0.5 to V_{EE} - 0.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise stated, R_{LF} = 1.8K, C_{LF1} = 15nF, C_{LF2} = 3.3pF.

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage		4.75	5.00	5.25	V		3
Supply Current	CLK_EN = 0	-	90	110	mA		3
	CLK_EN = 1	-	105	120	mA		3
DDI/$\overline{DDI}$ Common Mode Input Voltage Range		V_{EE} + (V_{DIFF}/2)	0.4 to 4.6	V_{CC} - (V_{DIFF}/2)	V	2	3
DDI/$\overline{DDI}$ Differential Input Drive		200	800	2000	mV		3
AUTO/$\overline{MAN}$, SMPTE	High	2.0	-	-	V		3
	Low	-	-	0.8			
CLK_EN Input Voltage	High	2.5	-	-	V		3
	Low	-	-	0.8			
LOCK Output Low Voltage	I_{OH} = 500µA	-	0.25	0.4	V	3	1
SS{2:0} Output Voltage	HIGH, I_{OH} = -180µA, Auto Mode	4.4	4.8	-	V		1
	LOW, I_{OL} = 600µA, Auto Mode	-	0.3	0.4			
SS{2:0} Input Voltage	HIGH, Manual Mode	2	-	-	V		3
	LOW, ManualMode	-	-	0.8			
CLK_EN Source Current	Low, V_{IL} = 0V	-	26	55	µA		1

NOTES

1. TYPICAL - measured on EB-RD35A board.
2. V_{DIFF} is the differential input signal swing.
3. LOCK is an open collector output and requires an external pull-up resistor.
4. Pins SS[2:0] are outputs in AUTO mode and inputs in MANUAL mode.

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise stated, R_{LF} = 1.8K, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Rate	SDI	143	-	540	Mb/s		3
Intrinsic Jitter Psuedorandom (2^{23} - 1)	270Mb/s	-	185	See Figure 6	ps p-p	2	4
	540Mb/s	-	164				
Intrinsic Jitter Pathological (SDI checkfield)	270Mb/s	-	462	See Figure 7	ps p-p	2	3
	360Mb/s	-	308				
	540Mb/s	-	260				
Input Jitter Tolerance	270Mb/s	0.40	0.56	-	UI p-p	3	9
	540Mb/s	0.35	0.43	-			
Lock Time Synchronous Switch	t_{SWITCH} < 0.5µs, 270Mb/s	-	1	-	µs	4	7
	0.5µs < t_{SWITCH} < 10ms	-	1	-	ms		
	t_{SWITCH} > 10ms	-	4	-	ms		
Lock Time Asynchronous Switch	Loop Bandwidth = 6MHz at 540 Mb/s	-	10	-	ms	5	7
SDO MUTE Time		0.5	1	2	µs	6	7
SDO to SCO Synchronization		-200	0	200	ps		7
SDO, SCO Output Signal Swing	75Ω DC load	600	800	1000	mV p-p		1
SDO, SCO Rise and Fall Times	20% - 80%	200	300	400	ps		7

NOTES

1. TYPICAL - measured on EB-RD35A board, T_A = 25°C.
2. Characterized 6 sigma rms.
3. IJT measured with sinusoidal modulation beyond Loop Bandwidth (at 6.5MHz).
4. Synchronous switching refers to switching the input data from one source to another source which is at the same data rate (ie: line 10 switching for component NTSC).
5. Asynchronous switching refers to switching the input data from one source to another source which is at a different data rate.
6. SDO MUTE Time refers to the response of the SDO output from valid re-clocked input data to mute mode when the input signal is removed.

TEST LEVEL

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test

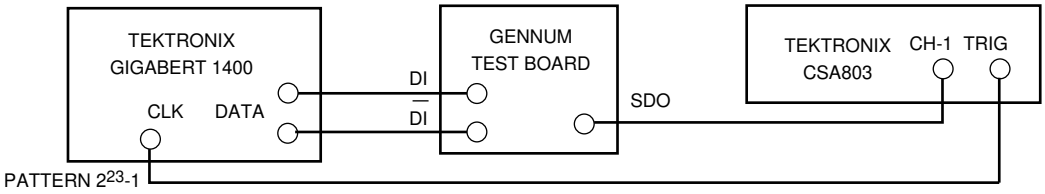
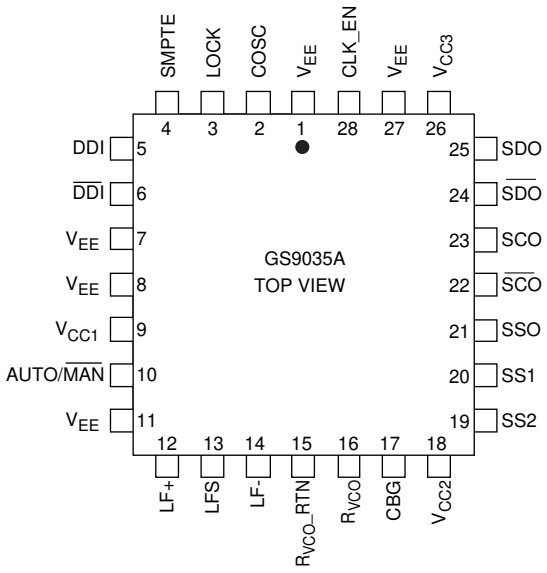


Fig. 1 Jitter Measurement Test Setup

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1,7,8,11,27	V_{EE}	I	Most negative power supply connection.
2	COSC	I	Timing control capacitor for internal system clock.
3	LOCK	O	Lock indication. When HIGH, the GS9035A is locked. LOCK is an open collector output and requires an external 10k pullup resistor.
4	SMPTE	I	SMPTE/Other rate select.
5, 6	DDI/$\overline{DDI}$	I	Digital data input (Differential ECL/PECL).
9	V_{CC1}	I	Most positive power supply connection.
10	AUTO/$\overline{MAN}$	I	Auto or Manual mode select. TTL/CMOS compatible input.
12	LF+	I	Loop filter component connection.
13	LFS	I	Loop filter component connection.
14	LF-	I	Loop filter component connection.
15	R_{VCO}_RTN	I	R_{VCO} return.

PIN DESCRIPTIONS (continued)

NUMBER	SYMBOL	TYPE	DESCRIPTION
16	R_{VCO}	I	Frequency setting resistor.
17	CBG	I	Internal bandgap voltage filter capacitor.
18	V_{CC2}	I	Most positive power supply connection.
19 - 21	SS[2:0]	I/O	Data rate indication (Auto mode) or data rate select (Manual mode). TTL/CMOS compatible I/O. In auto mode these pins can be left unconnected.
22, 23	$\overline{SCO}$/SCO	O	Serial clock output. $\overline{SCO}$/SCO are differential current mode outputs and require external 75Ω pullup resistors.
24, 25	$\overline{SDO}$/SDO	O	Serial data output. $\overline{SDO}$/SDO are differential current mode outputs and require external 75Ω pullup resistors.
26	V_{CC3}	I	Most positive power supply connection.
28	CLK_EN	I	Clock enable. When HIGH, the serial clock outputs are enabled.

TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25°C unless otherwise shown.)

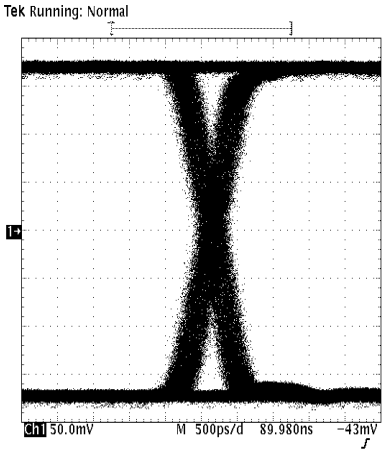


Fig. 2 Intrinsic Jitter (2^{23}-1 Pattern) 30Mb/s

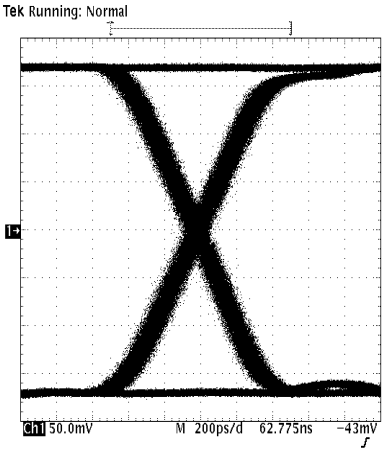


Fig. 4 Intrinsic Jitter (2^{23}-1 Pattern) 270Mb/s

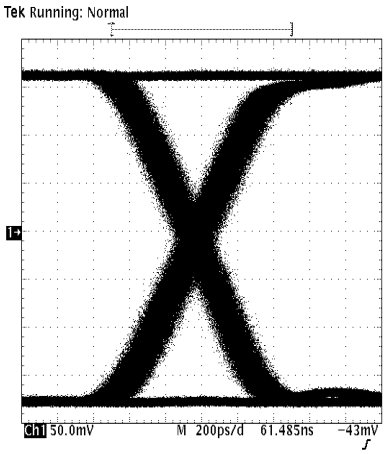


Fig. 3 Intrinsic Jitter (2^{23}-1 Pattern) 143Mb/s

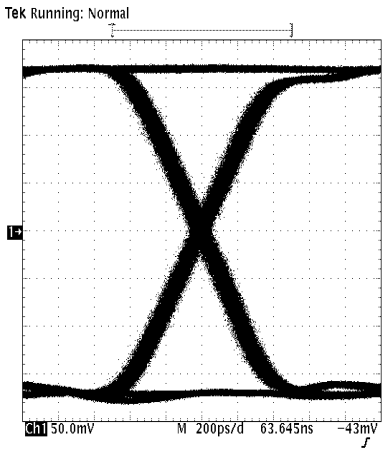
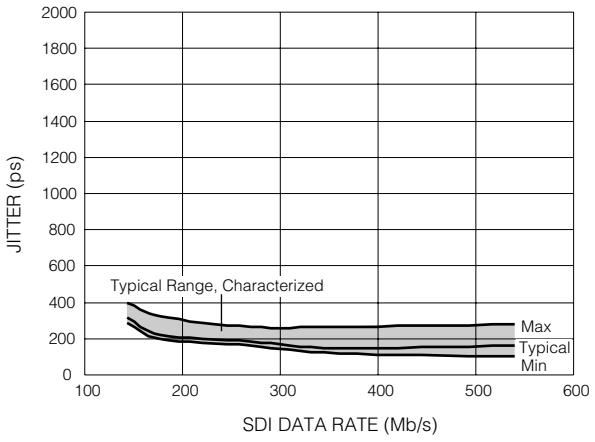
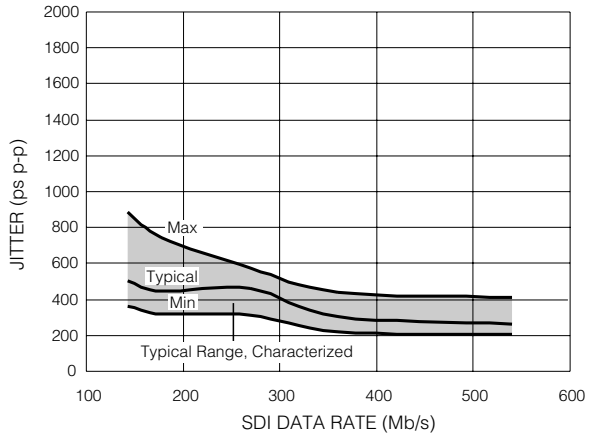


Fig. 5 Intrinsic Jitter (2^{23}-1 Pattern) 540Mb/s



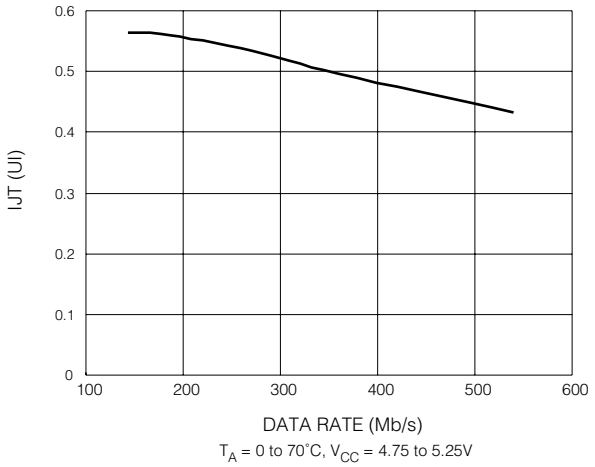
T_A=0 to 70˚C, V_{CC}=4.75 to 5.25V for the typical range

Fig. 6 Intrinsic Jitter - Pseudorandom (2^{23} -1)



T_A = 0 to 70˚C, V_{CC} = 4.75 to 5.25V for the typical range

Fig. 7 Intrinsic Jitter - Pathological SDI Checkfield



T_A = 0 to 70˚C, V_{CC} = 4.75 to 5.25V

Fig. 8 Typical Input Jitter Tolerance (Characterized)

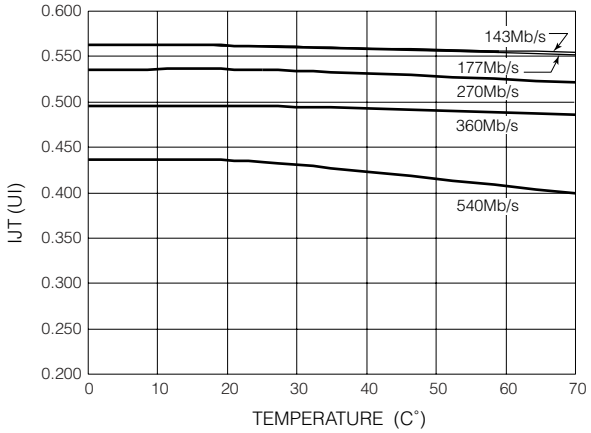


Fig. 9 Typical IJT vs. Temperature (V_{CC}=5.0V) (Characterized)

DETAILED DESCRIPTION

The GS9035A receives either a single-ended or differential PECL serial data stream at the DDI and $\overline{\text{DDI}}$ inputs. It locks an internal clock to the incoming data and outputs the differential PECL retimed data signal and recovered clock on outputs $\overline{\text{SDO}}$/SDO and $\overline{\text{SCO}}$/SCO respectively. The timing between the input, output, and clock signals is shown below.

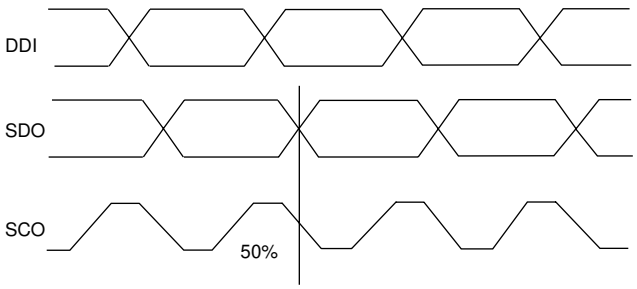


Fig. 10 Input/Output Clock Signal Timing

The GS9035A reclocker contains four main functional blocks: the Phase Locked Loop, Auto/Manual Data Rate Select, Frequency Acquisition, and Logic Circuit.

1. PHASE LOCKED LOOP (PLL)

The Phase Locked Loop locks the internal PLL clock to the incoming data rate. A simplified block diagram of the PLL is shown below. The main components are the VCO, the phase detector, the charge pump, and the loop filter.

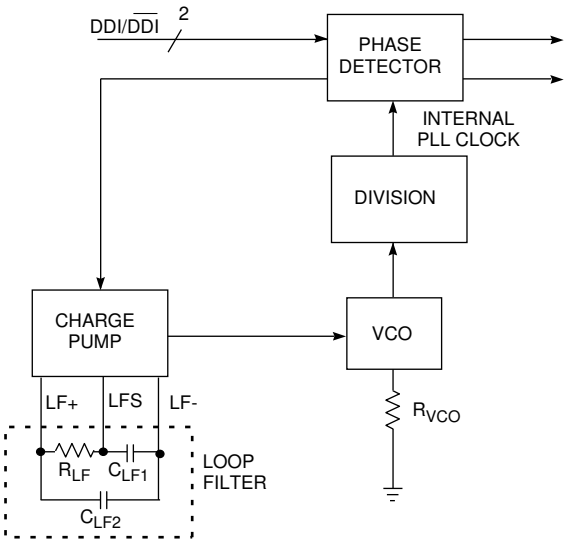


Fig. 11 Simplified Diagram of the PLL

1.1 VCO

The VCO is a differential low phase noise, factory trimmed design that provides increased immunity to PCB noise and precise control of the VCO center frequency. The VCO operates between 30 and 540Mb/s and has a pull range of -13 +25% about the center frequency depending on the signal data rate. A single low impedance external resistor, R_{VCO}, sets the VCO center frequency *(see Figure 12).* The low impedance R_{VCO} minimizes thermal noise and reduces the PLL's sensitivity to PCB noise.

For a given R_{VCO} value, the VCO can oscillate at one of two frequencies. When SMPTE = SS0 = logic 1, the VCO center frequency corresponds to the f_L curve. For all other SMPTE/SS0 combinations, the VCO center frequency corresponds to the f_H curve (f_H is approximately 1.5 x f_L).

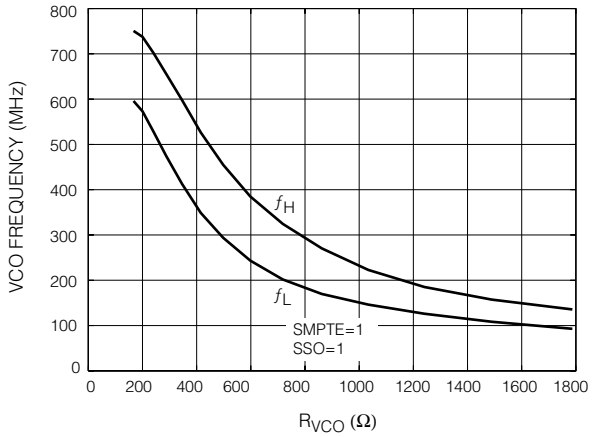


Fig. 12 VCO Frequency vs. R_{VCO}

The recommended R_{VCO} value for auto rate SMPTE 259M applications is 365Ω.

The VCO and an internal divider generate the PLL clock. Divider moduli of 1, 2, and 4 allow the PLL to lock to data rates from 143Mb/s to 540Mb/s. The divider modulus is set by the AUTO/$\overline{\text{MAN}}$, SMPTE, and SS[2:0] pin *(see Auto/Manual Data Rate Select section for further details).* In addition, a manually selectable modulus 8 divider allows operation at data rates as low as 30Mb/s.

When the input data stream is removed for an excessive period of time *(see AC electrical characteristics table),* the VCO frequency can drift from the previously locked frequency up to the maximum shown in Table 1.

TABLE 1: Frequency Drift Range (when PLL loses lock)

LOSES LOCK FROM	MIN (%)	MAX(%)
143Mb/s lock	-21	21
177Mb/s lock	-12	26
270Mb/s lock	-13	28
360 Mb/s lock	-13	24
540 Mb/s lock	-13	28

1.2 Phase Detector

The phase detector compares the phase of the PLL clock with the phase of the incoming data signal and generates error correcting timing pulses. The phase detector design provides a linear transfer function between the input phase and output timing pulses maximizing the input jitter tolerance of the PLL.

1.3 Charge Pump

The charge pump takes the phase detector output timing pulses and creates a charge packet that is proportional to the system phase error. A unique differential charge pump design ensures that the output phase does not drift when data transitions are sparse. This makes the GS9035A ideal for SMPTE 259M applications where pathological signals have data transition densities of 0.05.

1.4 Loop Filter

The loop filter integrates the charge pump packets and produces a VCO control voltage. The loop filter is comprised of three external components which are connected to pins LF+, LFS, and LF-. The loop filter design is fully differential giving the GS9035A increased immunity to PCB board noise.

The loop filter components are critical in determining the loop bandwidth and damping of the PLL. Choosing these component values is discussed in detail in the PLL Design Guidelines section. Recommended values for SMPTE 259M applications are shown in the Typical Application Circuit diagram.

2. FREQUENCY ACQUISITION

The core PLL is able to lock if the incoming data rate and the PLL clock frequency are within the PLL capture range (which is slightly larger than the loop bandwidth). To assist the PLL to lock to data rates outside of the capture range, the GS9035A uses a frequency acquisition circuit.

The frequency acquisition circuit sweeps the VCO control voltage such that the VCO frequency changes from -10% to +10% of the center frequency. Figure 13 shows a typical sweep waveform.

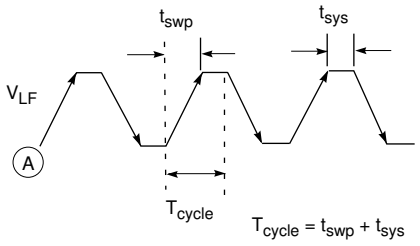


Fig. 13 Typical Sweep Form

The VCO frequency starts at point A and sweeps up attempting to lock. If lock is not established during the up sweep, the VCO is then swept down. The system is designed such that the probability of locking within one cycle period is greater than 0.999. If the system does not lock within one cycle period, it will attempt to lock in the subsequent cycle. In manual mode, the divider modulus is fixed for all cycles. In auto mode, each subsequent cycle is based on a different divider moduli as determined by the internal 3-bit counter.

The average sweep time, t_{swp}, is determined by the loop filter component, C_{LF1}, and the charge pump current, I_{CP}:

$$t_{swp} = \frac{4}{3}\frac{C_{LF1}}{I_{LF1}} \quad \text{[seconds]}$$

The nominal sweep time is approximately 121µs when C_{LF1} = 15nF and I_{CP} = 165µA (R_{VCO} = 365Ω).

An internal system clock determines t_{sys} (*see section 7, Logic Circuit*).

3. LOGIC CIRCUIT

The GS9035A is controlled by a finite state logic circuit which is clocked by an asynchronous system clock. That is, the system clock is completely independent of the incoming data rate. The system clock runs at low frequencies, relative to the incoming data rate, and thus reduces interference to the PLL. The period of the system clock is set by the COSC capacitor and is

$$t_{sys} = 9.6 \times 10^4 \times COSC \quad \text{[seconds]}$$

The recommended value for t_{sys} is 450µs (COSC = 4.7nF).

4. AUTO/MANUAL DATA RATE SELECT

The GS9035A can operate in either auto or manual data rate select mode. The mode of operation is selected by a single input pin (AUTO/$\overline{MAN}$).

4.1 Auto Mode (AUTO/$\overline{MAN}$ = 1)

In auto mode, the GS9035A uses a 3-bit counter to automatically cycle through five (SMPTE=1) or three (SMPTE=0) different divider moduli as it attempts to acquire lock. In this mode, the SS[2:0] pins are outputs and indicate the current value of the divider moduli according to Table 2. Note that for SMPTE = 0 and divider moduli of 2 and 4, the PLL can correctly lock for two values of SS[2:0].

TABLE 2: Data Rate Indication in Auto Mode

AUTO/$\overline{MAN}$ = 1 (Auto Mode) f_H, f_L = VCO center frequency as per Figure 12			
SMPTE	SS[2:0]	DIVIDER MODULI	PLL CLOCK
1	000	4	$f_H/4$
1	001	2	$f_L/2$
1	010	2	$f_H/2$
1	011	1	f_L
1	100	1	f_H
1	101	-	-
1	110	-	-
1	111	-	-
0	000	4	$f_H/4$
0	001	4	$f_H/4$
0	010	2	$f_H/2$
0	011	2	$f_H/2$
0	100	1	f_H
0	101	-	-
0	110	-	-
0	111	-	-

4.2 Manual Mode (AUTO/$\overline{MAN}$ = 0)

In manual mode, the GS9035A divider moduli is fixed. In this mode, the SS[2:0] pins are inputs and set the divider moduli according to Table 3.

TABLE 3: Data Rate Select in Manual Mode

AUTO/$\overline{MAN}$ = 0 (Manual Mode) f_H, f_L = VCO center frequency as per Figure 8			
SMPTE	SS[2:0]	DIVIDER MODULI	PLL CLOCK
1	000	4	$f_H/4$
1	001	2	$f_L/2$
1	010	2	$f_H/2$
1	011	1	f_L
1	100	1	f_H
1	101	8	$f_L/8$
1	110	8	$f_H/8$
1	111	-	-
0	000	4	$f_H/4$
0	001	4	$f_H/4$
0	010	2	$f_H/2$
0	011	2	$f_H/2$
0	100	1	f_H
0	101	1	f_H
0	110	8	$f_H/8$
0	111	-	-

5. LOCKING

The GS9035A indicates lock when three conditions are satisfied:

1. Input data is detected.
2. The incoming data signal and the PLL clock are phase locked.
3. The system is not locked to a harmonic.

The GS9035A defines the presence of input data when at least one data transition occurs every 1µs.

The GS9035A assumes that it is NOT locked to a harmonic if the pattern '101' or '010' (in the reclocked data stream) occurs at least once every $t_{sys}/3$ seconds. Using the recommended component values, this corresponds to approximately 150µs. (In an harmonically locked system, all bit cells are double clocked and the above patterns become '110011' and '001100', respectively.)

5.1 Lock Time

The lock time of the GS9035A depends on whether the input data is switching synchronously or asynchronously. Synchronous switching refers to the case where the input data is changed from one source to another source which is at the same data rate (but different phase). Asynchronous switching refers to the case where the input data to the GS9035A is changed from one source to another source which is at a different data rate.

When input data to the GS9035A is removed, the GS9035A latches the current state of the counter (divider modulus). Therefore, when data is reapplied, the GS9035A begins the lock procedure at the previous locked data rate. As a result, in synchronous switching applications, the GS9035A locks very quickly. The nominal lock time depends on the switching time and is summarized in the table below:

TABLE 4: Lock Time Relative to Switching Time

SWITCHING TIME	LOCK TIME
<0.5µs	10µs
0.5µs - 10ms	$2t_{sys}$
> 10ms	$2T_{cycle} + 2t_{sys}$

In asynchronous switching applications (including power up) the lock time is determined by the frequency acquisition circuit as described in section 2, *Frequency Acquisition*. In manual mode, the frequency acquisition circuit may have to sweep over an entire cycle (depending on initial conditions) to acquire lock resulting in a maximum lock time of $2T_{cycle} + 2t_{sys}$. In auto tune mode, the maximum lock time is $6T_{cycle} + 2t_{sys}$ since the frequency acquisition circuit may have to cycle through 5 possible counter states (depending on initial conditions) to acquire lock. The nominal value of T_{cycle} for the GS9035A operating in a typical SMPTE 259M application is approximately 1.3ms.

The GS9035A has a dedicated LOCK output (pin 3) indicating when the device is locked. It should be noted that in synchronous switching applications where the switching time is less than 0.5µs, the LOCK output will NOT be de-asserted and the data outputs will NOT be muted.

5.2 DVB-ASI

Design Note: For *DVB-ASI* applications having significant instances of few bit transitions or when only K28.5 idle bits are transmitted, the wide-band PLL in the GS9035A may lock at 243MHz being the first 27MHz sideband below 270MHz. In this case, when normal bit density signals are transmitted, the PLL will correctly lock onto the proper 270MHz carrier.

6. OUTPUT DATA MUTING

The GS9035A internally mutes the SDO and $\overline{SDO}$ outputs when the device is not locked. When muted, SDO/$\overline{SDO}$ are latched providing a logic state to the subsequent circuit and avoiding a condition where noise could be amplified and appear as data. The output data muting timing is shown in Figure 14.

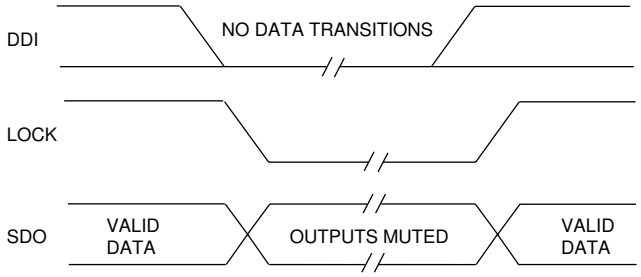


Fig. 14 Output Data Muting Timing

7. CLOCK ENABLE

When CLK_EN is high, the GS9035A SCO/$\overline{SCO}$ outputs are enabled. When CLK_EN is low, the SCO/$\overline{SCO}$ outputs are set to a high Z state and float to V_{CC}. Disabling the clock outputs results in a power savings of 10%. It is recommended that the CLK_EN input be hard wired to the desired state. For applications which do not require the clock output, connect CLK_EN to Ground and connect the SCO/$\overline{SCO}$ outputs to V_{CC}.

8. STRESSFUL DATA PATTERNS

All PLL's are susceptible to stressful data patterns which can introduce bit errors in the data stream. PLL's are most sensitive to patterns which have long run lengths of zeros or ones (low data transition densities for a long period of time). The GS9035A is designed to operate with low data transition densities such as the SMPTE 259M pathological signal (data transition density = 0.05).

9. PLL DESIGN GUIDELINES

The performance of the GS9035A is primarily determined by the PLL. Thus, it is important that the system designer is familiar with the basic PLL design equations.

A model of the GS9035A PLL is shown below. The main components are the phase detector, the VCO, and the external loop filter components.

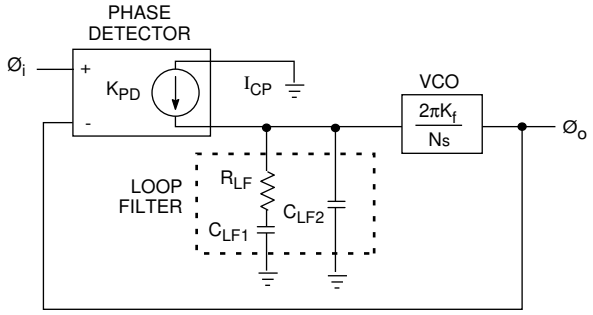


Fig. 15 PLL Model

9.1 Transfer Function

The transfer function of the PLL is defined as $Ø_o/Ø_i$ and can be approximated as

$$\frac{Ø_o}{Ø_i} = \frac{sC_{LF1}R_{LF} + 1}{\left[s\left(C_{LF1}R_{LF} - \frac{L}{R_{LF}}\right) + 1\right]} \frac{1}{\left[s^2C_{LF2}L + s\frac{L}{R_{LF}} + 1\right]}$$

Equation 1

where

$$L = \frac{N}{DI_{CP}K_f}$$

N is the divider modulus

D is the data density (=0.5 for NRZ data)

I_{CP} is the charge pump current in Amps

K_f is the VCO gain in Hz/V

This response has 1 zero (w_Z) and three poles (w_{P1}, w_{BW}, w_{P2}) where

$$w_Z = \frac{1}{C_{LF1}R_{LF}}$$

$$w_{P1} = \frac{1}{C_{LF1}R_{LF} - \frac{L}{R_{LF}}}$$

$$w_{BW} = \frac{R_{LF}}{L}$$

$$w_{P2} = \frac{1}{C_{LF2}R_{LF}}$$

The bode plot for this transfer function is plotted in Figure 16.

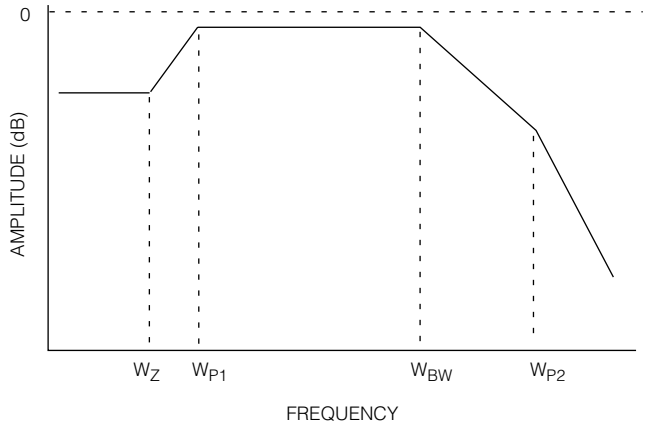


Fig. 16 Bode Plot for PLL Transfer Function

The 3dB bandwidth of the transfer function is approximately

$$w_{3dB} = \frac{w_{BW}}{\sqrt{1 - 2\frac{w_{BW}}{w_{P2}} + \frac{(w_{BW}/w_{P2})^2}{1 - 2\frac{w_{BW}}{w_{P2}}}}} \approx \frac{w_{BW}}{0.78}$$

9.2 Transfer Function Peaking

There are two causes of peaking in the PLL transfer function given by Equation 1.

The first is the quadratic

$$s^2 C_{LF2} L + s\frac{L}{R_{LF}} + 1$$

which has

$$w_O = \frac{1}{\sqrt{C_{LF2} L}} \quad \text{and} \quad Q = R_{LF}\sqrt{\frac{C_{LF2}}{L}}$$

This response is critically damped for Q = 0.5.

Thus, to avoid peaking:

$$R_{LF}\sqrt{\frac{C_{LF2}}{L}} < \frac{1}{2}$$

or

$$\frac{1}{R_{LF} C_{LF2}} \frac{L}{R_{LF}} > 4$$

Therefore,

$w_{P2} > 4\, w_{BW}$ $\quad L = \frac{2N}{I_{CP} K_f}$

However, it is desirable to keep w_{P2} as low as possible to reduce the high frequency content on the loop filter.

The second is the zero-pole combination:

$$\frac{sC_{LF1}R_{LF} + 1}{s\left(C_{LF1}R_{LF} - \frac{L}{R_{LF}}\right) + 1} = \frac{\frac{s}{w_Z} + 1}{\frac{s}{w_{P1}} + 1}$$

This causes lift in the transfer function given by

$$20\ \text{LOG}\frac{w_{P1}}{w_Z} = 20\ \text{LOG}\frac{1}{1 - \frac{w_Z}{w_{BW}}}$$

To keep peaking to less than 0.05dB,

$w_Z < 0.0057\, w_{BW}$

9.3 Selection of Loop Filter Components

Based on the above analysis, select the loop filter components for a given PLL bandwidth, f_{3dB}, as follows:

1. Calculate

   where

   I_{CP} is the charge pump current and is a function of the R_{VCO} resistor and is obtained from Figure 17.

   K_f = 90MHz/V for VCO frequencies corresponding to the f_L curve.

   K_f = 140MHz/V for VCO frequencies corresponding to the f_H curve.

   N is the divider modulus.

   (f_L, f_H and N can be obtained from Table 2 or Table 3).

2. Choose $R_{LF} = 2(3.14)\, f_{3dB}\, (0.78)L$

3. Choose $C_{LF1} = 174\ L / (R_{LF})^2$

4. Choose $C_{LF2} = L/4(R_{LF})^2$

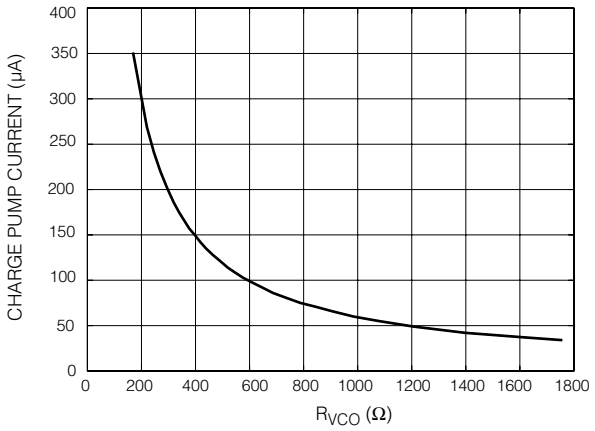
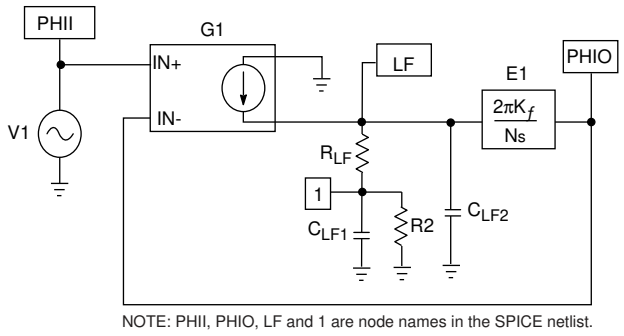


Fig. 17 Charge Pump Current vs. R_{VCO}

9.4 Spice Simulations

More detailed analysis of the GS9035A PLL can be done using SPICE. A SPICE model of the PLL is shown below:



NOTE: PHII, PHIO, LF and 1 are node names in the SPICE netlist.

Fig. 18 SPICE Model of PLL

The model consists of a voltage controlled current source (G1), the loop filter components (R_{LF}, C_{LF1}, and C_{LF2}), a voltage controlled voltage source (E1), and a voltage source (V1). R2 is necessary to create a DC path to ground for Node 1.

V1 is used to generate the input phase waveform. G1 compares the input and output phase waveforms and generates the charge pump current, I_{CP}. The loop filter components integrate the charge pump current to establish the loop filter voltage. E1 creates the output phase waveform (PHIO) by multiplying the loop filter voltage by the value of the Laplace transform ($2pK_f/Ns$).

The netlist for the model is given below. The .PARAM statements are used to set values for I_{CP}, K_f, N, and D. I_{CP} is determined by the R_{VCO} resistor and is obtained from Figure 17.

```
SPICE NETLIST * GS9035A PLL Model
.PARAM ICP = 165E-6 KF= 90E+6
.PARAM N = 1 D = 0.5
.PARAM PI = 3.14
.IC V(Phio) = 0
.ac dec 30 1k 10meg
RLF 1 LF 1000
CLF1 1 0 15n
CLF2 0 LF 15p
E_LAPLACE1 Phio 0 LAPLACE {V(LF)} {(2*PI*KF)/(N*s)}
G1 0 LF VALUE{D * ICP/(2*pi)*V(Phii, Phio)}
V1 2 0 DC 0V AC 1V
R2 0 1 1g
.END
```

10. I/O DESCRIPTION

10.1 High Speed Inputs (DDI/$\overline{\text{DDI}}$)

DDI/$\overline{\text{DDI}}$ are high impedance inputs which accept differential or single-ended input drive. Two conditions must be observed when interfacing to these inputs:

1. Input signal amplitudes are between 200 and 2000mV
2. The common mode input voltage range is as specified in the DC Characteristics table.

Commonly used interface examples are shown in Figures 19 and 20.

Figure 19 illustrates the simplest interface to the GS9035A. In this example, the driving device generates the PECL level signals (800mV amplitudes) having a common mode input range between 0.4 and 4.6V. This scheme is recommended when the trace lengths are less than 1in. The value of the resistors and the DC connection (V_{CC} or Ground), depends on the output driver circuitry of the previous device.

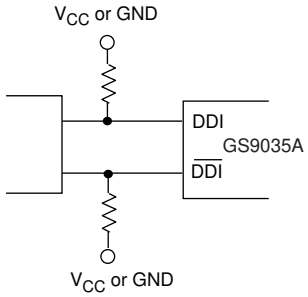


Fig. 19 Simple Interface to the GS9035A

When trace lengths become greater than 1in, controlled impedance traces should be used. The recommended interface for differential signals is shown in Figure 20. In this case, a parallel resistor (R_{LOAD}) is placed near the GS9035A inputs to terminate the controlled impedance trace. The value of R_{LOAD} should be twice the value of the characteristic impedance of the trace. Both traces should be in a symmetric arrangement and same physical transmission line dimensions since common-mode signals or common-mode noise is not terminated. In addition, series resistors, R_{SOURCE}, can be placed near the driving chip to serve as source terminations. They should be equal to the value of the trace impedance. Assuming 800mV output swings at the driver, R_{LOAD} =100Ω, R_{SOURCE} =50Ω and Z_O = 50Ω.

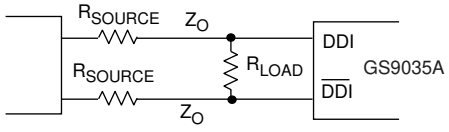


Fig. 20 Recommended Interface for Differential Signals

Figure 21 shows the recommended interface when the GS9035A is driven single-endedly. In this case, the input must be AC-coupled and a matching resistor (Z_O) must be used.

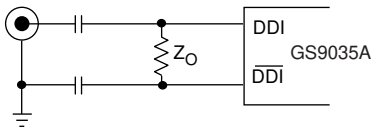


Fig. 21 Recommended Interface for Single-Ended Driver

10.2 High Speed Outputs (SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$)

SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$ are current mode outputs that require external pullup resistors (*see Figure 22*). To calculate the output sink current use the following relationship:

Output Sink Current = Output Signal Swing / Pullup Resistor

A diode can be placed between V_{cc} and the pullup resistors to reduce the common mode voltage by approximately 0.7 volts.When the output traces are longer than 1in, controlled impedance traces should be used. The pullup resistors should be placed at the end of the output traces as they terminate the trace in its characteristic impedance (75Ω).

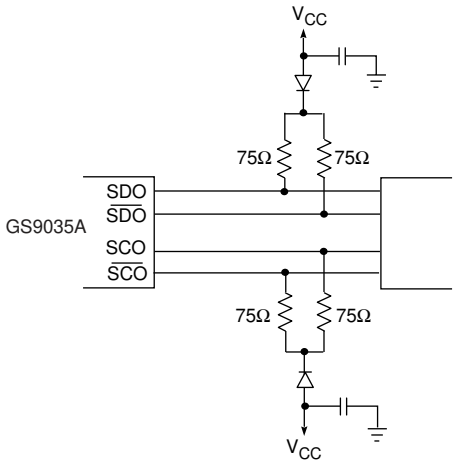


Fig. 22 High Speed Outputs with External Pullups

TYPICAL APPLICATION CIRCUIT

The figure below shows the GS9035A connected in a typical auto rate select SMPTE 259M application. Table 4 summarizes the relevant system parameters.

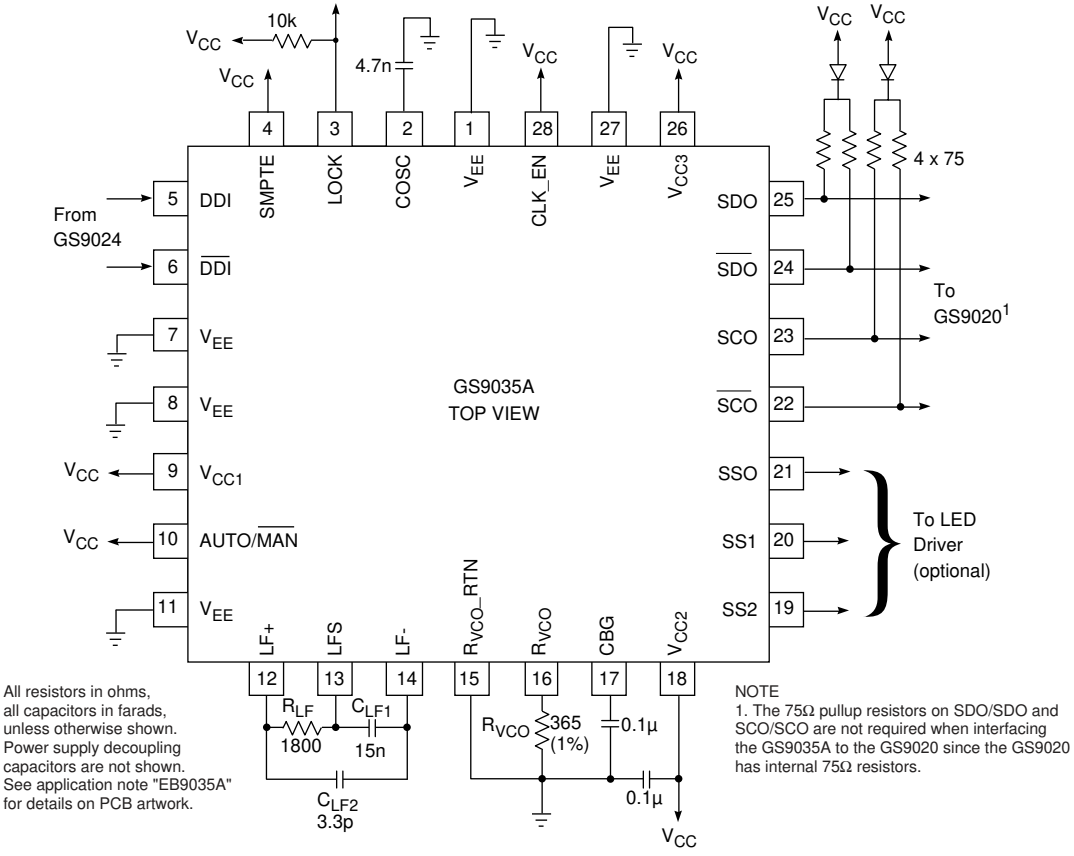
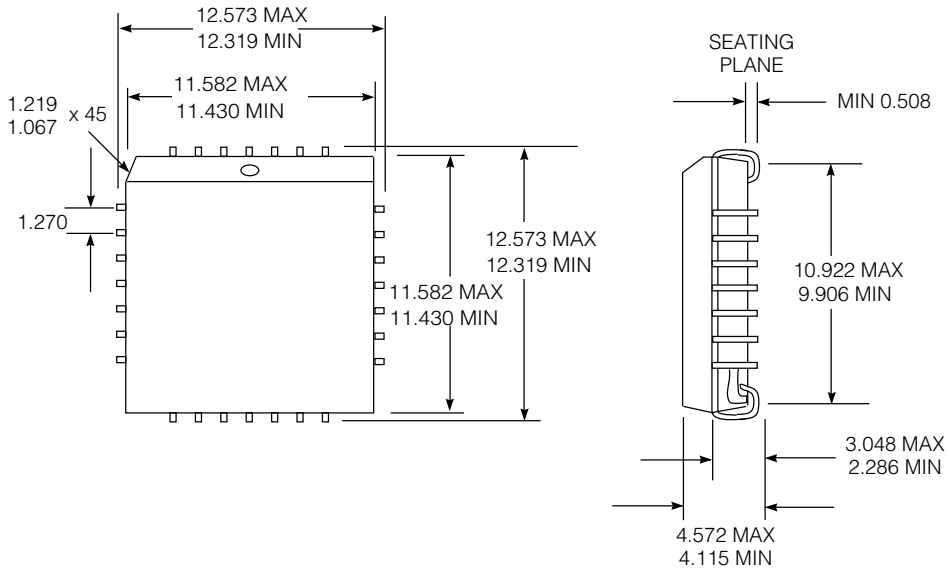


TABLE 5: System Parameters

R_{VCO} = 365Ω, f_H = 540MHz, f_L = 360MHz			
SMPTE	SS[2:0]	DATA RATE (Mb/s)	LOOP BANDWIDTH
1	000	143	1.2MHz
1	001	177	1.9MHz
1	010	270	3.0MHz
1	011	360	4.5MHz
1	100	540	6.0MHz

PACKAGE DIMENSIONS



All dimensions in millimetres.
28 pin PLCC (QM)

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GENNUM CORPORATION

MAILING ADDRESS:
P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

SHIPPING ADDRESS:
970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

GENNUM JAPAN CORPORATION
Shinjuku Green Tower Building 27F, 6-14-1, Nishi Shinjuku,
Shinjuku-ku, Tokyo, 160-0023 Japan
Tel. +81 (03) 3349-5501, Fax. +81 (03) 3349-5505

GENNUM UK LIMITED
25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523