**MOTOROLA**

4-Bit Comparator

ELECTRICALLY TESTED PER:
MIL-M-38510/31101

The 54LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3; B_0-B_3), A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A > B}$), "A less than B" ($O_{A < B}$), "A equal to B" ($O_{A = B}$). Three Expander Inputs, $I_{A > B}$, $I_{A < B}$, $I_{A = B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A < B} = I_{A > B} = L$, $I_{A = B} = H$. For serial (ripple) expansion, the $O_{A > B}$, $O_{A < B}$ and $O_{A = B}$ outputs are connected respectively to the $I_{A > B}$, $I_{A < B}$, and $I_{A = B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to applications section of data sheet for high-speed method of comparing large words.

The Truth Table which follows describes the operation of the 54LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A > B}$, $O_{A < B}$, and $O_{A = B}$ Outputs Available

LOGIC DIAGRAM

MPO
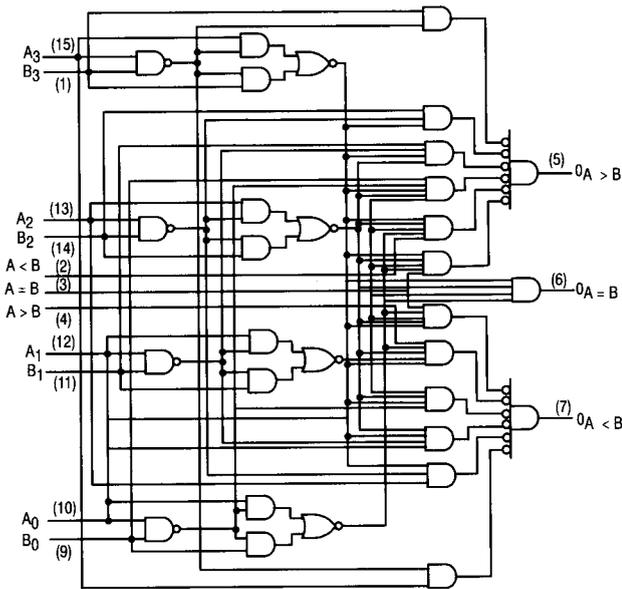
AVAILABLE AS:

1) JAN: 38510/31101BXA
2) SMD: N/A
3) 883: 54LS85/BXAJC

X = CASE OUTLINE AS FOLLOWS:
   PACKAGE: CERDIP: E
            CERFLAT: F
            LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
B_3	1	1	2	V_{CC}
$A < B_{IN}$	2	2	3	GND
$A = B_{IN}$	3	3	4	GND
$A > B_{IN}$	4	4	5	GND
$A > B_{OUT}$	5	5	7	V_{CC}
$A = B_{OUT}$	6	6	8	OPEN
$A < B_{OUT}$	7	7	9	V_{CC}
GND	8	8	10	GND
B_0	9	9	12	GND
A_0	10	10	13	GND
B_1	11	11	14	GND
A_1	12	12	15	GND
A_2	13	13	17	GND
B_2	14	14	18	GND
A_3	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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TEST CIRCUIT AND WAVEFORMS
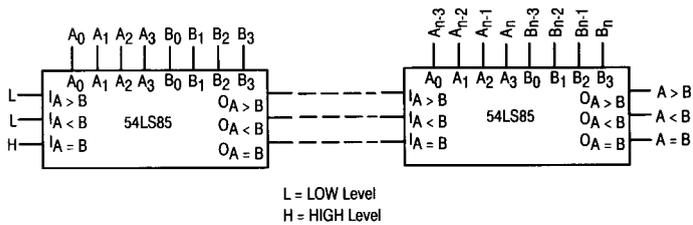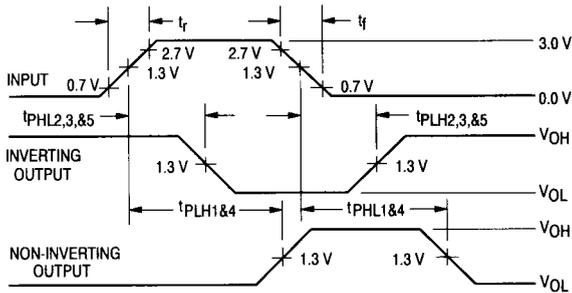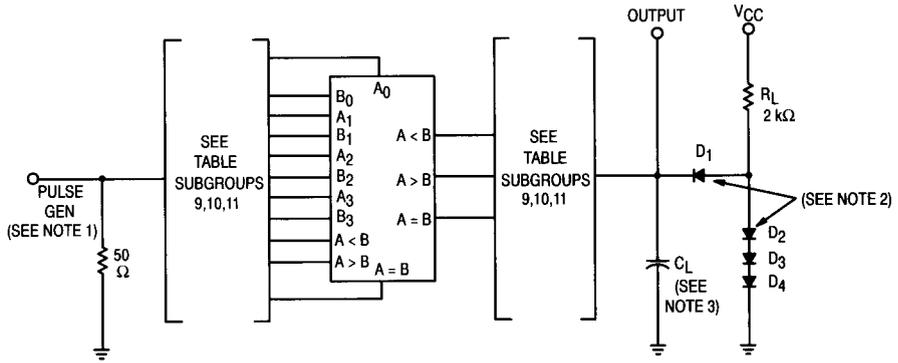
Figure 1. Comparing Two n-Bit Words

L = LOW Level
H = HIGH Level

NOTES:

1. The input pulse generator has the following characteristics:
   $V_{gen} = 3.0$ V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_p = 0.5$ μs, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50$ Ω.
2. All diodes are 1N3064 or equivalent.
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
4. Voltage measurements are to be made with respect to network ground terminal.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).
6. The 54LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 54LS85 as shown in Figure 2 in positions #1, 2, 3 and 4.

Table 1	
Word Length	**Number of Packages**
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

TRUTH TABLE									
Comparing Inputs				Cascading Inputs			Outputs		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Figure 2 shows a high-speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two words. The parallel technique can be expanded to any number of bits, see Table 1.
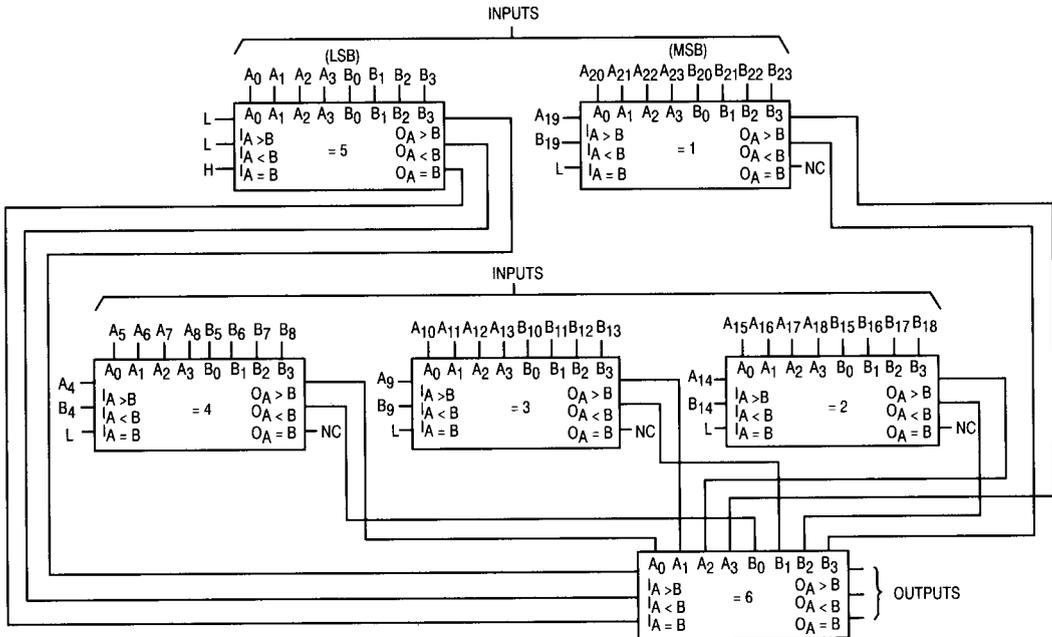
MSB = Most Significant Bit
LSB = Least Significant Bit
L = Low Level
H = HIGH Level
NC = No Connection

Figure 2. Comparison of Two 24-Bit Words

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, $V_{IN(B\ or\ A)}$ = 0.7 V, other inputs are GND, (A = B_{in}) = 0.7 V or 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 2.0 V or 0.7 V (all inputs), (A = B_{in}) = GND, 0.7 V or 2.0 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} − 2.7 V, other inputs are open, $B_{0,\ 3}$ = GND.
I_{IH}	Logical "1" Input Current		60		60		60	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND or 5.5 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, $B_{0,\ 3}$ = GND.
I_{IHH}	Logical "1" Input Current		300		300		300	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input = GND.
I_{IL}	Logical "0" Input Current	− 0.1	− 0.38	− 0.1	− 0.38	− 0.1	0.38	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input = 5.5 V.
I_{IL}	Logical "0" Input Current	− 0.4	−1.14	− 0.4	−1.14	− 0.4	−1.14	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input 5.5 V, (A = B_{in}) = − 0.32 mA (min).
I_{OS}	Short Circuit Output Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs are GND, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		20		20		20	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs are GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "1" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output High-Low	2.0 —	35 30	2.0 —	42 38	2.0 —	42 38	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Low-High	2.0 —	35 36	2.0 —	42 45	2.0 —	42 45	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output High-Low	2.0 —	33 36	2.0 —	39 34	2.0 —	39 34	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Low-High	2.0 —	36 36	2.0 —	42 37	2.0 —	42 37	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PHL3} t_{PHL3}	Propagation Delay /Data-Output High-Low	2.0 —	20 17	2.0 —	28 23	2.0 —	28 23	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH3} t_{PLH3}	Propagation Delay /Data-Output Low-High	2.0 —	20 22	2.0 —	25 28	2.0 —	25 28	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PHL4} t_{PHL4}	Propagation Delay /Data-Output High-Low	2.0 —	25 26	2.0 —	36 33	2.0 —	36 33	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH4} t_{PLH4}	Propagation Delay /Data-Output Low-High	2.0 —	20 20	2.0 —	28 25	2.0 —	28 25	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output High-Low	2.0 —	20 17	2.0 —	26 21	2.0 —	26 21	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output Low-High	2.0 —	22 22	2.0 —	30 28	2.0 —	30 28	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.

NOTE:
1. The limit specified for $C_L = 15$ pF is guaranteed but not tested.

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